A DTCNN CMOS Implementation of a Pixel-Level Snake Algorithm

V. M. Brea*, A. Paasio®, D.L. Vilariño* and D. Cabello*

Abstract – In this paper an analog CMOS implementation of an active contour technique known as Pixel-Level Snakes (PLS), projected onto a Discrete Time Cellular Neural Network (DTCNN) is introduced.

The DTCNN architecture consists of two main processing steps, which process gray scale and B/W images. It has been proved that all the analog circuits meet the template robustness requirements. HSPICE simulations of the proposed circuitry with power supplies of 2.5v and 3.3v composed of transistors belonging to the 0.25 µm technology process of Thomson are given.

1 Introduction

Active contours or snakes [1] consist of deformable closed curves which evolve towards the salient features of an image (extremes, edges ...) guided by both external and internal energy terms.

In classical techniques a discrete set of control vertices are considered for the process of minimization of the energy, calculated as sum of internal and external energies. In Pixel-Level Snake concept (PLS), all the contour pixels are taken into account and, as a consequence, the contour approach is as accurate as the image discretization allows. This leads to a higher flexibility for the evolution dynamics of the snake allowing the solution of complex tasks as is the case of the topologic transformations [2].

Since all the interactions among pixels at PLS algorithm locally interact, CNN [3] seem to be a suitable way to implement a circuit for such a task. Particularly, the easy control and inherent robustness of DTCNN [4] facilitates its hardware implementation [5,6].

A VHDL description of a DTCNN circuit for the PLS algorithm introduced in [2] has been proposed in [7]. Since the complexity of the task leads to the use of cyclic time variable cloning templates, local memories and programming templates [8] have been included in the circuit. The VHDL simulations shown in [7] provide some guidelines for the development of the successive design stages towards a final physical implementation.

In this work a DTCNN CMOS realization of such a circuit is introduced. Since the energy that guides the evolution of the snake is a gray scale image and the rest of processing steps starts from binary inputs, the circuit consists of two main processing steps. Both of them are discussed within Section 2. In Section 3, HSPICE simulations of an isolated cell of the DTCNN are given.

2 Circuitry of the Array Cell

The PLS algorithm for image segmentation is a cyclic processing along the four cardinal directions. It basically consists of an expansion followed by a guided thinning of the contours. The guiding process is carried out by means of a comparison of the energy among neighboring pixels along the current processing direction. In our application, the contour is guided towards the maximum of the energy function, calculated as a sum of external and internal energies.

The external energy is a gray scale image extracted from the image under processing (gray scale) which contains the most meaningful information for the guiding of the active contours. Its size coincides with that of the original one and it is fed to the circuit from outside. The internal energy is a gray scale image with the same size of the image under processing. It is extracted in a dynamic way from the B/W contour image and tries to keep smooth the contour shape. Another constraint is to keep the continuity of the contour so that breakpoints are not allowed at the end of each processing direction [9].

A schematic representation of one cell of the array together with the processing cycles of the network are shown in Fig. 1. The two main parts of the circuit are clearly recognized. On the one hand the EP-IE block which guides the evolution of the contour, and on the other hand the circuitry which performs the rest of processing steps. The EP-IE circuit is described in the next Subsection, while the rest of circuitry will be described in Subsection 2.2.

2.1 Gray Scale Image Processing Circuit

The EP-IE circuit shown in Fig. 2 guides the evolution of the contour. This is performed by a
is codified as entire and positive values within the PLS algorithm. In our application the external energy are enough to ensure a correct operation of the final contours are close to the initial ones, a great range of variation of the guiding energy is not required. Five bits of adjustability for the external energy are enough to ensure a correct operation against mismatching effects [10].

All the transistor dimensions guarantee a transmission gate decrease the gate voltage error to an acceptable level [11].

The local external energy is uploaded into an analog energy is good enough. The current gain of the smaller range of variation than that of the external contour shape during its evolution [9]. Thus, a role of a “second order term” which smoothes the neighbor energy and/or deformed along the current processing direction. If the local energy is higher than that the neighbor energy and/or the internal energy adder is properly set to select one of the currents from the set \{0, \ldots, 12\} $\mu$A, depending on the outputs from $IE(1)$, $IE(2)$ and $IE(3)$ processing cycles (Fig. 1).

The external and internal energies are summed inside each cell and sent to the appropriate neighbor one along the current processing direction through one of the switches labelled with $sd_{-n}$, $sd_{-w}$, $sd_s$ and $sd_e$ in Fig. 2. Then, the energy comparison between neighboring cells is performed by the positive feedback decision circuit. As a result, one of the output nodes of the positive feedback decision circuit will be high, while the other one will be low. The OTA transforms the differential signal into a single one that together with $cpd(3)$ drives an OR-gate. Its output is the guiding information for the next processing direction selected as input to $LLM(0)$ (Fig. 1) when $sel_{ep}$ is high, during the $EP$ processing cycle.

The output from $EP-IE$ goes low when the local energy is lower than that the neighbor energy and $cpd(3)$ is low. Then, the contour will be shifted and/or deformed along the current processing direction. If the local energy is higher than that the neighbor energy and/or $cpd(3)$ is high, the $EP-IE$ output goes high and the contour will keep still.

### 2.2 B/W Contour Image Processing Circuit

The B/W active contour image is shifted and/or deformed by the circuit outside the box labelled with $EP-IE$ in Fig. 1. The DTCNN threshold function

![Figure 1: An isolated DTCNN cell together with its processing steps labelled with their LLM events.](image-url)
between zero and one is performed by LLM(0) [6,7].

LLM and SPM memories keep the outputs from the previous processing steps. Their outputs feed the multipliers which drive the neighbor cells within a neighborhood of radius one. The selection of these outputs is performed by global digital control signals which drive a set of switches inside the cells. The high state of the digital control signals is risen from 2.5v, the voltage power supply for the current steering D/A converters and the memories, to 3.3v to ensure a correct operation of the NMOS switches.

Figure 3: Multiplier Circuit.

The structure of the multipliers is shown in Fig. 3. They are composed of two PMOS transistors, the loads of two current steering D/A converters [12], and two NMOS switches driven by the appropriate LLM output. There are 38 D/A converters (one for each template coefficient, and one for each sign: positive or negative) driven by digital words which might be provided by a ROM. The mismatching effects leads to the use of two PMOS transistors instead of a PMOS and a NMOS [12]. At this situation, two switches per multiplier, and a current inverter implemented by a NMOS current mirror and a switch controlled by sel_ep at the input of LLM(0), are required. This leads to a number of 155 transistors per cell. Nevertheless, and since for this circuit implementation the mismatching errors decrease with higher currents, smaller area results from rising the voltage power supply from 2.5v to 3.3v for the current steering D/A converters and the multipliers [12].

3 Simulation Results

In this Section an example of simulation of an isolated DTCNN cell is shown in Fig. 4. The frequency of the clock signal, ck, depends on the cell array size (fanout). The presence of a buffer between the common circuitry and the multipliers inside the cells makes the clock frequency faster. A valid frequency for an isolated cell is 400ns.

We have simulated some B/W image operations followed by a gray scale image processing shown in Fig. 4. The multipliers involved in these successive steps are those which drive the cell itself: A0, B0 and w_k (Fig. 1 and 2). At the beginning of the processing reset goes high, and as a consequence LLM(0) output goes low. The initial contour image is a black pixel, (high voltage), uploaded into the SPM memory through the d_in NMOS switch. When reset goes low, the programming templates are: A0=4, B0=4 and Offset=1, and the high switch control signals are sel_a and sw_2 (Fig. 1). At this situation, LLM(0) output goes high, as it can be seen in Fig. 4. Then, from 600ns until 1600ns, the template coefficients are: A0=0, B0=1 and Offset=1, and LLM(0) output goes low.

The last operation is the guiding of the contour by EP-IE output when sel_ep is high. We have compared a local external energy of 20μA with a neighbor one of 23μA. The internal energy is provided by the A0, B0 and w_k multipliers. Since LLM(4) is high at the beginning of the cycle, the only active multiplier is w_k, which will provide a local...
internal energy of 4 µA. Thus, the comparison is between a 24 µA local energy and a 23 µA neighbor energy. Since the neighbor energy is less than that the local one, the contour does not evolve, and \( LLM(0) \) output is high.

### 4 Conclusions

An analog DTCNN CMOS implementation of a PLS algorithm for image segmentation has been proposed. The evolution of the B/W active contour image is performed by a DTCNN circuit programmed by a set of cyclic time variable cloning templates. This process is guided towards the maximum of the energy by means of a current comparator.

It has been proved that all the analog circuits runs properly against mismatching effects. At the time of this work simulation results of one isolated DTCNN cell are available. Successive steps towards the final physical implementation will be developed. The validity of the proposed circuit is illustrated by HSPICE simulations with transistors of the 0.25 µm technology process of Thomson.

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### References


