Predicting Propagation Delay in SCL Gates

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Abstract - An approach for the modelization of propagation delay in CMOS SCL gates is proposed in this communication. The method is based on an appropriate linearization of the gate and the equivalent circuit obtained is analyzed under the dominant-pole approximation. The resulting expressions of propagation delay are simple and show its dependence on design and process parameters. The compactness of expressions obtained and the clear physical meaning of their terms allow the deep understanding of the SCL circuits behavior, and hence they are helpful since the earliest design phases.

The approach was validated by simulating an SCL inverter under various bias and load conditions. The worst-case error obtained is lower than 20%, but in realistic cases it is significantly lower, typically about 5%.

1 Introduction

A low switching noise performance of digital logic is becoming more and more important, due to diffusion of mixed-signal ICs, which include complex high-speed digital circuitry and analog blocks in a common substrate [1-6]. For this reason, the interest in low switching noise CMOS logic circuits is increasing, among which Source-Coupled Logic (SCL) is the most promising [6-13].

A differential SCL inverter, shown in Fig. 1, is made up of a source-coupled pair (M1-M2) realized by two NMOS transistors working in the saturation region biased by a constant current source $I_B$. Depending on the value of the differential input voltage $v_{i}=v_{i1}-v_{i2}$, current $I_B$ is steered to one of the active loads (M3-M4), implemented with PMOS transistors working in the linear region. This load converts the current variation into a differential output voltage, $v_{o}$, given by $v_{o1}-v_{o2}$. Fig. 1 also includes an equivalent capacitive load represented as two capacitors $C_L$, accounting for input capacitance of following gates and wiring parasitics. The low switching noise feature of SCL circuits is achieved thanks to the fact that current supplied by $V_{DD}$ is constant, avoiding voltage spikes on the power line $V_{DD}$ and reducing in turn signal degradation of the analog section [14]. Of course, this noise reduction is achieved at the expense of a static power dissipation.

Let us briefly analyze the static behavior of the gate. When input $v_i$ is high, the whole current $I_B$ flows through transistors M1 and M3, hence $v_{o2}=V_{DD}$ and $v_{o1}=V_{DD}-V_S$, where $V_S$ is the source-drain voltage drop when the current of M3 is equal to $I_B$. Thus, the differential output voltage is at the low level $-V_S$. The case of low input $v_i$ is dual, and the logic swing of the gate is hence equal to $2V_S$. It is worth noting that $V_S$ must be always chosen lower than the NMOS threshold voltage, $V_{Th}$, in order to avoid NMOS transistors entering the triode region.

Concerning the dynamic behavior of the SCL gate, it should be clear that its delay depends on the value of bias current $I_B$, on the parasitic capacitances associated with the NMOS and PMOS transistors and on the load capacitance, $C_L$.

In this paper, an approach to SCL gates delay modeling is proposed. It is based on a suitable linearization of the circuit, and leads to simple expressions, which are helpful since in the early design steps to understand the fundamental dependence of delay on design and process parameters. The approach is validated by simulations with Spectre using a 0.35-µm CMOS technology, in a wide range of bias currents and for different load capacitance values.

2 Proposed Approach

Let us consider the SCL gate in Fig. 1. The NMOS transistors work in the saturation region, and their source voltage is the same for both input logic values,
since it is fixed by the NMOS transistor in the ON state. Thus, after linearizing the circuit around the bias point with \( V_V = 0 \), the half-circuit concept applies [15], since the circuit is symmetrical and input is differential.

The equivalent linear half circuit obtained is shown in Fig. 2, where transistor M1 (M2) is represented by its small-signal model, and transistor M3 (M4) is linearized as an equivalent resistance \( R_D \). The capacitive effects associated with transistors consist of \( C_{dv} \), which represents the drain-bulk junction capacitance, and \( C_{gd} \), which schematizes the channel or overlap contribution between gate and drain. Subscripts \( n \) and \( p \) in Fig. 2, refer to NMOS and PMOS devices, respectively. Explicit evaluation of parameters \( R_D \), \( C_{gd,n} \), \( C_{db,n} \), \( C_{gd,p} \), \( C_{db,p} \) is developed in the following section.

![Figure 2: Equivalent linear circuit of the SCL inverter.](image)

The network in Fig. 2 is a first-order circuit, with a time constant \( \tau \) that can be evaluated circuitually by applying the open-circuit time constant method [15]. As known, the delay of a circuit with a first-order behavior and a related time constant \( \tau \) is 0.69\( \tau \) [14]. Since all capacitances see the same resistance, i.e. \( R_D \), the propagation delay \( \tau_{PD} \) of the SCL gate results to be

\[
\tau_{PD} = 0.69 R_D \left[ C_{gd,n} + C_{db,n} + C_{gd,p} + C_{db,p} + C_L \right] \tag{1}
\]

The obtained expression is simple and can be hence profitably used in pencil-and-paper calculations. Equation (1) shows how delay depends on design and process parameters and allows to get the necessary intuitive insight into the circuit behavior to meet assigned design specifications.

The resistance \( R_D \) and parasitic capacitances in (1) are obtained through linearization of the original circuit, and their dependence on bias current, transistors aspect ratio, and process parameters must be specified.

### 2.1 Evaluation of PMOS equivalent resistance

Consider the expression of the drain current, \( id \), of a PMOS transistor in the triode region used in the BSIM3v3 MOSFET model, which represents the standard model for deep submicron CMOS technologies [17]:

\[
ld = \frac{id_{SAT}}{1 + R_D \frac{id_{SAT}}{V_{SD}}} \tag{2a}
\]

where the parameter \( R_D = (R_{DSW} \cdot 1E-6) / W_{eff} \), which depends on the empirical model parameter \( R_{DSW} \), accounts for source/drain parasitic resistance and has a heavy effect in today’s CMOS processes with lightly-doped drain (LDD). It is worth noting that \( R_D \) is not a physical resistor, but it only represents a corrective factor. The term \( id_{SAT} \) is given by:

\[
Id_{SAT} = \mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} \frac{1}{1 + \frac{2}{\sqrt{V_T}}} \left[ V_{SD} + V_T - A_{bulk} V_{SD} \right] \left( \frac{V_{SD}}{2} \right) \tag{2b}
\]

In (2b) parameters \( W_{eff} \) and \( L_{eff} \) are the effective channel width and length, \( C_{OX} \) is the oxide capacitance per area, \( V_T \) is the threshold voltage, \( V_{SG} \) and \( V_{SD} \) are the source-gate and source-drain voltages, \( E_{SAT} \) is the critical electric field at which the carrier velocity becomes saturated. Moreover, due to the active-load connection, we have to set in all the equations \( V_{SG} = V_{DD} \) and source-bulk voltage, \( V_{SB} \), equal to zero.

Parameter \( A_{bulk} \) in (2b) is slightly greater than the unity and is given by

\[
A_{bulk} = \frac{1}{1 + K_{ET} V_{SB} + A_{l,eff} \left[ 1 + \frac{K_{ox} \theta_B}{2} - V_{SB} \right] \left[ \frac{A_{1,eff} L_{eff}}{L_{eff} + 2 X_L X_{dep}} \right] + B_0 \left[ \frac{W_{eff} + B_1}{L_{eff} \cdot V_{SB}} \right] \}} \tag{3}
\]

which depends on \( W_{eff} \), \( L_{eff} \) and various other BSIM3v3 model parameters. Function \( A_{bulk} \) can be simplified considering its maximum value, \( A_{bulk,max} \). This can be obtained by setting \( W_{eff} \) at its minimum value and maximizing the resulting function with respect to \( L_{eff} \), with straightforward calculations. As an example, for the adopted 0.35-\( \mu \)m CMOS process we get \( A_{bulk,max} = 1.34 \).

In (2b), we can neglect terms \( A_{bulk} V_{SD}/2 \) and \( V_{SD} / E_{SAT} L_{EFF} \), because \( V_{SD} \) is small. Thus, (2b) becomes

\[
Id_{SAT} = \frac{V_{SD}}{R_{int}} \tag{4}
\]

where we have defined

\[
R_{int} = \frac{\mu_{eff} C_{OX} \frac{W_{eff}}{L_{eff}} \left[ V_{DD} - V_T \right]^{-1}} \tag{5}
\]

which represents the “intrinsic” resistance of the PMOS transistor in the triode region (i.e., it does not account for the parasitic drain/source resistance).

In (2b) and (5), the effective carrier mobility \( \mu_{eff} \) is defined as:
\[ \mu_{\text{eff}} = \frac{\mu_0}{1 + (U_d + U_c V_{SB}) \left( \frac{V_{SG} + V_T}{T_{OX}} \right)^2 + U_B \left( \frac{V_{SG} + V_T}{T_{OX}} \right)} \]

where \( U_d, U_b \) and \( U_c \) are model parameters, \( T_{OX} \) is the oxide thickness and \( V_{SB} \) is the source-bulk voltage. Since \( V_{SG} = V_{DD} \) and \( V_{SB} = 0 \), \( \mu_{\text{eff}} \) is a constant in our calculations.

To simplify the expression of \( I_D \), we expand (2a) in Taylor series truncated at the first-order term

\[ i_D = I_{DSAT0} \left[ 1 - R_{DS} \left( \frac{I_{DSAT0}}{V_{SD}} \right) \right] \]

Substituting (5) into (7), we obtain the equivalent resistance of the PMOS transistors \( R_D = V_{SD} / i_D \):

\[ R_D = \frac{R_{\text{int}}}{1 - \frac{R_{DS}}{R_{\text{int}}}} \]  

(8)

From (8), resistance \( R_D \) depends on process parameters and aspect ratio of the PMOS transistors.

### 2.2 Evaluation of parasitic capacitances

Let us consider the capacitances associated with the NMOS transistors, \( C_{gd,\text{n}} \) and \( C_{db,\text{n}} \). As \( M1 \) and \( M2 \) work in the saturation region, the former is roughly equal to the overlap capacitance between the gate and the drain, equal to \( C_{gd,\text{n}} W_{\text{eff},\text{n}} \) (\( C_{gd,n} \) is a model parameter which represents the overlap gate-drain capacitance per unit channel width). Since voltages move rapidly over a wide range, the junction capacitance \( C_{db,n} \) is evaluated by modifying its value in a zero-bias condition via coefficients \( K_j \) given by [14]

\[ K_j = \phi \left[ \frac{(\phi - V_j)^{1-m}}{1-m} - \frac{(\phi - V_j)^{1-m}}{1-m} \right] \]

(9)

where \( \phi \) is the built-in potential across the junction, \( m \) is the grading coefficient of the junction, and \( V_1 \) and \( V_2 \) are the minimum and maximum direct voltages across the junction, respectively. The drain-bulk PMOS capacitance \( C_{db,p} \) can be evaluated in the same way as for \( C_{db,n} \).

The capacitance \( C_{gd,p} \) is equal to the sum of the overlap contribution \( C_{gd,p,\text{int}} \) and the intrinsic one associated with the channel charge of the PMOS transistors working in the triode region, \( C_{gd,p,\text{int}} \). The latter contribution becomes dominant for low values of the bias current, since the PMOS channel length must be high to guarantee an assigned value of \( V_T \). Unfortunately, the evaluation of \( C_{gd,p,\text{int}} \) is significantly more complex than for long-channel devices, since in submicron technologies decomposition of channel capacitance into gate-source and gate-drain capacitances no longer applies [16-17]. Actually, assuming \( C_{gd,p,\text{int}} = \frac{1}{2} W_{\text{eff},p} L_{\text{eff},p} COX \)

leads to unacceptable errors.

In BSIM3v3 capacitance model, the channel charge transfer is modeled by transcapacitances \( C_{ij} \), defined as

\[ C_j = \frac{\partial Q_j}{\partial V_g} \]  

(10)

where \( Q_j \) is the charge associated with the MOSFET terminal \( i \), and \( V_g \) is the voltage of the terminal \( j \). The contribution \( C_{gd,p,\text{int}} \) accounts for the variations of the drain charge \( Q_D \) due to the drain-gate voltage, but since gate, source, and bulk terminals of M3-M4 are at a fixed voltage, \( C_{gd,p,\text{int}} \) can be expressed as a physical capacitance equal to \( C_{dd} \), defined by (10).

The expression of \( Q_D \) used in BSIM3v3 model in the strong inversion is given by

\[ Q_D = -W_{\text{eff}} L_{\text{eff}} COX \left[ \frac{V_{SD} - V_T}{2} - \frac{3}{4} A_{\text{bulk}} V_{SD} + \frac{A_{\text{bulk}} V_{SD}^2}{8} \right] \]

(11)

hence, deriving (11) with respect to \( V_D \) and approximating \( A_{\text{bulk}} \) to its maximum value \( A_{\text{bulk, max}} \), yields

\[ C_{dd} = \frac{3}{4} A_{\text{bulk, max}} W_{\text{eff}} L_{\text{eff}} COX \]  

(12)

### 3 Model validation and remarks

To test the model accuracy, the circuit in Fig. 1 was simulated under different bias and load conditions with Spectre, using a 0.35-\( \mu \)m technology. The supply voltage, \( V_{DD} \), was set to 3.3 V, and the bias current, \( I_{SS} \), was varied from 5 \( \mu \)A to 100 \( \mu \)A. The load capacitance, \( C_L \), was set equal to 0 F, 50 fF and 500 fF, whose values cover well the typical load conditions with a load capacitance much lower, comparable, or much higher than the gate parasitic capacitance. The transistors aspect ratios were chosen to obtain \( V_T = 350 \) mV as well as a small-signal gain around the logic threshold voltage equal to 3.

The simulated and theoretical propagation delay for \( C_{L} = 0 \) F, 50 fF and 500 fF is illustrated in Figs. 3, 4 and 5, respectively. It is evident, by inspection of these figures, that the model fits well the simulated results in all the considered cases. Indeed, the maximum error of the model is equal to 19%, 15% and 14% for \( C_{L} = 0 \) F, 50 fF and 500 fF, respectively. Thus, the error decreases with the load capacitance, and for the case \( C_{L} = 0 \) F represents an upper bound: in actual circuits the error is lower. The average error was less than 5%. It is of interest to notice that neglecting the effect of parameter \( R_{DS} \) in evaluating (2a) would have lead to an error higher than 50%;
about the same error has been observed by approximating $C_{gd,p}$ to its long-channel expression.

The approach was validated with circuit simulations of an SCL inverter under several bias and load conditions. The error shown is always lower than 20% and typically under 5%, hence the approach exhibits good accuracy in estimating delay for assigned values of bias current and load.

4 Conclusions

In this communication, an approach for delay modeling of SCL gates is proposed. It is based on circuit linearization and dominant-pole approximation, leading to simple expressions that are also well suited for pencil-and-paper estimation. Since the approach is based on a simplified circuit analysis, its expressions have a manifest physical meaning, allowing the designer to have an intuitive understanding of the circuit behavior.

References


