1-V CMOS Class AB Current Mirror

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***Abstract* - A CMOS class AB current mirror whose supply requirements are restricted to one threshold voltage plus three saturation voltages is presented. The circuit uses two poly resistors and two auxiliary differential amplifiers to achieve low-voltage operation, as well as control of quiescent currents and input bias voltage. A design example is implemented in a 0.5-µm standard technology and uses a 1-V supply. It exhibits input and output resistances of 5 kΩ and 3.6 MΩ, respectively and a DC current gain of 0.03 dB over a bandwidth of 140 MHz.**

1 Introduction

Current mirrors both in their class A and class AB versions, are widely used building blocks for analog and digital applications. Class AB topologies are capable of managing large bipolar currents and, compared to class A solutions, provide better dynamic range [1], reduced sensitivity to process tolerances [2], and allow the quiescent current to signal amplitude ratio to be increased, thus reducing offset and power consumption. All these properties are normally achieved at the expense of increased supply voltage requirements. This limitation has greatly restricted the use of these circuits in recent years, especially in CMOS applications where the trend is towards power supply voltages lower than 2 V.

The most popular class AB current mirror capable of managing a bipolar current is the one shown in Fig. 1. This has been used in a wide range of applications such as current conveyors, current comparators, input stage of current amplifiers, etc [3-5]. However, this circuit requires a power supply at least equal to $2(V_T+2V_{DS,SAT})$. Hence, it is unsuitable for supplies lower than 1.5 V, when using standard technologies with thresholds around 0.6V.

A first attempt to overcome this drawback was made in [6], by adopting an active-bootstrapped technique to minimise the quiescent drain-source voltage of diode-connected transistors M1 and M3. A more effective approach was recently proposed in [7], which exploits dynamic biasing. However, this method requires a switched-capacitor biasing network. This constitutes an overhead often precluding its use in applications where circuit simplicity is of primary importance. Moreover, switching noise can represent a limit in certain high-accuracy applications [5].

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In this paper, a continuous-time CMOS class AB current mirror which can be operated from a 1-V supply voltage is presented. The circuit uses poly resistors and two auxiliary differential amplifiers to achieve low-voltage operation, as well as control of quiescent currents and input bias voltage. Simulations on a designed example implemented in a 0.5-µm standard technology show input/output resistances of 5 kΩ / 3.6 MΩ, DC current gain of about 30 10^{-3} dB, and bandwidth of 140 MHz.

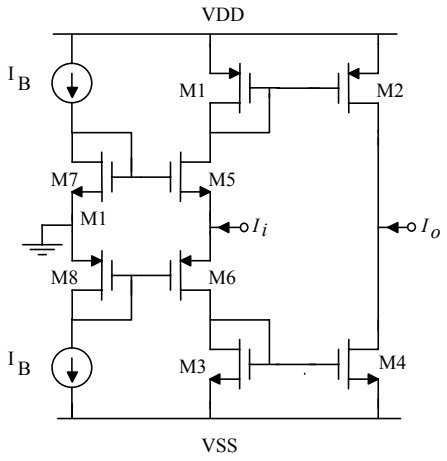

Figure 1: Conventional class AB current mirror.

2 Proposed Solution

Figure 2 illustrates a simplified schematic of the proposed class AB current mirror.

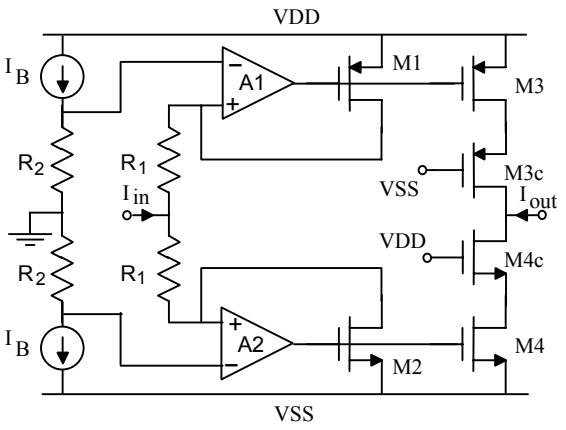

Figure 2: Simplified schematic of the proposed circuit.

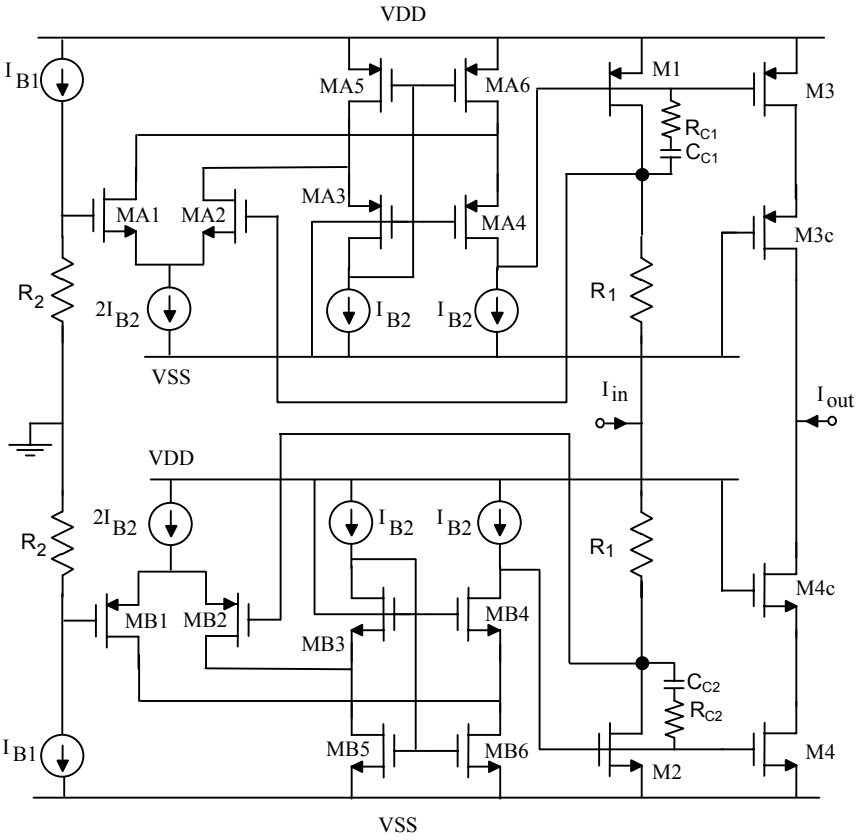

Figure 3: Detailed schematic of the proposed circuit.

In this scheme, transistors M5-M8 of Fig. 1 are replaced by resistors R_1-R_2 and auxiliary amplifiers A1-A2. The amplifiers input terminals are biased to a value close to the supply voltages (VDD or VSS for A1 and A2, respectively). Therefore, they are not critical, provided they work within their input common mode ranges.

Transistors M1-M2 are the input devices. Their drain potentials, thanks to the action of A1 and A2, are kept to a constant value, $V_{GND}+R_2I_B$ and $V_{GND}-R_2I_B$, respectively, just over their saturation voltages. In this way, the quiescent current of M1-M2 is controlled by a resistance ratio and is ideally given by $(R_2/R_1)I_B$. Also, the analog ground is accurately reflected to the input terminal. Input signal current is provided to transistors M1-M2 via resistors R_1 and is mirrored to the output terminal through M3-M4. Of course, the input resistance of the circuit is about equal to $R_1/2$. Thus, a trade off between input resistance and current consumption must be achieved. Cascoded transistors M3c and M4c are used to increase the output resistance and to limit the channel-length modulation effects on the output current linearity.

A more detailed schematic diagram of the circuit is illustrated in Fig. 3. Low-voltage auxiliary amplifiers with n-type and p-type source-coupled pair (transistors MA1-MA2 and MB1-MB2) have been adopted. The symmetry of the topology ensures low systematic and random offsets. Observe that these offsets appear directly as an input offset voltage.

The amplifiers form a high-gain loop which usually need frequency compensation. It can be provided by Miller capacitors C_{C1} and C_{C2} with series nulling resistors R_{C1} and R_{C2} to eventually avoid the right-half-plane zero. We observe that in order to maintain transistors M1-M2 in saturation and to satisfy the minimum common-mode input range of A1-A2, the proposed circuit can be operated form a supply voltage as low as $V_T+3V_{DS,SAT}$.

The main limitation of the solution is however its sensitivity to fabrication process variations. Indeed, variations in I_{B1} (as well as in the value of resistors R_2) can cause an unacceptable decrease (increase) of the gate potential of transistor MA1 (MB1), This means, in turn, that transistors implementing current generators $2I_{B2}$ can leave their saturation region. Considering MA1 (which is the most critical one, since its threshold is affected by the body effect in an n-well process) it needs a gate voltage not lower than $V_T+2V_{DS,SAT}$. In order to compensate for the unavoidable tolerances, the simple tuning circuit in

Fig. 4 can be used, where nominally resistor R is perfectly matched to resistor R_2 (in Figs. 2 and 3). Assuming to have generated a reference voltage V_R greater than $V_T+2V_{DS,SAT}$, the negative-feedback action of the error amplifier, A, ensures that the current of transistor M is equal to $(V_R–V_{GND})/R$.

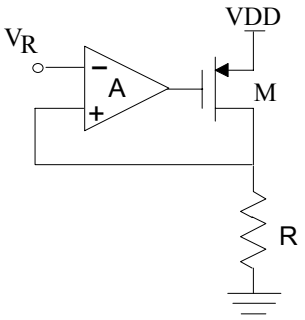

Figure 4: Tuning section for reducing the effects of process tolerances.

3 Simulation Results

The circuit in Fig. 3 was simulated using SPICE and the process parameters of a standard 0.5-µm CMOS technology. Since the transistor threshold voltages are around 0.6V, a 1-V power supply was chosen. Transistor dimensions and other electrical parameters are given in Table 1.

Component	Value
M1, M3	240/0.5
M2, M4, M4c	200/0.5
M3c	400/0.5
MA1, MA2, MB3-MB6	20/0.5
MB1, MB2, MA3-MA6	50/0.5
I_{B1}	30 µA
I_{B2}	5 µA
R_1, R_2	10 kΩ
VDD	1 V
VSS	0 V

Table 1: Component values.

Equal values for R_1 and R_2 were chosen to simplify design and to minimize the effects of resistors tolerances. No explicit frequency compensation was necessary. Indeed, compensation is accomplished by the parasitic gate-source and gate-drain capacitances of the relatively large input/output devices (M1-M4).

The circuit input resistance was found to be 5.01 kΩ while the output one was 3.6 MΩ. Figure 5 shows the dc transfer characteristic I_{OUT} versus I_{IN}. With the chosen design values, the maximum delivered current before output (soft) saturation is about 100 µA.

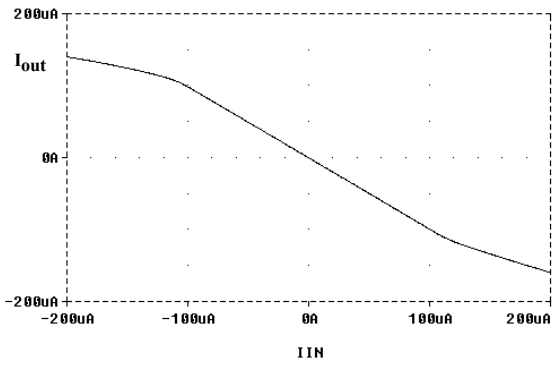

Figure 5: Transfer characteristic I_{OUT} versus I_{IN}.

THD of the short-circuit output current for a 10-μA_{p-p}, 50-μA_{p-p} and 100-μA_{p-p}, 100-kHz input signal was –64 dB, –56 dB and –42 dB, respectively.

Figure 6 shows the frequency response of the current gain. The DC value is 0.03 dB and the –3-dB frequency is around 140 MHz.

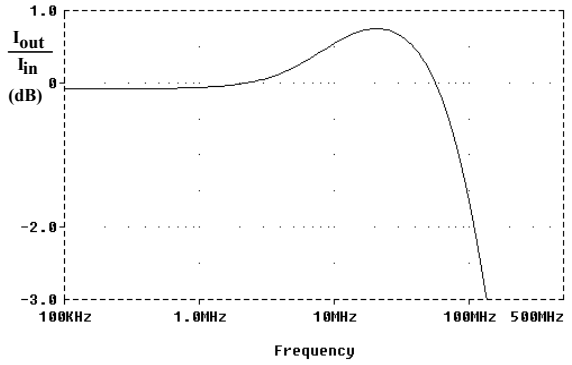

Figure 6: Magnitude of the current transfer gain I_{out}/I_{in}.

The response of the circuit to a 20-µA input step is shown in Fig. 7. The 1% settling time is lower than 70 ns in both positive and negative transitions.

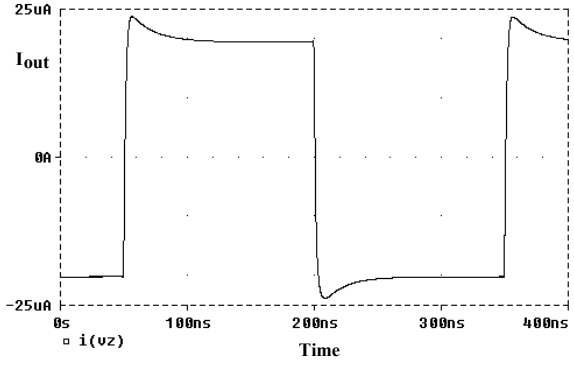

Figure 7: Response of the circuit to a 20-µA input step.

4 Conclusion

The current mirror described in this paper uses a novel biasing approach for designing class AB current-mode circuits with an extremely low-voltage capability. Actually, the circuit is an example of application of the proposed technique, which can be applied in the design of a wide variety of current-mode building blocks such as current comparators, current amplifiers, etc [5]. Investigations towards this direction are currently in progress.

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