A 29 dBm, 50% PAE, 1.9 GHz Power Amplifier
Using a 20 GHz f_T Silicon Bipolar Technology

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Abstract - This paper presents the design and measured performance of a monolithic integrated power amplifier for 1.9 GHz wireless communications. The chip was fabricated using a low-cost 20-GHz-f_T silicon bipolar technology. On-chip inductors and MIM capacitors were used to provide interstage matching and a variable-gain first stage was included for efficient power control purposes. At a 3.3 V supply voltage the amplifier delivers 29 dBm continuous-wave (CW) output power with 50% PAE. A 30.2 dBm maximum output power is attained at 4.5 V with 53% PAE. The small signal gain is 30 dB. This performance compares favorably with the results achieved by more expensive sub-µm Si bipolar technologies.

1 Introduction

Extended operating time has become a fundamental requirement for battery-operated systems such as handsets for mobile communications. Power amplifiers [1] are the most power consuming components in portable equipment, so high power-added efficiency is greatly required to enable long talk time and save battery life. Moreover mobile telephones must be small and lightweight. Power amplifier bias voltage dictates the required number of battery cells which principally affects overall size and weight. Therefore supply voltage reduction is a key design goal too.

Meeting both the above requirements by a silicon bipolar technology is a difficult challenge. Under low voltage conditions, silicon BJT conduction losses and charge storage effects become prominent, thus limiting the maximum achievable output power and PAE. In the past years GaAs and SiGe technologies have dominated the power amplifier market because of their excellent high-frequency performance even at low bias voltage [2-4]. However, the drawback with these devices is an increased chip cost, which in turn limits high volume production.

Recently, efforts have been made in the design of less expensive silicon bipolar power amplifiers for wireless applications. Outstanding performance has been reported by Simburger et al. both at 900 MHz [5] and 1.9 GHz [6]. Nevertheless these results were achieved by using advanced sub-µm silicon bipolar technologies with f_T values as high as 25 times the operating frequency. Additionally, a differential approach is proposed in [5] and [6] which suffers from off-chip balun losses unless high quality components are used for the output power combining.

This work demonstrates silicon BJT’s potentialities for 1.9 GHz constant-envelope applications. A monolithic single-ended power amplifier has been designed using a low-cost 20-GHz silicon bipolar process. The results presented herein show that an accurate design can lead to results as remarkable as the ones achieved by means of faster and more expensive technologies.

2 Theory and Circuit Design

Linearity is not the main problem in constant-envelope modulation schemes such as Gaussian Minimum Shift Keying (GMSK) which is used in GSM and DCS systems. Information is conveyed in the phase of the modulated signal whose amplitude is kept constant. Therefore, power amplifiers are usually operated in nonlinear high-efficiency classes. Power-added efficiency can be optimized by properly loading the transistors at both the fundamental and harmonic frequencies with multiple-resonator networks (class-F power amplifiers [7]). The goal of harmonic tuning is to shape the collector waveforms to let the collector current flow when the collector voltage is low and vice versa, thus minimizing transistor power consumption.

In class-F power amplifiers, an ideal 100% PAE is asymptotically achieved by using a load network which behaves either like an open or a short circuit at harmonic frequencies. Unfortunately, package parasitics and process tolerances make the implementation of such multi-resonator loads quite difficult at RF frequencies. Therefore, a single-resonator solution was selected for this work (only second harmonic control was allowed). According to nonlinear simulations, best power performance is achieved when an open circuit appears at the device output at the second harmonic frequency, i.e. with a series-resonant load. Such a load leads to a pulsed collector voltage, while the collector current is maintained sinusoidal as shown in Fig. 3 (mixed-C
mode [8] or Class C-E [9]). Dual waveforms (i.e., pulsed current and sinusoidal voltage) are generated if a parallel-resonant load is used. However, the resulting higher current peak would cause a reduction in PAE due to the increased voltage drop across the collector series resistance.

Fig. 1 shows a simplified circuit diagram of the amplifier. It is composed of a variable-gain first stage (T1-T3), a driver stage (T4), and a power stage (T5). The external voltage $V_C$ sets the amount of signal current in T1 which flows into T2. Thus, gain and power control is achieved without changing the bias current in T1 and hence the input matching.

![Variable-gain amplifier](image)

Figure 1. Simplified schematic of the PA.

To provide the final stage with a series-resonant load and achieve the waveforms given in Fig. 3, both lead and bondwire inductance $L_W$ was properly accounted for. In contrast, class A operation was selected for both the first and the second stage to meet gain requirements. Spiral inductors and MIM capacitors were used to provide on-chip interstage matching which was designed for maximum gain under large signal conditions. The goal of maximum bandwidth was also considered to compensate for device process tolerances. Since high quality passive components in the output matching network are required to preserve power performance, an off-chip solution was chosen in our design. Both driver and power stages use external pull-up inductors. As an alternative to RF chokes, PCB quarter-wave shorted stubs can also be employed for better second harmonic suppression.

The circuit shown in Fig. 1 was implemented in a standard 20-GHz-frequency self-aligned-emitter silicon bipolar process from STMicroelectronics. This low-cost technology requires only 17 mask steps and is provided with npn transistors, three metal layers, two poly resistor layers, and 0.7-fF/µm$^2$ metal-nitride-metal capacitors. On-chip spiral inductors are also available by recourse to the third metal layer (3-µm-thick AlTi, $3\times10^7$ S/m). A close honeycomb-patterned oxide trench is used to break up the buried layer below the metal spirals, thus preventing eddy currents and inductance reduction. No additional mask step is required, since the same trench is also employed for the lateral isolation of transistors. Spiral inductors fabricated with this technique exhibit Q values up to 9 at 1.9 GHz and resonant frequencies above 10 GHz, which make them suitable for on-chip matching networks. Fig. 2 shows the photo and the measured performance of inductor $L_2$.

![Inductor L2](image)

Figure 2. Inductor $L_2$. (a) Photo. (b) Measured inductance and Q.

To provide an accurate model of PA transistors free from measurement limitations due to high power levels, the model parameters were extracted from a unity scaled-down power cell. It consists of four 1.6×25 µm emitter fingers (160 µm$^2$ total emitter
The unity cell shows a maximum forward current gain of 60, a 19-V BV\textsubscript{CBO}, and a 6-V BV\textsubscript{CEO}.

An improved Gummel-Poon large signal model was used to accurately describe the nonlinear behavior of transistors. The standard model was modified to account for the Kirk effect which strongly affects BJT performance under high-current low-voltage conditions. Extensive S-parameter measurements were performed under various bias conditions in order to extract best-fitting nonlinear model parameters. Based on the results of circuit simulations, single-cell devices were used for the VGA, a 4-cell BJT for the driver, and a 20-cell one for the power stage.

Passive component modeling is an important issue as well, since changes in the matching circuitry can result in severe degradation of power gain and PAE. Therefore, extensive electromagnetic simulations using ADS Momentum were performed for inductors and an S-parameter modeling was defined to accurately account for high frequency effects.

The circuit was simulated using the harmonic balance method with ADS (Advanced Design System). Fig. 3 shows the simulated voltage and current waveforms at the collector of the power stage.

![Figure 3. Simulated output waveforms of the power stage.](image)

**3 Experimental Results**

A die photo of the fabricated amplifier is shown in Fig. 4. The chip size is 2.1 mm by 3.2 mm.

To achieve high gain, the minimization of emitter parasitic inductance is of paramount importance. Therefore, the die was molded in a small plastic 20 lead EP TSSOP package, which provides an exposed bottom pad for RF grounding and heat dissipation. Package size is 4.4 × 6.5 × 0.9 mm and thermal performance achieves a $\theta\text{JA}$ of 40 $^\circ$C/W. A 18 mil clearance around the die allowed ground downbonding, thus avoiding the cost of substrate via holes. Moreover, the wafers were lapped to a 9 mil thickness for shorter downbonds. The critical ground inductance was lowered to a suitable value by means of an on-chip ground plane (3\textsuperscript{rd} metal layer) and 25 downbonding wires.

![Figure 4. Die photo of the power amplifier.](image)

Measurements were performed on a 400-μm-thick FR4 substrate to agree with the production environment. Partially distributed impedance transformation networks were used for input and output matching. High-Q inductors and capacitors were employed at the output to preserve PAE performance.

Fig. 5 shows the CW output power and power-added efficiency characteristics versus input power at 1.9 GHz. A 29 dBm output power and 50% PAE are obtained while operating at 3.3 V. The small signal power gain is 30 dB. The second and third harmonic levels are 43 dB and 35 dB below the carrier respectively. Best power performance is achieved at 4.5 V bias voltage, since the circuit exhibits 30.2 dBm output power and 53% PAE with unchanged matching networks.

Output power versus operating frequency is shown in Fig. 6. It is worth mentioning that gain variation over the entire PCS transmit window (1850-1910 MHz) is less than ± 0.2 dB. This results from the use of maximum-bandwidth matching networks for process spread compensation.

Fig. 7 shows the dependence of the output power on control voltage $V_C$. Thanks to the proposed VGA stage, output power level is successfully controlled over a 20 dB dynamic range. To adjust the device to any desirable input control voltage range, the slope of the curve can easily be varied by merely changing the value of the series resistor $R_C$.  

![Figure 5. CW output power and power-added efficiency characteristics versus input power.](image)

![Figure 6. Output power versus operating frequency.](image)

![Figure 7. Dependence of the output power on control voltage $V_C$.](image)
The device achieved 29 dBm output power, 50% PAE, and 30 dB small signal gain at 3.3 V supply voltage. At 4.5 V an output power of 30.2 dBm was obtained with a power-added efficiency of 53%. This outstanding performance was achieved by optimum second harmonic tuning (series-resonant load) and emitter parasitic inductance minimization (exposed pad package). A power control function was also demonstrated, which is provided by a variable-gain first stage. To our knowledge, these results represent the best power performance reported so far for a 1.9-GHz-band monolithic PA using a non-sub-µm silicon bipolar process.

This work demonstrates the potential of silicon bipolar technology for low cost and high volume fabrication in portable wireless applications.

4 Conclusions

A 1.9 GHz three stage power amplifier with on-chip interstage matching was designed and implemented using a silicon bipolar process by STMicroelectronics.

References


