Some New Analogic CNN Algorithms for PCB Quality Control

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Abstract - In PCB production process different errors can occur. The detection of these errors is time consuming. To overcome this problem new analogic CNN algorithms were developed to detect the short circuit and the misalignment errors. These analogic algorithms were tested by software simulator, by a 20*22 CNN-UM chip and by a 64*64 CNN-UM chip by using a ALADDIN System.

1. Introduction

Several algorithms were developed in connection with Printed Circuit Board (PCB) quality control [2], [3], [4], [5], [6]. The layout error detection process is time consuming. The Cellular Neural Network (CNN) paradigm [7a], [7b] and it's analog VLSI implementations, [10] provide a very high computing power. Due to the local connectivity of the CNN cells, the local layout errors can detect the errors effectively. Analogic CNN algorithms were developed to detect certain types of layout errors [8]. Misalignment and a new short circuit detection analogic CNN algorithm will be shown in this contribution. The ALADDIN simulation environment, the CNN Chip Prototyping System (CCPS), with 20*22 CNN-UM chip [9], and 64*64 CNN-UM chip [10] were used in the development and test phases of our layout detection algorithms.

In the following chapters we would like to show two new analogic CNN algorithms for PCB layout error detection. The misalignment error detection algorithm is shown in section 2 and short-circuit detection in section 3. In section 4 two examples, some measuring results and the conclusions are given.

2. Misalignment Detection Algorithm

The errors caused by inaccurate alignment of artwork film to the drilled PCB plate are going to be detected by the analogic CNN algorithm. (Figure 1)

Here we assume that the minimal size of a geometrical object is covered by 2-3 pixels (CNN cells). Depending on the PCB technology different branches of the analogic CNN algorithm are used.

The algorithm is built up of three parts, in which the first and last three steps are common, and the main part of the algorithm can handle the different type of PCBs. In the first part we make a gray-scale to black&white conversion by using for example the average template or some non-linear filtering templates [9]. The base of the three parts is the logical AND function.

If the artwork film is of “FILLED” type, (see Figure 4) then we use logic AND function between the artwork film and the drilled PCB. In this case the pads have to have via-holes in the image. Due to the AND function, the via-hole with black color and the edge of the pads of the result is of black color. Some single black pixels can remain on the result image there are no errors and they are removed by the smkiller.tem. After that we increase the black objects (the errors) by the dilation.tem [9].
3. A Short Circuit Detection Analogic CNN Algorithm

An analogic algorithm is given here to detect short circuit between the two equipotential areas. The inputs of this analogic CNN algorithm are the two production layers of a PCB and the marker images to define the two objects belonging to two different equipotential nodes. The main steps of our short circuit detection analogic CNN algorithm can be seen in Figure 2.
In the first step by the algorithm the input images are converted into black & white ones. We start a wave from the marker image to reconstruct the layout elements belonging to this node. The tracks of the different signals can be found by a wave. The waves arise on the marker image but the form of the waves follows the tracks of the current production layer by using “recall.tem”. [9]

The same algorithmic step is used for the other production image and the other marker image. From the pads that we found on the top layer we start the waves on the bottom layer. The tracks were removed by some erosion steps, so the result image is generated.

Next we download the reference image into a platform. It is a black & white image and includes some pads of different signals (VDD, VSS). We shall compare the two images of the pads by using the logic AND function.(There are only the pads on the result image.)

If we get several pads on the result image, it means that there is at least one short-circuit on one of the production layers.

4. Conclusions

On Figures 3, 4 and 5 the inputs and result images the misalignment error detection can be seen (test image size were 314*302 pixels). On Figures 6, 7 and 8 the inputs and the result images can be seen (176*144).
The templates used in this layout error detection algorithm are stable due to symmetric “A” templates. The analogic CNN algorithms were tested not only on ALADDIN Software Simulator but they were implemented on a 20*22 binary input/binary output CNNUM chip, a 64*64 analog input/analog output CNNUM as well.

<table>
<thead>
<tr>
<th>Algorithms</th>
<th>Pentium 466 MHz</th>
<th>20*22 CNNUM</th>
<th>64*64 CNNUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Misalignment error detection</td>
<td>9.28 sec</td>
<td>52 msec</td>
<td>22 msec</td>
</tr>
<tr>
<td>Short-circuit detection</td>
<td>105 sec</td>
<td>N/A</td>
<td>90 msec</td>
</tr>
</tbody>
</table>

* The running time of the algorithms core is 30 msec.

Tabel 1. Running times of the two analogical algorithms on the PC and on the CNN chip

References