Non-quasi-static charge injection modeling in analog MOS switches

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Abstract – **In this paper, we present a simplified, design-oriented model for the transient behaviour of a short-channel MOS transistor operating in the non-quasi static regime. The proposed formulation is dedicated to model the charge injection effects in MOS analog switches at high operating speed. The model has been implemented in MATLAB: it is shown that the results are in good accordance with other, more complex models.**

1 Introduction

The error voltage on the hold node induced by the turning off of an MOS switch is one of the fundamental factors that limit the accuracy of switched-capacitor circuits [1], analog-to-digital and digital-to-analog converters, filters, sample-and-hold circuits [2] and current mode circuits [3]. An MOS transistor holds mobile charges in its channel when it is on. When the transistors turns off, part of the mobile charges is transferred to the hold capacitor and causes an error in the sampled voltage V_L (see Fig.1).

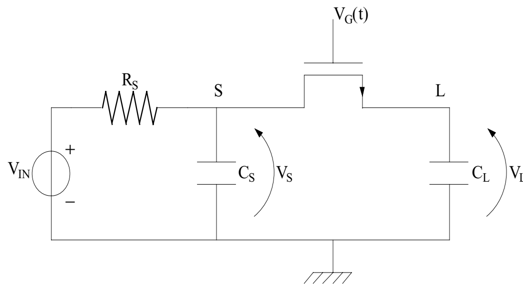

Figure1: Circuit for analysis of switch charge injection.

In addition to the charge from the channel, the charge associated with the feed through effect of the gate-to-diffusion overlap capacitance also enlarges the error voltage when the switch turns off [4].

In the QS (quasi-static) modeling approach, the channel charge is assumed to achieve equilibrium once biases are applied, thus the finite charging time of the carriers in the inversion layer is ignored. This gives erroneous simulation results for signals with rise or fall time comparable to or smaller than the channel transit time. In [5] a thorough analysis of NQS (non-quasi-static) models is introduced; on the other hand, in the NQS models (see for example [6]) the complexity of the formulations prohibits intuitive insight into NQS effects. Most of these models consider the transient and ac small-signal behavior separately, leading to inconsistent simulation results in the time domain and frequency domain.

Our aim is to model the charge injection in analog MOS switches and to present an effective, simple and "physical" model based on the NQS approach; the model should give intuitive physical insight to aid circuit designers to evaluate charge injection effects at high operating speed. The model has been implemented in MATLAB and it has been verified with a comparison with the results obtained in [6].

We based our approach on the model developed in [5], which represents a robust physical NQS (non-quasi-static) model for both transient and ac small-signal analysis: it is based on the channel charge relaxation approach; anyway it is dedicated to circuit simulation programs.

The model formulation and the basic assumptions adopted in its development are presented in Section 2. The MATLAB simulation results are introduced and discussed in Section 3. The conclusions are drawn in Section 4.

2 Model Formulation

We assume that the charge pumping phenomenon [3] is negligible and that the channel charge exits through the source and drain electrodes when the transistor turns off. This assumption holds true when operating at high speed.

The circuit schematic used for analysis is shown in Fig.1. Capacitance C_L is the lumped capacitance at the data-holding node. Resistance R_S could be the output resistance of an operational amplifier, while capacitance C_S could be the lumped capacitance associated with the amplifier output node. In the reference circuit, the resistance R_S is connected to a signal voltage source V_{IN}. In our analysis we assume that the value of V_{IN} is constant. In other words we take into account only a transient on the signal $V_G(t)$.

At first we set R_s and C_s to 0 to perform a comparison with results obtained in [6] and then to

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validate our model. Then we will come back to the ganeral case shown in Fig.1 to fully derive our model.

The KCL at node A requires (R_s =0 C_s = 0):

$$C_L \frac{dv_L}{dt} = -I_{DS}(t) + \frac{C_G}{2} \frac{d(V_G(t) - v_L)}{dt} \quad (1)$$

where v_L is the error voltage at the data-holding node,$V_G(t)$ is a ramp function which falls linearly from the high value V_h toward the low value V_L (in this work V_L=0) at a falling rate U: $V_G(t)=V_h$-Ut. C_G is the total gate capacitance, including both the channel capacitance and gate-to-source and gate-to-drain overlap capacitances (we assume that C_{OVd}= C_{OVs}= C_{OV}): C_G=WLC_{OX} + 2 C_{OV}, where C_{OX} is the gate capacitance per unit area.

From [5]:

$$I_{DS}(t) = I_{DS}(t)\big|_{DC} + \frac{|Q_{def}(t)|}{\tau} \quad (2)$$

where $I_{DS}(t)\big|_{DC}$ represents the current of the MOS transistor in strong inversion (linear region), then

$$I_{DS}(t)\big|_{DC} = \beta(V_h - V_{IN} - V_{TE} - U \times t)(v_L - v_S)$$

where

$$\beta = \mu C_{OX} \frac{W}{L}$$

and V_{TE} is the effective threshold voltage including the body effect [7] and μ is the electron mobility.

Q_{def} is a variable introduced to keep track of the amount of deficit (or surplus) channel charge necessary to achieve equilibrium at a given time t and τ represents the delay due to the RC distributed network in the channel [5]. The value of the channel relaxation time constant τ is composed of the diffusion component which dominates in the subthreshold region and of the drift component which dominates in the strong inversion region [5]. We neglect the subthreshold conduction of the MOS transistor, then τ is only composed of the drift component τ_{drift}. The drift component is computed on the basis of the RC Elmore equivalent ε (see below for the meaning of Q_{cheq}):

$$\tau \approx \tau_{drift} \approx \frac{C_G L^2}{2\varepsilon\mu Q_{cheq}}$$

Supposing that $\left|\frac{dV_G}{dt}\right| >> \left|\frac{dv_L}{dt}\right|$ equation (1) becomes:

$$C_L \frac{dv_L}{dt} = -I_{DS}(t) - \frac{C_G}{2} U \quad (3)$$

By arranging equations (1), (2) and (3) we obtain:

$$C_L \frac{dv_L}{dt} = -\beta(V_h - V_{IN} - V_{TE} - Ut)v_L + \frac{|Q_{def}|}{\tau} - \frac{C_G}{2} U$$

Q_{def} must satisfy the following equation [5]:

$$\frac{dQ_{def}(t)}{dt} = \frac{dQ_{cheq}(t)}{dt} - \frac{Q_{def}(t)}{\tau}$$

where

$$Q_{cheq}(t) = C_G(V_G(t) - V_{IN} - V_{TE})$$

Thus we obtain the following equations system:

$$\begin{cases} C_L \frac{dv_L}{dt} = -\beta(V_h - V_{IN} - V_{TE} - Ut)v_L + \frac{|Q_{def}|}{\tau} - \frac{C_G}{2} U \\ \frac{dQ_{def}(t)}{dt} = -C_G U - \frac{Q_{def}(t)}{\tau} \end{cases}$$

If we set $R_s \neq 0$, $C_s \neq 0$, we obtain the following equations system:

$$\begin{cases} C_L \frac{dv_L}{dt} = -\beta(V_h - V_{IN} - V_{TE} - Ut)(v_L - v_S) + \frac{|Q_{def}(t)|}{\tau} - \frac{C_G}{2} U \\ \frac{v_S}{R_S} + C_S \frac{dv_S}{dt} = \beta(V_h - V_{IN} - V_{TE} - Ut)(v_L - v_S) + \frac{|Q_{def}(t)|}{\tau} - \frac{C_G}{2} U \\ \frac{dQ_{def}(t)}{dt} = -C_G U - \frac{Q_{def}(t)}{\tau} \end{cases}$$

3 Simulation results

The previous model has been implemented using MATLAB. In this Section, we report the simulation results obtained using the ATMEL CMOS 0.5μm minimum channel length technology.

The quasi-static model can be used with acceptable results if the falling time t_F of $V_G(t)$ satisfies the condition [7]:

$$t_F \geq k\tau_0 \quad (4)$$

where

$$\tau_0 = (1+\delta)\frac{L^2}{\mu(V_h - V_{TE})}$$

and

$$\delta = \frac{\gamma}{2\times\sqrt{\phi_B + V_{SourceBulk}}}$$

γ is the body factor, Φ_B is the "built-in" potential.

It is emphasized that the above is only a rough rule of thumb. Depending on the application, the factor k is anyway > 10.

Using the ATMEL CMOS 0.5µm minimum channel length technology and assuming L = 5µm and V_h = 3V, we obtain: $\tau_0 \cong$ 28ns.

Then from (4): $t_F \geq$ 280ns.

Since $U = \frac{V_h}{t_F}$, we obtain: $U \leq 10^7$.

Figs.2, 3 and 4 show a comparison with the results presented in [6] (R_s = 0, C_s = 0). To this end the values of the parameters (in particular the values of L), reported in the figures captions, have been choosen following what reported in [6]. The value of the Elmore equivalent constant ε has been set to 32.

Fig.2 shows the error voltage on the hold node v_L at the end of the falling ramp of $V_G(t)$ against the gate voltage falling rate U for several values of the signal voltage level.

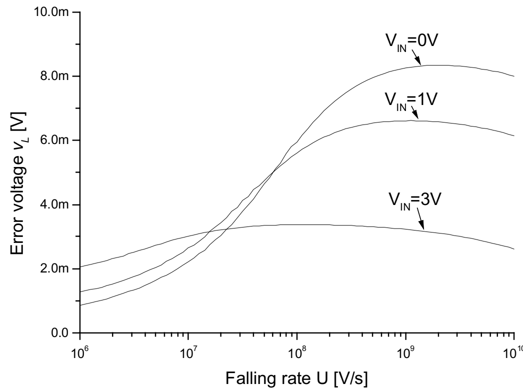

Figure2: Switch induced error voltage v_L against gate voltage falling rate U for several values of the signal voltage level. C_L = 2 pF, W = 4 µm, L = 3.3 µm ,V_h = 5V.

Fig.3 shows the error voltage on the hold node v_L against the ratio between the gate fall time t_F and the device transit time τ_0 for two values of the ratio between the load capacitance C_L and the pass-transistor capacitance C_G.

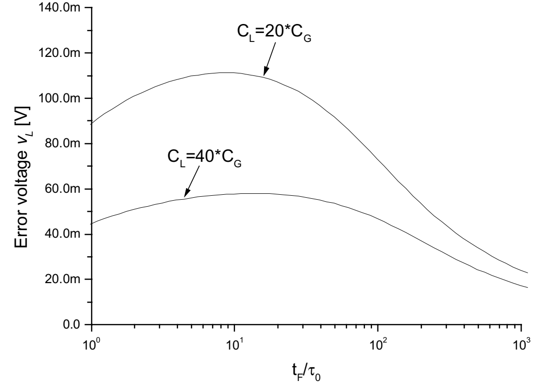

Figure3: Switch induced error voltage v_L against fall time / transit time ratio for two values og the load-capacitance/pass transistor capacitance ratio. C_L = 2 pF, W = 8 µm, L = 4 µm , V_h = 5V, V_{IN} = 0.

Fig.4 shows, for a 5-V gate falling ramp, the minimum precision achiavable with a switch pass-transistor as a function of the ratio between the load and pass-transistor capacitance. As can be seen, the precision increases with the capacitance ratio.

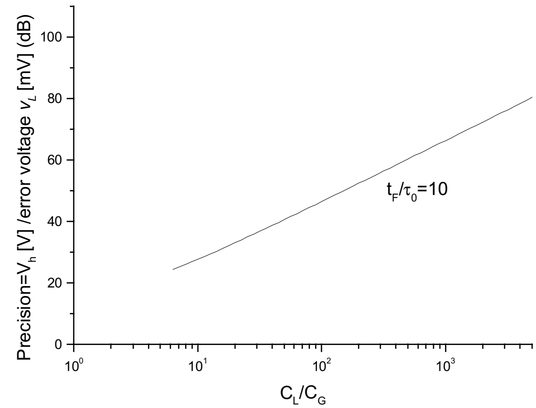

Figure4: Precision achiavable with pass-transistor against load-capacitance / pass-transistor capacitance ratio. C_L = 2 pF, W = 8 µm, L = 4 µm , V_h = 5V, V_{IN} = 0.

The results reported in Figs.2, 3, 4 are in good accordance with the results reported in [6]: the comparison results validate the model derivation.

In the results reported in Fig.5, we set $R_s \neq 0$, $C_s \neq 0$ (general case). Fig.5 compares the results using a Quasi-Static (QS) [5] and the Non-Quasi-Static (NQS) (our model) modeling approach

Fig.5 shows the error voltage on the hold node v_L at the end of the falling ramp of $V_G(t)$ against the gate voltage falling rate U for several values of the signal voltage level. The error voltage on the hold node v_L in

the QS model increases with increasing falling rate toward a saturation value. Conversely, the NQS approach, which takes into account channel charge inertia, gives an error voltage behavior which exhibits a maximum then it starts to decrease at higher values of U. Moreover the error voltage in NQS approach is lower than the value predicted from QS analysis.

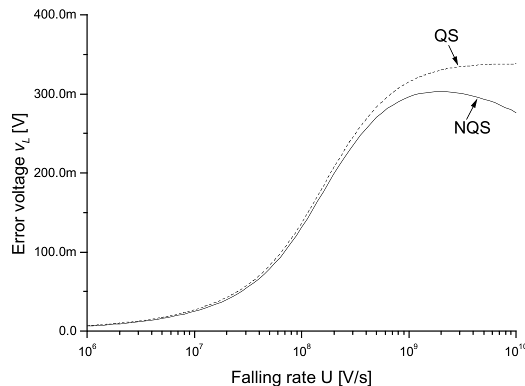

Figure5: Switch induced error voltage v_L against gate voltage falling rate U using our model (NQS) and a Quasi Static (QS) model. C_L = 5 pF, $C_S = C_L$, W = 50 μm, L = 5 μm , V_h = 3 V, R_S = 1 kΩ.

4 Conclusions

In this paper, a simplified, design-oriented model for the transient behaviour of a short-channel MOS transistor operating in the non-quasi static regime has been presented and discussed. The proposed formulation is dedicated to model the charge injection effects in MOS analog switches at high operating speed.

It has been shown, through simulations using MATLAB and the ATMEL CMOS 0.5μm minimum channel length technology, that the results are in good accordance to previously reported, more complex device models.

The model is intended for supporting circuit designers in their first step evaluation of achievable performance.

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