A Very Accurate Averaging Circuit Technique for the Switched Capacitor DAC.

Hristo Hristov* and Angel Popov*

Abstract - **A simple and efficient method for improving the linearity of a two - capacitor charge redistribution digital - to - analog converter (DAC) is presented. This method utilizes consecutive interchanging of the voltages on the capacitors for each bit being converted. It is shown that the accuracy achieved by the proposed algorithm is orders of magnitude higher compared to this of the conventional method. Simulations have been performed and have proved the feasibility of this new technique.**

1 Introduction

The most effective in terms of area digital-to-analog converter is the two-capacitor DAC, where the analog part of the device comprises only two equal-valued capacitors and a few switches [1]. The requirement for equality however is sometimes hard to be satisfied for technology-based reasons.

Many techniques for compensating the mismatch of the converting capacitors have been described. Some implement a calibration cycle and storing digital correction terms in RAM [2], or optimizing the switching sequence for each input vector [3]. Others propose shaping and filtering out the error [4], or splitting the input digital word to facilitate error – free conversion [5]. However, time and area are wasted for the completion of these correction cycles. This confronts the DAC's main advantage – its small size.

2 Charge Redistribution DAC Basics

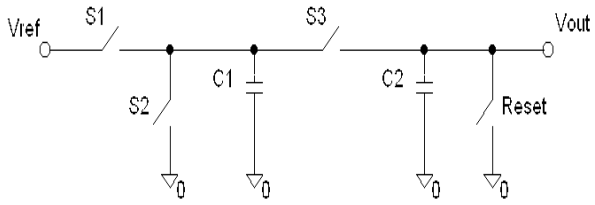

Figure 1: Basic schematic of the two-capacitor DAC.

* Sofia University of Technology, Computer Systems Department, 1756 Sofia, P.O. Box 90 BULGARIA, E-mail: h_hristov@vmei.acad.bg, anp@vmei.acad.bg, Tel: +359-2-651193.

The core schematic of the two-capacitor converter is shown in Fig. 1.

The conversion starts with closing of the 'Reset' switch. The least significant bit is considered first. Depending on the state of this bit either switch S1 or S2 is closed. Thus, capacitor C_1 is either connected to V_{ref} or discharged. When switch S1(S2) opens, S3 is closed to share the charge among C_1 and C_2. This is repeated until the last (MSB) bit. The resulting voltage on both capacitors at the end of the conversion is given by

$$V_{out} = V_{ref} \sum_{k=1}^{n} 2^{k-n-1}(1+\varepsilon)^{n-k}(1-\varepsilon)b_k \quad (1)$$

where n is the number of bits to be converted.

Here ε is the relative mismatch between C_1 and C_2 and is defined by

$$\varepsilon = \frac{C_2 - C_1}{C_2 + C_1} \quad (2)$$

The authors of this paper propose a method for reducing the influence of the capacitor mismatch error on accuracy without sacrificing much chip area.

3 Proposed Method

Consider the schematic, shown in Fig.2. It represents the basic two – capacitor DAC topology and as an addition - two sample–and–hold amplifiers.

The conversion of one bit consists of two phases – a precharging and an averaging one. The first determines the charging / discharging of capacitors C_1 and C_2, while the second is involved in refining the output. How this is done is described below.

3.1 Circuit Operation

Assume that the first bit to be converted is b_1. The precharging phase first takes C_1 as the charging capacitor and C_2 as the redistribution capacitor. The initial values of the charges on C_1 and C_2 are as follows:

$$Q_1 = V_{ref} C_1 b_1$$

$$Q_2 = 0$$

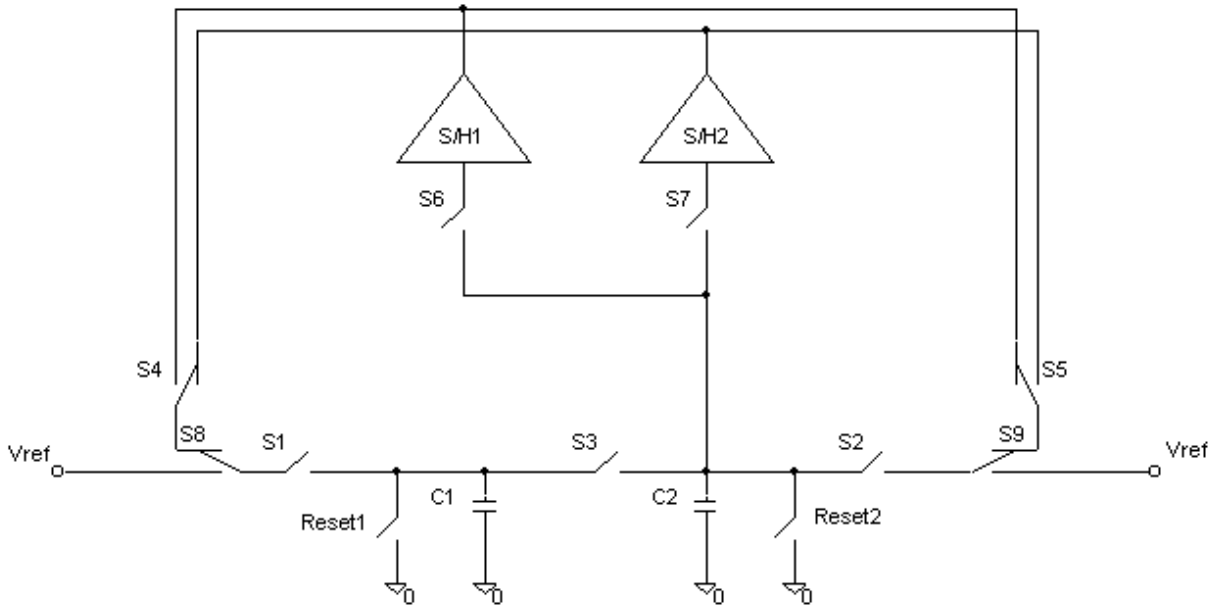

Figure 2: Proposed schematic with improved switching sequence.

These equations are the result of closing S1(or Reset1, depending on the value of b_1 while S8 is in position V_{ref}) and Reset2 switches. Next, S3 is closed to share the charges among C_1 and C_2. This ends up with a voltage V_1 across both capacitors:

$$V_1 = \frac{C_1}{C_1 + C_2} V_{ref} b_1 \tag{3}$$

It is easily shown that

$$V_1 = V_{nom} + \Delta V$$

where V_{nom} is the nominal (true) voltage and ΔV is the error voltage.

$$V_{nom} = 2^{-1} V_{ref} b_1$$
$$\Delta V = 2^{-1} \varepsilon V_{ref} b_1 \tag{4}$$

V_1 is stored in S/H1. Now C_1 is discharged (Reset1 is closed) and an operation similar to the one just performed is carried out. This time, however C_2 is the charging capacitor and C_1 – the redistribution one. Thus we obtain another voltage:

$$V_2 = \frac{C_2}{C_1 + C_2} V_{ref} b_1$$
$$V_2 = V_{nom} - \Delta V$$

It is stored in S/H2 and this is the end of the precharging phase.

In the averaging phase C_1 is charged to voltage V_1 and C_2 to voltage V_2. Now switches S8 and S9 are set to positions S4 and S5 respectively. Switches S4 and S5 are in turn set to positions S/H1 and S/H2 respectively.

$$Q_1 = V_1 C_1 = (V_{nom} + \Delta V) C_1$$
$$Q_2 = V_2 C_2 = (V_{nom} - \Delta V) C_2$$

After the closure of S3 the voltage across the capacitors will be

$$V_1^1 = V_{nom} - \Delta V \varepsilon$$

The superscript indicates the number of the cycle in the averaging phase.

Now C_1 is charged to V_2 and only after that is the new voltage stored in S/H2 – taken from C_2. C_2 is then charged to V_1. This complicated switching sequence is needed to avoid a third sample and hold amplifier.

After redistribution, the following voltage results

$$V_2^1 = V_{nom} + \Delta V \varepsilon$$

This is stored in S/H1. Now both sample-holds have the new voltages. If we substitute ΔV with its equivalent found in (4), we will get

$$V_1^1 = V_{nom} - 2^{-1} b_1 V_{ref} \varepsilon^2$$
$$V_2^1 = V_{nom} + 2^{-1} b_1 V_{ref} \varepsilon^2$$

As ε is normally less than unity, it is evident that these voltages will stand closer to the true voltage than V_1 and V_2 did. If the averaging phase is repeated, another pair of more accurate voltages appears.

If the averaging takes place for a bit with number k ($1<k<n$), i.e. before averaging begins C_2 has been

charged with voltage V_{k-1}, the following expression holds

$$V_{1,2}^{s} = \frac{1}{2}\left(1+\varepsilon^{s+1}\right)V_{k-1} + \frac{1}{2}\left(1\pm\varepsilon^{s+1}\right)b_k V_{ref}$$
$$V_{1,2}^{s} = \frac{1}{2}\left(V_{k-1}+b_k V_{ref}\right) + \frac{1}{2}\varepsilon^{s+1}\left(V_{k-1}\pm b_k V_{ref}\right) \quad (5)$$

Here s is the number of the cycle in the averaging phase, while the subscript 1,2 indicates V_1 or V_2. The usage of ± depends on which of the aforementioned voltages is used as an output.

4 Speed Considerations and Simulation Results

As the proposed circuit technique takes several cycles to obtain a value close enough to the true value, it is clear that the circuit will not achieve high speed of operation. This however is not as bad as it appears, for it will be shown that no more than two cycles are needed to attain 16-bit linearity with 3% capacitor mismatch. Moreover, averaging need not be done for every bit. Depending on the linearity achievable with a given technology one can choose the first MSBs for which averaging should be used and leave the rest of the input digital word "untouched" thus increasing the speed of operation.

Unfortunately extra clock cycles are not the only speed limitation with this circuit technique. As can be seen from Fig. 2, there are some cascaded switches, namely S1, S8, S4 and S2, S5, S9. This means increased time constant which reflects upon the maximum values used for C_1 and C_2. These values are in turn downside limited by kT/C noise inherent in SC circuits. So a trade-off has to be made between speed and accuracy.

The proposed circuit has been simulated to prove the functionality of the new method. A SPICE simulation result is shown in Fig. 3.

From the Figure

$$V_1 = 1{,}5510V$$
$$V_2 = 1{,}4540V$$
$$V_1^1 = 1{,}5003V$$
$$V_2^1 = 1{,}4991V$$

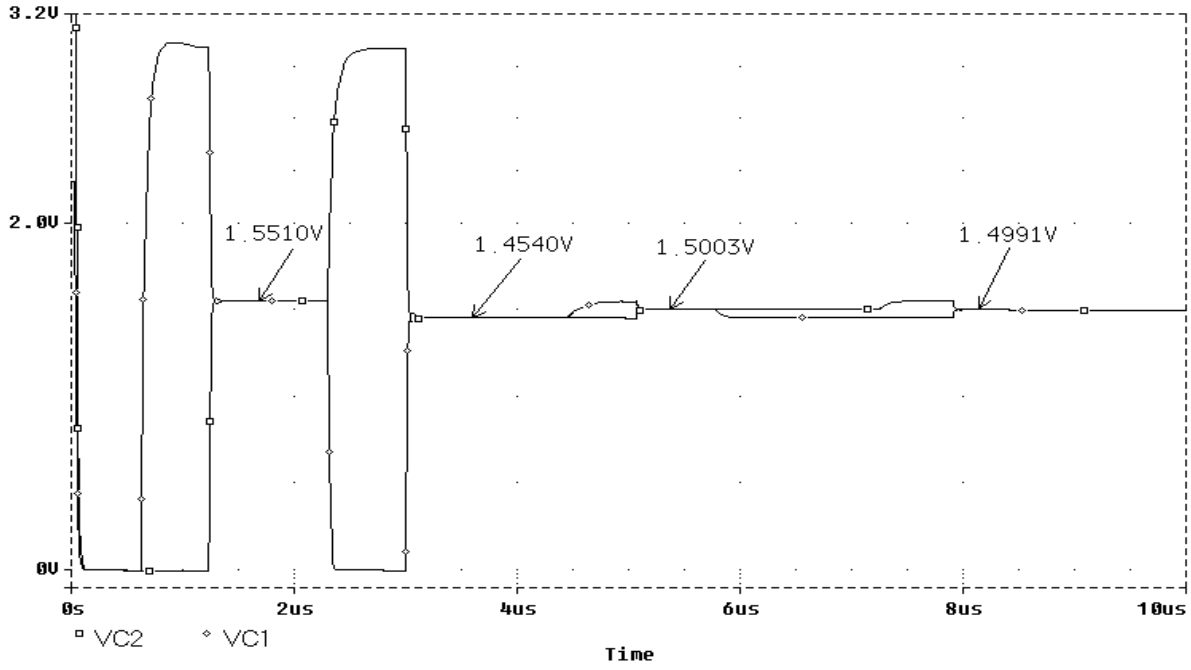

Figure 3: SPICE simulation result showing the precharging and averaging phases with V_{ref} = 3V, ε =0,03 and capacitors with nominal values of 10pF.

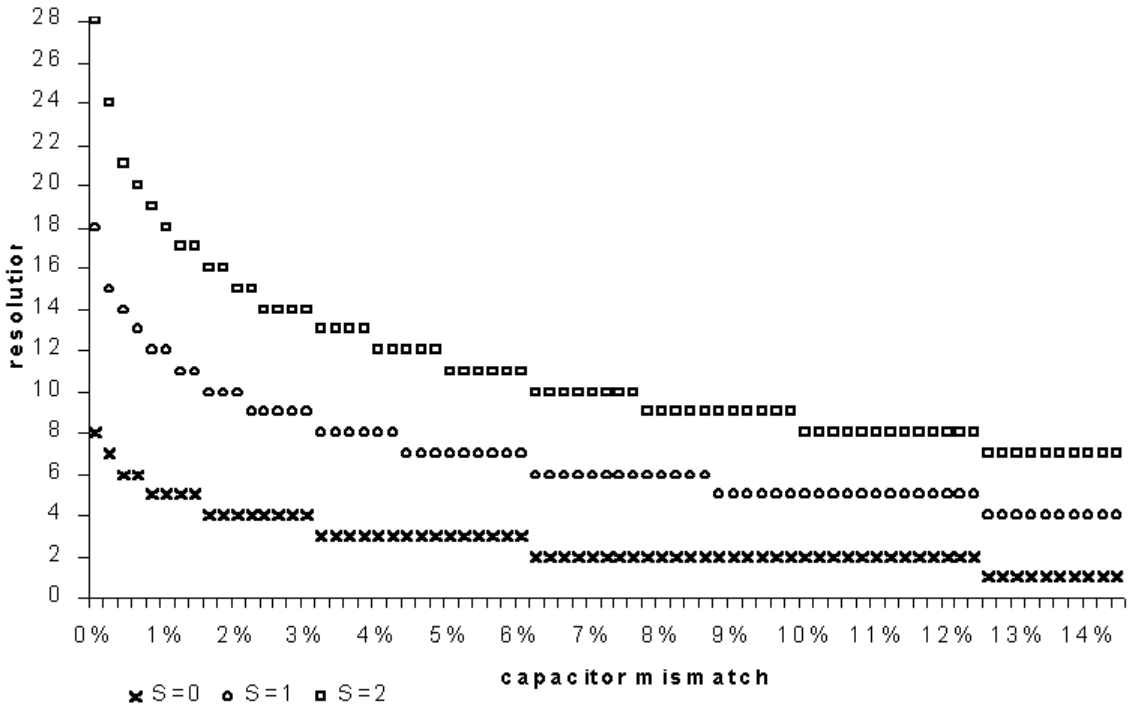

Figure 4: Theoretical resolution versus mismatch with 0,1 and 2 iterations.

The simulation shows that the proposed averaging technique is effective for at most two iterations. So the described algorithm in section 3.1 can be simplified and the second interchanging of capacitors skipped. Thus the speed of operation could be greatly increased without giving away much accuracy. Of course the complexity of the switching sequence should be chosen in accordance with the particular application.

Fig. 4 illustrates the theoretically achievable resolution versus capacitor mismatch. From the Figure, it can be concluded that even with poor matching it is possible to build a very accurate device.

5 Conclusions

A novel circuit technique that alleviates the matching constraints of the capacitors in a two-capacitor DAC has been presented. It uses consecutive interchanging of the roles of C_1 and C_2 to achieve good linearity despite poor layout. There is some speed degradation with this method but with optimal selection of the switching sequence a rather fast (compared to serial DACs) and accurate device could be laid out.

References

[1] R. E. Suarez, P. R. Gray and D. A. Hodges, "All – MOS charge redistribution analog – to –digital conversion technique." –Part II, IEEE J. Solid State Circuits, 1975, SC-10, pp. 379-385.

[2] H. S. Lee, D. A. Hodges, "Accuracy considerations in self – calibrating A/D converters", IEEE Trans. Circuits and Systems, vol. cas-32, No6, 1985, pp. 590-597.

[3] L. Wayten, and S. Audenaert, S.: "Two-capacitor DAC with compensative switching", Electron. Lett., vol. 31, No.17, 1995, pp. 1435-1437.

[4] J. Steensgaard, U. Moon, G. Temes"Mismatch shaping for two – capacitor DAC", Electron. Lett., vol. 34, No.17, 1998, pp. 1633-1634.

[5] P. Rombouts, L. Weyten, J. Ramn and S. Audenaert "Capacitor mismatch compensation for the quasi-passive switched capacitor DAC.", IEEE Trans. Circuits and Systems, Fundam. Theory Appl. vol.45, No.1, 1998, pp. 68-71.