Abstract — This paper describes how SOI technology can be exploited to construct novel high speed digital circuits. By having complete device isolation, series connection of cells in the dataflow can be realised within a power supply that would otherwise violate device breakdown. Using this arrangement, current from a preceding high speed stage is reused in upper slower stages. A prescaler, with a fixed divisor 128, has been designed and simulated using the STAG SOI model \[5\]. The design is to be fabricated using a 0.35\(\mu\)m SOI technology.

1 Introduction

In recent years, the explosion of mobile communications has prompted manufacturers to cope with consumer needs for multimedia whilst in transit. Handheld portable devices with built in transceivers are conceptualised as a means of delivering data, entertainment etc. With the tendency towards miniaturisation, power requirements must also reduce, in particular, high speed RF sections that consume a lot of power. It is these requirements that have provided impetus for the work presented in this paper with the aim of producing a low power prescaler, since such high speed dividers are ubiquitous blocks in wireless communications ICs of all types.

2 Bulk CMOS Divider architectures

Divider circuits have been presented on numerous occasions in the previous decade, operating at steadily increasing speeds. However, integration of high speed prescalers in MOS technology has been slower, and the speeds achieved using BiCMOS technology have not quite been matched. Incidentally, the latter configuration adds cost to standard volume production by introducing more expensive mask stages, not needed for the lower speed digital systems.

In the past few years, papers have been published on gigahertz MOS dividers that consume less power compared to their Bipolar cousins\[1, 2\]. These papers have helped realise the aim of producing monolithic gigahertz Phase Locked Loops (PLL) for embedded use. Designs based on standard CMOS logic, are limited by the charging of the gate capacitance of subsequent stages with a limited current. As the device transconductances increase with process scaling, the capacitances they present as a load to previous higher speed sections increases accordingly. In recent publications, RF IC research has turned to Source-Coupled Logic (SCL), as the topology offers a designer more degrees of freedom in the search for higher speeds. This freedom, along with inter-stage differential transmission of signals, provides a good step in achieving high speed frequency dividers despite the higher static current. Apart from the latter point, other drawbacks in-
been within the past two to three years that large commercial ICs have been shown in production [4]. SOI technology offers the designer the potential for integrating very high speed logic and mixed-signal circuits on the same piece of silicon. Lower diffusion capacitances and local isolation of devices improve the circuit performance achieved using the same dimensions in bulk MOS technology. Other important benefits of using SOI include reduced short channel effects and a lower nominal $V_T$ [3].

As with all IC designs, the need for accurate compact models and simulations tools becomes ever more crucial. SOI is even more demanding (especially in modelling body node behaviour and thermal effects) and for the design presented, an in-house partially depleted model, STAG [5], was used together with model parameters from a 0.35µm commercial technology.

4 ‘Stacking’ Circuits in SOI

Figure 3: Schematic diagram of a 3 input NAND gate.

As noted in the previous diagram, SOI technology gives devices their own local silicon islands that can all be tied to a common voltage or voltages relative to their own source terminals. This property allows the stacking of MOS devices with equal $V_T$’s which leads to a far easier design. By not having to tie the floating substrates to a common potential, a greater power supply voltage can be used without resulting in high drain to substrate and high source to substrate voltages, thereby reducing breakdown of the parasitic diodes at the interface between body and drain/source terminals. An example of this is shown in figure 3.

5 Stacked Divider in SOI

5.1 Divide by 2

Figure 4: Schematic diagram of a single divide by 2 stage used in the divider stack.

An integral part of the divider stack is the divide-by-2 macro cell, which is replicated and re-sized at each stage, and this has been highlighted by the dotted box in figure 4. The cell contains a master and a slave latch, which together make up a D-type flip-flop. The outputs are cross-coupled back to the inputs resulting in positive feedback. Each latch contains an inverter and a bistable latch. When current is steered into the differential pair, the outputs show the complement of the input. When the current is steered over to the cross coupled pair, the voltages present on the inverter outputs are transferred and stored on the latch. The slave latch drives the master inverter inputs and the master latch drives the slave inverter inputs.

5.2 Voltage mode versus Current mode

The SCL divider is run on a constant current source that has a certain minimum output voltage requirement. Lowering this minimum voltage would indeed lower the power supply voltage used throughout and the overall power consumption would drop too. Having large aspect ratio devices with large...
gate lengths results in slower rise and fall times on the output of that particular divider, according to simulations. Eliminating the current source altogether[1] lowers the supply voltage, but then demands a larger input signal to the clock input.

Figure 6 illustrates how SOI technology provides another solution by allowing divider sections to be stacked on top of one another. The output of one divider remains as a current and is passed through a resistor/cascode load to a subsequent divide stage where the current is implicitly steered to either inverter-bistable pair. As each divider clock input requires a phase and its complement, the remaining quadrature outputs are unused. They have their resistive loads tied to a common voltage and static dc current can be sunk into that node. The current entering the \((n+1)^{th}\) stage would be half the current entering stage \((n)\). As the frequency into divide stage \((n+1)\) is half that of the divide stage \((n)\), the reduction in current should not affect the overall behaviour of stage \((n+1)\), assuming the RC time constant on its output node is the same or less than previous stages. An important consequence of this method is the elimination of source followers and their associated power drain.

The cascode/resistor load pairing acts to provide a gain in the divide by 2 stages improving the sensitivity of the overall divider. The proposed divider has been designed with a logic difference of 600mV between output pairs, though the higher speed stages have loads that should generate 1V difference if the capacitance on those nodes were less.

5.3 Proposed/Final Design

With the current halving as it enters the next divide stage, the output signals deteriorate quickly with a doubling of load resistance. As one designs larger stacks, the resistor load does not simply multiply by 2, occasionally requiring 2.5 or 3 times the previous load resistance. Adopting a simplistic approach with 5 stages stacked one on top of another, the fifth output stops being periodic and is heavily corrupted by clock feed-through. Hence, a synchronous divide-by-8 unit is used after the second divider, which runs on a simulated 500μA and is coupled to the final off-stack divider (another synchronous divide by 4), by converting the output to
a voltage followed by a low impedance source follower. The synchronous divider is built around the cell shown in figure 4, but has the local feedback removed, unlike the asynchronous divider. The divisor 8 is achieved by using 4 master-slave latches with a global positive feedback.

This last stage incidentally, does not run off a separate current source, and instead uses half the total current input available from the first divide stage in the stack. A series of cascode transistors allows the final divide stage to sit just below the power rail whilst biasing the top of the first stage. Hence the current in the power hungry input stage is completely reused in the lower speed circuits.

The high frequency operation is assisted through the deployment of floating body devices. By not shorting the body node (local silicon island) to the source terminal, the drain to body reverse diode exhibits reduced apparent capacitive loading. Note however, if the floating body device operates with a too high $V_{DS}$, the device can move into the 'kink' region which is undesirable.

6 Simulation results

![Figure 8: Simulation of the 7GHz differential input.](image1)

The input to the circuit is a 600mV peak to peak signal biased around 1.8V. After capacitive ac coupling, the bias voltage between 50Ω terminations is set to 1.8V using a set of MOS diodes sitting under a PMOS current source. The output is a 2.5V CMOS periodic signal, generated from the differential outputs. A level translator is employed to produce a single ended output that would be fed into a cascade of buffers, and this would ultimately drive a wirebond pad and off-chip loads totalling 10pF.

For the circuit described, simulation results can be seen in figures 8 & 9 with the input differential signal above the final CMOS output waveform. The static current used in the simulations works out to be 2.5mA (excluding the bias blocks and level translator). With a 6V power supply, the simulated power consumption for the divide by 128 is 15mW.

7 Conclusion

This paper has demonstrated the ease with which SOI technology can be employed in high frequency prescaler design. The divider design presented, generates a coherent output that is 128 times lower in frequency than the input. A robust circuit model has allowed the authors to simulate the circuit with commercial technology data. The input to the circuit has been found to go as high as 7GHz which is more than adequate for applications such as Bluetooth (2.4GHz band) and possibly HiPERLAN(5.3GHz band).

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References


