A Robust and Universal Constant-g_m Circuit Technique for Low-Voltage Rail-to-Rail Amplifiers

J. M. Carrillo*, J. L. Ausín*, J. F. Duque-Carrillo*, and E. Sánchez-Sinencio**

Abstract **- A universal and robust circuit technique to maintain a constant transconductance in rail-to-rail amplifiers, based on an input stage made up of parallel-connected complementary differential pairs, is introduced in this paper. The principle of operation consists of comparing the total transconductance with a reference value and then, appropriated tail currents are generated for the complementary input pairs. Experimental results show a total g_m deviation of ±1.25%, over the full input common-mode range of a 3-V rail-to-rail amplifier fabricated in a 0.8-mm CMOS technology.**

1 Introduction

A simple way to achieve a rail-to-rail operational amplifier consists of using an input stage made up of an *n*-channel and a *p*-channel differential pairs driven in parallel. Figure 1 corresponds to a folded-cascode amplifier with an input stage based on a composite differential pair. For reasons that will become evident later, two biasing current transistors are shown in shadowed areas in this circuit schematic. One of the main drawbacks associated to this type of input stages, is that the net transconductance $g_{m,tot}$ varies, approximately, by a factor of two over the input common-mode (CM) range. This is due to the fact that for input CM voltages ($V_{i,cm}$) in the mid-supply range, both input pairs are properly biased and then, active. However, when $V_{i,cm}$ is close to the positive (negative) supply, only the *n*-channel (*p*-channel) differential pair is active, and therefore, $g_{m,tot}$ is almost halved. This variation does not allow optimal frequency compensation of rail-to-rail operational amplifiers.

In the last years, many constant-g_m techniques have been proposed [1]-[6]. However, strictly speaking, none of them is simultaneously robust and universal. By the term robust is understood that the accuracy of the circuit for maintaining constant the total amplifier transconductance, does not rely on any condition for matching *n*-channel transistors to *p*-channel transistors. By the term universal is understood that the accuracy is independent of the input transistor types and their operation regions. In other words, universal means in this context that the technique is valid for any g_m/I_D characteristic of the amplifier input devices. Hence, universal and robust are very desirable features in any constant-g_m circuit.

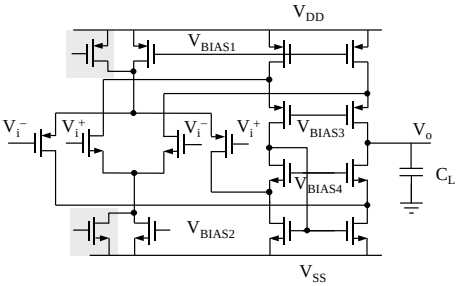

Figure 1: Low-voltage folded-cascode CMOS amplifier with rail-to-rail input stage.

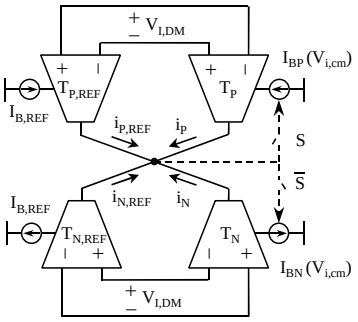

Figure 2: Conceptual circuit schematic to illustrate the operation principle.

2 Principle of Operation

Figure 2 shows a conceptual circuit schematic to illustrate the principle of operation of the proposed technique, which is simultaneously robust and universal. In this circuit, $T_{N,REF}$ and $T_{P,REF}$, as well as T_N and T_P represent transconductors based on simple differential pairs, which are replicas of the *n*-channel and *p*-channel

This work has been supported by the European Union and Spanish R&D Plan under Grant 1FD97-0254.

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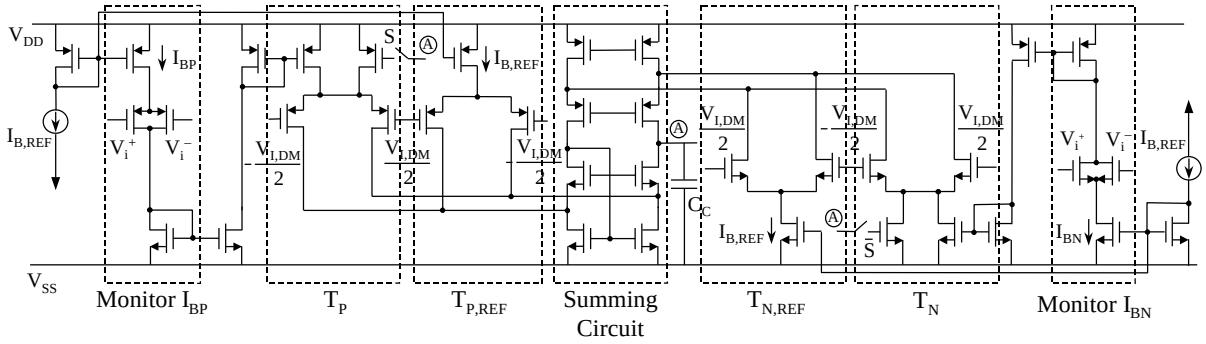


Figure 3: Circuit implementation of the circuit in Fig. 2.

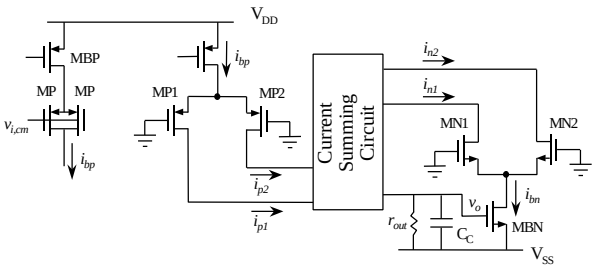


Figure 4: Simplified version of the circuit in Fig. 3 suitable for small-signal analysis.

differential pairs of the rail-to-rail amplifier, respectively. Also, for $V_{i,cm}$ in the mid-supply voltage range, the tail current $I_{B,REF}$ coincide with the nominal biasing currents, I_{BN} and I_{BP}, of both amplifier pairs, respectively, which for simplicity are assumed equals. However, these biasing currents are, at any moment, replica of the tail currents of the amplifier differential pairs, and hence, they are function of the input CM voltage. A simple current comparator, not shown in Fig. 2, compares I_{BN} and I_{BP} and its output voltage controls the switches S and $\overline{S}$, that close adequately the feedback loop. A constant dc differential voltage, $V_{I,DM}$, with zero CM component, is applied to the input terminals of all the transconductors with the polarity shown in Fig. 2. The negative feedback loop assures that the sum of the output currents of the four transconductors is zero. Assuming that $V_{I,DM}$ is a small enough dc voltage value so that every transconductor operates in the linear range, and neglecting the dc output offset currents generated by the transconductors, then $i_{P,REF} = g_{m,p,ref} \cdot V_{I,DM}$, $i_{N,REF} = g_{m,n,ref} \cdot V_{I,DM}$, $i_P = g_{m,p} \cdot (-V_{I,DM})$, and $i_N = g_{m,n} \cdot (-V_{I,DM})$, where $g_{m,p,ref}$, $g_{m,n,ref}$, $g_{m,p}$, and $g_{m,n}$ account for the small signal transconductances of $T_{P,REF}$, $T_{N,REF}$, T_P, and T_N, respectively. Therefore, it can be easily deduced that the following condition is satisfied:

$$g_{m,tot} = g_{m,p,ref} + g_{m,n,ref} = g_{m,p} + g_{m,n} \qquad (1)$$

Thus, if $I_{BP} > I_{BN}$, it indicates the $V_{i,cm}$ goes in the negative direction, and the switch controlled by the digital signal S is high. Then, the negative feedback action increases the biasing current I_{BP} to increase the transconductance $g_{m,p}$ and so, eq. (1) is still valid. Notice that the proposed technique guarantees a total constant $g_{m,tot}$ regardless of the operating region and the g_m/I_D characteristic of the transistors in any of two differential pairs, and also, it does not depend on the scaling of geometries of the *n*- and *p*-channel differential pairs to compensate their difference in mobility. Therefore, the technique results also appropriate for deep-submicron MOS devices.

3 Circuit Implementation

Figure 3 shows a circuit implementation of the constant-g_m control technique in Fig. 2. The four transconductors $T_{P,REF}$, $T_{N,REF}$, T_P, and T_N are specifically indicated over this circuit schematic. As stated above, $T_{P,REF}$ and T_P are replicas of the PMOS differential pair of the rail-to-rail amplifier, as well as $T_{N,REF}$ and T_N are replica of the NMOS counterpart. The common-drain common-source transistors in the monitor circuits, which also have the same aspect ratios as the *p*-channel and *n*-channel amplifier differential pair devices, sense the amplifier input CM voltage and generate the currents I_{BP} and I_{BN}, respectively. To avoid the inherent errors associated to current mirrors, which in turn would generate additional deviations in the total amplifier transconductance value, a folded-cascode topology has been chosen for summing the output currents of the transconductors.

Figure 4 shows a simplified version of the control g_m circuit in Fig. 3, suitable for analyzing the small-signal behavior. In particular, this simplified circuit is valid for CM voltages close to the positive supply voltage, that is, when the transistor current source of the *p*-channel differential pair goes into the resistive region and then, $I_{BP} < I_{BN}$. In other words, it is assumed that in this situation the *p*-channel amplifier input pair is in the transition region. Thus, $r_{o,bp}$ represents the output resistance of transistor MBP, which now is biased in the triode region, while r_{out} accounts for the incremental resistance of the current summing circuit

seen from the output terminal. When an input CM signal, $v_{i,cm}$, is applied, a small signal biasing current (i_{bp}) is generated. Then, the unbalanced PMOS differential pair (MP1-MP2) generates a differential current signal, Δi_p, which is proportional to i_{bp}. This differential current is given by

$$\Delta i_p = i_{p2} - i_{p1} = \frac{\Delta g_{mp}}{g_{m,p1} + g_{m,p2}} \cdot i_{bp} \qquad (2)$$

where $g_{m,p1}$ and $g_{m,p2}$ represent the transconductances of the transistors MP1 and MP2, respectively, and Δg_{mp} is $g_{m,p1} - g_{m,p2}$. Notice that the transistors of the differential pairs (MP1-MP2 and MN1-MN2) in the control loop, in spite of they are assumed perfectly matched, have a different transconductance value as a consequence of their different dc gate voltages (i.e., $V_{I,DM}/2$ and $-V_{I,DM}/2$, respectively). The control loop generates a voltage signal, v_o, which is converted in a signal current, i_{bn}, equal to $g_{m,bn} \cdot v_o$ by the transistor MBN. As before, a differential current signal Δi_n, proportional to i_{bn}, is generated by the unbalanced NMOS differential pair (MN1-MN2). It coincides with

$$\Delta i_n = i_{n2} - i_{n1} = \frac{\Delta g_{mn}}{g_{m,n1} + g_{m,n2}} \cdot i_{bn} \qquad (3)$$

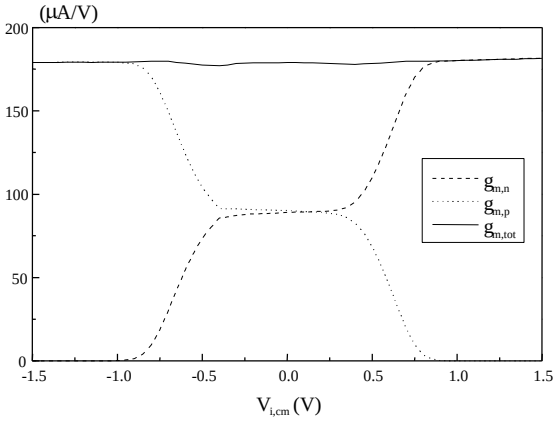
For large enough loop-gain, then $\Delta i_p \cong \Delta i_n$ and so, the change in transconductance in the PMOS amplifier differential pair, as a consequence of i_{bp}, is accurately compensated by i_{bn} causing the complementary change in the NMOS differential pair counterpart. In these circumstances, it can be easily deduced the following expression for the output voltage signal:

$$v_o = \frac{\dfrac{\Delta g_{mp}}{g_{m,p1} + g_{m,p2}} \cdot \dfrac{2 \cdot g_{m,p}}{2 \cdot g_{m,p} \cdot r_{o,bp} + 1}}{\dfrac{\Delta g_{mn}}{g_{m,n1} + g_{m,n2}} \cdot g_{m,bn}} \cdot v_{i,cm} \qquad (4)$$

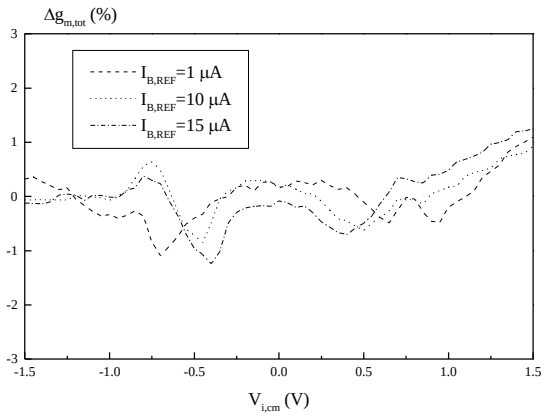
where, as expected, the numerator and denominator, both multiplied by the output resistance r_{out}, are the dc gains of the feedforward and feedback (loop-gain) paths, respectively. On the other hand, the gain-bandwidth product of the g_m-correction loop is given by

$$LGBW = \frac{\Delta g_{mn} \cdot g_{m,bn}}{(g_{m,n1} + g_{m,n2}) \cdot C_C} \qquad (5)$$

where C_C is the compensation capacitance. As deduced from eqs. (4) and (5), the gain and gain-bandwidth of the loop are proportional to Δg_{mn} and hence, to the dc differential voltage $V_{I,DM}$. Nonetheless, large $V_{I,DM}$ values can cause larger deviations in the total transconductance since the differential pairs of the circuit in Fig. 3 operate closer to their slew zone. However, on the contrary, very small $V_{I,DM}$ values can introduce large g_m deviations



(a)



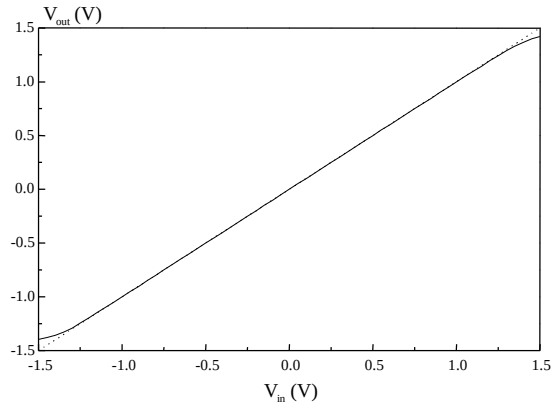
(b)

Figure 5: Measured amplifier transconductance over the full CM range with $V_{I,DM}$ = ± 50 mV with (a) $I_{B,REF}$ = 15 mA and (b) very different values of $I_{B,REF}$.

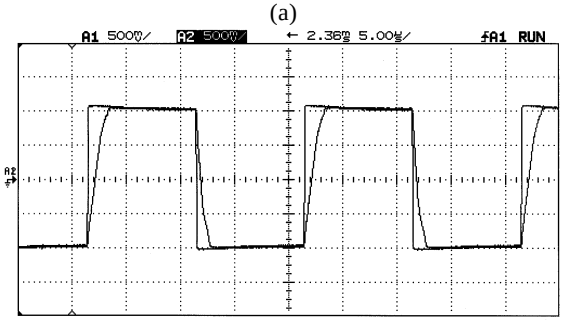
as a consequence of the dc output offset currents originated by the differential pairs in the control loop. Hence a tradeoff exists for choosing the $V_{I,DM}$ value.

4 Experimental Results

The rail-to-rail folded-cascode amplifier in Fig. 1, along with the constant-g_m circuit in Fig. 3, have been designed to operate with ±1.5 V of power supply voltage, by using the technological process parameters of a 0.8-mm standard CMOS technology. In Fig. 1, the biasing current transistors shown in the shadowed areas account for the transistors that inject the extra currents generated by the control-g_m loop (Fig. 3), while the other two bias current transistors (without shadowed areas) provide a constant biasing current for both differential pairs. Figure 5(a) illustrates the experimental behavior of the total amplifier transconductance when the input CM voltage sweeps



(a)



(b)

Figure 6: Experimental amplifier behavior in unity-gain feedback configuration: (a) dc transfer characteristic, (b) transient response.

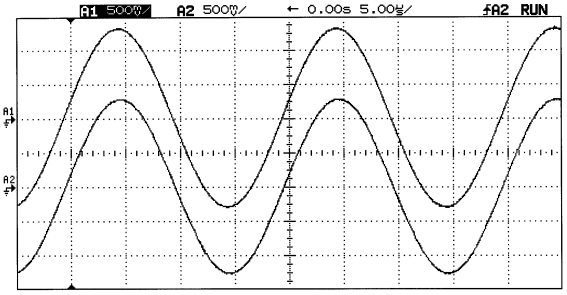


Figure 7: Measured amplifier response to a sinewave signal (top trace: input signal, bottom trace: output signal).

the entire voltage range. The nominal biasing currents in both amplifier differential input pairs were set to 15 μA, while $V_{I,DM}$ was set to ±50 mV. In the same plot the transconductances corresponding to the *n*-channel and *p*-channel differential pairs, are also shown. As observed, an almost constant total amplifier transconductance (less than ±1.25% of variation) is obtained over the full CM voltage range. In order to illustrate the universality of the proposed constant-g_m circuit technique, Fig. 5(b) shows the relative amplifier transconductance variations for rather different values of the nominal biasing currents, which demonstrates that the technique is almost independent of the g_m/I_D characteristic of the amplifier input transistors.

The dc and transient rail-to-rail amplifier behaviors have been measured. Figure 6(a) plots the dc transfer characteristic in unity-feedback configuration, while Fig. 6(b) illustrates the experimental amplifier transient response to a ±1-V 50-kHz input signal in the same configuration as before, with a load capacitance C_L around 20 pF.

Finally, Fig. 7 shows the measured amplifier response in unity-gain configuration to a 2.6-V_{pp} 50-kHz sinewave input signal. As observed, no switching noise can be appreciated in the response due to the switching of alternative bias sources in Fig. 3 (see also Fig. 2). This is due to the fact that the switching of the feedback loop occurs when no appreciable current is provided to the amplifier by the correction loop.

5 Conclusions

A circuit technique for maintaining a constant transconductance in rail-to-rail low-voltage amplifiers based on parallel-connected complementary differential pairs, has been presented. Unlike any other proposed constant-g_m technique, it is simultaneously universal and robust. Therefore, it is valid regardless of g_m/I_D characteristic of the input devices and does not rely on any condition for matching the transistors of one differential pair to the complementary one.

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