A Simplified Analysis of Noise in Switched Capacitor Networks from a Circuit Design Perspective

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Abstract - **This work proposes a way to analyze and quantify noise in SC networks. The proposed approach is simplified with respect to other results presented in the literature, in order to allow circuit designer to properly account for noise in their SC circuits. Each noise contributor is analyzed separately in the different phases of the circuit and all the contributes are merged using a high-level simulator such as MATLAB. The proposed analysis is exemplified in the case of a SC integrator and of a SC biquadratic filter.**

1 Introduction

Due to their characteristics, SC networks pose some challenges to the analysis of noise: in a first place SC circuits are sampled systems, therefore aliasing of high frequency noise components down to baseband has to be considered. Secondly and more importantly, SC circuits vary their configuration in different clock phases, therefore the usual theory developed for time-invariant networks cannot be applied straight-forwardly.

Of course the noise issue in SC circuits has been faced since their introduction [1], because of the huge range of applications of these systems. Furthermore integrated circuits evolution poses ever tighter constraints in terms of accuracy and dynamic range (DR), making noise optimization a key issue for the design of effective circuits. The literature offers therefore several analysis and computations of noise in SC circuits [1-4]. However the developed theories and procedures are often too complicated for their direct application during circuit design, being intended for computer simulation.

Conversely this work proposes a simplified approach to noise analysis in SC networks. The proposed approach allows to develop a simple model for the noise in a generic SC networks. This is a useful mean for the circuit designer, in order to evaluate the overall noise contributions and to optimize circuit parameters.

The theoretical bases of the proposed procedure are introduced in Section 2, where the case of a standard SC integrator is also discussed. The extension to more complicated systems is discussed in Section 3, using a SC biquad filter as an example. Finally conclusions are drawn in Section 4.

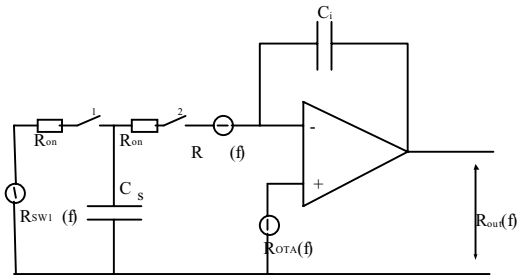

Figure 1: circuit schematic of the SC integrator, including the main noise sources

2 Noise theory

The main contributors to noise in a SC circuits are the MOS transistors, acting as switches, and the OTA, which both contribute with thermal and Flicker noise.

The thermal and Flicker noise spectral density of a MOS switch can be expressed in the form

$$R_{SWth}(f) = 4K\theta R_{ON}$$
$$R_{SWfl}(f) = \frac{K_{FSW}}{f} \qquad (1)$$

where K is the Boltzman constant, θ is the temperature and R_{ON} is the MOS switch ON resistance.

Similarly for the OTA, it holds

$$R_{OTAth}(f) = 4K\theta R_{eq}$$
$$R_{OTAfl}(f) = \frac{K_{FOTA}}{f} \qquad (2)$$

where R_{eq} is an equivalent noise resistor for the input referred noise of the OTA.

2.1 Basic model for the SC integrator

We can now consider the basic SC integrator, reported in Fig. 1. Since the circuit is controlled by two non-overlapping clock phases, we can basically single out two different circuit configurations, one corresponding to phase $\phi 1$ high and the other to phase

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$\phi 2$ high. Let us assume that the clock varies with a period T and a duty cycle d, defined as the time slot in which $\phi 2$ is high.

Let us now focus on the circuit configuration corresponding to phase $\phi 1$ high. Two different kinds of noise effects can be distinguished: some noise sources are indeed directly coupled with the integrator output node, while others will contribute to the output noise only after being sampled. Referring to Fig. 1, the noise associated to the switch $R_{sw1}(f)$ pertains to the latter category, while the noise of the OTA $R_{OTA}(f)$ pertains to the former one. Particularly the transfer function from the OTA input to its output, in phase $\phi 1$, can be expressed as

$$H_1(s) = \frac{1}{1+\frac{s}{\omega_u}} \qquad (3)$$

where ω_u is the unity gain frequency (in rad/sec) of the OTA. As a consequence of (3), the noise contribution of the OTA to the integrator output, during phase $\phi 1$, can be expressed as

$$R_{out1th}(f) = (1-d)4K\theta R_{eq}\frac{1}{1+\left(\frac{f}{f_u}\right)^2}$$
$$R_{out1fl}(f) = (1-d)\frac{K_F}{f} \qquad (4)$$

where R_{outth} and R_{outfl} refers to the thermal and Flicker noise respectively and the term (1-d) accounts for the fact that (4) is applicable only when $\phi 1$ is high.

Let us now consider the contribution of the closed switch. Observing the circuit schematic of Fig. 1 a very simple configuration can be singled out. In fact the noise $R_{sw1}(f)$ is just causing a noise voltage across the capacitor Cs. As soon as phase ϕ_1 ends, such noise voltage is sampled on the capacitor, and then undergoes exactly the same signal processing of the input signal. Therefore the noise contribution of $R_{sw1}(f)$ to the integrator output can be calculated by means of the discrete-time integrator realized by the circuit of Fig. 1. However it has to be considered that the noise source $R_{sw1}(f)$ is band-limited by the first order filter composed of R_{on} and C_s. It is realistic to assume the time constant

$$\frac{1}{\omega_{SW}} = R_{ON}\cdot C_s \qquad (5)$$

to be shorter than the sampling period, in order to make the SC filter working properly. As a consequence, when the noise is sampled onto C_s, an aliasing effect has to be taken into account. This can be done, considering that the noise source to be filtered by the integrator transfer function is

$$R_{SH1th}(f) = N_1 4K\theta R_{ON} \qquad (6)$$

where N1 defines the oversampling factor, expressed as

$$N_1 = \frac{\omega_{SW}}{2\pi}\cdot 2T \qquad (7)$$

The aliasing effect does not apply to the Flicker noise contribution, assuming that the dominant components of this noise are concentrated in frequency range lower than the Nyquist frequency 1/2T. Therefore

$$R_{SH1fl}(f) = \frac{K_{FSW}}{f} \qquad (8)$$

In summary, during phase ϕ_1, two basic noise contributions have to be considered: one is related to large band noise sources, which have been referred directly to the integrator output; the other is composed of sampled noise voltages, referred to the integrator input.

A similar approach can be used for the evaluation of noise contribution during phase $\phi 2$. In this case both the switch and the OTA contribute directly to the noise at the integrator output. The corresponding transfer functions can be found to be

$$H_{2SW}(s) \cong \frac{-\alpha}{1+s\cdot\left(\frac{\alpha+1}{\omega_u}\right)}$$
$$H_{2OTA}(s) \cong \frac{\alpha+1}{1+s\cdot\left(\frac{\alpha+1}{\omega_u}\right)} \qquad (9)$$

where α is defined as C_S/C_I. Considering the transfer functions expressed in (9), the thermal noise contributions to the output can be easily evaluated to be

$$R_{2SWth}(\omega) = d4K\theta R_{ON}\frac{\alpha^2}{1+\left(\frac{\omega}{\omega_u}\right)^2(1+\alpha)^2}$$
$$R_{2OTAth}(\omega) = d4K\theta R_{eq}\frac{(1+\alpha)^2}{1+\left(\frac{\omega}{\omega_u}\right)^2(1+\alpha)^2} \qquad (10)$$

The Flicker noise contributions, due to the low-frequency characteristic of this noise source, can be evaluated simply considering the DC gain of transfer functions (9), yielding

$$R_{2SWfl}(f) = d\frac{K_{FSW}\cdot\alpha^2}{f}$$
$$R_{2OTAfl}(f) = d\frac{K_{FSW}\cdot(1+\alpha)^2}{f} \qquad (11)$$

The contributions expressed in (10) and (11) are not the only ones. Indeed both the OTA and the switch cause a noise voltage drop on capacitor Cs, which is then sampled when phase ϕ_2 ends. It is apparent that

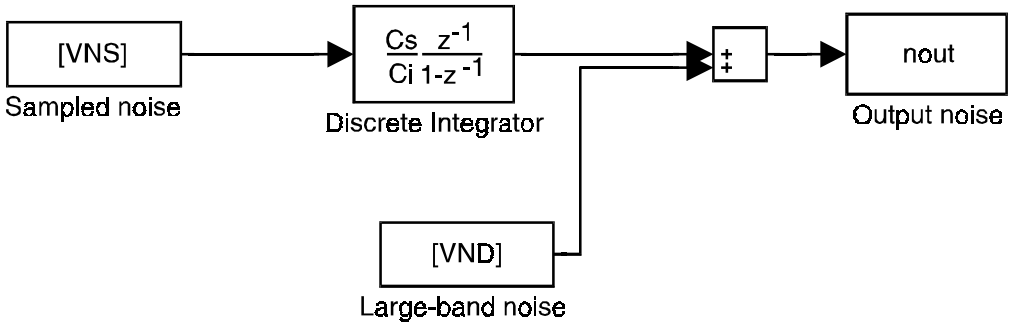

Figure 2: block diagram of the equivalent system for noise simulation

once sampled, such a noise voltage undergoes the processing typical of an inverting discrete-time integrator. We have therefore singled out another sampled-noise contributions. In force of considerations similar to the ones drawn for the case of the phase ϕ_1, we can assume a thermal noise source referred to the integrator input equal to

$$R_{SH2th}(\omega) = N_2 4K\theta \cdot \left(R_{ON} + R_{eq}\right) \qquad (12)$$

where N2 takes into account the aliasing effect. With this regard if we assume that the time constant associated to the R_{ON}-C_s network is much shorter than the one associated to the finite bandwidth of the OTA, we can still assume a dominant pole response of the whole circuit. Therefore N2 can be expressed as

$$N_2 = \frac{\omega_p}{2\pi} 2T \qquad (13)$$

where ω_p is the dominant pole of the closed-loop OTA and can be expressed as

$$\omega_p = \frac{\omega_u}{\alpha + 1} \qquad (14)$$

The Flicker noise contribution is easier to evaluate, because it is not prone to aliasing effect. Hence

$$R_{SH2fl}(f) = \frac{K_{FOTA} + K_{FSW}}{f} \qquad (15)$$

2.2 Noise simulations for the SC integrator

Based on the results discussed so far, a simple model for noise simulations can be developed in a high level environment such as MATLAB/Simulink. This tool may seem useless, because the output noise of the integrator can be calculated analytically quite easily, just summing the contribution found in the previous Section. However it will be shown in the next Section that this model is the basis to simulate noise in more complex SC circuits, where analytical calculation is quite challenging.

The proposed model basically takes into account two different kinds of noise: the noise that is sampled and input-referred to the discrete-time integrator and the noise that is large-bandwidth and output-referred to the integrator. With regard to this latter contribution, it is worth to observe that the SC circuit is anyway a discrete-time system. Therefore if the noise power has to be compared to the signal power it is advisable to introduce a sampling block also for the output-referred noise. This assumption is consistent with the fact that the SC circuit output is taken as samples and the continuos time output voltage behaviour is not considered.

The model for noise simulations is reported in Fig. 2: the sampled-noise source refers to the noise evaluated in (6) (8) (12) and (15), while the wide-band noise source refers to (4) (10) and (11). The sampled source acts as input to a discrete-time integrator, while the wide-bandwidth one is sampled and added to the integrator output. The resulting power spectrum is shown in Fig. 3: the transfer characteristic of an ideal integrator can be easily recognized. The calculated SNR is equal to 63dB.

3 Extension of the model

In this Section we will show how the noise model developed for the SC integrator can be easily extended to a more complex SC network. To this aim we will consider a SC biqudratic filter (biquad). This filter has a Q factor of about 2 and its frequency response in centered at 130Hz, as shown in the frequency response of Fig. 4 [5]. The required OTA are switched and realized using a simple 2 stage architecture. The main circuit parameters of the OTA and of the biquad are summarized in Tab. 1.

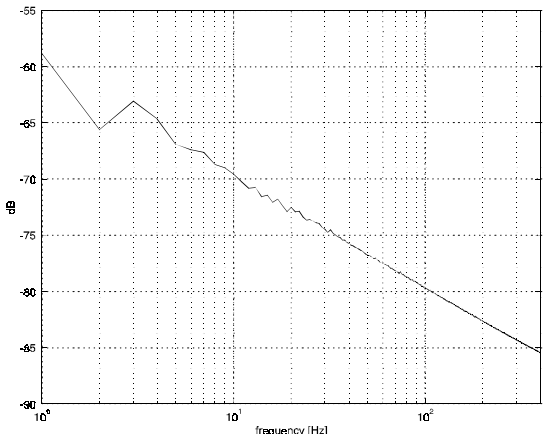

Figure 3: simulated output noise spectrum for the SC integrator

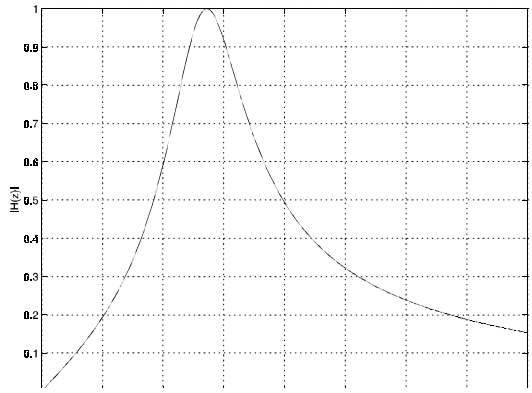

Figure 4: simulated transfer function of the SC biquad

OTA tail current	40nA
Max Capacitor	1.9 pF
Min Capacitor	0.2 pF
Total current	260 nA
Sampling frequency	2048 Hz

Table 1: main circuit parameters of the SC biquad

As in the case of the SC integrator, the noise contributors for the biquad are the two OTAs and the switches. The same considerations drawn in the previous Section apply, therefore the contribution of each noise source can be analyzed separately during phases $\phi 1$ and $\phi 2$, and equivalent sampled noise sources referred to one of two integrators input and wide-band noise sources, referred to the integrators output, can be singled out.

In order to obtain an equivalent model of the system, which includes noise effects, the various transfer functions for the noise sources, similar to the ones expressed by (9), have to be evaluated. This can be done either by hand, assuming some simplifications, or using a SPICE-like simulator, just to calculate the DC gain and the dominant poles of the transfer function. Once these calculations are performed, a simple high-level model of the system can be simulated.

3.1 Simulation results for the biquad

The simulated noise spectrum for the SC biquad is reported in Fig. 5. The shaping imposed by the filter response is apparent. The evaluated SNR is 70dB.

4 Conclusions

This work has proposed a simplified approach to noise analysis in SC networks. The procedure is based on the separate analysis of the main noise contributors in the two clock phases. The key point is to obtain equivalent noise sources that can be referred either to the input or to output of discrete-time integrators. At this point a standard simulation environment for time-invariant systems, such as MATLAB, can be used, even if the SC networks are not time-invariant.

The obtained noise analysis can be used before the detailed circuit design, based on system-level specifications in terms of settling time, accuracy and DR. The obtained information can be used to fix capacitor values in the considered network, which heavily influence the choice for the OTA architecture and its design. The noise model can be used a-posteriori as well, in order to estimate the noise contribution of the completely designed circuits.

References

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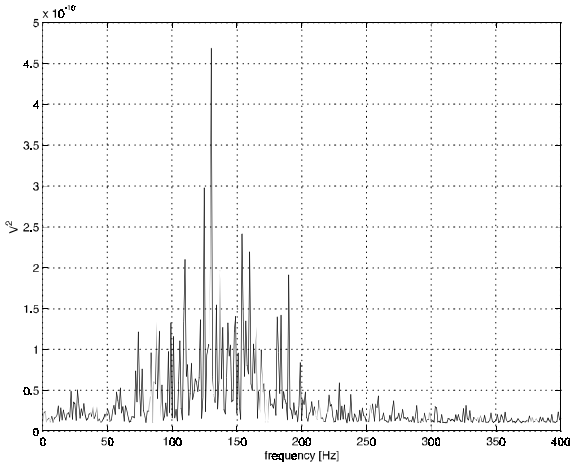

Figure 5: simulated output noise spectrum of the SC biquad