A Completely Integrated 2.7GHz Voltage Controlled Oscillator with Low Phase Noise

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Abstract - **The implementation of a low-phase-noise and low-cost VCO is discussed. The VCO uses on-chip schottky diode varactors and regular bondwires for its resonator. The VCO was implemented for the local oscillator (LO) of a GPS receiver. The VCO oscillates at 2.7-GHz which is double the LO. This frequency is divided to generate I and Q components of the LO. The core VCO uses MOS devices and can easily be integrated in any standard CMOS process with better performance. Regular bondwires used to form the resonator makes the design compact and cost-effective. Also the high-Q bondwire inductance helps reduce the power and phase noise. An automatic amplitude control (AAC) loop has been used to control the amplitude of the oscillation. The implemented VCO has a phase noise of -112dBc/Hz at an offset of 200kHz from the 2.7GHz carrier and the core consumes 2.5mA from a 3V supply.**

1 Introduction

Important careabouts for GPS RF front-end for cellular telephones are cost, power and reduction of external components. The VCO used in the frequency synthesizer of the GPS IC is a negative Gm-LC tuned oscillator which generates differential LO signals. Possibilities to integrate the LC resonator was explored to reduce cost and component count without increasing the power. Using an external LC resonator for frequencies above 2GHz has problem of package resonance very close to the desired oscillation frequency. This can make it impossible to use off-chip LC resonator. Also board design for off-chip resonator could be quite critical as VCO frequency can get pulled by on-board signals. To overcome this problem and at the same time reduce cost, this VCO with completely integrated resonator was designed. This paper is organized as follows. In Section 2 we talk about the VCO with external resonator, its problems and possible solutions. In Section 3 we discuss the VCO with completely integrated resonator and then in Section 4 we present the silicon results.

2 VCO with External Resonator

Figure [1] shows a negative Gm-LC VCO with external resonator. L1 and L2 are the bondwires connecting an off-chip LC resonator. This combination showed parasitic resonance around 6GHz. This problem is normally not so severe for VCO frequencies below 1GHz. There are techniques to kill the gain (or Q) of this parasitic mode. This can be achieved by using series resistances R1 and R2 (figure [1a]) or low pass filtering (figure [1b]). Depending on the desired oscillation frequency and package self resonance these schemes may or may not be effective. Emitter degeneration resistor, Re is used to linearise the amplifier to reduce the noise up-conversion. PMOS transistors M1 and M2 are used to bias the amplifier and the differential resonator.

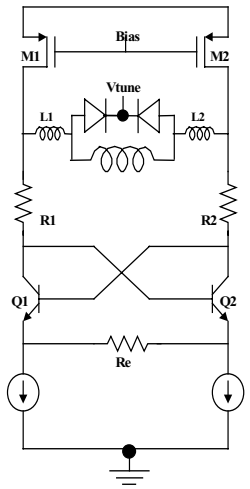

Figure 1a

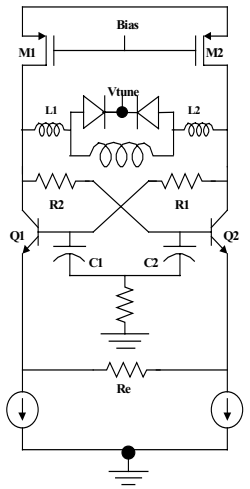

Figure 1b

Figure 1a: Gm-LC tuned VCO with off-chip resonator

Figure 1b: Filtering to attenuate package resonance

In figure[1a] R1 and R2 reduce the Q of the bondwires and hence loop gain at package resonance. The circuit in figure [1b] does low pass filtering of the resonator response using the RC combinations R1,C1 and R2,C2. This filtering attenuates the high frequency package resonance quite effectively though it increases the current drawn in the VCO as the filtering reduces the loop gain. VCO of figure[1b] was designed to generate GPS LO frequency of 1.35GHz. A polyphase was used to generate I and Q components of LO. This VCO was quite sensitive to off-chip components and board layout. Some parts oscillated at the high frequency package resonance mode.

3 VCO with Integrated Resonator

3.1 Bondwire vs On-chip Metal Spiral

Inductors can be built in integrated circuits by either on-chip metal spiral or by bondwires. On-chip metal spiral inductors using regular metal levels have Q in the range of 4 to 6 in the desired frequency. Use of copper could get a Q around 8, but using copper would mean extra cost. Low Q would cause high phase noise. Even if acceptable phase noise can be achieved it would be only at the expense of a large power. Only thing that goes in favour of metal spiral is the control of the absolute inductance. But these days high precision packaging assembly line can control the bonding process within a micron. A detailed package modeling showed a small variation of the bondwire inductance and it was well within 5%. GPS LO needed only one oscillation frequency. So there was no problem to compensate for this small variation in the bondwire inductance by the available tuning range of the on-chip varactor diodes even after taking care of the capacitance variation of the diode over process and temperature. The Q of the bondwires is higher than 20. So bondwire became our choice for inductor. Considering all the uncertainty in the wire length, height, spacing, diameter and vertical bend the variation of the inductance is expected to be within +/-5% ([1]).

3.2 The Varactor

The varactor used was a schottky diode on NWEL. This schottky diode offers a good Q (above 15) in the 2GHz range when the signal is applied on the anode (the schottky contact). If the signal is on the cathode (NWEL side) the Q is very poor due to losses in the NWEL-psubstrate junction. Also the large NWEL-psubstrate capacitance reduces the tuning range of the diode. Since signal should be applied to the schottky contact and a DC bias (tuning voltage) to the NWEL such that the diodes are reverse biased, the schottky contacts are biased at ground to maximize the tuning range. This helps reduce the VCO gain and hence the reference spurs. Due to the low compare frequency (10KHz) our PLL was quite sensitive to reference spurs. In order to bias the varactors at ground potential, PMOS cross-coupled pair was used for the Gm amplifier. In figure[2] D1 and D2 are the schottky varactor diodes.

3.3 The Amplifier

PMOS transistors (M1 and M2 in fig [2]) form the cross coupled Gm pair. The directional dependency of Q of the varactor made this decision. The PMOS devices are AC coupled to allow large swing at the drain nodes keeping them deep in saturation. This makes the amplifier linear and reduces noise up-conversion. The gate bias is provided through the resistors by the AAC loop. The critical noise sources for MOS device at RF frequency were modeled by estimating the effective gate resistance and substrate resistance. The layout of the MOS devices was done to optimize these parasitic effects. Since C_{gs} of the MOS devices come in parallel with the varactor, they just get accounted for in the LC resonator, and hence low ft of the PMOS device is not a concern. The drains of M1 and M2 are connected to the VCO ground on the board using bondwire inductances L1 and L2, which come out to two pins P1 and P2.

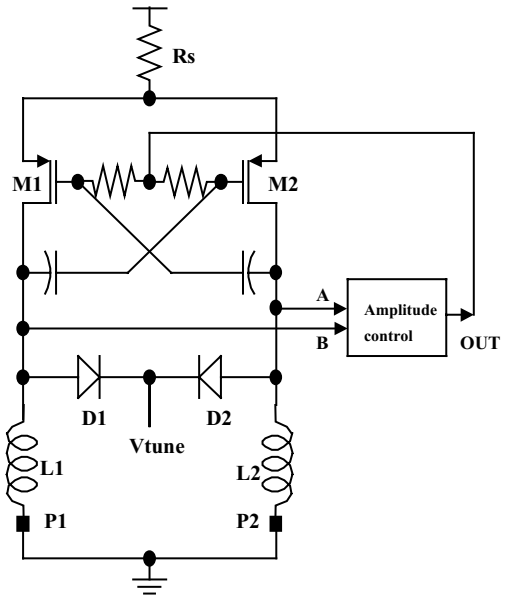

Figure 2: VCO with integrated resonator. L1 and L2 are bondwires

No special bonding, like pad to pad or package to package bonding was used. A detailed package modeling for the final location of the pads estimated an inductance of 1nH. The VCO layout has been centered symmetrically on one side to match the two bondwires. Also the adverse effect of the mutual inductance was reduced by not keeping these two bondwires L1 and L2 next to each other as opposing current and field in these two bondwires would have reduced the resulting inductance and Q. The supply pin (no AC signal) for the VCO was kept between these two pins to provide isolation between the inductances L1 and L2. The resistance of the metal interconnect connecting all the gate fingers was taken into account. The length of each gate finger and number of fingers was optimized to reduce the overall distributed gate resistance. The gate was connected from both sides as it reduces the effective resistance by a factor of 4. The drain diffusion is always shared between two fingers to reduce capacitance at the drain

node. But the source diffusion is separated at a regular interval to insert a backgate diffusion. The effective backgate resistance is reduced to improve the Q of the drain to bulk capacitance.

The MOS devices are placed such that the metal resistance from the drain to the bondpad is minimum. Special bondpads are used to improve the Q of the bondpad capacitance. The close-in phase noise specification was quite demanding. To keep the 1/f noise low, a fairly large channel length (0.6 microns) was used. This means large device size and large gate capacitance and drain junction capacitance. This large fixed capacitance reduces the varactor tuning range. So there is a trade-off between close-in phase noise and tuning range. A large fixed capacitance also will cause more non-linearity in the VCO gain, which will effect the PLL loop bandwidth, settling time and phase noise. The ground pins P1 and P2 are strongly connected to the ground bus immediately outside. Any noise coupled to them is coupled to the common mode node and does not effect the VCO performance. The drains are biased at ground and the gates are biased at a much higher voltage by the AAC loop. When there is no oscillation the AAC loop will bring the gate voltage down which will increase the MOS drain current and Gm. This large Gm will ensure a VCO loop gain much higher than 1 and proper start-up. The realized transconductance Gm of the back-to-back connected PMOS pair is half of the transconductance of each PMOS transistor. Metal connection at the common source node of the PMOS pair is critical as any small parasitic resistance can cause enough source degeneration and will increase the PMOS drain current to achieve the required Gm.

3.4 The Automatic Amplitude Control

An amplitude control loop (figure [3]) was employed to set the oscillation amplitude at a desired level. The output of the amplitude control loop controls the DC bias at the gates of the PMOS devices. The common mode source degeneration resistance (Rs in fig[2]) is used to set the gain of the amplitude control loop for stability purpose. This resistance also helps to attenuate the phase noise contribution of the amplitude control loop. The differential output of the core VCO is applied between inputs A and B of the amplitude control circuit. The transistors Q1 and Q2 with emitter degeneration, linearly amplify the VCO output. The transistors, Q3 and Q4 do a full-wave rectification of the amplified VCO output. The rectified signal of node n1, is averaged by the low pass filtering at node n2. This average is compared with reference voltage level at node n3 by the differential pair Q7 and Q8. The output of this error amplifier (OUT) sets the gate bias of the core VCO devices M1 and M2.

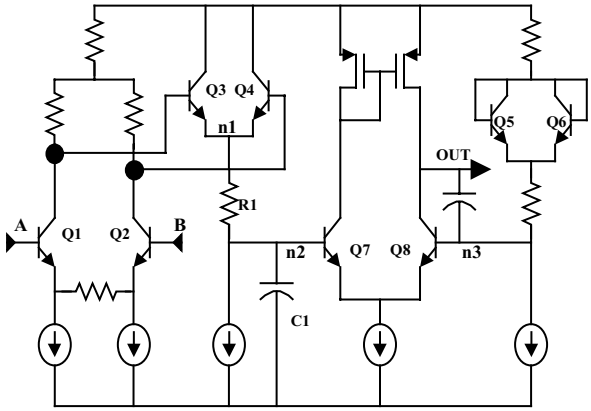

Figure 3: The automatic amplitude control circuit

The noise in the reference level generation effects the close-in phase noise of the VCO. Devices used within the loop, ie. for rectification and filtering, effect the far-off phase noise beyond the bandwidth of the AAC loop. The loop was optimized accordingly to reduce its contribution to the phase noise. The AAC loop was needed at the first place to maintain a good linearity of the VCO amplifier so that the up-conversion of MOS 1/f noise is minimized. Phase noise would be minimum at an optimum amplitude and hence we need amplitude control. This was needed to satisfy the demanding specification of close-in phase noise.

4 Silicon Results

Figure[4] shows the phase noise as measured on silicon for the VCO frequency of 2.7GHz. The synthesizer compare frequency is 10KHz. So VCO phase noise down to 1KHz frequency offset is also important. The $1/f^3$ phase noise corner is at 20KHz offset.

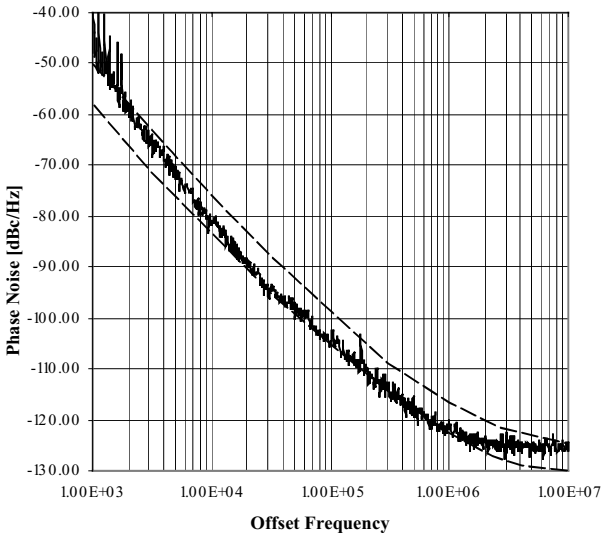

Figure 4: Measured Phase Noise at 2.7GHz

The dashed lines are two extremes of phase noise from simulation. The silicon measurements lie within this limit. At elevated temperature the phase noise increases and approaches the worst case simulation result.

In figure[5] VCO tuning range is shown. The dots are simulation results and the solid line is from silicon measurements. The actual frequency is within 2% of what was predicted by simulation. The tuning range is better than +/- 10% and the VCO gain K_v is 200MHz/volt at VCO frequency of 2.7GHz.

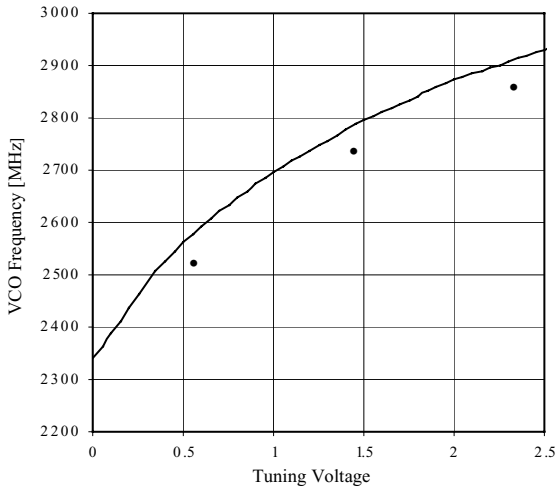

Figure 5: Measured VCO gain and tuning range

Figure[6] shows the photomicrograph of the VCO section of the GPS receiver chip. M1 and M2 are the back-to-back connected PMOS devices, L1 and L2 are the bondwire inductors, D1 and D2 are the varactor diodes, AAC is the amplitude control circuitry and BIAS is the PTAT current bias and current mirror circuits.

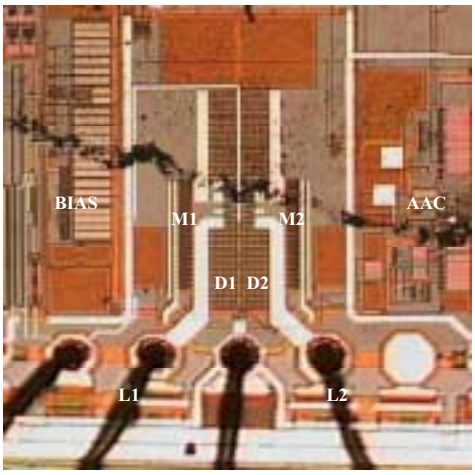

Figure 6: Photomicrograph of the VCO

4 Conclusions

A completely integrated 2.7GHz CMOS VCO is implemented for GPS receiver front end chip. The GPS receiver is fabricated in RFBiCMOS1 process of Texas Instruments.

The VCO has low phase noise down to very low offset frequency of 1KHz. The ground pins are effectively used to form the differential LC resonator along with on-chip varactors. This VCO is implemented at the lowest possible cost as no area is needed for metal spiral inductor and no special bonding technique is used. It also makes it possible to use a smaller package.

The tuning range is 20% and power consumption is 2.5mA in the VCO core and 1.5mA in the amplitude control circuit.

References

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