A Novel Low Power Multiplexer-Based Full Adder

Abdulkarim Al-Sheraidah*, Yingtao Jiang*, Yuke Wang*, and Edwin Sha*

***Abstract* - 1-bit full adder circuit is a very important primitive cell in the design of Application Specific Integrated Circuits. This paper presents a novel low-power multiplexer-based 1-bit full adder that uses 12 transistors (MBA-12T). In addition to reduced transition activity and charging recycling capability, this circuit has no direct connections to power supply nodes and the entire signal gates are directly excited by the fresh input signals, leading to noticeable reduction in short-current power consumption. Intensive HSPICE simulation shows that the new adder has more than 26% in power savings over conventional 28-transistor CMOS adder and it uses 23% less power than 10-transistor adders (SERF [1] and 10T [4]) and is 64% faster. This new MBA-12T adder thereby, is a good primitive cell to build larger low power VLSI systems.**

1 Introduction

With the explosive growth in laptops, portable personal communication systems (PCS's), and the evolution of the shrinking technology and flexible-circuits, the research effort in low power microelectronics has been intensified. Today, there are an increasing number of portable applications requiring small-area low-power high throughput circuitry, such as the trendy PalmPilot electronic organizer. Therefore, circuits with low power consumption become the major candidates [1][2][3] for design of microprocessors and system-components.

The 1-bit full adder is one of the most critical components of a processor that determines its throughput, as it is used in the ALU, the floating-point unit, and address generation for cache or memory accesses [1]. It is therefore inherent that full-adders have great impact on the systems that use these adders. A variety of full adders using static and dynamic logic styles have been reported in literature [1]-[8]. 34 of them have been found in [8] alone, including the most well known static complementary CMOS adders using 28 transistors (Fig. 1.f) and 40 transistors. In specific, there are two works of research ([1] and [4]) in this field that shape our study. In [1], Static Energy Recovery Full (SERF) adder is proposed, which requires only 10 transistors to implement a full adder. This adder makes use of the design architecture shown in Fig. 1-a, where an intermediately generated $XNOR(A,B)$ signal is shared to generate the carry out and the sum outputs. SERF (Fig. 1.b) has been shown to consume 26% less power than a Transmission Function Adder (TFA) [1]. In [4], a novel 4-transistor XOR-XNOR gate is proposed. These gates along with Wang's XOR-XNOR and the inverter-based XOR-XNOR circuit sets [4][5] can be utilized according to the design architecture in Fig. 1-a to build a set of new 10-transistor 1-bit full adders (see Figs. 1.c - 1.e, named as 10T09A, 10T09B, 10T13A, respectively).

In this paper, we introduce a novel low-power multiplexer-based 1-bit full adder that uses 6 identical multiplexers with 12 transistors in total (this adder will be called MBA-12T thereafter). This new adder has low short-circuit current and reduced transition activity than previously proposed low-power adders.

In order to examine all the proposed low-power adders, MBA-12T is tested along with the 28-transistor complementary CMOS adder and four other low-power 10-transitor full adders [1][4] using HSPICE [9]. The testing result shows that the MBA-12T consumes 26% less power than 28-transistor CMOS adder. Meanwhile, MBA-12T exhibits at least 23% in power-savings over the least power-consuming 10-transistor adder and a minimum of 64% in speed improvement over the fastest of all other tested adders.

The rest of this paper is organized as follows. In Section 2, the new adder is proposed. In Section 3, we present the simulation environment setup and simulation results, followed by a brief discussion on these results. Section 4 concludes the paper.

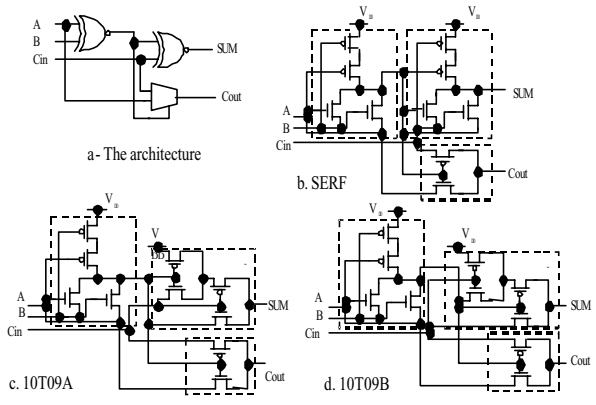

Figure 1: Full adders

* University of Texas at Dallas, HW/SW Codesign Lab for DSP & Communications, Department of Computer Science, Richardson, TX, USA 75083 Email:yuke@utdallas.edu Tel: +001-972-8834139, Fax:+001-972-8832349.

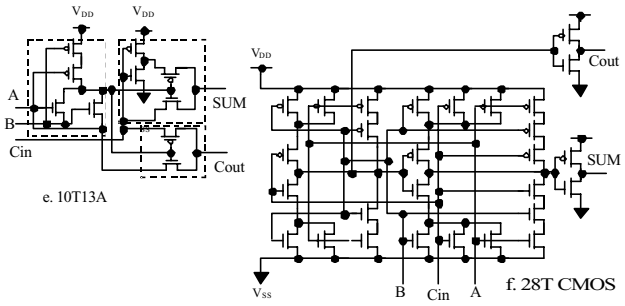

Figure 1: Full Adders (cont'd).

2 The New Multiplexer-Based Full Adder

In this part a 1-bit full adder that utilizes a novel multiplexer-based architecture, built upon 6 identical multiplexer gates, is shown in Fig. 2. Substituting each of the multiplexer gates with a 2-transistor circuit (Fig. 2.b) gives us the new MBA-12T adder, which requires a total of 12 transistors to realize the function of a full adder (Fig. 3).

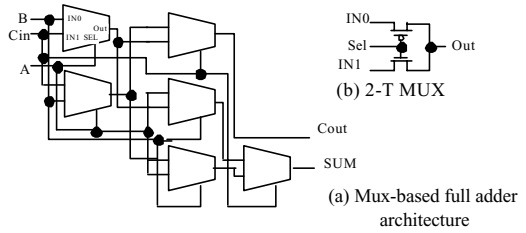

Figure 2: a- The architecture, b- the 2-T Mux

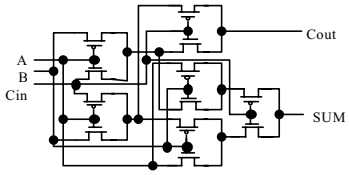

Figure 3: The new 12-transistor full adder.

There are three major sources of power dissipation in a digital CMOS circuit: logic transition, short-circuit current and leakage current [6][7]. In the following, we will show how low power consumption is achieved in the new MBA-12T adder due to reduction in short-circuit current and switching activity.

The short-circuit current is defined to be the direct current passing through the supply and the ground, when both the NOMS and PMOS transistors are simultaneously active [2][6]. The SERF, 10T-09A, 10T09B, and 10T13A adders (Fig. 1) all suffer the same short-circuit current problem as they have some internal nodes driven by signals with slow raise and/or fall times. This leads to significant (20%) short-circuit power dissipation for loaded inverters [6]. Such problem was partially solved in SERF, 10T09A, and 10T09B adders as a result of absence of a connection to V_{SS} port. In this case, no direct path from supply to ground can be formed. The new MBA-12T adder moves one step further and provides the best solution for the short-circuit current problem as all of its internal gate nodes are directly excited by fresh input signals (A, B, and C_{in}). On top of that, MBA-12T does not have direct connections to V_{DD} or V_{SS} port, which can substantially reduce the probability of a direct path formation from positive voltage supply to the ground during switching.

Since the new MBA-12T uses 12 transistors, the internal node capacitance increases by about 20% compared to SERF, 10T09A, 10T09B, and 10T13A adders (see Fig. 1). However, the switching activity of the MBA-12T adder will be considerably lower than that of previously proposed 10-transistors adders. That's because all of those adders (SERF and 10T's) use an internally generated signal (A XNOR B) to control the output transistor gates (4 gates in total). Hence the probability that a power-consuming transition (p_t) occurs is $\{p_{XNOR(A,B)} = 8/12 = 0.6667$, $p_t = [(6 \quad (1/2) + 4 \quad 0.6667]/10 = 0.5666\}$, i.e., at least 13.34% higher than that of the MBA-12T adder with switching probability calculated to be only 0.5: $\{p_i = 1/2, p_t = 12 \quad (1/2)/12 = 0.5\}$.

Similar to SERF, ADDER-10T09A, and 10T09B, the new MBA-12T adder has the ability of reclaiming all the node charges during the discharge cycle of those nodes. But unlike SERF, 10T09A, and 10T09B the new MBA-12T adder will only use the input signals (A, B and C_{in}) to charge any of its nodes, thereby, making the new MBA-12T adder the first self-sustaining 1-bit full adder of its kind.

Threshold loss problem [6] impacts the new adder only at its output nodes (*Sum* and C_{out}); that is, weak logic '1' can drop to $V_{DD} - V_{tN}$ and a worst-case logic '0' equals to $|V_{tP}|$ volts. However, SERF will have a worst case logic '1' equal to $V_{DD} - 2V_{tN}$ at its C_{out} output port when A, and B are both equal to logic '1', as shown in Fig. 4. Thus, The operational supply voltage range for the SERF adder is limited to $V_{DD} > 2V_{tN} + |V_{tP}|$.

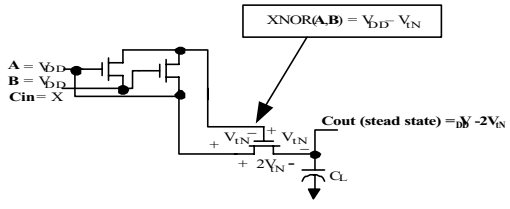

Figure 4: Worst case logic '1' for SERF

3 Simulation Results

We have performed intensive simulations using HSPICE [9] on the new MBA-12T along with 28-transistor complementary CMOS, SERF, 10T09A, 10T09B, and 10T13A adders (Fig. 1) at the schematic level under comparable simulation conditions. The technology being used is 0.35 um CMOS digital technology (TSMC 35, Canadian Microelectronic Corporation) with supply voltage 3.3 Volts. To establish an impartial testing environment, the simulations have been carried out using a comprehensive input signal pattern (Fig. 5), which covers every possible transition for a 1-bit full adder.

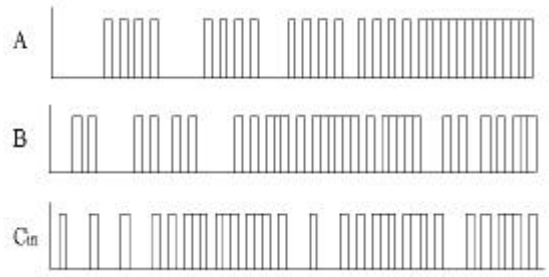

Figure 5: Simulation input patterns

In our experiment, 6 frequencies (toggle rates) have been chosen for each input signal, swinging from 10 to 200 MHz. Also, 6 different loads (500fF, 250fF, 125fF, 62.5fF, 31.25fF, and 0.9765625fF) have been inserted to the output ports (*Sum* and C_{out}). In total, for each adder circuit, 36 HSPICE simulation runs (6-frequencies by 6-loads) have been conducted.

Simulation results show that the new MBA-12T adder consumes at least 26% less power than that of the conventional 28-transistor complementary CMOS adder (Fig. 1.f) under all above mentioned simulation conditions (Fig. 6). This is quite understandable as MBA-12T has much lower transistor count, thus much lower internal capacitance than 28-transistor CMOS adder. Furthermore, as can be seen from Fig. 6, MBA-12T has a minimum power saving of 33.4%, 31.4%, 23.7%, and 29.3% over SERF, 10T09A, 10T09B, and 10T13A respectively. On average, the new MBA-12T consumes 37.5%, 36.5%, 30.9%, and 36.3% less power than respective SERF, 10T09A, 10T09B, and 10T13A. Thus, the ranking of those adders in terms of power savings will be as follows: MBA-12 is the first, 10T09B the second, 10T09A the third, 10T13A the fourth, and SERF the fifth.

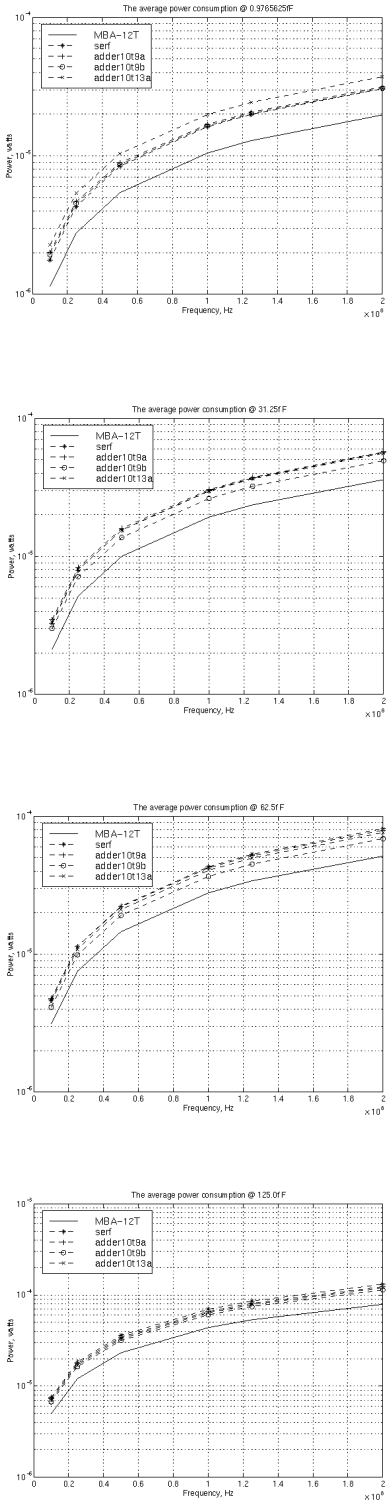

Figure 6: Average Power Measurements

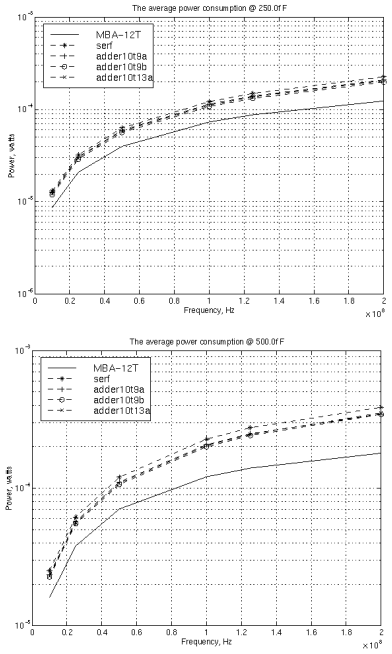

Figure 6: Average Power Measurements (Cont'd)

The critical delay under various load conditions is presented in Fig. 7. Opposite to our expectations, the new MBA-12T on average, exhibits a speed improvement by 78.9%, 78.2%, 78.4%, and 78.5% over SERF, 10T09A, 10T09B, and 10T13A respectively. The critical delay of SERF, 10T09A, 10T09B, and 10T13A is determined by the C_{out} signal.

Finally, the average power-delay product of MBA-12T (Fig. 8), on average, is 59.7%, 60.1%, 55.9%, and 67.5% smaller that of respective SERF, 10T09A, 10T09B, and 10T13A adders.

4 Conclusions

In this paper, a novel low-power multiplexer-based 1-bit full adder (MBA-12T) is presented, which is constructed using 6 identical multiplexers and a total of 12 transistors. MBA-12T adder exhibits charge recycling capabilities and has very low short-circuit current. HSPICE simulations have been performed to evaluate MBA-12T and five other adders, including 28-transistor complementary CMOS, SERF and 10T adders. Simulation results show that MBA-12T consumes 26% less power than conventional 28-transistor CMOS adder. In addition, MBA-12T consumes 23% less power than the most power efficient 10-transistor adders and is 64% speedier than the fastest of all other tested adders. MBA-12T therefore, is suitable to be applied to build larger low power high performance VLSI systems.

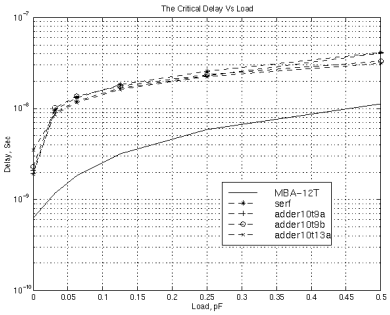

Figure 7: Critical Delay Measurements vs.

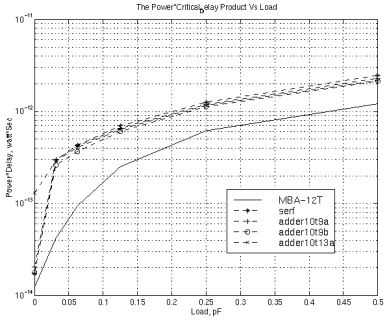

Figure 8: Power*Critical_Delay Product vs. Load

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