Abstract — In this paper we present the top down design of an APS circuit using an analytical model of its architecture. The model is applied to compare the designs of a 50 frames/s 512x512 pixels imager in a 2µm CMOS both in BULK silicon and in SOI technologies. SOI Results show a reduction by two of the power consumption and a dynamic range increase of 0.85 V under 3V supply. It results in an SNR of 79 dB instead of 76. Fixed Pattern Noise (FPN) is also reduced from 2.7 mV to 1.8 mV which represents 0.26% and 0.08% of the dynamic range respectively. Potential results achievable in SOI have to our knowledge never been reached by BULK APS imagers up to now.

1 Introduction

Since the beginning of the 90’s, CMOS technology, thanks to its unceasing progress, has been considered as a more and more serious competitor against its rival, the CCD technology, for the fabrication of imagers. Up to now however, only very few studies have considered the use of silicon-on-insulator technologies (SOI) for CMOS Imagers because of the apparent difficulty for the photosensor implementation. However solutions have already been proposed [1]. In this paper, we compare the design of a CMOS APS imager in BULK silicon and SOI. We developed, for this purpose, an analytical model using the gm over Id method [2], in order to establish analytical relationships between specifications and design parameters. We demonstrate that the well known advantages of SOI fully depleted CMOS(FDSOI) [3] may result in significant improvements of the performances of the photosensor readout circuitry. Potential results achievable in SOI have to our knowledge never been reached by BULK APS imagers up to now.

The paper will be organized as follows: in section 2 we briefly explain the architecture of the imager we considered. In section 3, we present the model of the APS circuit. In section 4, design results are discussed.

2 Circuit description

2.1 Pixel

As a case of study, we considered the classical integrating APS cell with 4 transistors, a photodiode and the integrating capacitor $C_{pix}$, made of the parasitic capacitances of the gate node of $M_b$ and eventually an added capacitor (Fig. 1) [4]. $M_b$ is the active transistor of the pixel, the three others working as switches. In the readout phase, when $M_{act}$ is switched on, $M_b$ is biased in a buffer configuration by the column current $I_{mirc}$, so as to copy its gate voltage ($V_{gs}$) to the column bus. The offset between the pixel output signal $V_{pix}$ and the signal resulting from the integration of the photocurrent on $C_{pix}$ is then related to the gate-to-source voltage of $M_b$, $V_{gs}$, which depends on its threshold voltage, drain current and size.

Figure 1: schematic view of studied pixel.

2.2 Column amplifier

The architecture of the column amplifier under study (figure 2) has been recently proposed in [5] in order to compensate for pixel non uniformity or fixed pattern noise (FPN). In general, column amplifiers introduce their own "column” FPN which must be corrected in the output stage, limiting the bandwidth. We choose the present amplifier because it compensates for its uniformities to the first order and so does not need a compensation in the output stage. It contains 4 switches, a coupling capacitor C, a transistor $M_I$ which works as a current source, and the transistor $M_m$.

During the first phase, when switches S1 and S2 are on, $M_m$ acts as a current copier and charge or discharge the capacitor C until its drain current equals the current of the source $M_I$ independently of its own offset. During the second phase, when S1 and S2 are switched off and the pixels of a row are reset, it appears (at the input of the column
amplifiers and at the gate of $M_m$) a voltage swing proportional to the light on the pixels and free of their offsets. In the third phase, when switches S3 and S4 are on, $M_m$ and the output readout bus current mirror, $M_{mir}$, work as a buffer. The output signal is free from the offset of the threshold voltage of $M_m$ but not from the offset due to the $M_f$ current mismatch. This will be evaluated in the next section.

Figure 2: schematic view of our column amplifier.

3 Model description

To design our imager we developed an analytical model expressing the different specifications (i.e. timing, power consumption, SNR which splits in dynamic range and readout noise requirements, chip area and fixed pattern noise (FPN)) as a function of device parameters.

3.1 Timing requirements

The different rise/fall times for both the pixels and the column amplifiers outputs have been fixed for 512x512 pixels and 50 frames/s. In both cases the buffers have to load a capacitor $C_o$ (equal to either $C_{col}$ or $C_{bus}$) from its initial value, $V_{low}$, to its final value, $V_{fj}$, depending of the pixel value, in a given time $t_{ch}$. The transient current available to load the capacitor is the difference between the drain current of the source follower, $I_{d, sf}$, and the bias current of the mirror, $I_{mir}$. So the transient evolution of the output voltage of the buffer, $V_s$, is given by:

$$I_{d, sf} - I_{mir} = C_o \frac{\partial V_s}{\partial t}$$  \hspace{1cm} (1)

To model the current $I_{d, sf}$ of the source follower we used the EKV model [6] to provide a continuous current-voltage relationship from weak inversion (at the end of the load) to strong inversion (at the beginning of the load). Solving this equation with Matlab, we found that the temporal requirement are not dominated by large signal conditions (slew rate), which would end in a W/L minimum of the source follower, but by slow variations around the equilibrium value of the output voltage. This can be expressed as a requirement on the transimpedance of the source follower ($g_{ms, sf} = ng_{ms, sf}$, where $n$ is the body factor). The corresponding time constant $\tau = \frac{g_{ms, sf}}{C_o}$ must be smaller than $t_{ch}$ to minimize the error, i.e.

$$ng_{ms, sf} > \frac{C_o}{t_{ch}}$$ \hspace{1cm} (2)

with, from simulation, factor $\alpha$ equal to 3 for an error lower than 0.1mV.

3.2 Power consumption

The power consumption is the sum of static power due to the bias currents of each column mirror, $I_{mir}$, the bias current of the output mirror, $I_{mir}$, the bias current of one transistor $M_f$ at a time, and the reference currents for the mirrors. For a 512x512 pixels imager, this gives:

$$P_{stat} = V_{dd}[513I_{mir} + 3I_{mir}]$$ \hspace{1cm} (3)

The dynamic power consumption is dissipated in each pixel integration capacitor, $C_{pix}$, in each column bus capacitor, $C_{col}$, and in the output bus capacitor of the column amplifiers, $C_{bus}$:

$$P_{dyn} = \gamma f_{pixel} V_{dd}^2 [C_{pix} + C_{col} + C_{bus}]$$ \hspace{1cm} (4)

where $0 \leq \gamma \leq 1$ is used to account for the dynamic power consumption dependence on the level of the signal. A mean value is calculated for a signal level of $V_{dd}/2$ resulting in $\gamma = 1/4$. $f_{pixel}$ is the inverse of the time available to read a pixel at the output equal in the our case to 13.1MHz.

3.3 Dynamic range

Minimizing the loss in dynamic range is of prime importance in a low voltage imager.

At the pixel level, the voltage swing at the gate of the source follower ranges from $V_{sat}$ to $V_{sat, diode}$, the latter being the saturation voltage of the diode due to the dependence of the length of the depletion region on reverse bias voltage. The optimization of this voltage is beyond the scope of this paper. The output voltage of the pixel ranges from $M_{mir}$ saturation voltage, $V_{sat, mir}$, to $V_{dd}$ - $V_{gsb, high}$. The subindex "high" or "low" will be used because of the dependence of $V_{gs}$ with respect to the source voltage, caused by the body effect. We will use the subindex "low" ("resp. "high") when
the source voltage is at is minimum (resp. maximum) for non saturation conditions: \( V_{sat/m} \) (resp. \( V_{dd} - (V_{gb})_{high} \)). The total conditions for non saturation of the pixel are at the gate of \( M_b \) and at the output of the pixel respectively:

\[
max((V_{gb})_{low} + V_{disat/m}, V_{sat/diode}) = V_{sat1}
\]

\[
V_{sat1} < V_{gb} < V_{dd}
\]

\[
V_{sat1} - (V_{gb})_{low} < V_{gb} < V_{dd} - (V_{gb})_{high}
\]

This can give us the pixel maximum input and output swings, \( \delta V_{inp} \) and \( \delta V_{outp} \), as respectively:

\[
\delta V_{inp} = V_{dd} - (V_{sat1})
\]

\[
\delta V_{outp} = \delta V_{inp} + (V_{gb})_{low} - (V_{gb})_{high}
\]

By a similar way we can calculate the input and output swings for the second stage, \( \delta V_{in_{Acol}} \) and \( \delta V_{out_{Acol}} \) respectively. We then have to match the dynamic range of the two stages together such that:

\[
\delta V_{in_{Acol}} \geq \delta V_{outp}
\]

### 3.4 Noise

For optimizing the imager SNR, we have to estimate the influence of design parameters on the total output noise, which requires an analytical model. We used following transistor thermal and flicker noise source expressions referred to the MOS gate:

\[
S_{V_{th}} = \frac{4kT\alpha}{g_m}
\]

\[
\alpha = \frac{2}{3 + \left( \frac{g_m}{\tau}\right)^2}
\]

\[
S_{V_{fg}} = \frac{K_f}{W\lambda C_{ox}} \left( 1 + \frac{v\mu C_{ox}}{2g_m}\right)
\]

where \( K_f \) is a technological parameter we set equal to \( 4.7 \times 10^{-7} \frac{A^2}{V^2} \) and \( v \) is 8.510^3 \frac{V}{A} [7].

The spectral noise at the gate of the transistor is then:

\[
S_{V_{th}} = S_{V_{fg}} + S_{V_{th}}
\]

To estimate the noise of the imager, we take into account the noise of the buffers of the pixels and column amplifiers, as well as the \( kT/C \) noise due to the reset of the pixel integrating capacitor.

The spectral density of noise of a buffer \( S_{V_{b}} \) at the gate of its source follower (sf) is, assuming a current gain of one in the mirror:

\[
S_{V_{b}} = S_{V_{fg}} + \frac{g_m^2}{2\tau^2 \lambda_{mirror}} S_{V_{mirror}}
\]

The equivalent stochastic noise at the input of the buffer, \( V_{gsf} \), has its autocorrelation \( R_{out} \) function of time \( t_1 \) and \( t_2 \) between 2 successives events:

\[
R_{out}(t_2 - t_1) = \frac{1}{2\pi} \int_{-\infty}^{\infty} S_{V_{b}} e^{j\omega(2t_1-t_2)} \frac{1}{1 + \left( \frac{w_{eq}}{w_{eq}} \right)^2} \, dw
\]

where \( w_{eq} = \frac{V_{gsf}}{V_{ref}} \) is the passband of the buffer. Due to the double sampling (DS, section 3.5), the actual buffer pixel noise \( \Delta V_{gbp} \) is the difference on the pixel buffer noise, \( V_{gsf} \), with autocorrelation \( R_{outp} \) sampled at two different times distant from half of the given time to read a line \( (\frac{t}{2}) \). So its autocorrelation, \( R_{gbp}(t, t) \), which exprime the equilibrium noise power at the gate of the buffer due to DS is:

\[
R_{ds}(t, t) = 2(R_{outp}(0) - R_{outp}(\frac{t}{2}))
\]

The DS has also an other well-known effect, i.e. increase the reset noise on the integration capacitor by a factor of two because of the difference of two uncorrelated signals, so that:

\[
V_{r_{sat}}^2 = \frac{2kT}{\lambda_{int}}
\]

The noise of the column amplifier buffers is just superimposed on the output signal and can be calculated using eq. 16 with \( t_1 = t_2 \).

### 3.5 Fixed pattern noise

Fixed pattern noise (FPN) is related to the statistical variation of pixels elements and column amplifiers properties and so, to transistors mismatch. It is usually removed by DS or correlated DS (CDS), however to the first order only. There remains some residue to this FPN which can be important if no care is taken. To lower it, it’s important to model and quantify FPN as a function of the design parameters, which includes the layout level and the technological matching parameters given by the foundry, i.e. \( \sigma_\beta = \sigma (\delta \beta / \beta) \) and \( \sigma_{V_{t}} \).

For two transistors far from each other on the same wafer, the mismatching is related to gradients across the wafer:

\[
\sigma_{V_{t}}^2 = S_{V_{t}}^2 D^2
\]

where \( S_{V_{t}}^2 \) is the process dependent parameter.

For two close transistors with same size, same shape and same orientation, we generally have:

\[
\sigma_{V_{t}}^2 = \frac{A_{V_{t}}^2}{WL}
\]

\[
\sigma_{\beta}^2 = \frac{A_{\beta}^2}{WL}
\]
with $A_{\alpha,\beta}$ and $A_{\beta,\gamma}$ process dependent parameters.

In the case of imagers, the mismatching due to gradients usually dominates because of the great distance between the transistors of the farthest pixels.

We identified the different sources of mismatch on the signal path from the pixel to the output of the column amplifiers. The dominant term is the mismatch introduced by the current mirror $M$ of each column amplifier on the bias current of the transistors $M_m$. The imprecision of the output current of the mirrors is:

$$\sigma_{I_{ds,mi}}^2 = \sigma^2(\delta I_d/I_d) = \sigma_{Mm}^2 + \left(\frac{g_m}{I_d}\right)_M^2 \sigma_{V_{th,mi}}^2. \quad (22)$$

This yields an output voltage mismatch given by:

$$\sigma_{V_{out,mi}}^2 = \left(\frac{g_m}{I_d}\right)_M^2 \frac{\sigma_{I_{ds,mi}}^2}{\left(\frac{V_{th,mi}}{\left(\frac{V_{th,mi}}{2}\right)}\right)^2} \sigma_{m}^2. \quad (23)$$

where $V_{th,mi}$ is Early voltage of the output mirror.

4 Results

We implemented our model in Matlab and optimized two designs, one in FDSOI, the other in BULK, using the classical parameters of 2um CMOS processes. The results show a net advantage for SOI (Table 1) as explained here under.

The better subthreshold slope of FDSOI MOS transistors allows to reduce the threshold voltage ($V_{th}$), when compared to BULK for identical on-off current ratio. Typical $V_{th}$ values for 2um process are 0.4V for FDSOI and 0.7V for BULK. This results in a direct dynamic range gain by reducing the gate to source voltage needed for the same bias current (eq. 6).

The reduction of the body factor in FDSOI ($n=1.1$ vs $n=1.4$ in BULK 2um) provides better buffers linearity and also a further increase in dynamic range by reducing the gate to source voltage needed for the same current (eq. 7). This also leads to higher transconductance for the same drain current and thus higher $\frac{g_m}{I_d}$ (35 $V^{-1}$ max compared to 26 $V^{-1}$ in BULK) which in case of the source followers is an advantage for reducing noise from the mirrors and FPN (eq. 15 and eq. 23).

The reduction of a factor of three of the SOI drain-source parasitic capacitors for transistors of the same size, when compared to BULK, allows an important reduction of the bus capacitances, directly reducing the dynamic power consumption (eq 4) and lowering the timing requirements in SOI (eq. 1). This allows for a reduction of the bias current of the buffers and then a reduction of static power consumption as well(eq. 3). Finally, this also allows an increase in dynamic range by reducing the required $V_{th,s,f}$.

Table 1: imager performances under 3V supply, P.O. stands for pixel output

<table>
<thead>
<tr>
<th>Performances</th>
<th>SOI-2um</th>
<th>BULK-2um</th>
</tr>
</thead>
<tbody>
<tr>
<td>P.O. Readout noise</td>
<td>0.25mV</td>
<td>0.22mV</td>
</tr>
<tr>
<td>P.O. dynamic range</td>
<td>2.3V</td>
<td>1.45V</td>
</tr>
<tr>
<td>SNR</td>
<td>70dB</td>
<td>76dB</td>
</tr>
<tr>
<td>$P_{stat}$</td>
<td>38.5uW</td>
<td>75uW</td>
</tr>
<tr>
<td>$P_{dyn,mean}$</td>
<td>127uW</td>
<td>226uW</td>
</tr>
<tr>
<td>$P_{tot,mean}$</td>
<td>150uW</td>
<td>301uW</td>
</tr>
<tr>
<td>FPN</td>
<td>1.8mV</td>
<td>2.7mV</td>
</tr>
<tr>
<td>FPN/Output dynamic range</td>
<td>0.08%</td>
<td>0.26%</td>
</tr>
</tbody>
</table>

5 Conclusions

We have presented the top down design of an APS circuit using an analytical model of its architecture. The model has been applied to the design of an 50 frames/s 512x512 pixels imager in a 2um CMOS both in BULK silicon and in SOI technologies. This has allowed a fair comparison of the two technologies performances in the domain of APS imager. SOI Results demonstrate a reduction by two of the power consumption and a dynamic range increase of 0.8 V for the imager under 3V supply. It results in an SNR of nearly 80 dB instead of 76 dB. Fixed Pattern Noise (FPN) is also reduced from 2.7 mV to 1.8 mV which represents 0.2% and 0.08% of the dynamic range respectively. Potential results achievable in SOI have to our knowledge never been reached by BULK APS imagers up to now.

References