Using an Event-Driven Model to Optimise Charge Pump Phase Locked Loops

Pascal ACCO
LESIA – Laboratoire d'Étude des Systmes Informatiques et Automatiques,
INSA – Institut National des Sciences Appliques, DGEI,
135 avenue de Rangueil, 31000 Toulouse, France.
e-mail: pascal.acco@insa-tlse.fr
WWW: http://www.lesia.insa-tlse.fr/

***Abstract* —**
The design of CP-PLL is a difficult exercise because of the wide range of applications and the complexity of modelling. As shown in [1] a good behavioural model of the second order CP-PLL is the event driven model proposed in [3]. The event-driven model can run very fast simulations with a good accuracy. In this paper we will define a criterion to measure the quality of a design. This criterion will be suitable for most applications. An optimisation of this criterion is possible and will help to design the filter parameters.

1 Introduction

In [1] the event-driven model for a CP-PLL is compared to the Spice transistor-level model. It appear that the event-driven model gives almost the same results than the Spice model. The differences are due to non-linearities that are not modelled in the system such as the VCO characteristic and the current source dynamics.

The cost of the high accuracy of the Spice-model is the time taken to run one simulation. This time can reach one day to simulate a 20 μs long response (Sparc 5 - 200 MHz). Event-driven simulation on the same computer is 140 millions times faster.

Moreover, the model equations are very easy to determine compared to those found in the discrete time non-linear model in [4]. This relative simplicity allows one to add some complex phenomena such as overload and noise generation in the circuit.

To help the designer, a simulation can be done for each set of parameter values. A criterion can be applied to these simulations to determine the quality of each design. The parameters that give the best criterion value will be taken as a starting point by the designer.

2 Introduction of noise in the model

In this paper we will consider the same CP-PLL and use the same notation as in [3]. We will introduce white Gaussian noise at the input and at the output of the model as shown in 1. This noise will allow us to develop a criterion to measure the noise rejection of the CP-PLL.

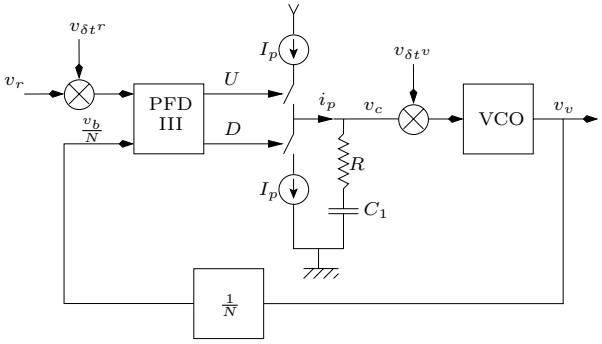

Figure 1: CP-PLL model with input and output noise

The noise effects are represented in the model by small variable delays on the expected input and output falling edges. The input delay δt^r and the output delay δt^v have a Gaussian distribution centred on zero with respective standard deviations σ_r and σ_v.

The noise in the VCO input voltage $v_{\delta t^v}$ can not be directly represented in the model because it is not constant between two events. So, we consider that the time of the next falling edge of the VCO output is delayed of δt^v. The relation between $v_{\delta t^v}$ and δt^v is not explicit as it is the solution of a variable bound integration of the noise $v_{\delta t^v}$.

Usually those standard deviations are smaller than the input signal period T and their values are around 200 ps. The probability of a noise value greater than the period T is small but not zero. So, to respect the principle of causality, noise samples whose absolute values are greater than T will

be erased from the sequence.

The dates of the events are disturbed by the introduction of these noise. When the noise sample is large and negative the date of the next event can be smaller than the date of the initial event. In these cases the date of the next event will be chosen at t_{min} seconds after the initial event.

To introduce noise in the event-driven model, the equation which determines next event date (1) is changed in (2):

$$t_{k+1} = min(t^v_{k+1}, t^r_{k+1}) \quad (1)$$

$$t_{k+1} = max(min(t^v_{k+1} + \delta t^v, t^r_{k+1} + \delta t^r), t_{min}) \quad (2)$$

With equation (2) the PFD pulse width can not be smaller than t_{min}. This time correspond to the delay introduced by the gates and the buffers in the reset feedback signal of the state machine described in [5].

When the event is a VCO feedback signal falling edge the VCO phase must be a multiple of 2π which means the VCO falling edge. This is obtained by replacing the term t_{k+1} by t^v_{k+1} in the VCO phase equation (3). When the input noise is introduced the phase of the input signal can no longer be deduced from the time variable. A falling edge will not appear when the time is a multiple of the period T because this period is not constant but noisy. A new variable φ^r_k is added to represent the phase of the input signal. Its equation (4) has to be added to the event-driven model.

$$\varphi^r_{k+1} = \varphi^r_k + \frac{(t_{k+1} - t_k)}{T} 2\pi \quad (4)$$

As for equation (4) when the event is an input signal falling edge the term t_{k+1} is replaced by t^r_{k+1} in (4).

With these equations the output or input signal falling edge event are recognised by testing respectively whether φ^v_k or φ^r_k is a multiple of 2π.

3 Optimisation criterion

The PLL design constraints chosen in this study are the input noise rejection constraint, the VCO noise rejection constraint and the fast locking time constraint (which include the stability constraint).

A criterion which estimates all these constraints and displays the relative strength of each constraint will be defined. This criterion will be used to design a PLL for different kinds of applications. The design of a frequency synthesiser makes the fast dynamics more important than the noise rejection, whereas in the design of a clock recovery system noise rejection is the most important constraint.

In [2] a linear combination of the locking time and the residual noise at the N-divider output is proposed to solve this problem. This criterion is not used here because it can not measure directly the noise at the VCO output.

An image of the VCO output frequency is the instantaneous VCO input voltage. The event-driven model permits us to calculate very easily this voltage at any moment of the simulation. The criterion proposed in this paper is described by (5).

$$A_{k+1} = A_k + \int_{t_k}^{t_{k+1}} |v_{goal} - v_c(t)|\, dt \quad (5)$$

$$\text{with } A_0 = 0$$

$$\text{and } v_{goal} = \frac{F_r N}{K_v}$$

This equation is the recurrence equation that calculates at each step the integration of the difference between the steady-state voltage value v_{goal} and the instantaneous voltage value of the VCO input $v_c(t)$. The steady-state voltage value is the VCO input voltage for which VCO frequency is equal to NF_r. The expression for $v_c(t)$ is linear between events, so a simple analytical expression of the primitive of the integration exists and is very rapidly calculated.

The criterion function F chosen is the VCO input voltage error mean value. After one simulation the criterion value is obtained by dividing the last value of the integration A_n by the length of the simulation t_n where n is the number of the last iteration.

A bad input and/or output noise rejection will increase the criterion. The strength of input and output noise constraints increases with the values of the white Gaussian standard deviation σ_r and σ_v.

A low dynamic or an unstable system will increase the criterion because of its long acquisition time. The strength of this criterion is increased by choosing an initial capacitor voltage value far from its steady-state value.

The jump voltage across the resistor which appears directly on the VCO input also increases the cost function F. This permits us to take into account the modulated noise generated at the VCO output by these jump voltages. This is the main advantage compared to the criterion proposed in [2] which can not "see" these modulations from the N-divider output.

This criterion can assess the strength of each design constraint (noise rejection and dynamics) and also measures the noise generated by the jump voltage across the resistor. This recursive criterion can be calculated in the same time of the simulation and does not significantly increase the simulation time.

$$\varphi_{k+1}^{v} = \varphi_{k}^{v} + 2\pi \left[\frac{\alpha K_v}{2} \left(t_{k+1}^2 - t_k^2 \right) + \left[f_{v0} - K_v \left(\alpha t_k - v_k - \alpha I_p R \right) \right] \right] \left(t_{k+1} - t_k \right) \quad (3)$$

The relative choice of σ_r and σ_v is easy because those two variables are defined as the standard deviation of the noise that can be measured and is in the range of 200 ps.

But the choice of the initial error voltage at the VCO input is not immediate and need to be adjusted on some well known good design to get an idea of its value.

4 Optimisation by parametric sweep

As the simulation and evaluation time cost are very low, a sweep of all physically reachable values of (R,C) could be done. For each point in the (R,C) parametric plane a simulation and an evaluation is done. The results are stored in a matrix which could be plotted to see the evolution of the criterion as a function of R and C. The optimal value is immediately found without complex algorithm. This sweep also allows one to see the criterion degradation when the parameters are different from the optimal values.

For example, in the case of clock recovery systems the noise rejection is the most important constraint. In this case the criterion is calculated with a strong noise at the input and in the VCO. As the fast dynamic is not important in these designs the initial voltage error is zero.

A parametric sweep of all the resistor values from 0 to 100 $K\Omega$ and all the capacitor value from 50 pF to 1000 pF is done for a simulation horizon of 20 μs. This kind of sweep represents 65025 simulations computed in 40 seconds with a Sparc 5 processor running at 200 MHz. The equivalent time with the Spice model is around a few centuries.

To help the design it is interesting to evaluate what can be the best design for a given capacitor value. For each capacitor value, all the resistors values are swept and the value that gives the best criterion is stored.

fig. 3 displays the optimal resistor for each capacitor value. fig. 2 represents the criterion value for each capacitor value and their corresponding optimal resistor. When the capacitor is smaller than a few pF, the criterion value increases suddenly, this is connected to the overload phenomenon. This phenomenon occurs when the VCO input voltage becomes greater than the power supply V_{cc}. The modelling of overload phenomenon is not described in this paper. For larger capacitors, the quality increase up to the optimal value. With fig. 2, the designer can directly choose the value of the capacitor and manage the compromise between a large and expensive capacitor and a good design. In this case a good compromise is a $300pF$ capacitor and a $17.5K\Omega$ resistor.

5 Conclusion

An optimisation method using the event-driven model for the CP-PLL has been proposed. This method gives the optimal design considering an evaluation criterion of the noise rejection and the fast dynamic of the circuit. The very low run time execution of this model permits a designer to try all possible values. With this method help is given to improve the compromise between a small capacitor and a good design. This kind of model could be applied to the third-order CP-PLL model. The corresponding event-driven model needs to solve an implicit equation at each step. An optimisation algorithm should be used instead of brute force in this case.

References

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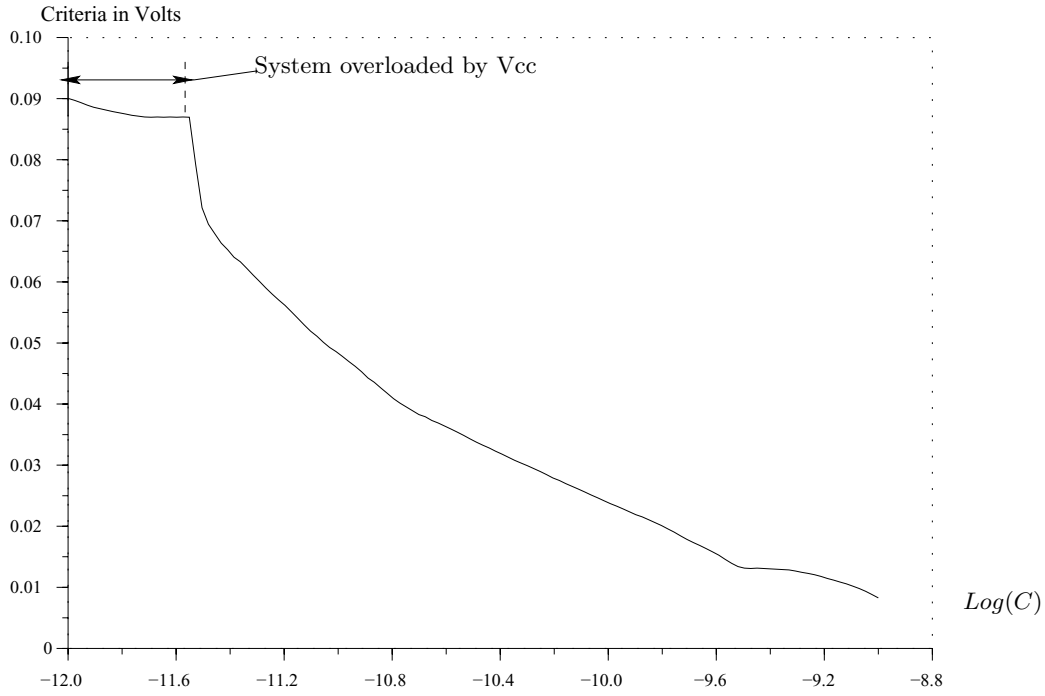

Figure 2: Criterion vs capacitor

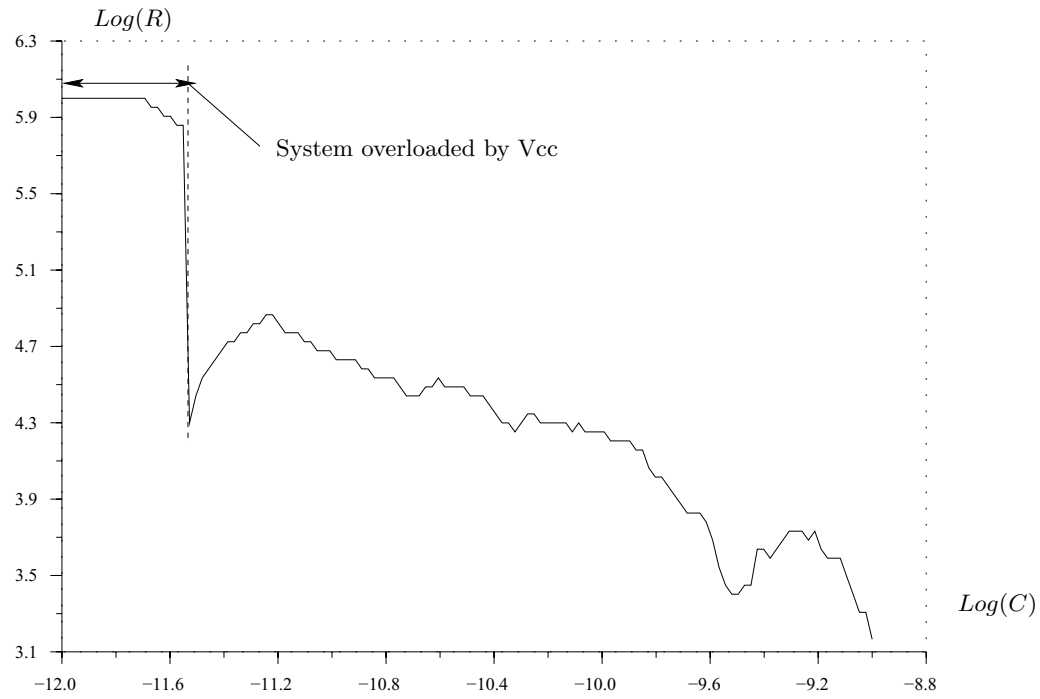

Figure 3: Optimal resistor vs capacitor

Parameters for this optimisation:

Input signal frequency $F_r = 4$ MHz	Current pump value $I_p = 10\ \mu A$
Divider value $N = 50$	PFD minimal pulse width $t_{min} = 1$ ps
VCO gain $K_v = 100$ MHz/V	Power supply voltage $V_{cc} = 3.3$ V