An Improved Current Mirror Based Approach for Linear Spatial Filtering

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***Abstract* — In this paper a current mirror structure is presented that can be used to build large processor arrays performing linear spatial filtering. The proposed structure practically halves the number of transistors when compared to previous solutions. This improvement has been made possible by moving the processing into positive range. The advantages of positive range image coding in image transfer are also discussed. Simulation results are included for a small filter network.**

1 Introduction

Linear spatial filtering has been shown to be very effective means for image processing, e.g. [1]. Linear filtering has been proposed to be used in different Cellular Nonlinear Network algorithms also [2]. Even though the processor structure of the CNN allows also nonlinear image processing, in this case only the linear region in the nonlinear transfer function is required. In this paper we propose a current mode structure that can be used to linear image processing but can also be included as a part of CNN cell structure to perform the required tasks in the algorithm.

2 Positive Range Processing

Conventionally in the analog circuits, and in analog computation, a ground level is defined as some voltage level between power supplies if voltage mode computing is performed. If, on the other hand, all the meaningful signals are coded as currents, a typical choice of the ground level is the zero current. With this type of current mode coding the direction of current flowing into some node determines its sign. In accordance of CNN framework suggestions have been made where the processing takes place in positive range only [3, 4, 5]. In this study we suggest to do the linear filtering also in positive range. This mapping is shown to preserve the actual processing result where, at the same time benefits can be seen in hardware realization and in time to transfer image information.

The conventional image coding approach in analog domain is seen on the left hand side of Fig.1. In this case the input values can be either positive or negative and also the output of the processing can have both polarities.

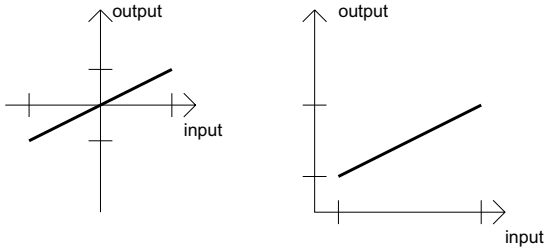

Figure 1: The conventional and the modified input/output range.

The modified input/output range can be seen on the right hand side of Fig.1. In this modified case an offset has been added to the input and this results in the change of output range too. This addition of offset does not destroy the result of the processing in any way because the system is linear and we can use the superposition idea to separate the processing result from the offset. The magnitude of the offset that guarantees always positive results can be extracted from the filtering task by examining the dynamic range of signals in different nodes. The use of positive range results in simplification of the hardware, but we suggest to set the processing range in such a manner that the minimum possible output is clearly above zero. The benefits of this in current mode are explained later in this paper.

3 Processing element

In this section the proposed hardware construction is introduced. The new circuit is based on the same type of current mirror building blocks than first described in [6]. The basic structure is illustrated in Fig. 2.
The basic idea of the concept is described in more detail in [6] so here the functionality of the circuit is only briefly discussed. We first introduce a circuit where only one directional currents (positive) are output from the evaluation block and we then describe how the other current direction (negative) can be realized.

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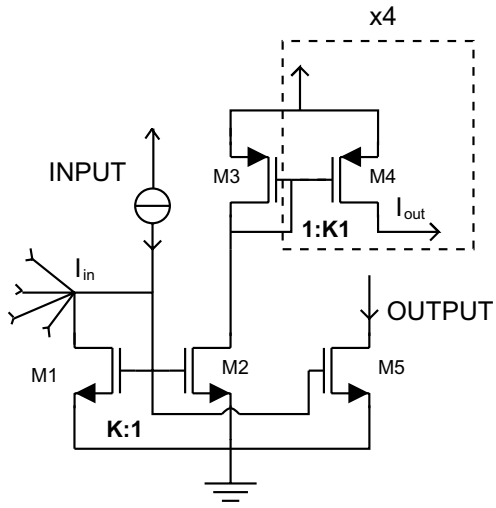

Figure 2: Calculation unit schematic consisting of two current mirrors.

The idea of the current mode circuit is to sum current contributions from the neighborhood and lead this contribution to a first current mirror (M1, M2). Additionally to the contributions from the neighbors, also the input current, representing the original image content, is added in the same node. This input current, together with a possible offset current used in the positive range processing, is depicted by a current source $INPUT$ in Fig. 2. A scaled version of the sum current is lead to the input of the second current mirror, where another current scaling may be possible. Replicas of the output of the second current mirror are connected to the input summing nodes of adjacent processing units. In Fig. 2 four output currents are generated and they can be connected to e.g. cells in the four main directions. The result of the processing is available as current from the drain of the current source transistor M5.

In the above we have described how to construct structures having output currents to the neighbors from PMOS type current sources. These contributions are equivalent to positive couplings between cells. Following the idea in [6] also negative couplings can be realized. These type inhibitory signals are easily generated by leading a scaled version of the sum current through M1 in Fig. 2 to the summing nodes of the neighbor cells.

Because of the limited space, we refer the reader to [6] for a detailed analysis on how the spatial transfer function can be controlled by controlling the different mirroring ratios in the current mirror structure.

3.1 Comparison to prior art

In [6] it was stated that because the sum of the currents entering the first current mirror can be either positive or negative and because the structure of Fig. 2 can only handle one directional currents, two current mirror structures are required to realize the calculation unit, or the cell. In this previous structure there is one NMOS and one PMOS diode connected transistor at the input of the cell. Moreover, a sort of current comparator structure is required at the input of the cell to inhibit a direct current flowing between power supply and ground through the two diode connected transistors. In this paper we propose to move the processing to positive range because then it can be guaranteed that the current entering the cell summing node is always unidirectional, in our case we define that direction as positive. Now, if only one directional sum current can be guaranteed, only one mirroring structure is needed instead of two as in the prior art. Also, there is no need to have current comparator at the input of the cell. Therefore it can be stated that by using positive range processing the transistor count can be more than halved, a very attractive feature when realizing massive parallel processing arrays.

Another feature that is advantageous in having the result as positive only current is obvious when we want to memorize or write out the result in a fast manner. Namely, in the case of memorizing the result by a switched current memory, only one memory transistor is required if the result can be guaranteed to be always positive. The second advantage of our approach is that the minimum output current is much larger than zero. Very small currents are not preferred because writing a current close to zero to either a memory or to a proceeding processing stage is very time consuming.

4 Simulation Results

Here we will show simulation results for a simple resistive network and for the equivalent CM circuit operating in positive range. The resistive network we use in the simulations is shown in Fig.3. It is a one dimensional network with four nodes.

In the simulation for the resistive network we use an input image shown in Fig.4 where the white pixel is coded as -1 and the black pixel as 1.

In the simulation we use 1A as the unity current so that the node voltages are also in the range [-1, 1] and can be directly interpreted as gray-level values. Because we are only interested in the final result no transient simulation is shown for the resistive network, we only state that the output values of the

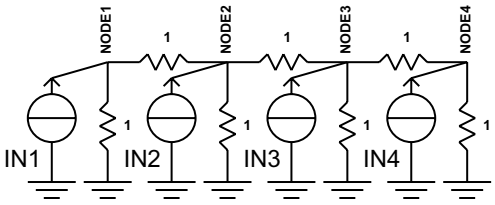

Figure 3: Resistive network.

Figure 4: Input image.

nodes are 0.67, 0.33, 0.33 and -0.33 from NODE1 to NODE4, respectively.
Simulation results for transistor realization are shown for a 1×4 network for a 0.5 micron process. The power supply is set to 2.5V and the boundary conditions are realized as zero-flux. The schematics of the cell used in the simulations is shown in Fig.5.

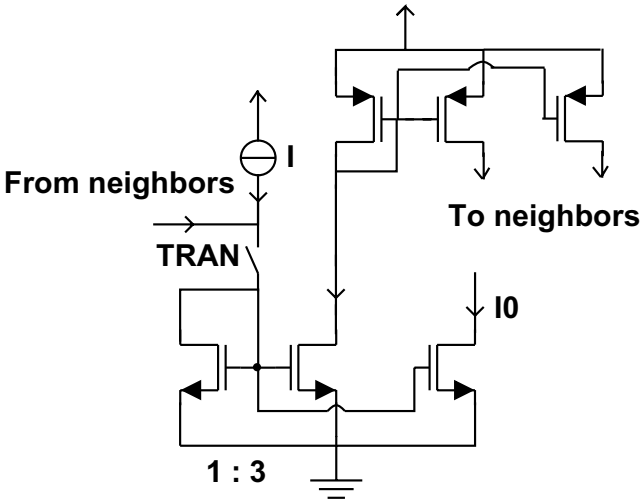

Figure 5: Simulated cell schematics.

By using the CNN notation the template representing the network of Fig.3 is

$$A = [\,1 \quad -2 \quad 1\,] \qquad B = [\,1\,] \qquad I = 0 \qquad (1)$$

The above template results in mirroring ratios 3 to 1 in the NMOS mirror and 1 to 1 in the PMOS mirror. In the following transient simulation white pixel is coded with an input current level 5μA and black pixel with current 15μA. Transient is started at time 5ns in Fig.6 and the network is seen to converge within 100ns. The converged values for the output currents are 13.16μA, 11.57μA, 11.64μA and 8.33μA for the four nodes. When these values are mapped linearly to the range [-1 1] we get pixel values 0.63, 0.31, 0.33 and -0.33, respectively. These values are the same as obtained with the resistor network with an accuracy about 2% of the full range.

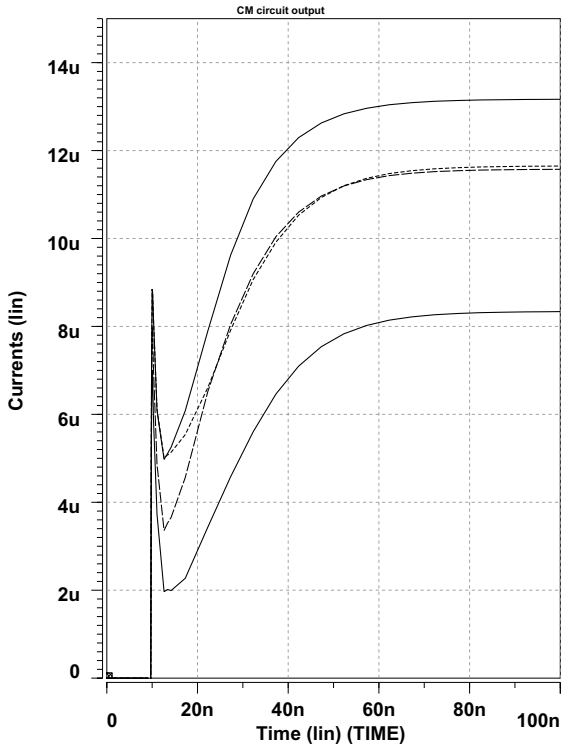

Figure 6: Simulated cell outputs.

5 Conclusions

A simplification to a current mirror based spatial filter hardware was suggested. Advantages were achieved by moving the processing into positive range. The number of current mirrors in the structure was halved and also the further processing of the result is much faster compared to the prior art structure. Simulation results show correct behavior with reasonable current levels.

References

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