On the Use of High-Frequency MOSFET Models in Symbolic Analyzers

O. Guerra[1], F. V. Fernández[1,2], E. Roca[1] and A. Rodríguez-Vázquez[1,2]

Abstract – Traditional quasi-static small-signal MOSFET models used for hand analysis and for automated symbolic analysis are inaccurate for some high-performance, high-frequency designs. A methodology for incorporating a complete quasi-static small-signal model corresponding to modern MOSFET charge models into state-of-the-art approximated symbolic analysis strategies is proposed. The capabilities of this model to improve the quality of circuit designs is illustrated with a practical example.

1. Introduction

To solve typical limitations of traditional MOSFET models, like poor modeling of weak-inversion and moderate-inversion currents, inaccurate predictions of device output conductance and transconductances, non-scalability, non-physical parameters, poor predictions and discontinuities in the modeling of the transition regions between different modes of device operation, poor high frequency performance, difficulty with parameter extraction, inadequate temperature modeling, and unnecessarily large numbers of parameters, third-generation MOSFET models like the BSIM3 [1] and the MM9 from Philips [2] have been introduced and are becoming increasingly popular.

Symbolic analysis of analog integrated circuits relies on the substitution of each semiconductor device by its corresponding small-signal model at the corresponding operating point. For MOS transistor circuits, this analysis has been traditionally based on the five-capacitance quasi-static model in Fig. 1. This is not only characteristic of symbolic analyzers but it is also the way in which analog designers commonly perform manual analysis and design.

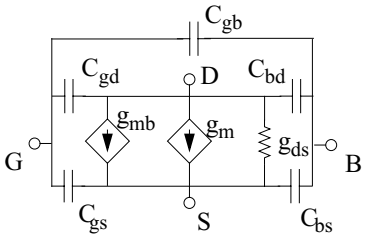

Figure 1. Typical small-signal equivalent model for a MOSFET transistor.

However, the results predicted by symbolic analysis using these small-signal models can significantly vary from those predicted by electrical simulators using the BSIM3 or MM9 models, especially at high frequencies. This paper demonstrates that these deviations can be critical in the design of analog integrated circuits for some sets of specs.

To solve this problem, the use of small-signal charge models with a better correspondence with the third-generation MOSFET models is proposed. A methodology is proposed to incorporate this small-signal model into state-of-the-art approximated symbolic analysis techniques. Its application to solve the inaccuracies of the model in Fig. 1 is demonstrated with a practical example.

2. The complete quasi-static charge model

Let us consider the transistor in Fig. 2. Under small-signal conditions, the charging component of the small-signal currents can be formulated as [3]:

$$\begin{aligned} i_d &= C_{dd}\frac{dv_d}{dt} + C_{dg}\frac{dv_g}{dt} + C_{db}\frac{dv_b}{dt} + C_{ds}\frac{dv_s}{dt} \\ i_g &= C_{gd}\frac{dv_d}{dt} + C_{gg}\frac{dv_g}{dt} + C_{gb}\frac{dv_b}{dt} + C_{gs}\frac{dv_s}{dt} \\ i_b &= C_{bd}\frac{dv_d}{dt} + C_{bg}\frac{dv_g}{dt} + C_{bb}\frac{dv_b}{dt} + C_{bs}\frac{dv_s}{dt} \\ i_s &= C_{sd}\frac{dv_d}{dt} + C_{sg}\frac{dv_g}{dt} + C_{sb}\frac{dv_b}{dt} + C_{ss}\frac{dv_s}{dt} \end{aligned} \quad (1)$$

As can be observed, eq. (1) models the capacitance effect of every transistor terminal on every other terminal. Fig. 3 shows a circuit topology which adds the small-signal currents in (1) to the conventional transport component of the drain and source currents.

Taking into account the internal dependencies between the currents flowing through the terminal nodes of the transistor, it can be demonstrated that only 9 independent capacitance parameters are needed for a complete description [3]. Therefore, the 16 devices modeling the charging currents in Fig. 3 can be reduced to 9.

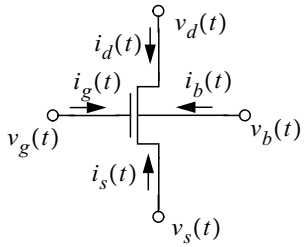

Figure 2. MOSFET transistor with small-signal voltages and charging currents.

[1] IMSE-CNM, Edif. CICA, Avda. Reina Mercedes s/n, E-41012 Sevilla, Spain. Phone: +34-955056666, FAX: +34-955056686, E-mail: pacov@imse.cnm.es

[2] Escuela Superior de Ingenieros, Isla de la Cartuja s/n, E-41092 Sevilla, Spain, Phone: +34-954487378, FAX: +34 954487377

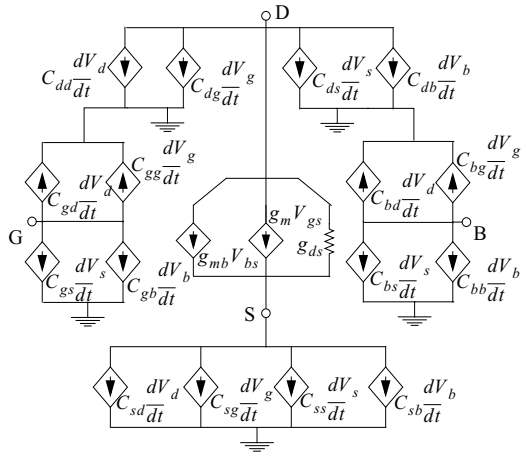

Figure 3. Complete quasi-static small-signal MOST model.

3. Incorporating the complete quasi-static charge model into symbolic analyzers

The capacitance parameters in eq. (1) can be practically handled using the transcapacitance concept. A transcapacitance can be defined as a voltage-time-derivative controlled current source, that is, like a voltage controlled current source whose current is not controlled by the voltage in the controlling branch but the time-derivative of such voltage. Capacitors correspond to a special case of these transcapacitances in which the controlling and controlled branches are the same. In the Laplace domain, it can be formulated as a voltage-controlled current source whose weight (like in capacitors) is frequency-dependent.

The differentiating characteristics of these transcapacitances poses some technical difficulties to their use within approximated symbolic analysis methodologies (based on the combination of Simplification Before and During Generation techniques) [4] .

Simplification Before Generation techniques perform the approximation by replacing those elements whose contribution to the network function is small, with a zero-admittance (element removal) or zero-impedance element (contraction of terminal nodes) [5]. In our practical implementation, this simplification is performed at a reduced number of sampling frequencies, increasing this number only in case that the maximum allowable error is exceeded in some other frequency point. To check the posible frequency points to add, special error control techniques have been developed.

As stated before, the transcapacitance device can be seen as a hybrid between a capacitor and a voltage-controlled current source. Thus, like a capacitor device, it has a complex frequency-dependent value and, like a voltage-controlled current source it has two branches: a controlled one and a controlling one. This means that the transcapacitance value must be first updated at each frequency point, to subsequently evaluate the contribution of the device and perform the appropriate simplification operation on it. Also, it must be checked if the voltage drop in the controlling nodes has been set to zero, which means that the device has to be deleted.

Simplification During Generation techniques perform approximations while the system of circuit equations is being solved providing only the dominant contributions of the circuit characteristic at hand. Most efficient Simplification During Generation methodologies are based on the two-graph method [6]. In this method, common spanning trees to the voltage and the current graphs are generated in decreasing order of weight at each given frequency value until the error criteria are met. Dealing with transcapacitances, the voltage graph will include a branch connecting the controlling nodes and the current graph a branch connecting the controlled nodes; both with the weight given by the transcapacitance value evaluated at the current frequency value.

4. A practical design example

We will consider the design of the simple OTA in Fig. 4 with a reduced set of specifications:

$$GBW \geq 50\text{MHz} \qquad SR \geq 80\text{V/}\mu\text{s}$$
$$PM \geq 60^\circ \qquad A_o \geq 45\text{dB} \tag{2}$$

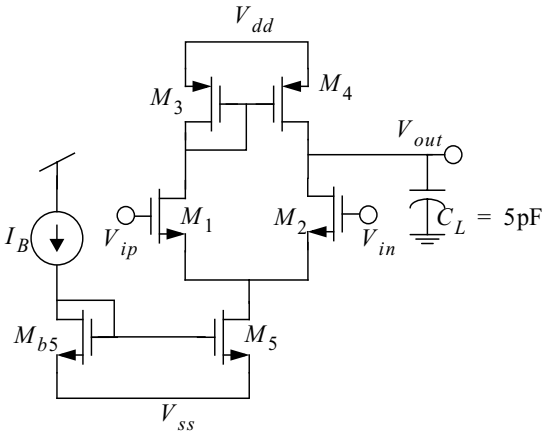

Figure 4. OTA schematic

A design plan will first be developed based on the use of the small-signal model in Fig. 1. To simplify the interpretation of analytical equations, both transistors in the differential pair and both transistors in the current mirror are considered fully matched:

$$M_1 \equiv M_2 \equiv M_n$$
$$M_3 \equiv M_4 \equiv M_p \tag{3}$$

Small-signal analysis of this circuit yields a network function from which the following expressions for poles and zeros can be easily extracted (pole splitting technique was applied to extract the poles):

$$
\begin{aligned}
p_1 &= -g_1 g_2 / [g_{mp} C_{gdp} + \\
&\quad + g_1 (C_{gdp} + C_5 + C_{gdn}) + g_2 (C_{gdn} + C_3 + C_{gdp})] \\
p_2 &= -[g_{mp} C_{gdp} + g_1 (C_{gdp} + C_5 + C_{gdn}) + \\
&\quad + g_2 (C_{gdn} + C_3 + C_{gdp})] / [C_{gdp} (C_{gdn} + C_3) + \\
&\quad + (C_5 + C_{gdn})(C_{gdn} + C_3 + C_{gdp})] \qquad (4) \\
z_1 &= \frac{g_{mn}}{C_{gdn}} \\
z_2 &= -\frac{g_1 + g_{mp}}{C_2 + C_3}
\end{aligned}
$$

where

$$
\begin{aligned}
g_1 &= g_{mp} + g_{dsn} + g_{dsp} \\
g_2 &= g_{dsn} + g_{dsp} \\
C_3 &= C_{bdn} + 2C_{gbp} + C_{bdp} + 2C_{gsp} \\
C_5 &= C_L + C_{bdn} + C_{bdp}
\end{aligned} \qquad (5)
$$

Taking into account numerical values of the parameters, eq. (4) can be approximated to:

$$
\begin{aligned}
p_1 &= -\frac{(g_{dsn} + g_{dsp})}{C_L + C_{gdn} + 2C_{gdp} + C_{bdn} + C_{bdp}} \\
p_2 &= -\frac{g_{mp}}{C_{bdn} + 2C_{gbp} + C_{bdp} + 2C_{gsp} + C_{gdn} + C_{gdp}} \qquad (6) \\
z_1 &= \frac{g_{mn}}{C_{gdn}} \\
z_2 &= -\frac{2g_{mp}}{C_{bdn} + 2C_{gbp} + C_{bdp} + 2C_{gsp} + C_{gdn}}
\end{aligned}
$$

There is a dominant pole, p_1, which together with the analytical expression for the low-frequency voltage gain:

$$
A_o = \frac{g_{mn}(2g_{mp} + g_{dsn} + g_{dsp})}{2(g_{dsn} + g_{dsp})(g_{mp} + g_{dsn} + g_{dsp})} \approx \frac{g_{mn}}{(g_{dsn} + g_{dsp})} \qquad (7)
$$

provide a symbolic expression for the GBW:

$$
GBW \approx \frac{g_{mn}}{C_L + C_{gdn} + 2C_{gdp} + C_{bdn} + C_{bdp}} \qquad (8)
$$

Pole p_2 and zero z_2 form a pole-zero doublet that should be placed above GBW to avoid settling time problems. Zero z_1 is at a very high frequency and does not have to be taken into account.

With these equations and the prescribed specifications a transistor sizing is performed and the electrical simulation of the resulting circuit gives the magnitude and phase plots in Fig. 5. As can be observed the phase margin obtained is much smaller than that prescribed. Fig. 5 also shows the magnitude and phase plots obtained by numerically evaluating the analytical transfer function provided by the symbolic analysis tool SYMBA. Unexpectedly, large deviations appear. According to the evaluation of the analytical expressions the phase margin spec should be met but according to the electrical simulator this does not happen.

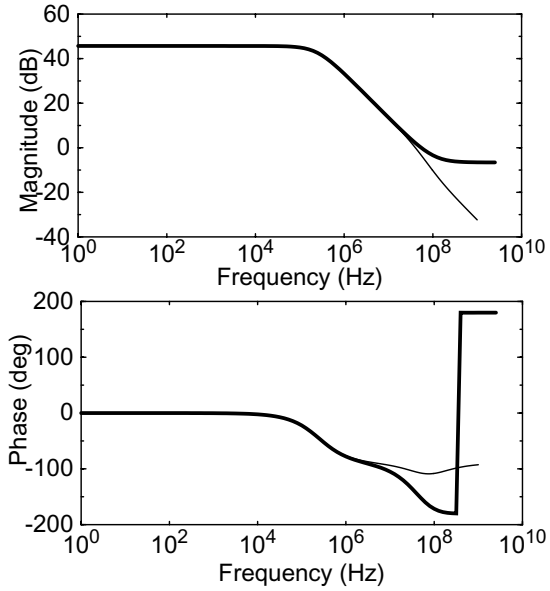

Figure 5. Bode plots of Fig. 4: SPICE simulation (thick line) and evaluation of symbolic network function (thin line).

To trace the origin of the problem, an electrical simulation was performed to obtain the numerical location of poles and zeros (see Table 1). Table 1 also shows the results of the numerical evaluation of eqs. (4) and (6). It can be observed that the location of the dominant pole is quite accurate and the pole-zero doublet has been correctly placed above the GBW. Therefore, the pole-zero doublet cannot be responsible for such deviations. Neither the performed approximations in eq. (6) can. However, unexpectedly a zero appears at the right-half of the s-plane around the frequency of the GBW in the electrical simulation while eqs.(4) and (6) predicts such zero at a much higher frequency. This explains the problem in the phase margin but the analytical equations based on the small-signal model in Fig. 1 are unable to explain such zero location.

The problem can be rooted by using the model in Fig. 3. If a small-signal analysis is performed using this model, the following expressions are obtained for poles and zeros:

$$
\begin{aligned}
p_1 &= -\frac{g_2 + g_1}{g_2 C_3 + g_1 C_7 - g_{mp} C_{gdp}} \\
p_2 &= -\frac{g_2 C_3 + g_1 C_7 - g_{mp} C_{gdp}}{C_3 C_7 - C_{dgp} C_{gdp}} \qquad (9) \\
z_1 &= -\frac{g_{mn}}{C_{dgn}} \qquad z_2 = -\frac{g_1 + g_{mp}}{C_3 + C_{dgp}}
\end{aligned}
$$

	p_1 (kHz)	p_2 (MHz)
electrical simulator	–246.23	–54.407
evaluation of eq. (4)	–245.93	–53.044
evaluation of eq. (6)	–247.08	–56.145
	z_1 (MHz)	z_2 (MHz)
electrical simulator	+50.7296	–107.5895
evaluation of eq. (4)	+203940	–104.22
evaluation of eq. (6)	+203940	–112.29

Table 1. Pole/zero positions.

where

$$\begin{aligned} g_1 &= g_{mp} + g_{dsn} + g_{dsp} \\ g_2 &= g_{dsn} + g_{dsp} \\ C_3 &= C_{ddn} + C_{ddp} + 2C_{ggp} + C_{gdp} + C_{dgp} \\ C_7 &= C_L + C_{ddn} + C_{ddp} \end{aligned} \tag{10}$$

For typical values, equation (9) can be approximated to:

$$\begin{aligned} p_1 &= -\frac{g_{dsn} + g_{dsp}}{C_L + C_{ddn} + C_{ddp}} \\ p_2 &= -\frac{g_{mp}}{2C_{ggp} + C_{dgp} + C_{ddn} + C_{ddp}} \\ z_1 &= -\frac{g_{mn}}{C_{dgn}} \\ z_2 &= -\frac{2g_{mp}}{2C_{ggp} + 2C_{dgp} + C_{ddn} + C_{ddp}} \end{aligned} \tag{11}$$

Equations using the model do match the pole/zero positions. In particular, it explains the zero in the right half of the s-plane at a frequency close to the GBW (notice that C_{dgn} is a negative parameter). Table 2 compares the pole/zero positions obtained by electrical simulation and those obtained by evaluating eqs. (9) and (11).

Moreover, the comparison of the magnitude and phase plots in Fig. 6 obtained by electrical simulation in Fig. 6 and those obtained by evaluation of the symbolic transfer function obtained using the model in Fig. 3 reflects and almost perfect matching.

	p_1 (kHz)	p_2 (MHz)
electrical simulator	–246.23	–54.407
evaluation of eq. (9)	–245.95	–53.961
evaluation of eq. (11)	–247.14	–52.099
	z_1 (MHz)	z_2 (MHz)
electrical simulator	+50.7296	–107.5895
evaluation of eq. (9)	+50.729	–107.05
evaluation of eq. (11)	+50.729	–105.35

Table 2. Pole/zero positions.

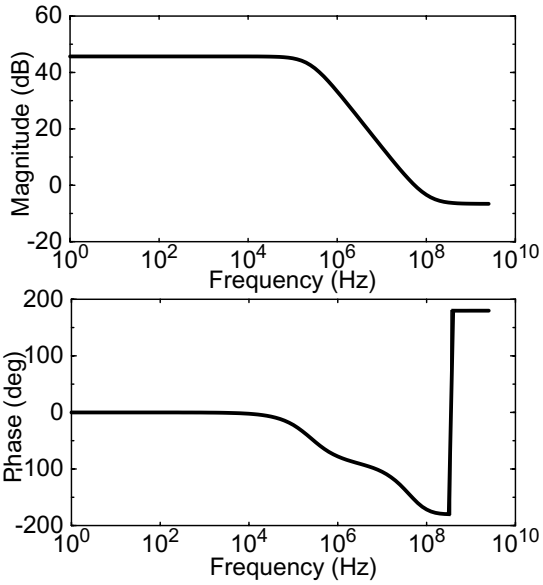

Figure 6. Bode plots of Fig. 4: SPICE simulation (thick line) and evaluation of symbolic network function (thin line).

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