A Simple Model for Digital/Analog Crosstalk Simulation in Deep Submicron CMOS Technology

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Abstract — This paper illustrates a simple model of digital/analog crosstalk, suitable for simulation of digital switching noise in integrated circuits with highly doped substrate and epitaxial layer. The proposed model is suitable for analog simulations using any SPICE-like simulator, and is useful during the design phase to compare different design/layout strategies and evaluate design robustness. A comparison between simulation results and experimental measurements on integrated test structures is presented.

1 Introduction

Competitiveness in a more and more demanding consumer electronics market requires low-cost high-performance integrated circuits (ICs). Single chip solutions reduce costs and increase reliability [1]. Moreover, they can help to reduce weight and size of hand-held electronic products.

In mixed analog/digital integrated systems, performance limitations come mainly from the analog section which interfaces the digital processing core with the external world. In addition to the difficult task of designing state-of-the-art analog-digital interfaces, mixed-signal microintegrated circuits offer an additional challenging aspect. In such ICs, coupling from switching digital nodes and power supplies to analog devices through the common substrate is a serious limitation to analog circuit performance.

This paper discusses some aspects of computer simulation of noise generation and propagation in high-density ICs with highly doped substrate, and proposes a simple model suitable for SPICE-like simulation of noise effects. Experimental results on a test chip designed to characterise crosstalk mechanisms are presented and compared with simulation outputs.

2 Technology Aspects

Technology development is driven by market demand. Main targets are: lower cost, high performance, and high integration density [2].

Modern CMOS technologies use a heavily doped substrate (p+) covered by a lightly doped epitaxial (epi) layer of the same polarity (p). The epi layer is very thin (< 10 µm) and has a high resistivity, in the range of 0.1 Ω·m, while the resistivity of the substrate can be as low as 0.1 mΩ·m.

Being the epi layer 1000 times more resistive than the bulk, any noise current injected by a digital device flows into the deep substrate, as qualitatively shown in Fig. 1. Due to the very low bulk resistivity, the substrate can be substantially considered as a single node. On the other hand, the local voltage inside well regions is affected by the non-negligible resistance due to the light well doping concentration and the epi layer resistance. This means that the noise affecting an analog device is independent of the distance from the digital switching noise source, at least to a first approximation [3]. Fig. 2 illustrates a simple scheme of parasitic resistances in a twin-well submicron epitaxial CMOS technology. Traditional layout techniques for shielding analog parts (guard rings) are less effective in this technology, since they provide a conductive path only for the surface current, while the low-resistivity bulk provides a pathway for most of the injected disturbance [4].
3 Simulation Model

From the above discussion, it is apparent that adequate analysis techniques are required to investigate the effects of digital noise injection and predict the robustness of analog and mixed analog-digital structures. Noise coupling between digital and analog sections can be the dominant noise source, unless mixed-signal systems are carefully designed. In particular, disturbances injected by the digital circuitry are strongly correlated with the clock, and, therefore, they cannot be modeled as white noise. Timing characteristics of noise coupling must be accounted for, especially when the analog circuitry is driven by a clocking scheme correlated with the digital section.

Several techniques for the analysis of substrate coupling in mixed-signal ICs have been recently presented in the technical literature. General methods based on 3-D modeling share a common difficulty in practical applications: their accuracy rely on the knowledge of the substrate doping profile. Moreover, they are not practical when dealing with large circuits, for which a complex network of lumped elements should be generated. Simpler methods consist in discretizing the substrate region, thus obtaining a mesh network of lumped resistive elements. By superposing the active network to the substrate mesh, critical points of the substrate can be identified and the network can be further simplified. Such a technique can combine the advantages of accuracy and computational efficiency [5].

It is worth to point out that digital-noise aspects should be addressed during the design process, so as to avoid incorrect circuit operation as well as difficulties during chip debugging. In this respect, it is very important for the designer to estimate noise effects before the layout phase, to be able to compare different design/layout strategies and to evaluate design robustness. Although very sophisticated models can provide an accurate evaluation of digital noise injection and propagation, it is therefore important to provide the designer with a simple model for this evaluation. In particular, this model should rely on a non detailed information of circuit layout and should be used with conventional SPICE-like simulators. Indeed, SPICE-level description and analysis are still considered the best solution for noise sensitive circuits [6].

A circuit-level model for digital-noise injection in the technology considered, must account for epi layer resistance, high substrate conductivity, bonding inductance, and different ground biasing in analog and in digital sections. In all technologies with epi layer and highly doped bulk, high conductivity makes the heavily doped substrate similar to a short circuit between substrate points in the whole chip, thus vanishing the effect of placing analog devices far from digital ones.

Device simulations confirm that current flow lines are distributed mainly in the heavily doped substrate [7]. Therefore, the resistive path between any two points A and B on the chip surface can be modeled with a lumped network (at least up to frequencies in the gigahertz range), as illustrated in Fig. 3, where \( R_{lat} \) represents the resistance between nodes A and B through the epi layer, \( R_{epi} \) is the resistance between any node in the surface and the bulk, and \( R_{bulk} \) represents the resistance in the bulk path from A to B. Assuming that the current flow is spatially distributed as shown in Fig. 4, the epi layer resistance \( R_{epi} \) can be calculated from technology parameters, as:

\[
R_{epi} = \frac{R_{area}}{R_{perimeter}} \approx \frac{\rho_{epi} t_{epi}}{A} + \frac{\rho_{epi}}{p} \quad (1)
\]

where \( \rho_{epi} \) is the epi resistivity, \( t_{epi} \) is the epi layer thickness, and \( A \) and \( p \) are the area and the perimeter of the biasing region, respectively [8].

Since the bulk resistance \( R_{bulk} \) has a very low value and the lateral resistance \( R_{lat} \) is very high, they can be considered as a short and an open circuit, respectively, and the overall resistance can be approximated with \( 2R_{epi} \).

When a digital gate switches, the digital noise injected into the substrate through capacitive coupling and the voltage drop across bonding inductances change the body bias of any analog device. This effect produces a change in the drain current of MOS devices biased in the active region, thus affecting the analog signal.

The combined effect of bonding inductance and coupling capacitance creates a high-pass network for injected noise. Hence, any isolation scheme attenuates crosstalk effects only at low frequencies. At high frequencies, the capacitive transmission becomes dominant, thus vanishing the isolation benefits [9].

From the above considerations, we can derive the simple equivalent circuit used illustrated in Fig. 5 for the simulation of crosstalk effects on a single analog MOS device (M3). MOS transistors M1 and M2 represent the largest switching element of the digital section (for instance, the last stage of

![Figure 3: Lumped element model of substrate resistivity](image-url)

![Figure 4: Current flow through the epi layer](image-url)
From small signal analysis, the output noise voltage $v_{out}$ results:

$$v_{out} = -R_L i_d = -R_L \cdot g_{mb} v_{sb}$$  (2)

where $R_L$ is the external load resistance, $i_d$ is the small-signal component of the drain current through the analog MOS transistor, $v_{sb}$ is the variation of the substrate voltage due to the injected noise, and $g_{mb}$ is the bulk transconductance of the analog MOS device. Equation (2) assumes that $R_L$ is much larger than the impedance of $L_6$; this assumption is valid for frequencies up to several hundred megahertz.

### 4 Experimental Results

To provide the designer with relevant information for a successful design, the crosstalk model has to be validated. It should be underlined that, in our case, a qualitative validation is sufficient, as our model is intended for pre-layout estimation of crosstalk effects. This validation was carried out by designing a mixed test chip, including a digital section to inject switching noise into the substrate through a capacitor, and an analog section to collect digital noise [10]. In our case, the digital section is an inverter driven by an external clock or, alternatively, by a ring oscillator, while the analog section is a single MOS transistor in common-source configuration. Fig. 6 illustrates an example of a test structure.

Fig. 7 shows the result of an HSPICE simulation of the switching noise effect on the single-transistor amplifier when the injecting digital circuit is driven by an external clock. Transient analysis shows a variation in the drain voltage of the analog MOS transistor, due to the switching of digital circuitry. Oscillations occur after each switching, with an intrinsic frequency dependent on bonding parasitics.

Fig. 8 illustrates the corresponding measurement on an integrated test structure, showing a good agreement in qualitative behaviour. Measurements carried out on several MOS transistors in the test chip (at different distances from the digital section, with or without guard rings) confirmed also that the injected disturb is independent of the distance...
and guard rings are not effective.

Crosstalk noise was also analyzed in a more realistic situation to investigate the possible impact of digital circuitry on analog blocks located on the same silicon die. For these measurements, a digital decimation filter was used as a source of digital noise. This filter is made up of approximately 130,000 gates. Fig. 9 illustrates the result of HSPICE simulation, using the crosstalk model described above. Fig. 10 shows the measurement of the voltage noise collected on the substrate (node $V_{sub}$ in Fig. 5), when the filter is operated at 66 MHz clock frequency. The agreement between simulated and experimental values is apparent.

5 Conclusion

This paper has presented a simple model for SPICE simulations of crosstalk effects in mixed analog/digital circuits in submicron CMOS technology with heavily doped substrate and epitaxial layer. This model is intended to be used before any detailed information about the layout is available. Simulation results are in agreement with experimental measurements on integrated test structures. The proposed model can be exploited in the design of analog/digital interfaces, to provide analog designers with a simple analysis tool capable of accounting for crosstalk effects.

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References


