Substrate effects in HBT modelling for RFIC design

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Abstract: **Substrate effects in complete design models for HBT's in IC's are identified by a one-step model extraction processes that, unlike most other known substrate effect identification procedures, does not require initial test substrate preparations. The method identifies and quantifies substrate effect components that are important for interstage designs and distinguish them from less important substrate capacitances and losses in probe pads.**

1 Introduction

Accurate modelling is a prerequisite for broadband design of RF IC's. Initial trials with a commercial SiGe HBT process for designing L-band modulators and demodulators in radar applications, where the requirements are 400MHz and/or 800 MHz phase linear signal bandwidth around carriers, have shown that we must supply substrate effects to the model that the vendor provides. Unlike other small signal modelling approaches and more theoretical investigations [1], the one that is used in this work does not rely upon separate test-jig substrate identifications followed by a subsequent model deembedding process. Instead all components in the complete equivalent circuits are identified in one step. Here we employ an extraction process, which utilizes uncertainty data from measurements in conjunction with the model network sensitivity matrix.

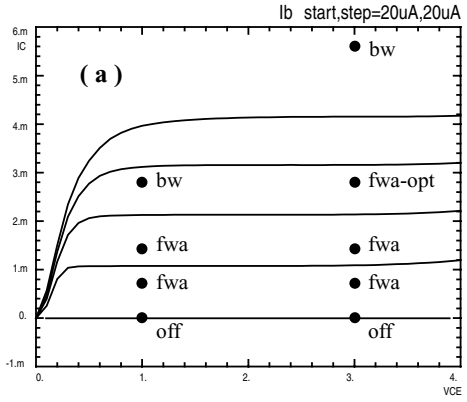

Figure 1: Measured HBT DC characteristics. The dots indicate point where models are fitted to either the forward active, the base-widening, or the cut-off model. They are denoted fwa, bw, and off respectively.

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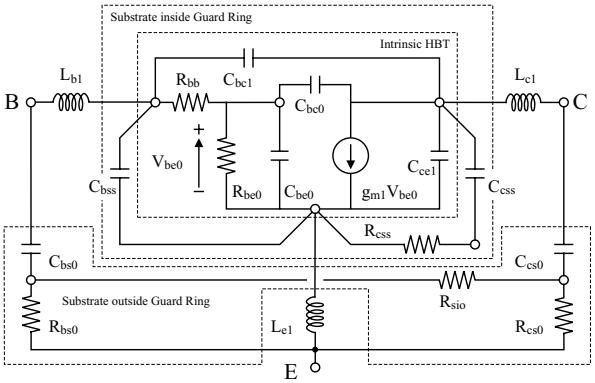

Figure 2: Small signal equivalent circuit for HBT in forward active state, fwa.

It gives us at tool by which we fast and efficiently may survey and select model structures that stay stable and consistent across the required operating range of the transistors. The basic method was originally developed in [2], and has proved successful in a series of modelling tasks including the one discussed in [3].

2 Model Structures ,

Biasing and operating ranges of the HBT npn transistors in this investigation are confined to the ranges in the DC characteristics of Figure 1. They are close to the ratings. The transistor is small, 4um^2 emitter, and it is closely surrounded by a guard ring that connects the substrate to the emitter terminal. Small signal models are extracted and compared in the bias point that are indicated by heavy dots in the figure. As explained in [2] or [3], the model extraction process must proceed until we get model responses that fit within the measurement uncertainty limit estimates. This is a conditions for benefiting

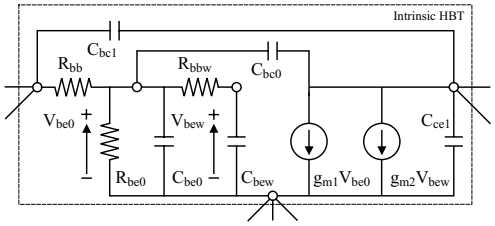

Figure 3: Replacement for the intrinsic part of the equivalent circuit from Figure 2 to account for distributed effects under base-widening conditions. The resultant model is called the base-widening model, bw.

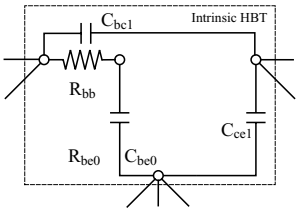

Figure 4: Replacement of the intrinsic part of the equivalent circuit from Figure 2 if the transistor is cut-off. The complete model is called the cut-off or off model.

from sensitivity matrix data. To achieve this goal in all selected bias point, three model topologies were required, one for the normal forward operation, one at high currents where base-widening effects may be sensed so a distributed description of the carrier transport through the base is required. Finally a model that applies to the cut-off operation with zero DC current. The models are referred to as "fwa", "bw", and "off" respectively and they are detailed in Figure 2, Figure 3, and Figure 4. Examples of the fitting accuracies for each type of model are illustrated in Figure 5

3 Parameter Extractions

Only the forward active model in Figure 2 shows the complete equivalent circuit. As seen here, the model is subdivided into a section representing intrinsic HBT operations, which is encircled by three components, C_{bss}, C_{css},and R_{css}, that represent substrate effects inside the guard ring and beneath the transistor. Finally, the transistor connections to the terminal probe pads are described by small series inductances, pad to substrate capacitances and substrate losses outside the transistor. The important point in the process of identifying substrate effects is that only the intrinsic part of the model needs substitution between the different mode of operations. Model topologies for substrate effects both inside and outside the guard ring and for the transistor leads remain the same in all cases with reasonably stable component values across all the operating points.

To elaborate this point further, Table 1 summarizes model extraction data for a forward active situation. Shown here is a column of resultant component values and then two columns with intersection and relative deviation data. They are derived from the sensitivity matrix by singular value decomposition and summarize statistical estimates for the parameter values. The intersection column data are interpreted as the relative deviation for each particular parameter if all other parameters were precisely extracted. In contrast, the relative deviation parameters, which are always higher, take into account mutual correlations between all parameters in the model extraction process. The ratio between these two figures give a simple estimate of how independent a given parameter is. Scanning trough the

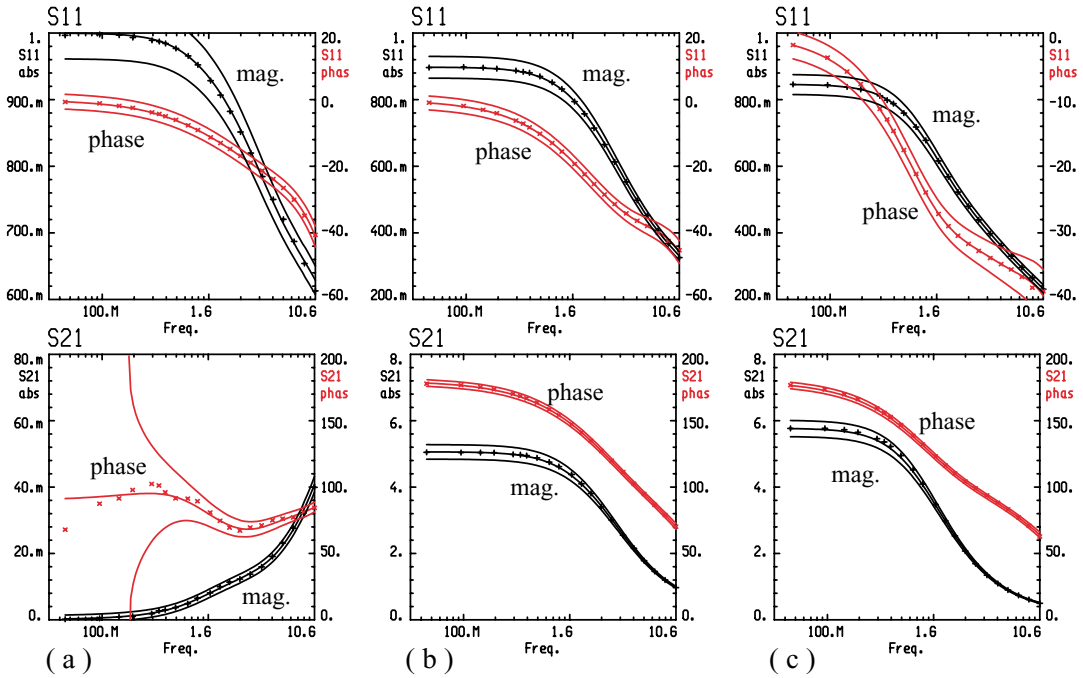

Figure 5: Examples of model fitting in (a) cut off at 3V,0mA, (b) forward active at 3V,2.8 mA, and (c) base-widening at 3V,5.6 mA. Each set of magnitude or phase curves holds four entities. First points of measured data selected as targets in fits, 2nd, a center curve showing fitted model responses, 3rd, the upper and, 4th, the lower 99.9% uncertainty estimates of the network analyzer and probe station setup.

Parm.	Value	Intersc %	Rel. dev %
Rbb	102.6	.25	1.55
Cbc0	2.2231f	3.75	21.93
Cbe0	493.36f	.21	1.59
Rbe0	824.43	.99	2.31
Gm1	60.008m	.15	.40
Cbc1	8.2417f	.57	2.09
Cce1	59.088f	.94	2.92
Cbss	70.782f	.78	1.52
Ccss	136.96f	1.04	8.64
Rcss	247.97	.93	3.75
Lb1	198.15p	2.10	5.42
Lc1	150.83p	5.33	13.97
Le1	115.28p	.77	1.88
Cbs0	115.95f	3.98	8.78
Rbs0	1.5869K	2.85	15.15
Ccs0	141.34f	2.82	9.50
Rcs0	931.74	1.92	19.08
Rsio	17.984K	2.51	9.26

Table 1 Extracted parameter values and their statistical data for the forward active HBT model at 3V, 2.8mA.

table, the general pattern - with two prominent exceptions - is, that if we moves from the intrinsic transistor outwards through the guard ring to the pads, we simultaneously goes from accurately determined components to more and more uncertain and cross correlated components. The two exceptions are the intrinsic feed-back capacitance C_{bc0}, which is highly correlated by the larger overlay capacitance C_{bc1} and, therefore, more uncertain. The other exception is the common emitter lead inductance L_{e1} that is accurately determined due to its strong influence upon both gain and feed-back in the transistor.

If a component in the model shows a relative deviations of more than 100%, it should be left out, especially if it correlates with other parts of the model. Otherwise it convoys uncertainty to other components. This observation is the fact behind the employment three models instead of one in the present HBT model extraction. In principle, the base-widening intrinsic circuit from Figure 3 contains all circuit components that are present in the other two intrinsic models. However, components that are superfluous in the forward active or the cut-off cases make the complete base-widening equivalent circuit useless here because uncertainty will spread also to important parameters. This leaving out approach is a key to the present extraction method, since it gives a fast way of surveying and selecting model topologies that suit a given set of experimental data.

4 Substrate Effects

Substrate effects from inside the guard ring are often the most important in a design process, since they are present in all transistors. Their significance are illustrated by Figure 6. It is clearly observed that the design kit model responses differ from actual measured data. In some respects, like the difference in S_{21} magnitudes, the difference may be ascribe to process tolerance. It is also seen that the S_{11} and S_{21} roll-off frequencies are nearly the same in both design kit data and measurements. This is, however, not the case with the two other magnitudes, S_{12} and S_{22}, a fact that is illuminated further by the third set of curves denoted “inside model”. This set shows simulated responses from the parts of the fitted models that hold the intrinsic HBT and substrate effects from inside the guard rings, but leaves out effects of lead inductances and substrate outside the guard rings according to the subdivision in Figure 2. Including the effects from inside the guard ring we clearly get much more realistic frequency dependencies of both the transistor feed-back effects and the output impedances through S_{12} and S_{22}. To be more accurate in the design phase, each transistor should therefore be surrounded by elements from the model identifications above that have no counterparts in the vendor supplied design kit models. This is firstly the substrate effects from inside the guard ring but, surprisingly, the overlay diode capacitance C_{bc1} should also be included. Table 2 summarizes the

model type	Vce V	Ic mA	Cbc1 fF	Cbss fF	Ccss fF	Rcss Ohm
co	1	0.0	11.3	73.8	172.	282.
fwa	1	0.7	10.5	51.2	179.	249.
fwa	1	1.4	10.6	60.8	159.	235.
bw	1	2.8	9.1	54.1	170.	251.
co	3	0.0	9.9	74.2	176.	288.
fwa	3	0.7	8.7	51.5	183.	257.
fwa	3	1.4	8.6	59.7	169.	243.
fwa	3	2.8	8.2	70.8	137.	248.
bw	3	5.6	6.4	54.9	218.	247.

Table 1 Substrate and overlay elements inside guard ring in all parameter extractions. Model types refer to Figure 1 to 4.

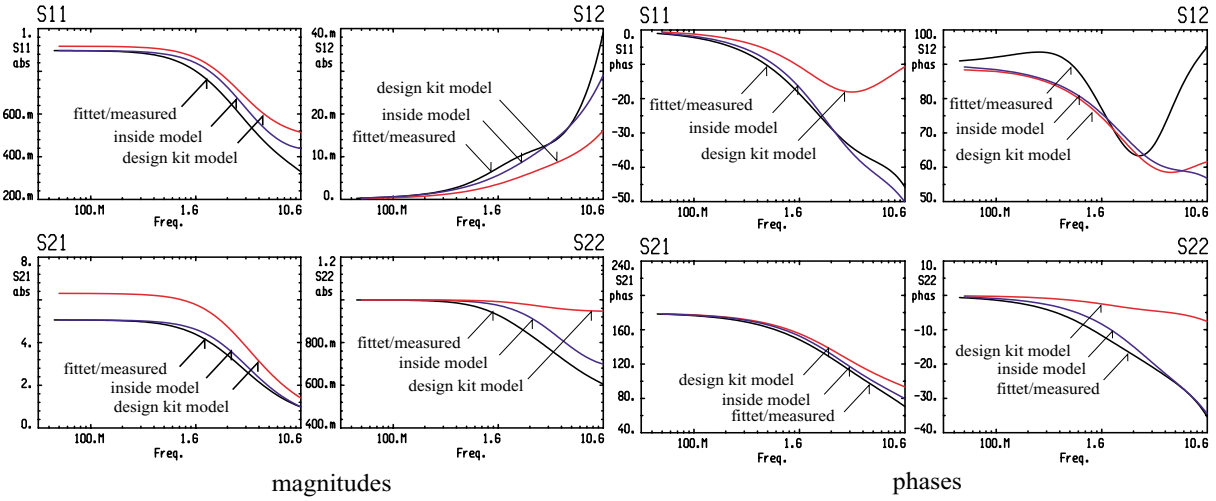

Figure 6: Differences between s-parameters from the vendors design kit, measured/fitted data, and responses from that part of the fitted model that holds intrinsic functions and substrate effects inside the guard ring. All curves in this example apply to the forward active data at 3V, 2.8mA bias

corresponding extracted component values. They stay reasonably constant across all investigated bias points despite large differences in operating modes. In a design process they may safely be included as constant values.

Comparing the measured and fitted magnitude data in Figure 6 with the corresponding responses from the model inside the guard ring shows that substrate losses outside the guard ring mostly influences the magnitude of S_{22}. The most prominent effects from regions outside the guard ring are, however, the phase shifts that are introduced by lead inductances and pad capacitors. Their effects are significant for the experimental identification process and must be known there. This part of the model is, on the other hand, not of same great importance for design, because it contributes nothing to interstage connections inside circuits on the same chip. It is consequently not a severe limitation that most of the model components outside the guard ring are determined with large tolerances compared to the tolerances of components inside the guard ring and in the intrinsic HBT model.

5 Conclusions

The paper has demonstrated how substrate effects in a HBT process may be experimentally identified by a direct one-step model identification process, which owes its accuracy to systematic use of measurement uncertainty data and the sensitivity matrix of the model extraction process. The method identifies important substrate parameters for interstage designs and provide circuit elements, that may be used directly around the vendor supplied design models to get more realistic simulations.

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