Design and Optimisation of Integrated CMOS FIR SC Channel Filter for a GSM Receiver

Adam Dabrowski*, Damian Cetnarowicz*, Rafal Dlugosz*, Pawel Pawlowski*

***Abstract* - In this paper we present the design of a switched-capacitor (SC) FIR channel filter for a basic band GSM receiver. Among problems that have to be discussed and solved are: enlargement of the frequency range of typical SC FIR filters, optimisation of the filter dynamic range, minimization of the chip area, minimization of the power consumption, reduction of influence of parasitic capacitance on the filter performance, etc. One of the most important tasks was the proper design of the operational amplifiers (OA's) used in the filter, as the OA properties strongly influence the overall filter performance and its power consumption.**

1 Introduction

Switched-capacitor (SC) technique is one of the most important and interesting solutions for many classes of analog integrated circuits, especially for those realizing various signal processing tasks at moderate frequency range. Large popularity and spread of SC designs, observed in the last two decades, was possible due to rapid progress in CMOS and GaAs technologies. Especially important is the possibility for integration of perfect switches, precise capacitors (with respect to capacitance ratios), and more than satisfactory operational amplifiers (OA's).

Realization of SC filters was initially based on the replacement of resistors in active-RC structures by equivalent configurations of switches and capacitors. However, the SC technique offers also another very interesting possibility, namely the direct realization of typical discrete-time filter structures: FIR and IIR.

Theoretically, at least four basic FIR SC filter structures exist. Among them are: tapped delay line structure, reversed delay line structure, parallel (multi-C) structure, and rotator structure [1, 2, 5]. In addition to these basic structures, different composite structures can be obtained by combinations of them [1, 5]. All of them have specific advantages and disadvantages. Thus, it is reasonable to search for the optimum structure for every specific application.

*Poznan University of Technology, Institute of Electronics and Telecommunication, ul.Piotrowo 3a, 60-965 Poznan, Poland, tel. (+48 61) 665 2 745, fax (+48 61) 665 2 572 or (+48 61) 665 2 170

E-mail: [dabrow, dcetnar, dlugosz, ppawl]@et.put.poznan.pl

For a GSM channel filter, which is the subject of this paper, the optimum solution occurred to be a cascade of two delay line structures [4].

Typically, SC FIR filters are composed of four basic elements: operational amplifiers (OA's), switches (S's), unit capacitors (UC's), and of coefficient capacitors (CC's). More complicated building blocks, e.g., delay elements, summers, sample-and-holds, etc., can be built with these basic elements [1, 5]. Multiplying of signal samples with constant filter coefficients and then summing these intermediate results can be performed in a single block, namely in the SC summer.

SC filter length is, in general, independent from the maximum signal frequency but it is limited by the maximum chip area and the minimum signal-to-noise ratio (SNR) [5]. Both these parameters depend on the technology. The circuit presented in this paper was realized with 0,8 ìm CMOS technology. However, the results obtained can be quite straightforward extrapolated also to other CMOS technologies [2].

2 Task Specification

A problem considered in this paper consists in elaboration of a method for the design of a low-pass FIR SC filter, according to the standardized specifications shown in Fig. 1, required for a GSM receiver channel filter [2].

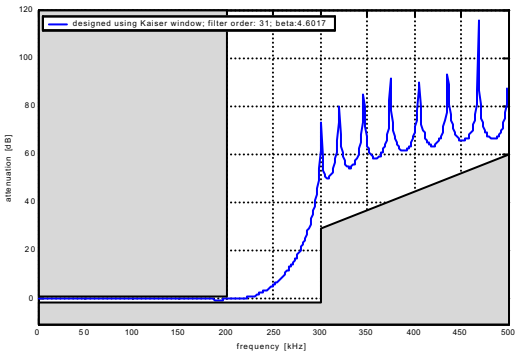

Figure 1. Specifications for a GSM channel filter together with the attenuation of the filter designed using Kaiser window

The attenuation curve plotted also in Fig. 1 is the frequency response of an FIR filter of order 31, designed using Kaiser window with the parameter β=4.6017. As it can be seen in Fig. 1, the required

specifications are safely fulfilled with this filter. Furthermore, its frequency response is nearly optimal because it fulfils the given requirements with a margin, which is almost uniformly distributed along the frequency axis. Instead of looking for the optimum approximation, which is, in fact, quite unreasonable because further discrete optimisation of the filter coefficients will still be necessary, this solution is henceforth assumed as the ideal transfer function for the GSM channel filter, which has to be designed. Its SC realization can be based on the delay line structure presented in Figure 2. Values of the corresponding coefficients are listed in Table 1.

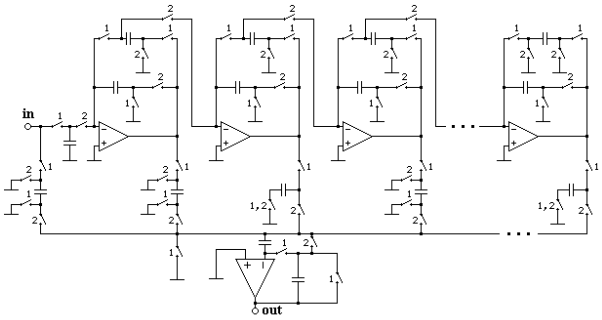

Figure 2. Delay line structure with Gillingham delay elements and the recharge summer [8]

k	$h(k)$	C_k / C	relative error [%]
1 (32)	-0.000759437	-1/1318	0.09
2 (31)	-0.00144393	-2/1318	-5.09
3 (30)	0.00239717	3/1318	5.05
4 (29)	0.00367784	5/1318	-3.15
5 (28)	-0.0053547	-7/1318	0.81
6 (27)	-0.00751148	-10/1318	-1.01
7 (26)	0.0102554	14/1318	-3.58
8 (25)	0.0137331	18/1318	0.55
9 (24)	-0.0181589	-24/1318	-0.28
10 (23)	-0.023872	-31/1318	1.47
11 (22)	0.0314544	41/1318	1.10
12 (21)	0.0420089	55/1318	0.66
13 (20)	-0.0579115	-76/1318	0.43
14 (19)	-0.0853702	-112/1318	0.46
15 (18)	0.147218	194/1318	0.02
16 (17)	0.449207	592/1318	0.01

Table 1: Values of the FIR SC GSM filter coefficients

3 FIR SC Filter Coefficients

An FIR SC filter coefficient $h(k)$ is a ratio of two capacitances: a coefficient capacitance divided by a feedback (or accumulator) capacitance [5].

$$y_{\text{out}}(n) = \sum_{k=1}^{N+1} h(k) u_{\text{in}}(n-k+1) \quad \text{where} \quad h(k) = \frac{C_k}{C}. \quad (1)$$

The latter is the common denominator for all coefficients.

Manufacturing of SC integrated circuits is associated with a limited accuracy of capacitors. Capacitors are realized as multiples of small unit capacitors connected in parallel [4]. Thus, FIR SC filter coefficients are quotients of two integers and should be optimised using discrete optimisation techniques.

The bigger the multiples of unit capacitors in the capacitor realizations the smaller are the coefficient errors. Due to this fact, unit capacitors should be chosen as small as possible. The smallest realizable unit capacitor value is, however, limited by parasitic capacitance. Another technological and economical limit is the maximum acceptable chip area, which, in turn, limits the sum of all capacitor values [2]. Both these limits result in restrictions for the minimum obtainable coefficient error and can cause that a filter structure, which looks interesting at first sight, may occur to be impracticable because of unacceptable coefficient errors. In fact, realisation of a filter with coefficients listed in Table 1 requires 3 688 unit capacitors, which is a quite impractical number. However, this FIR filter can be decomposed, e.g., into two FIR filter sections connected in cascade. To this end, the roots of the transfer function have to be calculated. Each pair of the conjugated roots has to be assigned to one of the sections in order to obtain real coefficients of the final filter realization. A proper decomposition of the considered filter into two sections allows to reduce the total number of unit capacitors to only 336 [4]. The corresponding capacitor values given as multiples of unit capacitors are:

for FIR1: C_k ={2, 7, 9, 10, 17, 15, -5, -17, -5, 11, 7, -5, -4, 2, 1, -1} with C = 54,

and for FIR2: C_k ={1, -1, -1, 2, 4, -2, -9, -1, 11, 11, -4, -19, -19, -14, -9, -7, -2} with C = 47.

This decomposition is, in fact, an optimisation problem [4]. Recently, the authors have developed a genetic algorithm, which makes it possible to optimise decompositions of the considered filter into more that two sections. Each section contains an output OA, which requires a significant chip area, and thus, limits the maximum number of sections. Moreover, a large number of sections degrades the overall filter performance.

One of the most important design tasks was the selection and optimisation of the appropriate OA structure. Since the accumulator capacitors in the summers of both sections are relatively large: 54 and 47

UC's, respectively, the required OA should be quick enough to recharge these capacitors during the required instants. On the other hand the OA should be optimised for power consumption. Taking these conflicting criteria into account, the Miller OA shown in Figure 2 was chosen. Its structure is relatively simple and the dynamic range is high [5]. Other OA structures were examined in previous authors' publications [5].

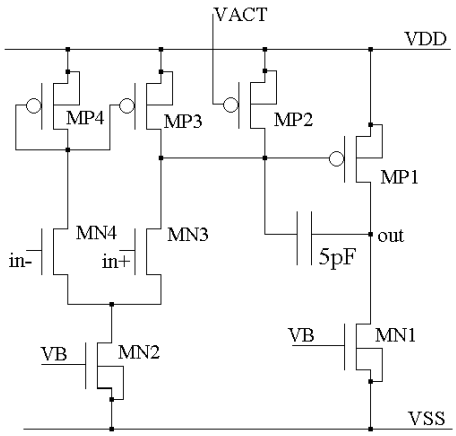

Figure 3. Miller OA used in the designed filter

Performance of the designed filter was evaluated by PSPICE simulations with the control clock frequency of 1 MHz and the sinusoidal input signal with amplitude of 1 V and frequency ranging up to 500 kHz [4]. First, both sections were simulated separately. Then, the whole filter was simulated. Obtained frequency responses are shown in Figure 4.

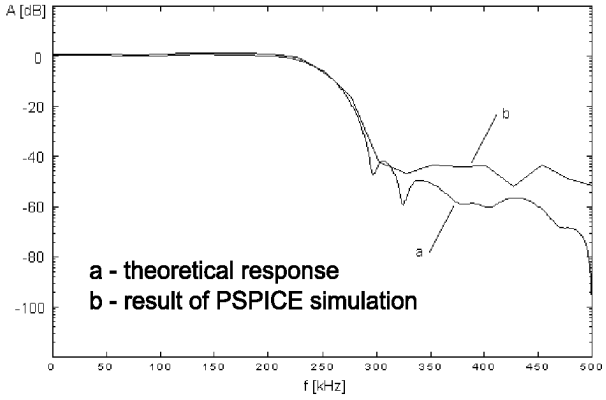

Figure 4. Frequency response of the whole FIR filter (a cascade connection of two sections)

The presented frequency responses show an important problem – a clearly visible discrepancy between the theoretical and the simulated response in the stopband. This difference results from the OA offset voltage, which is present at outputs of both sections.

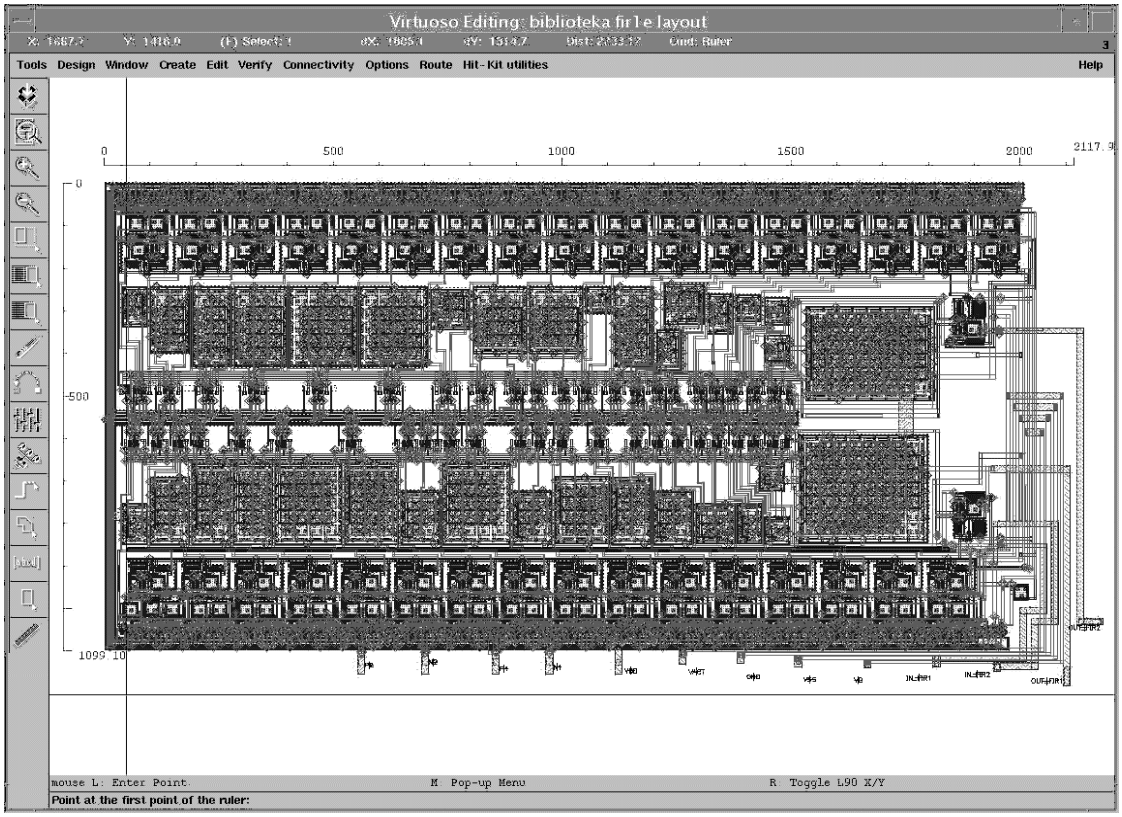

Figure 5. Layout of the designed GSM channel FIR filter of order 31

4 Design of the Layout

Optimisation of the filter coefficients, preliminary PSPICE simulations and other calculations gave us enough information about the appropriate circuit parameters and made the final design of the layout possible. The filter was realized with CMOS 0.8 µm technology using CADENCE software environment. Area of the whole circuit equals about 2.3 mm^2 and exactly agrees with the theory [2]. The filter layout is shown in Figure 5. Placement of particular elements is a result of the multi-criteria optimisation.

SC circuits are mixed integrated circuits, i.e., those with a digital and an analog part. Such a combination may cause that signals from a digital part (in our case the clock signals) influence the effective signal in the analog part. Because of this danger the following design rules have to be taken into consideration:

a) the most sensitive analog elements (OA's and capacitors) have to be placed in the longest possible distances from the clock paths,

b) such sensitive elements as UC's and CC's, as well as digital paths, should be placed in special areas (n-wells, connected to the VDD voltage) separated from the other parts of the circuit by a voltage barrier,

c) CC's must be realized precisely using a special layout – they have to be parallel connections UC's. Such configurations allow to preserve equal area-to-perimeter ratios in capacitors of different values. In consequence, edge parasitic capacitance influences to the same extent all capacitors, and thus, a precise control of capacitor ratios is possible. To assure the full symmetry of all CC's, it is necessary to add some dummy UC's (connected to VDD) around the effective UC's (i.e., those realizing particular CC's). This idea allows additionally to preserve uniformity in the etching of layers.

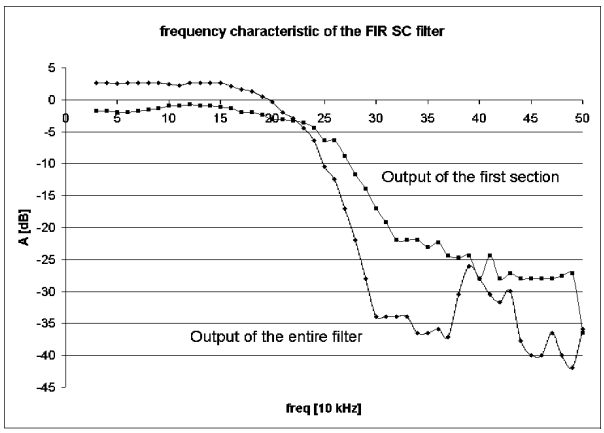

Figure 6. Frequency response of the first section and of the entire filter (two sections)

5 Verification of the Circuit in HSPICE

Next important step was verification of the designed circuit. We checked correctness of the layout as well as its functionality using HSPICE simulator including extraction of the circuit parameters. Especially important is the verification of the circuit attenuation in the stopband since the passband attenuation is usually less sensitive to different imperfections of the circuit elements. The frequency response of the first filter section and of the entire filter is shown in Figure 6.

6 Conclusions

A prototype version of the presented integrated GSM channel FIR SC filter has already been manufactured and is now put to the test. Now the authors are also designing the next, improved version of this filter, as it is still possible to achieve its better performance. In the new design the following changes and modifications are planned:

a) reduction of supply voltage from 5 V to 3 V,

b) of the power consumption from 700 mW to 15 mW,

c) of the OA offset from 5 mV to 0.5 mV,

d) minimisation of the DC offset at the filter output.

Main difficulty of the presented design process and of the design of a new filter version is the necessity of a multi-criteria optimisation, as an improvement of particular parameters interacts with many other parameters mostly in a destructive way. Influence of parasitic capacitance on the accuracy of our filter rather is small and the signal quality is acceptable.

References

[1] A. Dabrowski, R. Dlugosz, "Chip area estimation for SC FIR filter structures in CMOS technology", Chapter 22 in „Mixed Design of Integrated Circuits and Systems", Kluwer, Boston 1998.

[2] R. Dlugosz, A. Dabrowski, "CMOS Realization and Comparison of Basic SC FIR Filter Structures", Proc. of the 5th Int. Conf. Mixed Design of Integrated Circuits and Systems, 1998.

[3] R. Dlugosz, A. Dabrowski, "Design of the multi-phase clocks systems for SC FIR filter structures", Proc. of the 6th Int. Conf. Mixed Design Integrated Circuits and Systems, 1999.

[4] D. Cetnarowicz, A. Dabrowski, "Design principles for FIR SC channel filter for GSM", Proc. of the 7th Int. Conf. Mixed Design of Integr. Circ. Syst., 2000.

[5] A. Dabrowski, "Multirate and multiphase switched-capacitors circuits", Chapman & Hall, London 1996.

This work is supported by the project TB-44-55/2001-DS.