Educating the 21st Century System and Circuit Integrators: SoC Masters at KTH

Hannu Tenhunen, Elena Dubrova
Royal Institute of Technology
Electronic System Design Laboratory
Electrum 229, 16440 Kista/Stockholm, Sweden
{hannu, elena}@ele.kth.se, Ph: 46-8-7521142, Fax: 46-8-7521240

Abstract

Our life and our future is changing due to the rapid growth of the internet, communication technologies, pervasive and ubiquitous computing enabling the availability and invisibility of the complex electronics. The key driving force for this development during this decade will be System-on-Chip technologies and Socware engineering, where the complex functionality is integrated towards ULSI scale single chip solutions. This on-going transition from traditional Application Specific Integrated Circuits (ASIC) has lead to new challenges and paradigm shifts in design methods and automation, system and circuit architectures and circuit techniques in order to harvest the potential benefits of the deep submicron CMOS technologies. To meet the future challenges, we have at Royal Institute of Technology (KTH) initiated the globally first Master Program on System-on-Chip design and Socware engineering of ULSI systems. The program, which is taught completely in English, consists of 40 credit units of courses (9 months study program) and 20 credit units thesis work (6 months) and is primarily targeted to students who have a previous B.Sc. education or at least 120 credit units of course work from technical universities.

Introduction

For more than 20 years integrated electronics has been the main new technological force shaping our everyday life. Today's trend is that of shifting from personal computers to personal communication *and* computing, where the system knowledge and expertise now being capsulated to single-chip solutions incorporating both hardware and software. This revolution is enabled and fueled by deep submicron CMOS technologies, where gigascale integration will be possible in the very near future. In mobile and personal communication, competitiveness of the systems industries will be directly geared to their ability to integrate their own system knowledge more effectively on silicon than their competitors do. The competitiveness and the success of start-up companies to corporation is defined by the silicon chips of very high degree of complexity. If the benefits of these new technologies are to be harvest, a new generation of advanced engineers will have to be educated and deployed to industries

In this paper we shortly outline KTH curriculum approach to System-on-Chip education. In our approach we aim to balance between circuit issues, architecture issues and software issues. The goal is to provide a broad and solid educational background to those key engineers who will shape our future.

Technical challenges

Currently all key system know-how in electronic products is integrated to application specific integrated circuits. ASICs are the key enabling integration technology. Currently the industry and academia is doing a transition from micron/submicron technologies to deep submicron CMOS integration, which are pushed forward by the global application and production technology evolution. Within few years first above 50 M transistor circuits will emerge from Swedish system industries. Thus the 5-10 year research objectives is to look the key design challenges for system on a silicon integration for complexities exceeding 100 M transistor on chip (Ultra large Scale Integrated (ULSI) circuits). As stated earlier, the design and verification cost of such ULSI circuits can be of the same level as the prototyping minifab costs when utilizing current state-of-art techniques. Thus a **non-incremental** methodology and the supporting tools are clearly needed to address the main bottlenecks ion system-on-chip integration approach

The key key technical challenges in adopting full scale SoC approach are

- Significant design efficiency and quality improvements for addressing orders of magnitude larger integration challenges with more strict time schedules and smaller project teams resulting to new work method with supporting design paradigms and tools.
- Functional design for heterogeneous ASICs consisting of multiple DSP and RISC core processors, with embedded software integrated on chip memories resulting to much higher design abstraction and specification levels in the design process requiring new description languages and synthesis techniques.
- Significant improvement of reusability and enhanced reusable macro generation in all phases of the design, resulting to more efficient IP encapsulation.
- Design optimization strategies in environment where the cost of an interconnection is much higher (for area, power consumption, speed and cost) than a cost of logic

cells or transistors resulting to new design paradigms. Most of the current design paradigms and algorithms are based on research in early 1980s, where the situation was completely reversed.

- Chip and system level synchronization strategies for complex circuits consisting of complex building blocks resulting to high system performance and standardized way to integrate complex IP to designs.

- Low power design strategies for deep submicron design for orders of magnitude reduced power consumption resulting to efficient power management techniques as well as emphasis of codesign of system and implementations aspects.

- Mixed signal design strategies for integrating the analog interfaces to system circuits. The key issues is digital noise rejection techniques as well a s robust analog circuit techniques for low voltage operation constraint resulting to high yield and robustness of the mixed signal system chips.

Program overview

Our new study program consists of one year of full-time course studies (equaling 40 credit units; cf. below), and then six months of closely coordinated master's thesis project work (equaling 20 credit units). Thesis work is normally started after the summer trainee period at one of the participating companies. After completing the course requirements and your Master's thesis, you will be awarded the degree of **Master of Science** (”Teknologie magister” in Swedish) from Royal Institute of Technology (KTH).

The study program includes all the key areas of knowledge and skills required to command the *System-on-Chip* technology, in design as well as management. The key skills are in complex circuit design, System-on-Chip architectures, integrated software issues, and reusability and intellectual property management. The key program approach issues and the driving forces shaping the content and form of our program are:

- **Internationalization.** The key organizational form for future system integration tasks is small core competence teams, distributed all over the globe. Hence a work effort of this type requires the ability to co-operate with engineers from other cultures and with differing backgrounds. At KTH we provide a truly international faculty to this very end, with teachers, course assistants and students from all over the world, ready to guide you into this sphere of global effort.

- **Interdisciplinary approach.** In order to fully master the complexity and heterogeneity of the next generation System-on-Chip designs, profound interdisciplinary understanding of the key design issues. This is ensured by our course mix, from deep submicron and digital noise issues to formal techniques and system modeling, with the System-on-Chip concept as the guiding star. This very approach does make our program a unique one and a totally new pedagogical venture in system integration teaching.

- **Competence.** In order to achieve the proper balance between theory and practice, small project assignments and hands-on lab sessions are included in the courses. The learned course knowledge will be transformed to practical competence in your Master's thesis work. This will be performed in close co-operation with our faculty as well as with the participating industry. To this end we have selected a number of world-leading high-tech companies in Europe and the USA, which support our program and are helping us for the knowledge integration and giving you a head start in your new career. In addition, our course content also reflects very closely the advanced stage of research performed here at our department; thus both academic expertise and industrial practice are very much in evidence throughout the program.

The technical content of our program can be classified as follows:

- **Design of heterogeneous System-on-Chip architectures.** This includes custom hardware, digital signal processors (DSP), microprocessors, and embedded software and operating systems, all on the same CMOS circuit (Course group A).

- **Circuit level integration and implementation** of heterogeneous blocks such as digital hardware, software, and analog interfaces while optimizing power consumption, performance, cost and noise (Course group B).

- **Design methodologies and CAD** issues for specification, design and validation (Course group C).

Our curriculum will provide an excellent gateway to an interesting career as either a SoC expert or designer in industry, or as a starting-point for Ph.D. studies. KTH is today one of the major research universities in Europe and therefore provides excellent opportunities for able and well-qualified postgraduate students. As mentioned above, the necessary industrial background infrastructure in Kista already exists. Kista Science Park has earned general recognition as a world top-rate one and many of the leading high-technology companies have set up R & D Centers here. The strong research content in our own activities and strong support from the leading industries provide us both the with technical and economic resources and the scientific content for our program, which is not possible anywhere else.

Student eligibility

Applicants should have completed their university or polytechnic institute level education in mathematics, electronics and computer science as per below. Professional experience acquired in related fields will be considereda merit. Our formal requirements are:

- Awarded B.Sc. or B.Eng. degree from a university or polytechnic institute corresponding to at least 3-year full-time academic study program (= 120 credit units in the Swedish academic system); OR equivalent of 3 year studies at university level towards master's level degree, corresponding to at least 120 credit units of course work.

- In both cases above, the studies must have included minimum six months (= 20 credits) of courses in any combination from the following subjects: Microelectronics, Electronics, Computer science or engineering, or Communication engineering.

- Good oral and written skills in English. Applicants outside the Nordic countries and European Union not having English as their native tongue are required to have completed a TOEFL language test with minimum score 550 (213, computer-based) or an IELTS test with minimum score 5.5.

-

- Students who have completed their Master's degree in other related areas of science or engineering are also encouraged to apply.

More info can be found at http://www.ele.kth.se/SoC/.

Curriculum Summary

The System-on-Chip (SoC) Design program is aimed for senior undergraduate and first-year graduate students in Electrical Engineering and Computer Science. The program emphasizes design methods, architectures and circuit design towards system level integration on silicon. The objectives of the overall curriculum are to give a solid background both for graduate studies and industrial employment.

The 20-credit master's thesis project, normally of 6 months duration, should usually take place in quarters 1 and 2 of the second academic year; the summer preceding this is normally used to prepare and specify the thesis project work. This thesis work is performed in industry and the students receive a typical salary of summer and thesis workers in these companies.

The program consists of 40 credit units of courses and thesis work of 20 credit units. The courses in italic font are compulsory. The capital letters A, B, and C in brackets indicate the course focus area as defined above. Quarters 1-4 indicate first and second half of the autumn and spring semesters, respectively.

Course	**Credit units**	**Quarter**
Embedded Systems (A)	5	1
Digital circuit Design (B)	5	1-2
Hardware Modeling (C)	4	1-2
Digital Hardware Organization (A)	4	2
Design of Fault-tolerant Systems (A)	4	3
SoC Architectures (A)	4	3
Digital Systems Engineering (B)	5	3
System Modeling (C)	5	3
Radio Electronics (B)	5	3
Design Documentation & IPR issues (C)	4	4
Electronic System Packaging (B)	5	4
Anatomy of CAD tools (C)	5	4
Low power analog & mixed-signal ICs (B)	5	4
System ASIC design (A)	5	4
Special topics in SoC (C)	5	4
Master's thesis (2nd year) (A-B-C)	20	1-2

Each student in the program has both a mandatory part from each group of courses as well as elective part, which can reflect student's personal interest. Because Royal Institute of Technology is the largest Nordic technical university, additional courses given in English, are available and, depending on the student's profile, can be incorporated into this program on an individual basis.

Conclusion

In this paper we outlined our approach towards System-on-Chip education at KTH. The key content issues are defined based on future technology evolution, the key strategic application and competence areas for industries in Kista, and the globalization of the industrial R&D and business at all levels. The first round of students have started the curriculum in Septemeber 2000. The program content will be improved based on student and industrial feedback received.