

A compact computational core for image processing

Ari Paasio* Asko Kananen* Mika Laiho* and Kari Halonen*

Abstract — In this paper we suggest a new coefficient structure that can be used in many bipolar or gray-scale image processing tasks. In bipolar image processing, almost all the proposed templates in the CNN literature can be executed. In gray-scale tasks, a very important subclass, namely the weighted ranked order filtering, can be realized. A compact CNN-UM cell structure is proposed that is based on the new coefficient with additional changes to the CNN-UM core.

1 Introduction

The Cellular Nonlinear Network Universal Machine structure proposed in [1] offers a model that can be used in many image processing tasks. The model offers two main features that end up with high processing speed. These features are analogic computing and local intermediate result storage. In order to obtain the promised high computing power the architecture must be realized by hardware, where only limited amount of e.g. silicon area can be used. These limited resources require that the physical size of the processor has to be minimized. Otherwise the second advantage of the approach may be lost because intermediate results can not be stored locally but they have to be written outside the processor grid. A major area where differences can be seen between the proposed CNN cells is the realization of the computational core. By minimizing this core remarkable savings in area can be achieved. In this article we propose a compact coefficient building block which together with other modifications to the cell structure can be used to achieve smaller processors and higher spatial resolution. Some of the modifications include replacing dedicated hardware with template operations while other modifications include restricting the available template operations, e.g. in gray scale, only ranked order filtering is available. A comparison between different approaches in realizing the BW operations is discussed in [2], where the main message is to carefully weight the necessity of each operation, because by replacing some 'difficult' templates by 'easier' ones, huge improvements in almost all the figures of merit may be achieved.

*Helsinki University of Technology, Electronic Circuit Design Laboratory, Department of Electrical and Communications Engineering, P.O.Box 3000, FIN-02015 HUT, Finland. E-mail:apa@ecd1.hut.fi, Tel: +358-9-4515013, Fax: +358-9-4512269.

2 Building blocks

2.1 Coefficient for bipolar image processing

A compact CNN cell was proposed in [3] and analyzed in more detail in [4]. In this scheme a coefficient multiplier consisted of two complementary current sources and of a switch. Two current sources were required because one was required to realize the positive coefficients and the other the negative ones. Because our main goal is to achieve as high a cell density as possible, even at the cost of the speed of evaluation, we have come to the conclusion, that negative coefficients are not actually required in the off-center locations in the A- and B-templates. If such entries would be encountered in the B-template the task can be split into sub-tasks containing only nonnegative template coefficients. This can be achieved by first decomposing the B-template into templates containing only non-negative or nonpositive entries by using the techniques presented e.g. in [5]. The procedure continues by applying the templates with nonnegative coefficients to the original image and by applying the templates with nonpositive coefficients to an inverted image. The effect of inversion of the image to the template is discussed in [6] where it is stated that this inversion changes the polarity of the B-template entries, in this case resulting in nonnegative coefficients. Finally, the results of the sub-tasks are combined as in [5]. If there are off-center nonzero entries in the A-templates it usually means that there is some type of wave propagating in the network asynchronously. Most of the propagations can be realized by non-negative coefficients, one exception being the Connected Component Detector (CCD) [7]. Therefore, in our proposed network the CCD will no longer be available. Fortunately, there are many algorithms still where the CCD is not used. We propose the structure shown in Fig.1 as a new compact coefficient used in the off-center multiplier positions.

2.2 Switch circuit for ranked order extraction

A compact structure for analogue rank extractor is suggested in [8]. It extracts an input current with a programmable rank from a set of input currents. Because the circuit is analyzed in [8] we present here only transistors that are required for one input

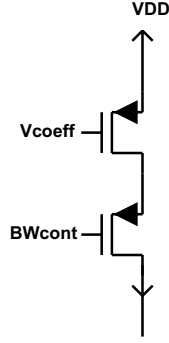


Figure 1: Coefficient circuit for bipolar image processing.

current. These are shown in Fig.2.

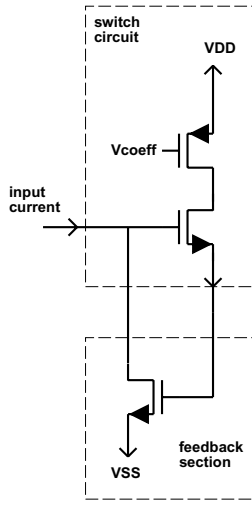


Figure 2: Required transistor for one input current for RO-filtering.

The structure can be thought to consist of two major parts. Namely, there is a switch circuit including a current source and a switch and the second part consists of a single feedback transistor. The total number of transistors for an N input ranked order extractor is $3 * N + 2$ where the two additional transistors are, one for setting a bias to program the desired rank, and another to provide the actual output of the system.

2.3 New coefficient

It can be seen from Figs. 1 and 2 that both of the coefficients have a current source and a switch. Now, if we don't evaluate both types of tasks simultaneously, we can combine the two structures in such a way that only one current source is required. This structure is shown in Fig.3.

Because the current source transistors can not normally be implemented as minimum size due to

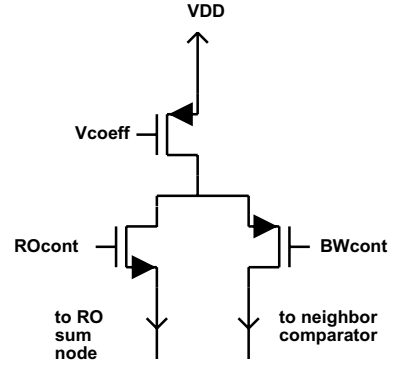


Figure 3: New compact coefficient.

the associated accuracy requirements, and because there are rather many coefficients even in the 1-neighborhood realization, it is beneficial to have as few transistors of this type as possible. A good feature in both, the positive range high gain processing and the ranked order filtering is that the accuracy requirements are not very strict for the coefficients. In [6] it was estimated that the coefficients can vary about 15% from their nominal values while still preserving the input-output mapping. In [8], on the other hand, it is also stated that relatively inaccurate coefficient magnitudes are enough to achieve correct operation, at least if all the weights are equal.

3 Cell structure

Here a new cell structure is proposed. Because in our approach we use different strategies for bipolar image processing and for gray scale rank order processing, the cell contents are described separately for these two classes.

3.1 Bipolar image processing section

The new cell is able to perform bipolar image processing with practically the same level of operations than the cell used in [3]. However, modifications from [3] are proposed in several areas. The one discussed already above is that only positive off-center coefficients are realized. These coefficients are available with the proposed structure in Fig.3. Additionally to the coefficients a current comparator is required and that can be effectively realized by an inverter. Additional features in the cell include transient mask, which conditionally disables the BW transient according to one local memory content. The final feature we include in the cell are the local logic memories where the design strategies follow the ones reported in [3]. Note that the

local logic unit is not included. This block can be omitted due to two facts. The first one is that all the necessary logic operations with two or less inputs are available with normal transient evaluation if the transient mask is included. The second fact is that our BW structure, although slow compared to a dedicated LLU, converges fast enough so that we consider the reduction of the layout area worth making this decision. The basic logic operations required are e.g. *FALSE*, *INV*, *OR* and *XOR* and the remaining operations can be obtained from these by either inverting one or both of the inputs or the output. Now, apart from *XOR*, these operations are available even without the transient mask, and the *XOR* can be obtained with the help of the mask.

3.2 Gray scale processing section

In the cell we need to realize gray scale image memories. These are most conveniently realized by switched current memories. In using the RO-circuit we must provide the cell input current to neighboring cells, and this is easily achieved by multi output current mirror. Additionally, in the cell, there is a group of feedback transistors required by the RO-circuit. One feedback transistor is assigned for one input current from the neighborhood. Finally, of course the switch circuits need to be implemented. Because the current source transistor can be shared with the BW block, only switch transistors, one per input current, add to the circuitry. Additional transistors for the RO-processing, one per cell, are a bias transistor and an output transistor having its output connected to the cell current memories.

4 Conclusions

In this paper a compact structure has been suggested to perform a variety of image processing tasks. A very compact coefficient structure was presented that allows small cell size, and therefore, makes it possible to realize processor arrays with high spatial resolution. The proposed structure can not be used to execute every possible CNN template, quite the opposite, the functionality has been limited to the operations most commonly used in the CNN-UM algorithms.

References

- [1] T. Roska, L. O. Chua, "The CNN Universal Machine: An Analogic Array Computer", *IEEE Transactions on Circuits and Systems-II*, vol. 40, 1993, pp.163–146.
- [2] A. Paasio, A. Kananen, L. Koskinen, K. Halonen, "Different possibilities for realizing the

bipolar image processing tasks in CNN field", in *Proceedings of ECCTD'01*.

- [3] A. Paasio, A. Kananen, K. Halonen, V. Porra, "A QCIF Resolution Binary I/O CNN-UM Chip", *Journal of VLSI Signal Processing Systems*, vol. 23, 1999, pp.281–290.
- [4] A. Paasio, K. Halonen, "A New Cell Output Nonlinearity for Dense Cellular Nonlinear Network Integration", *IEEE Transactions on Circuits and Systems-I*, vol.48, 2001, pp.272–280.
- [5] P. Foldesy, L. Kek, A. Zarandy, T. Roska, G. Bartfai, "Fault-Tolerant Design of Analogic CNN Templates and Algorithms - Part I: The Binary Output Case", *IEEE Transactions on Circuits and Systems-I*, vol. 46, 1999, pp.312–322.
- [6] A. Paasio, A. Dawidziuk, "CNN Template Robustness with Different Output Nonlinearities", *International Journal of Circuit Theory and Applications*, vol. 27, 1999, pp.87–102.
- [7] T. Matsumoto, L. O. Chua, H. Suzuki, "CNN Cloning Template: Connected Component Detector", *IEEE Transactions on Circuits and Systems*, vol. 37, 1990, pp.633–635.
- [8] A. Paasio, K. Halonen, "An analogue circuit for weighted rank order filtering", in *Proceedings of ECCTD'01*.