Integrated RF Front-End for WCDMA and GSM 900

Jussi Ryynänen[1], Kalle Kivekäs[1], Jari Heikkinen[2], Jarkko Jussila[1], Aarno Pärssinen[3], Kari Halonen[1]

Abstract – **This paper presents an RF front-end that has been designed both with Si BiCMOS and with SiGe BiCMOS. As the front-end is in principle similar in both designs, it gives a good platform for the comparison between the different processing technologies. The main design target has been to meet the WCDMA and GSM system specifications with low power consumption.**

1 Introduction

The first third generation WCDMA networks are designed to be launched during this year. The performance of the terminal designed for WCDMA should be compatible with terminals designed for existing systems, although the WCDMA receiver uses higher frequency range and larger channel spacing than present systems [1]. Furthermore, the future terminal should be able to connect to different networks depending on the network coverage and the services requested by the consumer. To our knowledge, the recently published RF receivers for multi-band terminals have been implemented by using several parallel front-ends [2,3]. Although a high integration level can be reached, the straightforward parallel architecture wastes a lot of chip area. The front-ends presented in this paper use the same signal path in both modes, except of the first stage in the LNA [4].

The supply voltage of the digital circuitry is decreasing with the evolution of CMOS technologies. Analog and RF circuits are following the development because of reduced breakdown voltages, lower power consumption and possibility to a single supply [5]. The first RF front-end has been designed using a 25 GHz f_T BiCMOS process and the other using a 45 GHz f_T SiGe BiCMOS process. The minimum MOS gate length is 0.35 μm in both processes.

[1] Helsinki University of Technology, Electronic Circuit Design Laboratory, P.O. Box 3000, FIN-02015 HUT, Finland. E-mail:jry@ecdl.hut.fi, Tel: +358-9-4512988, Fax: +358-9-4512269.
[2]Nokia Networks, Espoo, Finland
[3]Nokia Research Center, Helsinki, Finland

2 Architecture and Circuit Design

2.1 Architecture

The block diagram of the RF front-end is shown in Figure 1. The front-end uses direct conversion architecture. It is suitable for multi-system design because only one LO is required and no bulky and expensive off-chip channel or image filters are required. In the designed front-end there are two separate single-ended inputs, one input for each system due to the required separate pre-selection filters. The single-ended-to-differential conversion is performed before the downconversion mixers, thus enabling a double-balanced topology. Furthermore the signal path between the LNA and mixer is DC decoupled. Hence, the low-frequency distortion generated by the second-order nonlinearities in the LNA is filtered out. Otherwise, it would partly leak through the mixer to baseband. A fully differential signal path could also be used throughout the front-end [6]. However, it would double the power consumption of the LNA, increase chip area, and require a balun in front of the LNA, which increases the loss before the front-end. The front-end has tunable gain to relax the baseband gain control requirements and to provide better linearity at higher signal levels. In the silicon front-end, the variable gain is carried out in both the LNA and mixer. In the SiGe front-end there is no longer adjustable gain in the mixer. The reception in the WCDMA is continuous and the digitally controlled gain adjustment in the mixer could cause large slowly decaying transients. Only very small changes in the offset at the mixer output are allowed.

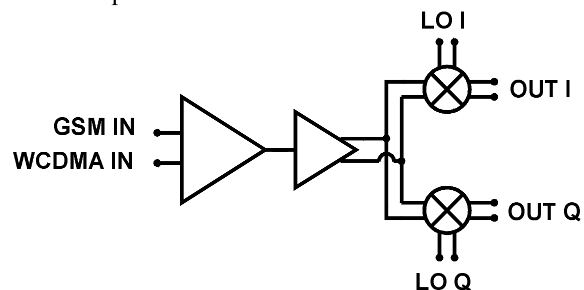

Figure 1. Block diagram of RF front-end.

2. 2 LNA

The schematic of the LNA is illustrated in Figure 2. The use of common emitter cascode topology in all modes ensures sufficient NF and gain with good

reverse isolation. In addition the cascode transistors are used to select the operation mode. Depending on the selected mode either input transistor Q1 or Q2 is turned on while the other is off. In WCDMA, the inductors Lb1 and Le1 are used for input matching while Lb2 and Le2 are adopted in GSM. In GSM mode, there is also a capacitor connected between the base and emitter of transistor Q2. This reduces the value of the base inductor Lb2. In the SiGe design also a small capacitor was added between base and emitter of Q1. All matching elements are placed on-chip excluding the base inductors, which are realized using bond wires. The LNA gain is controlled with switches in discrete steps by changing the load impedance of the LNA. At the maximum gain, the load of the LNA is a damped resonator tuned at 950 MHz for GSM and at 2.1 GHz for WCDMA. The parallel resistor in the resonator increases the operation band with negligible deterioration in the noise performance. The first gain step is realized by adding another resistor in parallel to the load resonator for additional damping of the resonator Q value. A larger gain step is performed by using the resonator of the other system as a load. For example, at maximum gain the WCDMA utilizes the left resonator in Figure 2, when Q3 is on and Q4 turned off. At minimum gain the current flows through Q4 and Q1, and the output is taken from port 2. The LNA gain, and mode control are implemented using MOS switches, which steer the current mirror biasing of Q1-Q4. Single-ended LNA is more sensitive to supply-noise. An on-chip decoupling capacitor with a small series resistor provides efficient damping without susceptibility to unwanted resonances. The decoupling structure is connected between the common supply and ground of the front-end.

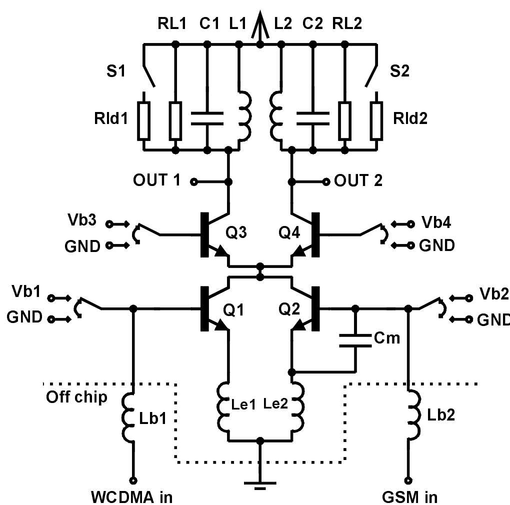

Figure 2. Dual-mode LNA.

2.3 Single-Ended-to-Differential Converter

The single-ended-to-differential converter is shown in Figure 3. The converter enables the use of double-balanced mixers, isolates LNA load resonators and improves reverse isolation. The conversion is performed either with the transistor Q5 or Q6 depending on the chosen LNA resonator. The passive baluns are not feasible because of the wide operation range of 900 MHz – 2.2 GHz, and linearity requirements rule out the differential pair option. To improve the balance, a dummy transistor Q7 is added to compensate the effect of the collector capacitances of Q5 and Q6 [7]. In order to achieve a good balance, the load impedances seen from the emitter and collector of Q5 and Q6 must match. Therefore, the supply inductances must also be equal. This was solved by using separate supply pads in the converter to insure the equal length, and number of bond wires. The simulations for SiGe front-end show that the gain and phase imbalances are less than 0.2 dB and 1 degree, respectively.

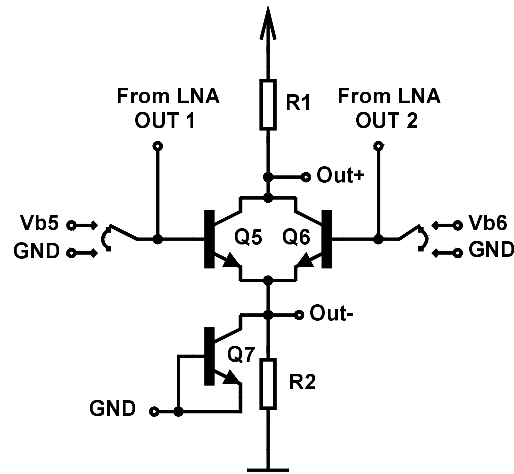

Figure 3. Single-ended-to-differential converter.

2.4 Mixer

The double-balanced mixers utilize NMOS input devices with bipolar switching core in Figure 4 [1]. The mixers are current boosted to relax the low supply voltage conditions [8]. The additional dc current is fed through the current sources that are long-channel, resistor degenerated PMOS devices (Mp1 and Mp2). By current boosting, a lower mixer noise figure is achieved without deteriorating the linearity. Furthermore, boosting enables increased mixer conversion gain by allowing the higher impedance loading at the mixer output without changing the optimum quiescent point of active devices. Decreasing the gm by source degeneration minimizes the noise

generated in the current sources. However, at some point the noise due to the enlarged degeneration resistors starts to dominate the noise performance of the current sources. Thus a better method to reduce the current source noise is by minimizing the gm using only very small long-channel PMOS devices without degeneration. Bipolar switching transistors Q1-Q4 are used instead of respective NMOS transistors. The benefits using bipolars are lower flicker noise, higher f_T, and that they typically require smaller LO signal swing to exhibit proper on-off switching. The higher f_T, guarantees that the errors in device conduction times due to the differences between the on-off transition times are smaller. It is required in order to achieve a symmetrical on-off switching, and thus reduce the second-order distortion caused by the non-ideal LO signal duty-cycle. The NMOS transistors Mn1 and Mn2 provide better linearity than bipolars in the input stage. Nevertheless, the emitter degenerated bipolars could provide the same odd-order linearity. On the other hand, the emitter degeneration is made of either quite small resistors or inductors. The matching of quite small resistors, especially at RF, is usually only adequate. Hence, the even-order linearity performance is easily deteriorated. The disadvantage using inductors is due to their large physical size. To increase the invulnerability against the even-order distortion, the mixer layout must be as symmetric as possible. Si mixer provides three 4 dB gain control steps with maximum voltage gain of 14 dB. Adjustable gain was not implemented in SiGe mixer. The mixer has an RC low-pass pole at the output to relax the out-of-band linearity requirements of the following baseband stages. Due to the two separate frequency bands the quadrature LO signal generation cannot be implemented with a single RC-CR filter. Hence, an external LO signal generation have been utilized. Therefore, the front-end is designed to be integrated with an on-chip PLL, which can provide the quadrature LO signals and a properly determined LO-to-mixer interface in both bands.

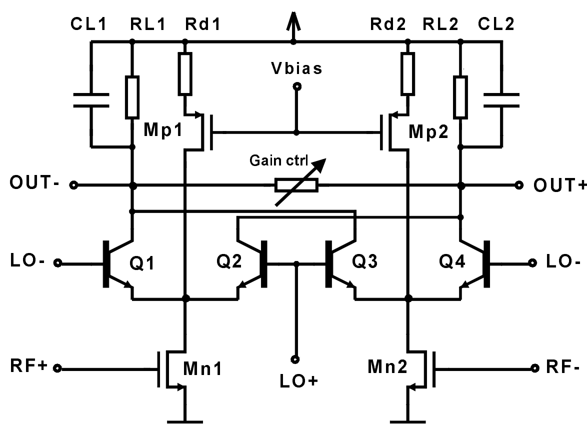

Figure 4. Downconversion mixer.

3 Experimental Results

The collected results from the both designs are shown in Table 1. The results labeled as Si are measured from the processed silicon front-end. The simulation results from the second front-end are labeled as SiGe. It must be noted that the minimum gain of the SiGe front-end is higher because of the gain control at the mixer was removed. It can be seen that the NF in the Si front-end operating in the WCDMA is significantly higher than in the GSM. The high NF resulted from the inadequate simulation models in the first run. The difference between the simulation and measurement results was verified later by simulations with new models. The design was corrected in the SiGe front-end, which shows now similar noise performance in both modes. In addition, the overall noise characteristics were sligthly improved in both modes due to SiGe process [9]. The RF responses of the both designs are shown in Figure 5. The maximum gains in both modes are now in the same level using SiGe transistors. The input matching, shown in Figure 6, is independent of the gain mode. The reported S11 values cover both MS and BS reception bands. Some attention was also paid on improving the linearity. In the SiGe front-end this was achieved with the expense of slightly higher power consumption. In the case of direct conversion receivers the IIP2 is very important parameter. The reported IIP2 values for the Si front-end were higher than +35 dBm. The value of IIP2 is very sensitive to different mismatches and therefore no simulation results for the SiGe front-end is given. However, it is expected to be at the same range.

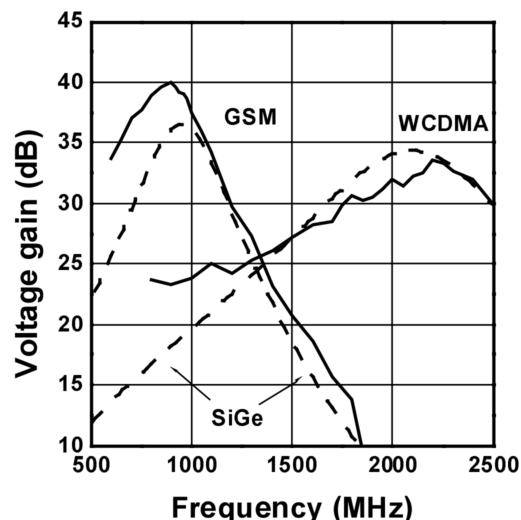

Figure 5. Maximum gain responses on both bands.

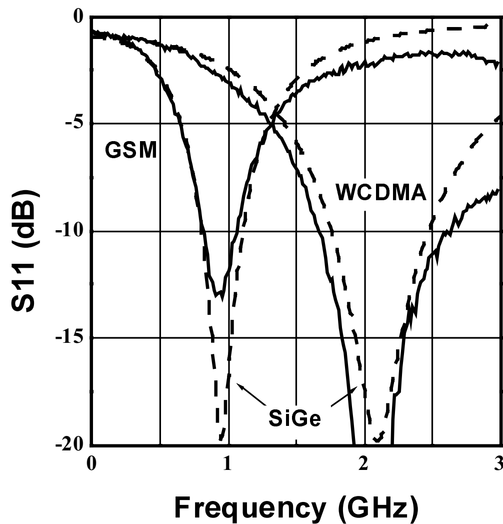

Figure 6. Input matching on both bands.

TABLE I. PERFORMANCE IN WCDMA AND GSM MODES.

		WCDMA		GSM	
		Si	SiGe*	Si	SiGe*
NF@max gain	[dB]	4.3	2.4	2.3	2.0
NF@min gain	[dB]	15.9	8.3	12.3	7.9
Voltage gain max	[dB]	33	34.4	39.5	36.6
Voltage gain min	[dB]	6.5	22.5	12	24.1
IIP3 @max gain	[dBm]	-14.5	-11.9	-19	-11.8
IIP3 @min gain	[dBm]	-7	-6.7	-7.5	-10.6
ICP_{-1dB}@max gain	[dBm]	-25	-24.6	-29	-25.4
IIP2 @max gain	[dBm]	+34	NA	+35	NA
S11	[dB]	<-18	<-14	<-12	<-16
P(LO)	[dBm]	-10	-8	-10	-8
Power dissipation	[mW]	22.5	26.3	21.5	24.4
Supply voltage	[V]	1.8	1.8	1.8	1.8

*simulation results

4 Conclusion

A dual-band, dual-mode RF front-end for WCDMA and GSM wireless receivers is presented in this paper. Except of LNA input transistors and matching inductors, all on-chip devices can be utilized in both modes. The advances due to SiGe BiCMOS process are noticeable but not significant at these designs. Although the higher f_T relaxes the design of the circuits at 2 GHz band. One advance is in the bipolar transistor noise performance due to the higher current gain. This helps especially the design of receivers in which very low noise figure is required [10]. On-chip active balun allows single-ended RF input and double-balanced mixers at a large frequency range required in multi-band systems. The front-end meets the essential parameters of the GSM and WCDMA receivers.

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