A Versatile 1.5 V Current-Mode CMOS Analog Multiplier/Divider Circuit

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Abstract – **A novel current-mode multiplier/divider circuit, able to operate at supply voltages down to 1.5V and suitable for standard CMOS processes is presented. The circuit is based on the Voltage-Translinear principle, and can be employed in a wide range of analog applications. Measurement results for an IC prototype fabricated in a 2μ CMOS process verify the proposed approach.**

1 Introduction

Analog multipliers are one of the most frequently employed building blocks in analog signal processing applications. They are not only present in traditional applications such as modulators, mixers, automatic gain control, square rooting, PLLs, etc; also more recent fields such as artificial neural networks and analog fuzzy processors take advantage of this flexible building block. The design of analog multipliers constitutes an area of active research, and many solutions are now available to the designer. However, most of them are designed for voltage-mode applications (e.g., [1-3]). Current-mode multipliers, specially very low voltage, CMOS ones, are not so many. Nevertheless, they are the natural choice in conventional mixed-mode designs due to the scaling down of supply voltages that prevents an excessive power dissipation per unit area and gate oxide breakdown.

A recent approach of particular interest in the area of analog current-mode multipliers is the use of the Voltage-Translinear (VTL) principle [4], an extension of the classical Translinear principle [5] that is based on the approximately linear relationship existing between the gate-source voltage of a MOS transistor in strong inversion and saturation and its transconductance. The resulting topologies feature insensitivity to variations in temperature and processing, and wide dynamic ranges can be obtained since internal voltages are compressed in these circuits, thus being less constrained by supply voltage limitations. In [6], a multiplier/divider following this approach was proposed. It employs three second-order Voltage-Translinear loops in a stacked configuration. Even recognizing the pioneering value of this work, the resulting topology was not well suited for low-voltage applications, since the minimum supply voltage was given by $2V_{GS}+V_{DSSAT}$. The supply voltage employed in the simulations reported was 5V. Moreover, the stacked topology could suffer from the body effect if technology precludes the connection of the MOS bulk terminals to their source terminals. The circuit also exhibited a complexity that seemed unnecessary.

A second proposal in this way was presented by the authors in [7]. In this case, a different approach to the multiplier/divider design leads to a circuit where only two Voltage-Translinear loops are required, therefore resulting in a much simpler architecture requiring less silicon area and having a reduced power consumption. Voltage-Translinear loops follow an up-down topology in this case, so that the body effect becomes negligible. Measurement results of this circuit confirm the good properties in terms of accuracy and dynamic range of this approach. Nevertheless, the low-voltage capability of this technique was not fully exploited in this work, thus employing a supply voltage of 3.3V. In this paper, a novel multiplier/divider following the idea presented in [7] is proposed, where a novel biasing technique applied to the Voltage-Translinear loops leads to a minimum supply voltage of just $V_{GS}+2V_{DSSAT}$. Therefore, supply voltages of 1.5V, often required in battery-powered equipment, become feasible.

2 Principle of Operation

The procedure followed for obtaining the current multiplier/divider is to generate a current which is the geometric-mean of two currents I_x and I_y, i.e.,

$$I_{gm} = \sqrt{I_x I_y} \tag{1}$$

and to inject it into a squarer/divider circuit having the following input-output characteristic:

$$I_{out} = \frac{I_{in}^{\ 2}}{I_w} \tag{2}$$

Then, the squarer/divider output will be given by the expression

$$I_{out} = \frac{\left(\sqrt{I_x I_y}\right)^2}{I_w} = \frac{I_x I_y}{I_w} \tag{3}$$

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Hence, according to (3), a current-mode multiplier/divider could be obtained by this simple method. This idea is shown in Figure 1.

Since equations (1) and (2) are inverse one each other, it can be expected that both could be implemented in practice using the same basic topology, by just interchanging input by output and properly adapting the input and output impedances. A general approach to the design of the required blocks using Voltage-Translinear techniques will be provided in the next section.

3 Circuit Design

In order to implement the geometric-mean and squarer/divider cells, Voltage-Translinear techniques will be followed. Consider the second-order Voltage-Translinear loops shown in Fig. 2 in up-down (Fig.2a) and stacked (Fig. 2b) topologies. Applying the Kirchhoff voltage law to the loops, the gate-source voltages of the MOS transistors M_1 to M_4 become related in both cases by

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \tag{4}$$

Assuming MOS transistors operating in strong inversion and saturation, the drain currents and gate-source voltages can be related by the approximate formula:

$$I_d = \frac{k_n}{2}\left(\frac{W}{L}\right)\left(V_{GS} - V_{TH}\right)^2 \tag{5}$$

where k_n is the transconductance factor, W/L is the aspect ratio and V_{TH} is the threshold voltage. Using (4)-(5) and assuming identical MOS transistors we get

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4} \tag{6}$$

Now, let's assume that the drain currents in the Voltage-Translinear loops are chosen to be related by:

$$I_3 = I_4 = \frac{I_1 + I_2 + 2I_5}{4} \tag{7}$$

for a certain current I_5. Then, if we use (7) in (6) we obtain, after squaring both sides in (6) and rearranging the resulting expression, that currents I_1, I_2 and I_5 become related by

$$I_5 = \sqrt{I_1 I_2} \quad i.e., \quad I_2 = \frac{I_5^{\,2}}{I_1} \tag{8}$$

Therefore, a geometric-mean circuit is obtained if I_1 and I_2 are copies of the input currents and the output current is a copy of I_5. Alternatively, a squarer/divider is obtained if the output is a copy of I_2 and I_5 and I_1 are copies of the inputs.

Either the stacked or the up-down topology could serve as a geometric-mean or squarer/divider circuit. Nevertheless, as advanced in the introduction, the stacking of transistors in the topology of Fig. 2b precludes the use of low-voltage supplies, since the minimum supply voltage is $2V_{GS}+V_{DSSAT}$. Moreover, the body effect in the stacked VTL loop of NMOS transistors could be avoided only in a p-well technology, by placing loop transistors M_2 and M_3 in separate wells and connecting their source and bulk terminals. Otherwise, this second-order effect seriously affects the loop behavior. Therefore, only up-down VTL topologies will be considered in subsequent paragraphs.

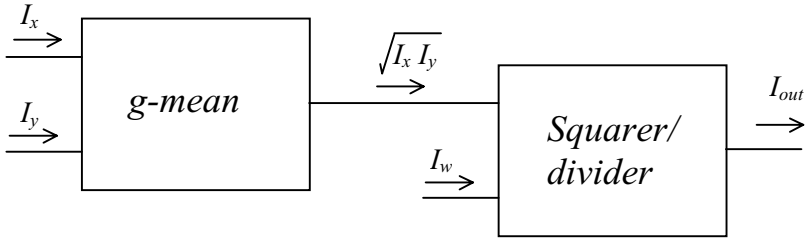

Figure 1. Simplified diagram of the multiplier/divider

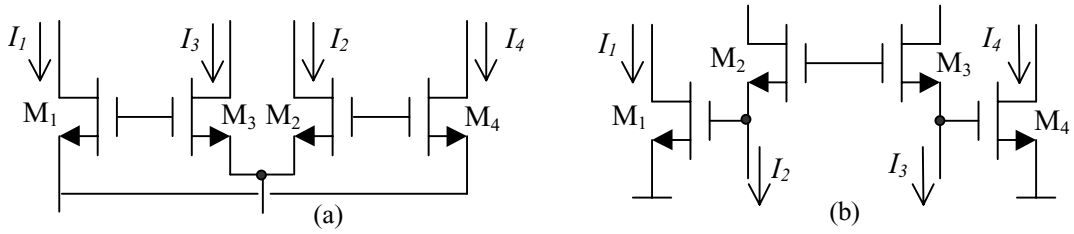

Figure 2. a) Up-down VTL loop b) Stacked VTL loop

The up-down topology is able to operate at supply voltages of $V_{GS}+2V_{DSSAT}$ if properly biased, and the body effect is practically cancelled out.

A detailed schematic of the proposed multiplier/divider is shown in Fig. 3. The geometric-mean circuit is shown on the left. M_{1A}-M_{4A} form the up-down Voltage-Translinear loop, whereas the remaining transistors inject the proper loop currents according to expression (7). The tail currents of the loop correspond to the drain currents of two outputs of a current mirror, thus avoiding the use of a diode-connected transistor at the bottom, as employed in [7]. This strategy allows one to employ a supply voltage as low as one V_{GS} plus $2V_{DS}$ of a saturated MOSFET. The correct operation of the current mirror employed at the bottom for sinking these tail currents is enforced by an external bias voltage, V_B.

The output current of the geometric-mean cell is reversed by a current mirror and then introduced into the squarer/divider circuit (shown in Fig. 3 on the right), as described in Section 1. Note that the topology of the squarer/divider circuit is quite similar to that of the geometric-mean circuit, being the strategy for injecting currents essentially the same. M_{1B}-M_{4B} form the up-down Voltage-Translinear loop. The aspect ratios of the MOS transistors are shown in Table 1.

4 Simulation and Measurement Results

The circuit of Fig. 3 was implemented in a double-poly, double-metal, 2μm CMOS n-well process of Alcatel/Mietec. Supply voltage was 1.5 V, and the bias voltage V_B shown in Fig. 3 was set to 1.2 V. Fig. 4 shows a microphotograph of the resulting circuit, being the total area occupied 0.2 mm^2.

The DC transfer characteristics of the multiplier/divider are shown in Fig. 5. Input currents were I_w=10 μA, I_y values ranging from 10 μA (lower line) to 25 μA (upper line) in 5 μA steps and I_x swept from 0 to 15 μA. Note that the resulting nonlinearity depends on the bias current setting selected for each case.

A four-quadrant multiplier can be readily obtained from the above multiplier/divider circuit by using a pair of them in a balanced structure. This configuration had to be simulated since only one multiplier was integrated; transistor models provided by the foundry for the fabrication run of the fabricated IC were employed.

Fig. 6 shows the operation of the resulting four-quadrant multiplier as an amplitude modulator. I_x had a 5 μA DC component, whereas its AC component was $2.5\ sin(2\pi ft)$ μA, with f = 10 kHz; I_y was a 1kHz triangular modulating waveform, and I_w = 5 μA.

The balanced arrangement also helps even-order harmonic distortion; simulations show that the second-order harmonic is improved in about 15 dB with regard to the non-balanced topology at 10 kHz and for identical output levels.

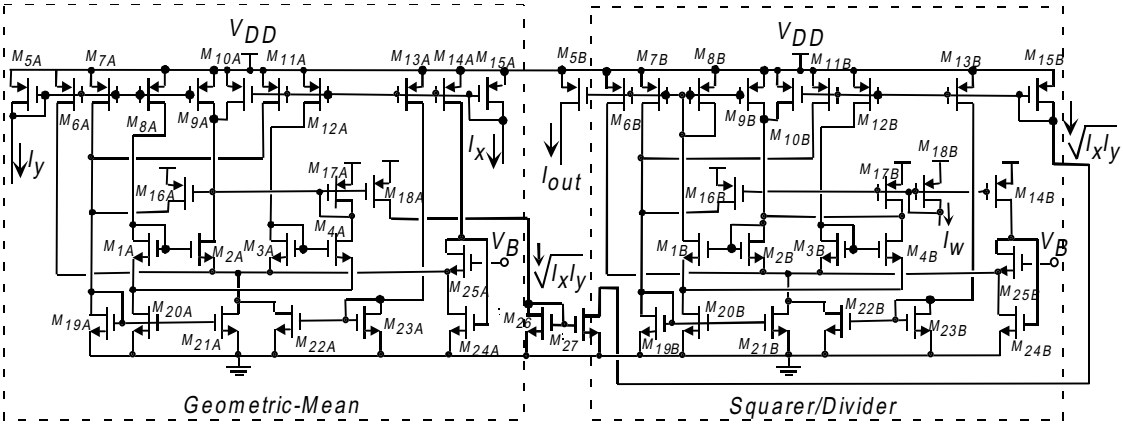

Figure 3. Multiplier/Divider schematic

	$M_{1A\text{-}4A}$	$M_{5A\text{-}6A}$	M_{7A}	M_{8A}	$M_{9A\text{-}11A}$	$M_{12A\text{-}18A}$	M_{19A}	$M_{20A\text{-}23A}$	M_{24A}	M_{25A}	$M_{26\text{-}27}$
L(μm)	4.8	3.2	3.2	3.2	3.2	3.2	3.2	3.2	4	2.4	3.2
W(μm)	80	160	400	160	80	160	224	112	12.8	48	32

Table 1. Transistor aspect ratios in Fig. 3 (transistors $M_{iB} = M_{iA}$ for all i)

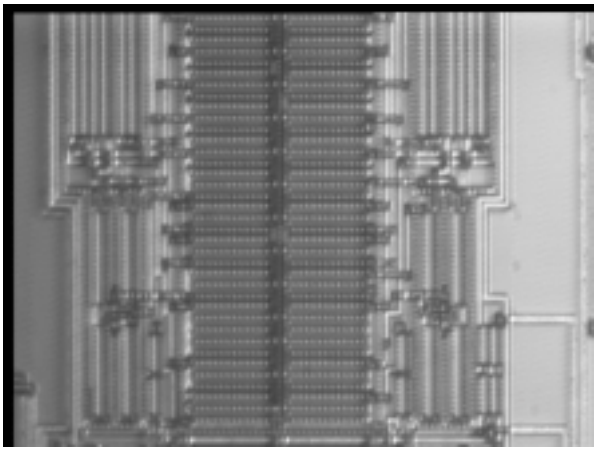

Figure 4. Microphotograph of the multiplier/divider

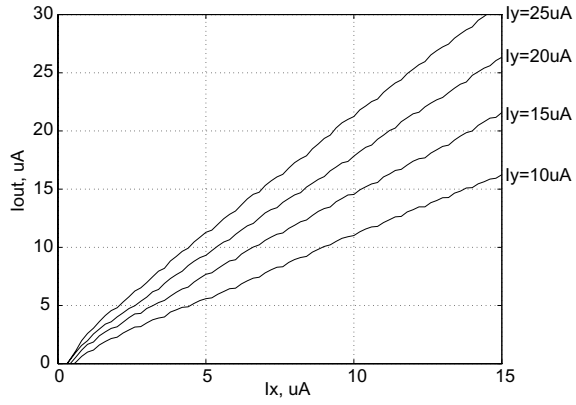

Figure 5. DC characteristics of the multiplier/divider

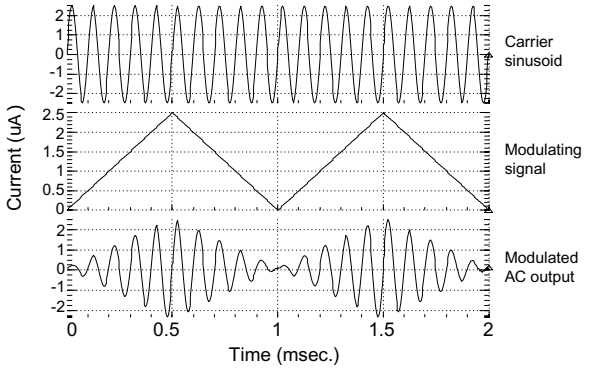

Figure 6. Balanced multiplier as an amplitude modulator.

5 Conclusions

The voltage-translinear principle has been applied to the design of a very low-voltage current-mode CMOS multiplier/divider circuit, well suited for standard CMOS processes and able to operate in battery-powered environments. Measurement results for an IC prototype demonstrate its correct operation.

Acknowledgment

This wok has been supported by the Spanish Dirección General de Investigación under grant TIC2000-0615-C02-02.

References

[1] S.Liu, C. Chang, "CMOS Analog Divider and Four-Quadrant Multiplier Using Pool Circuits", *IEEE J. Solid-State Circ.,* vol. 30, no. 9, 1995, pp. 1025-1029.

[2] S. Liu, Y. Hwang, "CMOS Four-Quadrant Multiplier Using Bias Feedback Techniques", *IEEE J. Solid-State Circ.,* vol. 29, no. 6, Jun. 1994, pp. 750-752.

[3] J. Ramirez-Angulo, A. Diaz-Sanchez, "Low-Voltage Programmable Filter Using Voltage Followers and Analog Multipliers", in *Proc. ISCAS,* pp.1408-1411, Chicago; Illinois, 1993

[4] E. Seevinck, R.J. Wiegerink, "Generalized translinear circuit principle", *IEEE J. Solid-State Circ.,* vol. 26, no. 8, Aug. 1991, pp. 1098-1102.

[5] B. Gilbert, "Translinear Circuits: A Proposed Classification", *Electron. Lett*., vol. 11, 1975, pp. 14-16.

[6] W. Gai, H. Chen and E. Seevinck, "Quadratic-translinear CMOS multiplier-divider circuit". *Electron. Lett.,* vol. 33, no. 10, May 1997, pp. 860-861.

[7] A.J. Lopez-Martin, A. Carlosena, "Design of MOS-Translinear Multiplier/Dividers in Analog VLSI", *VLSI Design Journal*, vol. 11, no. 4, pp. 321-329, 2000.