Edge-Triggered Flip-Flop Circuit Based on Resonant-Tunneling Diodes and MOSFETs

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Abstract

This paper presents a novel circuit that combines resonant tunneling diodes with MOSFETs to create a very compact and high-speed flip-flop implementation. This edge-triggered flip-flop circuit offers smaller circuit size and area as compared to a true single-phase CMOS flip-flop. The circuit can operate at lower supply voltage as compared to a conventional CMOS flip-flop and provides better noise immunity through isolation of dynamic storage nodes.

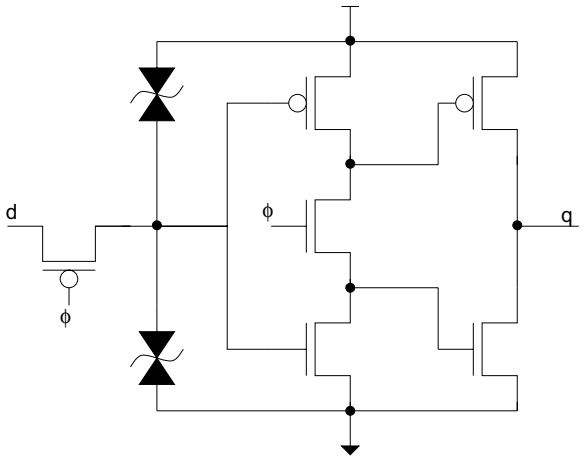
1 Introduction

RTD-based circuits have unique self-latching properties [1]. However, until the present time there have been no true single phase clocked (TSPC) edge-triggered flip-flop circuit implementations using RTDs. It is well known that edge-triggering is commonly required in VLSI circuits for accurately sampling an input at a clock edge so that further circuits are immune to any variations in the input signal that might otherwise lead to false evaluation. Here we present the design of a family of edge-triggered flip-flops using RTDs and MOSFETs [2].

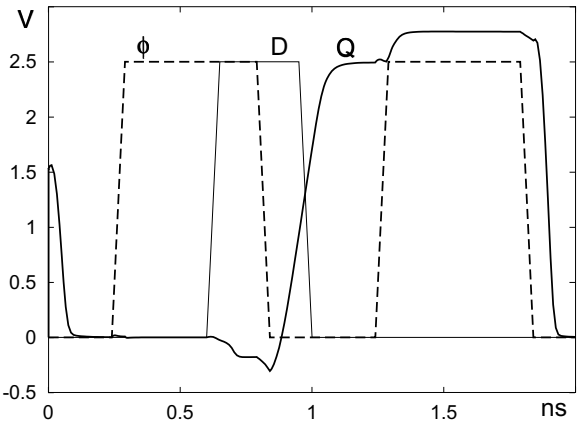
2 Edge-Triggered True Single Phase QMOS Flip-Flop

Fig. 1(a) is a schematic diagram of a QMOS negative edge-triggered D flip flop circuit. It uses an RTD latch followed by a CMOS TSPC output stage [3].

When the clock signal is high, the access transistor to the RTD-pair latch is turned on and the latch node tracks the input voltage. At this time the clock transistor in the second stage is turned off and hence the Q output is unaffected by any changes in the D input. When the clock signal goes low, the access transistor to the RTD latch is turned off. The RTD-pair latches the value of the D input at its common terminal. The clocked inverter is turned on, and following the inversion of the output stage, the Q node reflects the value of the D input at the time of the clock edge. Simulation traces of the QMOS TSPC D flip-flop are shown in Fig. 1(b). Since the QMOS TSPC flip-flop contains three MOS transistors



(a)



(b)

Figure 1: Negative edge-triggered QMOS TSPC D flip flop (a) circuit diagram, (b) simulation traces.

* This research has been supported in part by grants from DARPA and ARO MURI.

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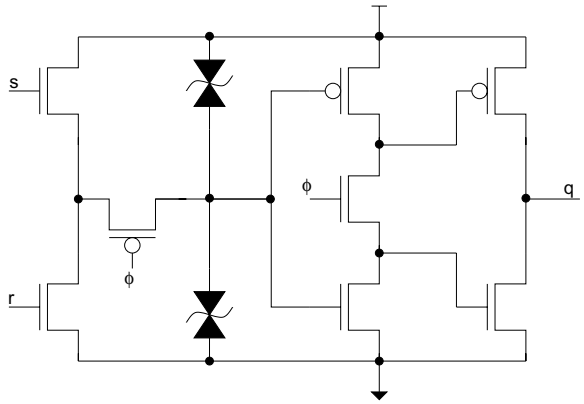
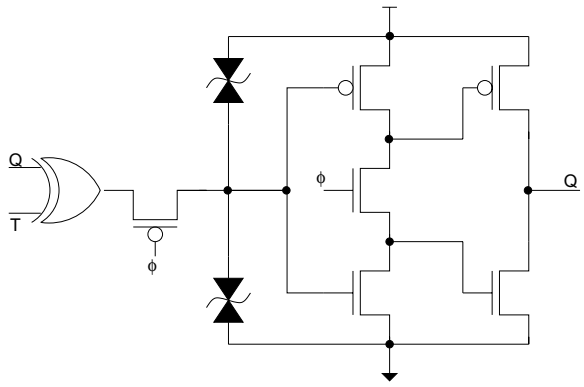
in series in the output stage, the threshold voltage drops of the PMOS and NMOS devices require the TSPC D flip-flop to operate at a larger supply voltage as compared to other QMOS flip-flop topologies.

The D flip-flop can be easily modified to operate as an S-R flip-flop. The circuit diagram of a QMOS S-R flip-flop is illustrated in Fig. 2(a). Fig. 2(b) shows a positive edge-triggered QMOS T flip-flop. The T flip-flop uses an XOR gate to generate the controlling feedback from the flip-flop output. An XOR gate can be implemented using just one RTD and three n-type FETs [4] and hence we achieve an extremely compact implementation of a T flip-flop.



(a)



(b)

Figure 2: Circuit diagram of a QMOS positive edge-triggered TSPC (a) S-R flip-flop, (b) T flip-flop.

Positive edge-triggered flip-flops can be derived from their negative edge-triggered versions by interchanging the p-type FET and n-type FET whose gate terminals are connected to the clock input. Asynchronous set operation can be added to the above edge-triggered flip-flops by adding a p-type MOSFET between the power supply and the Q output whose gate is controlled by an active low preset input. Similarly, asynchronous reset can be achieved by connecting an active high reset signal to the gate of an n-type MOSFET connected between ground and the Q output. Fig. 3 shows the schematic diagram of a QMOS positive edge-triggered D flip flop with asynchronous reset and preset.

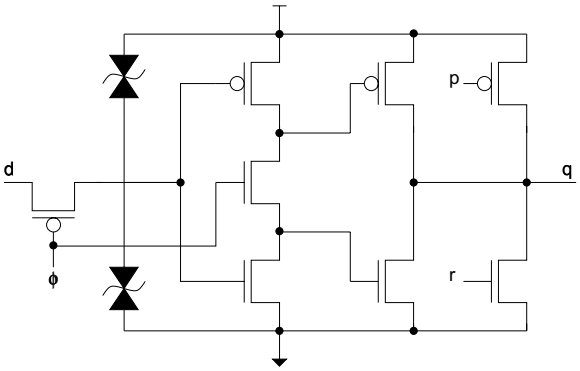


Figure 3: Circuit diagram of a QMOS positive edge-triggered D flip flop with asynchronous reset and preset.

3 Comparison of QMOS and CMOS Flip-Flop Circuits

In this section, we present a comparison between QMOS flip-flop circuits and CMOS flip-flop circuits based upon comparison of the circuit network topologies. Of prime interest using these approximate analyses is comparison of the timing behavior, area, and power consumption of the flip-flop circuits. Five different flip-flop circuits are considered for comparison, including two QMOS flip-flops and two CMOS flip-flops. These are: 1) C^2MOS master-slave flip-flop, 2) Bistable QMOS master-slave flip-flop, 3) CMOS TSPC flip-flop, and 4) QMOS edge-triggered TSPC flip-flop.

3.1 Flip-flop parameters

Three timing parameters of the flip-flop are of interest. The setup time, t_s, is defined as the time for which the input signal to the flip-flop must have stabilized prior to the arrival of the active clock edge. The hold time, t_h, is defined as the minimum time for which the input signal must be stable after the active edge of the clock in order to have correct evaluation. The *clock-to-Q* delay, t_d, is defined as the propagation delay from the active edge of the clock to the new valid output of the flip-flop. It is important to understand the relative importance of these timing parameters. The minimum delay of a single flip-flop stage governs the maximum operating frequency of the flip-flop and is given by $t_c = t_s + t_d$. The hold time,

t_h of the flip-flop must be less than or equal to t_d so that a new valid output of a flip-flop does not violate the hold time of a succeeding stage. Usually, in the presence of combinational logic between stages, hold time constraints are easily met and thus the setup time and *clock-to-Q* delay form the most important timing parameters of a flip-flop. For area comparison, we define the area of a flip-flop circuit as the sum of the channel areas of the various MOS transistors. Here, we make an assumption that RTDs are vertically integrated on top of source/drain regions of MOS devices and hence do not cause additional area overhead. The dynamic power dissipation of the circuits is compared by utilizing the fact that dynamic power is proportional to total capacitance of all the nodes switching during operation of the flip-flop.

3.2 Comparison method

To compare performance of QMOS and CMOS flip-flops, we use the unit transistor delay metric of [5] that has also been used by Rogenmoser to perform a comparative study of CMOS flip-flop circuits [6]. It is assumed that the time to discharge a node through an NMOS transistor equals the time to charge it though a PMOS transistor that is three times the size of the NMOS transistor. The capacitance at the output, C_n, assumed to be that of a unit inverter, composed of unit transistors, can be subdivided as: 1) PMOS gate capacitance, $0.6C_n$, 2) NMOS gate capacitance, $0.2C_n$, and 3) output capacitance of driving PMOS and NMOS transistors, $0.2C_n$. To account for other transistor and RTD configurations, the following assumptions are made. When two unit NMOS transistors are driving a node, the contribution to the load capacitance is $0.2C_n \times 2/4 = 0.1C_n$, instead of the $0.2C_n$ mentioned above. Similarly, when two unit PMOS transistors are driving a node, the contribution to the load capacitance is $0.2C_n \times 6/4 = 0.3C_n$. The contribution of the RTD to the output capacitance is considered the same as a unit NMOS transistor. The normalized delay through a transistor per C_n load capacitance is assumed to be τ_n. Further, assume that the standard load of the flip-flop circuits is a similar stage. Also, the area of a unit NMOS transistor is A_n and that of a PMOS transistor is $3A_n$.

3.3 Flip-flop network topology comparison

Fig. 4(a) shows the circuit diagram of a CMOS TSPC D flip-flop with annotated load capacitances. The setup time for the TSPC flip-flop is measured as the maximum of the delay from the data input to the QM_p or QM_n nodes. Since the QM_p node has the larger capacitance, the setup time, $t_s = 2\tau \times 0.8C_n = 1.6\tau_n$. The delay time, measured from node QM_p to node Q on arrival of the clock is, $t_d = 2\tau \times 0.4C_n + \tau \times C_n = 1.8\tau_n$. Area of the CMOS TSPC flip-flop is $16A_n$. Dynamic power dissipation, $P_d \propto 0.8C_n + 0.4C_n + C_n = 2.2C_n$.

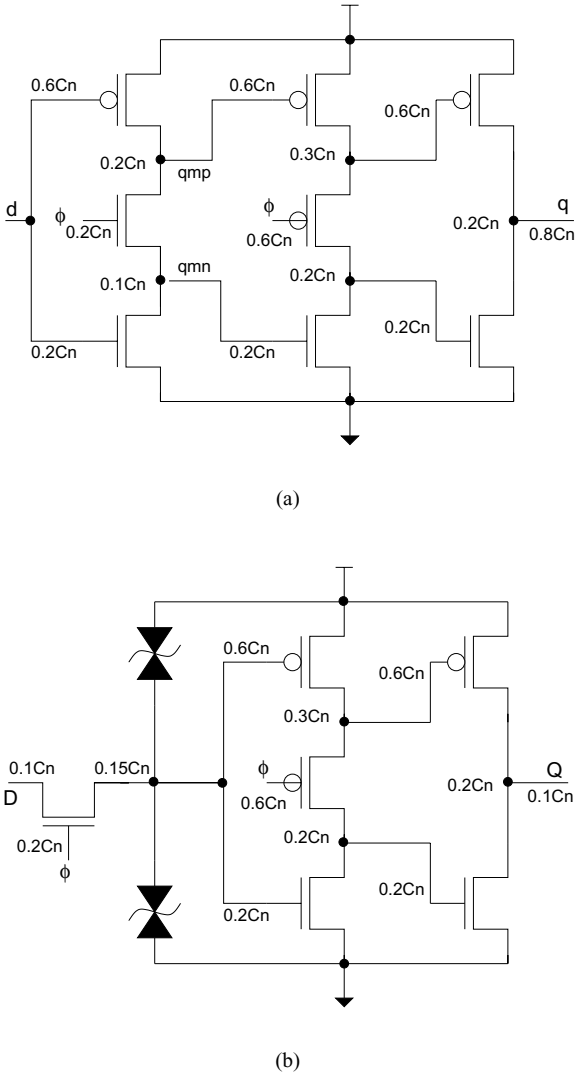


Figure 4: Circuit diagram of (a) CMOS TSPC D flip flop with annotated node capacitances, (b) QMOS TSPC D flip flop with annotated node capacitances.

Fig. 4(b) shows the circuit diagram of a QMOS edge-triggered TSPC D flip-flop with annotated load capacitances. The setup time of the QMOS TSPC flip-flop is, $t_s = \tau \times 0.95C_n = 0.95\tau_n$. The propagation delay of the QMOS TSPC flip-flop is, $t_d = 2\tau \times 0.4C_n + \tau \times 0.3C_n = 1.1\tau_n$. The area of the QMOS TSPC flip-flop is $12A_n$. Dynamic power dissipation, $P_d \propto 0.95C_n + 0.4C_n + 0.3C_n = 1.65C_n$.

To summarize the flip-flop comparisons, the results of the unit delay metric analyses are presented in Table 1 which indicate that the QMOS TSPC flip-flop has better

performance than an equivalent TSPC CMOS flip-flop.

Table 1: Comparison of QMOS and CMOS flip-flop circuits.

Parameter	C^2MOS	TSPC CMOS	TSPC QMOS
t_s	$2\tau_n$	$1.6\tau_n$	$0.95\tau_n$
t_d	$2\tau_n$	$1.8\tau_n$	$1.1\tau_n$
Area	$16A_n$	$16A_n$	$12A_n$
Dynamic Power	$2C_n$	$2.2C_n$	$1.65C_n$

The unit metric delay analysis provides a means of easily comparing flip-flop circuits based on their network topology. These basic analyses are substantiated with simulation-based comparison of CMOS and QMOS circuits in the following section.

3.4 TSPC flip-flop

A Monte-Carlo simulation of the QMOS D flip-flop and a conventional true single phase clock (TSPC) CMOS flip-flop using identical MOS devices is shown in Fig. 5. It can be seen that the QMOS flip-flop operates at a higher frequency than the CMOS TSPC flip-flop. Table 2 shows the comparison between a QMOS D flip-flop and a TSPC D flip-flop implemented in 0.25 micron CMOS technology.

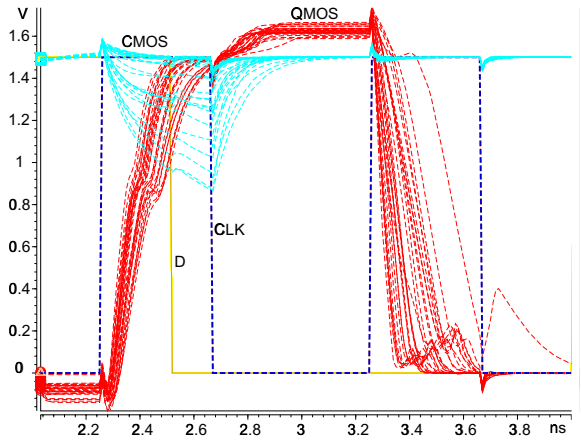


Figure 5: Simulation comparison of QMOS and CMOS TSPC flip-flops.

4 Conclusions

We have developed a novel flip-flop topology that combines RTDs with MOSFETs to yield compact implementation and high performance. The comparison with equivalent CMOS implementations demonstrates the advantages of the QMOS flip-flop. Simulation-based characterization has shown that QMOS flip-flop offers almost fourfold imporvement in area-power-delay characteristics over comparable CMOS.

Table 2: Comparison of QMOS and CMOS TSPC D flip-flops.

Parameter	CMOS	QMOS
Setup time (ps)	100	60
Hold time (ps)	200	90
Rise delay (ps)	200	90
Fall delay (ps)	120	80
Power (μW)	47	34
Power-delay (fJ)	14.1	5.1
Devices	8	8
Area (normalized)	1.33	1
Area-power-delay (normalized)	3.75	1

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