Tunneling-Phase Logic Based Cellular Nonlinear Networks


Abstract - A new scheme for high-level information processing based on cellular nonlinear networks composed of arrays of tunneling phase logic elements is described.

1 Introduction

The continued scaling of integrated circuit technology at its current Moore’s Law rate could lead to circuits containing over a billion transistors with 20 nanometer features by the year 2015. While the progress in electronics thus far has relied on the scaling of transistors and on an increasingly complex maze of interconnecting wires, future circuitry will require a major paradigm shift involving radically different fabrication technologies, device principles, and circuit architectures. Constraints on power dissipation at higher integration levels will mandate relatively simple, ultrasmall devices laid out in highly regular arrays and interconnected locally. This paper deals with an approach for realizing high-level information processing based on cellular nonlinear networks (CNN) composed of arrays of locally interconnected tunneling phase logic (TPL) elements.

2 Tunneling phase logic element

A basic mechanism for realizing TPL [1] is the influence of Coulomb blockade on the tunneling process in an ultra-small junction. TPL is a radical departure from other “single electron” approaches since the logic state is represented temporarily by the electrical phase of the tunneling events, rather than by the spatial position of electrons or by voltage or current levels. In TPL, the tunneling is locked at a frequency equal to half the reference or “pump” frequency. Since such subharmonic locking can occur in two different phase relationships with respect to the pump signal (either on the on-beat or the off-beat), the two phases can be used to represent binary logic states. The tunneling process produces an impulsive voltage waveform in which a spike occurs each time an electron tunnels, as shown in Fig. 1. It may be noted that the characteristics of a TPL element bears some similarly with those of a neuron. Capacitive coupling between elements can produce a strong interaction between the tunneling the element, as illustrated in Figs. 1 and 2. The nonlinear dynamics of single and two coupled TPL elements have been analysed in some detail [2].

Figure 1 — Simulated voltage waveforms across two capacitively coupled tunneling junctions. Spikes indicate single electron tunneling events, which are phase locked to an ac pump signal. Junction J1 is biased for tunneling from the beginning the time period. When J2 is biased on it locks to the opposite phase due to the capacitive coupling between the junctions.

Figure 2 — Trajectory of voltages across two coupled TPL elements during locking (the last half of the time period in Fig. 1. Inset shows dc and ac biasing arrangement.

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nonlinear interaction can potentially be exploited in various types of circuitry.

The earliest studies of TPL focused on circuitry for performing Boolean functions based on majority logic [1]. More recently, the TPL concept was extended to multiple valued logic which exploits the natural ability of TPL to represent N logic states by phase locking between Nth harmonics [3], [4]. Here, we exploit the nonlinear system dynamics in a two-dimensional array of locally interconnected TPL cells.

3 Cellular nonlinear network

In its most general form, a CNN is a two-dimensional array of nonlinear elements that are locally interconnected with nearest neighbors, or next nearest neighbors, with programmable coupling strengths and variable neighborhood system structures [5]. Several variations on the CNN theme, including a) continuous-time CNN, b) discrete-time CNN, and c) high-level CNN structure have been studied in detail.

The application of CNN to image processing has attracted a great deal of theoretical and experimental interest. This work includes the recent experimental demonstration of an image processing chip based on a 64x64 CNN array implemented in 0.35 µm CMOS [6]. The chip, which used gray-scale input and output with local analogue and logical memories for each cell, was tested at approximately 500ns per image processing step with an accuracy of approximately 5 bits per cell. Since much larger levels of integration are of interest even for near-term applications, such as enhanced imaging chips for the 1280x960 arrays used in present commercial digital cameras, implementations of CNN based on other more scalable technologies are of great interest. Theoretical study of the universal computation capability of CNN and other issues related to the extendability of this approach to more general applications are also of great interest for the set of applications envisioned here.

4 TPL-CNN Approach

In TPL-CNN we combine the device concept of nanoscale TPL with the architecture concept of CNN. The high integration density of TPL-CNN potentially allows increased robustness to be obtained through redundancy by using many devices per cell. Furthermore, although devices are locally interconnected the nonlinear system dynamics of CNN has a global character via propagating processes, which might also be exploited for robustness. Both of these factors could be extremely useful for compensating for two fundamental drawbacks of nanoscale devices: their lower yield, caused by sensitivity to imperfections and parameter variations, and higher error rate, caused by sensitivity to thermal noise and quantum fluctuations.

TPL-CNN can be viewed as a hybrid of continuous time and discrete-time CNN. Although each cell is connected only to its nearest neighbors, the nonlinear system dynamics in a 2D array of cells exhibit a...
output. In addition, the illumination of the array by an optical or e-beam pattern could provide a two-dimensional input for the TPL-CNN array. TPL-CNN might also function as a massive parallel platform for implementing logical computations based on local rules and many of the other computational tasks that can be implemented by CA.

A preliminary analysis of a 100x100 cell TPL-CNN array based on a simple cell configuration has been carried out as a step toward evaluating the feasibility of this approach [7]. The simulated evolution of the pattern revealed two important points. First, the short-time evolution of the pattern exhibits characteristics of interest for edge and corner detection. Second, the evolution of this pattern at longer times exhibits characteristics similar to what is seen in cellular automata arrays. This is illustrated in Fig. 3 which shows a snap-shot in time of the evolution of the phase states in the array (shown by different gray-scale values) from initial conditions represented by a black square with a white border (uniform phase states in two regions). These results indicate that image processing and more general information processing applications should be possible with TPL-CNN [5].

5 Conclusion
TPL-CNN could potentially allow image processing and more general information processing functions to be performed by arrays of nanoscale devices. Such operations could potentially be carried out at high speeds by directly operating on inputs composed of spatial patterns of information, in contrast to conventional circuitry where operations are performed on individual bits of data. Such architectures circumvent the interconnect problem through their local connectivity and could provide powerful new capabilities for information processing using techniques beyond the reach of conventional technology.

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References