

Circuit Paradigm in the 21st Century

**Proceedings of the 15th European
Conference on Circuit Theory and Design**

ECCTD'01

**Helsinki University Of Technology, Espoo, Finland
28-31 August 2001**

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Organized Under the Patronage of European Circuit Society, ECS



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FOREWORD

The first *European Conference on Circuit Theory and Design* (ECCTD) was held in 1972 in London. It was organized by a group of devoted European scientists from universities and industry. They all shared a belief that the *circuit paradigm* is an important underlying principle, first of all in electronics, telecommunications, and computing, but also in a variety of other applications. In the same year, the International Journal of Circuit Theory and Applications (CTA) was launched to encourage research and development of circuit theory and techniques. In the late 80's, the *European Circuit Society* (ECS, <http://eswww.it.dtu.dk/~el/ecs/>) was founded to serve all of us, in Europe and elsewhere, interested in the circuit paradigm.

The 15th ECCTD follows the format and tradition established by the previous biannual meetings in *London, Lausanne, Genoa, Warsaw, The Hague, Stuttgart, Prague, Paris, Brighton, Copenhagen, Davos, Istanbul, Budapest, and Stresa*. It is an honour for the Finnish members of the ECS to host the first ECCTD of the new Millennium. The theme of the conference, '**Circuit Paradigm in the 21st Century**' reflects the promising future views opened up by the rapid progress of many promising new technologies including ULSI systems on chip, cellular nonlinear circuits and nanoelectronics, in many application areas such as wireless telecommunications, neural computing, speech and video processing etc. Our aim is to bring together people from industry and academia to exchange ideas and to find the weak signals of today's research that will lead to important breakthrough applications tomorrow.

ECCTD'01 starts with a specialist workshop 'Design Automation Day' and tutorial short courses on a variety of topics including MOS modelling, Network Calculus, Grid Theory and Chaos Applications. Next morning, the keynote plenary lectures of Teuvo Kohonen and Sanjit Mitra open up the main conference. The plenary program continues each morning and afternoon, and all together nine distinguished invited speakers illuminate the future role of the circuit paradigm in their research areas: neural networks, molecular and analogic computing, analogue and digital signal processing, and telecommunication circuits. A special *Belevitch lecture* will be given by J. O. Scanlan in honour of Vitold Belevitch (1921-1999), one of the leading circuit theorists of the 20th century.

The technical program, a rich presentation of various fields of Circuit Theory and Design, is organized into 28 regular, 22 special, and 6 poster sessions. The poster presentations have been selected on the suitability of the content for visual presentation. There is no quality difference between oral and poster presentations, and many of the best papers are presented as posters.

The conference program reflects the strength of the wireless communication industry. There are full three-day sub-conferences on analogue, RF and mixed integrated circuit design for telecommunication systems, on VLSI design, and on simulation, modelling and design tools, and different aspects of signal processing.

ECCTD'01 is organized under the patronage of the European Circuit Society. The local organizer in Finland is EIS, the Society of Electronics Engineers in Finland. Other co-sponsors are the IEEE Circuits and Systems Society, and the IEEE Finland Section. We also want to acknowledge the generous support received from Helsinki University of Technology, the City of Espoo, Academy of Finland and several Finnish enterprises listed at the end of this book. The conference venue is the main building of Helsinki University of Technology, a masterpiece of architect Alvar Aalto.

We wish all participants a pleasant stay in Helsinki/Espoo. Welcome to ECCTD'01.



Veikko Porra
ECCTD'01 Conference Chairman



Martti Valtonen
Technical Program Chairman

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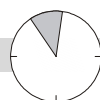
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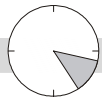
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Ekaterina Loskot, University of Oulu, Finland; *Irina Vendik*, St.-Petersburg Electrotechnical University, Russia; *Eino Jakku*, *Seppo Leppävuori*, University of Oulu, Finland

Nonlinear Microwave Signal Processing in Yttrium-Iron Garnet (YIG) Films **I-293**

Gennadiy Melkov, *Yurij Kobljanskyj*, *Alexander Serga*, *Vasil Tiberkevich*, National Taras Shevchenko University of Kiev, Ukraine; *Andrei Slavin*, Oakland University, Department of Physics, USA

Input Current Shaping Technique for PFC Flyback Rectifier by Using Inductor Voltage Detection **I-297**

Tanes Tanitteerapan, *Shinsaku Mori*, Nippon Institute of Technology, Japan

Analysis and Design of Controllable Class E Low dv/dt Synchronous Rectifier **I-301**

Itsda Boonyaroonate, *Shinsaku Mori*, Nippon Institute of Technology, Japan

A Power System Faults Analysis **I-305**

Mariana Dumitrescu, *Toader Munteanu*, "Dunarea de Jos" University of Galati, Romania; *Anatoli Paul Ulmeanu*, "Politehnica" University of Bucharest, Romania

Analysis and Modeling of the Non-Linear Sampling Process in Switched-Current Circuits - Application to Bandpass Sigma-Delta Modulators **I-309**

Jose M. de la Rosa, *Belen Perez-Verdu*, *Fernando Medeiro*, *Rocio del Rio*, *Angel Rodriguez-Vazquez*, Instituto de Microelectronica de Sevilla, IMSE-CNM, Spain

Stability Analysis of High Order Sigma-Delta Modulators **I-313**

Valeri Mladenov, *Hans Hegt*, *Arthur van Roermund*, Technical University Eindhoven, The Netherlands

Realization of A Non Integer Order Pid Controller **I-317**

Salvatore Abbisso, *Riccardo Caponetto*, *Olga Diamante*, *Eusebio Di Cola*, STMicroelectronics, Italy; *Luigi Fortuna*, University of Catania, Italy; *Domenico Porto*, STMicroelectronics, Italy

An Adiabatic Multi Stage Driver **I-321**

Christoph Saas, TU Munich, Germany; *Andreas Schlaffer*, Infineon AG, Germany; *Josef A. Nosseke*, TU Munich, Germany

A CMOS Adiabatic BUS-Driver **I-325**

Jacek Flak, *Veikko Porra*, Helsinki University of Technology, ECDL, Finland

A Novel Low Power Multiplexer-Based Full Adder **I-329**

Abdulkarim Al-Sheraidah, *Yingtao Jiang*, *Yuke Wang*, *Edwin Sha*, University of Texas at Dallas, USA

Storage Bandwidth Optimization and Memory Assignment for Low Power VLSI Systems **I-333**

Wen-Tsong Shiue, Silicon Metrics Corporation, USA



9:00 — 15:10

**DESIGN AUTOMATION DAY
Session Room D**

A Compact Computational Core for Image Processing **I-337**

Ari Paasio, *Asko Kananen*, *Mika Laiho*, *Kari Halonen*, ECDL/HUT, Finland

Pulse-Width-Modulation (PWM) Alternatives For The Implementation of Programmable Analog Processing Arrays (PAPAs) **I-341**

Servando Espejo, *Rafael Dominguez-Castro*, *Gustavo Linan*, *Ricardo Carmona*, *Angel Rodriguez-Vazquez*, Instituto de Microelectronica de Sevilla, Spain

ACE16k: a Programmable Focal Plane Vision Processor with 128 X 128 Resolution **I-345**

Gustavo Linan, *Rafael Dominguez-Castro*, *Servando Espejo*, *Angel Rodriguez-Vazquez*, Instituto de Microelectronica de Sevilla, Spain

Interpolation of 2D Signals Using CNN **I-349**

Alexandru Gacsadi, Univ. of Oradea, Romania; *Peter Szolgay*, Comp. and Aut. Ins, of HAS, Hungary

Design Aspects of an Optical Correlator Based CNN Implementation **I-353**

Szabolcs Tökés, *László Orzó*, *Tamas Roska*, MTA SZTAKI (Computer and Automation Institute of the Hungarian Academy of Sciences), Hungary

A CNN Model Framework and Simulator for Biological Sensory Systems **I-357**

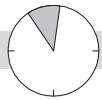
David Balya, MTA-SZTAKI, Hungary; *Botond Roska*, UCB, USA; *Tamas Roska*, MTA-SZTAKI, Hungary; *Frank S. Werblin*, UCB, USA

Ace Box: High-Performance Visual Computer Based on the ACE4k Analogic Array Processor Chip **I-361**
Akos Zarandy, Hungarian Academy of Sciences, Hungary

Some New Analogic CNN Algorithms for PCB Quality Control **I-365**
Timot Hidvegi, Peter Szolgay, Computer and Automation Institute, Hungarian Academy of Sciences, Hungary

An Analogic CNN Algorithm - a Switch Implementation **I-369**
Istvan Beszteri, Oy LM Ericsson AB, Finland; *Tamas Bezak*, Hungarian Academy of Sciences, Hungary; *Peter Szolgay*, University of Veszprem, Hungary

Thursday, August 30



10:50 — 12:10

SESSION R7: SPEECH AND AUDIO PROCESSING DEVICES AND APPLICATIONS
Session Room A

Multichannel Audio Acquisition for Medical Supervision in an Intelligent Habitat **II-1**
Eric Castelli, Dan Istrate, CLIPS/IMAG, France

A New Method to Represent Speech Signals via Predefined Functional Bases **II-5**
Umit Guz, B.S. Yarman, Hakan Gurkan, Isik University, Turkey

Conversion of Sampling Rate Using New Generation of DSP's **II-9**
Tomasz Marciniak, Adam Dabrowski, Poznań University of Technology, Poland

Comparative Study of Speaker Verification Techniques Based on Vector Quantization, Sphericity Models and Dynamic Time Warping **II-13**
Sofia Tsekeridou, Constantine Kotropoulos, Alexandros Xafopoulos, Ioannis Pitas, Aristotle Univ. of Thessaloniki, Greece

SESSION R8: ANALOGIC WAVE ALGORITHMS
Session Room B

Calculating Local and Global PDEs by Analogic Diffusion and Wave Algorithms **II-17**
Csaba Rekeczky, Tamas Roska, PPCU, Hungary

Feature Extraction from Brain Electrical Activity in Epilepsy Using Cellular Neural Networks **II-21**
Roland Kunz, Ronald Tetzlaff, Institut für Angewandte Physik, JWG Universität Frankfurt, Germany

CNN Analogic Wave Algorithms: Template Design Methods **II-25**
Pier Paolo Civalieri, Marco Gilli, Politecnico di Torino, Italy

Comparing Dynamic Behaviour in 1-D CNNs and Reaction-Diffusion-Convection Pdes: a Review **II-29**
Claudio Serpico, DIE, University of Naples "Federico II", Italy; *Gianluca Setti*, DI - University of Ferrara, Italy; *Patrick Thiran*, ICA-DSC EPFL, Switzerland; *Sergio Callegari*, DEIS - University of Bologna, Italy

SESSION S9: MEMORY EFFECTS in RF POWER AMPLIFIERS
Session Room C

Effects of Filter Ripple in Predistortion Linearizer Architectures **II-33**
Weiyun Shan, Lund University, Sweden; *Lars Sundström*, Ericsson Mobile Communications AB, Sweden; *Bo Shi*, Lund University, Sweden; *Michael Faulkner*, Victoria University of Technology, Australia

Analysis of Amplitude-Dependent Memory Effects in RF Power Amplifiers **II-37**
Joel Vuolevi, Timo Rahkonen, Univ. of Oulu, Finland

A Volterra Model for Common-Source FET Amplifiers in Third Order Intermodulation Distortion Simulations **II-41**
Joel Vuolevi, Timo Rahkonen, Univ. of Oulu, Finland

A 29 DBM, 50% PAE, 1.9 GHz Power Amplifier Using a 20 GHz Ft Silicon Bipolar Technology **II-45**
Francesco Carrara, University of Catania, Italy; *Angelo Magliarisi, Antonino Scuderi*, STMicroelectronics, Italy; *Giuseppe Palmisano*, University of Catania, Italy

SESSION S10: LOW-POWER CMOS SENSORS AND ELECTRONICS FOR DIGITAL SINGLE-CHIP CAMERAS
Session Room D

High Dynamic Range CMOS Image Sensors Featuring Multiple Integration and Auto-Calibration II-49
Markus Schwarz, Arndt Bussmann, Thorsten Heimann, Bedrich Hosticka, Jürgen Huppertz, Olaf Schrey, FhG-IMS Duisburg, Germany

Bulk vs SOI CMOS APS Optimal Design for Low Power Low Voltage Applications II-53
Aryan Afzalian, Pierre Delatte, Jean-Didier Legat, Denis Flandre, Ucl-dice, Belgium

A New Cmos Imager Using the Pseudo-Active-Pixel-Sensor(PAPS) Circuit for High Resolution Applications II-57
Chung-Yu Wu, Yu-Chuan Shih, National Chiao Tung University, Taiwan

A Test Chip for a Novel High-Dynamic-Range CMOS Image Sensor II-61
David Stoppa, Andrea Simoni, Lorenzo Gonzo, Massimo Gottardi, Gian-Franco Dalla Betta, Gemma Hornero, ITC-IRST, Microsystems Division, Italy

SESSION R9: SIMULATION AND MODELING II
Session Room E

The Implementation and Development of a Time-Domain Model of Dispersive Transmission Line II-65
Anu Lehtovuori, Martti Valtonen, Jarmo Virtanen, Helsinki University of Technology, Circuit theory lab., Finland

Computationally-Efficient Behavioral Modeling of Pulsed Injection-Locked Amplifiers II-69
Enrico Calandra, Palermo University, Italy

A New Approach to Adaptive Modeling of the Electromagnetic Near and Far Field II-73
Jan Wilk, University of the Federal Armed Forces Hamburg, Germany; *Horst Röhm*, Philips GmbH Hamburg, Germany

Effective Parameters for Complex Multilayers in Electromagnetic Analysis II-77
Ari Sihvola, Swiss Federal Institute of Technology, EPFL, Switzerland; *Stefano Vaccaro, Jean-Francois Zürcher, Juan Mosig*, EPFL, Switzerland

SESSION R10: LOW-VOLTAGE ANALOG INTEGRATED CIRCUITS
Session Room Y228

A Robust and Universal Constant-GM Circuit Technique for Low-Voltage Rail-To-Rail Amplifiers II-81
J. M. Carrillo, J. L. Ausin, J. F. Duque-Carrillo, University of Extremadura, Spain; *E. Sánchez-Sinencio*, Texas A&M University, USA

Cmos Real-Time Analog Computational Circuits for Very Low Voltage Applications II-85
Antonio J. Lopez-Martin, Alfonso Carlosena, Dept. of Electrical and Electronic Eng., Public University of Navarra, Spain

A Versatile 1.5V Current-Mode Cmos Analog Multiplier/Divider Circuit II-89
Antonio J. Lopez-Martin, Alfonso Carlosena, Dept. of Electrical and Electronic Eng., Public Univ. of Navarra, Spain

1-V CMOS Class AB Current Mirror II-93
Salvatore Pennisi, Univ. Catania, Italy

SESSION R11: ANALYSIS AND MODELING OF CHAOTIC CIRCUITS
Session Room 307

Bifurcations and Continuation in a Smooth Model of a Buck Converter II-97
Gerard Olivar, Enric Fossas, UPC, Spain

Two-Dimensional Basic Bifurcation Analysis of a Chaotic Oscillator Based on Hysteresis II-101
Federico Bizzarri, Marco Storace, D.I.B.E. - University of Genoa, Italy

Markov Chain Modeling of Chaotic Wandering in Simple Coupled Chaotic Circuits II-105
Yoshifumi Nishio, Martin Hasler, Swiss Federal Institute of Technology, Switzerland; *Akio Ushida*, Tokushima University, Japan

Frequency Studies of Bandpass Sigma-Delta Modulation II-109
Daniele Fournier-Prunaret, Veronique Guglielmi, SYD-LESIA-DGEI-INSA, France; *Orla Feely*, UCD, Ireland

**SESSION PS3: ANALYSIS AND DESIGN TOOLS.
MODELING AND SIMULATION**

Multilevel Newton-Raphson Method for Parallel Circuit Simulation II-113
Mikko Honkala, Janne Roos, Martti Valtonen, Helsinki University of Technology, Finland

Performance Estimation in Analog Computer Aided Design II-117
Faik Baskaya, Gunhan Dundar, Bogazici University, Turkey

A Complete Retargeting Methodology for Mixed-Signal IC Designs II-121
Rafael Castro-López, Francisco Fernández, Manuel Delgado-Restituto, Angel Rodriguez-Vázquez, IMSE-CNM-CSIC, Spain

VHDL-AMS Model of Sense Amplifier for Flash Memories II-125
Ivan Boccuni, ST-Microelectronics, MPG Group, Italy; *Rosario Gulino, Gaetano Palumbo*, DEES - University of Catania, Italy

High-Level Circuit and System Simulation With Java II-129
Ulrich Kaiser, Texas Instruments, Germany

Simulation of Multiconductor Transmission Lines Using Two-Dimensional Laplace Transformation II-133
Lubomír Braněk, Brno University of Technology, Czech Republic

Digital Filter Design Through Simulated Evolution II-137
Massimiliano Erba, Roberto Rossi, University of Pavia, Italy; *Valentino Liberali, Andrea Tettamanzi*, University of Milan, Italy

Digital Standard Cell Library Migration Using a Genetic Approach II-141
Kenneth Francken, Georges Gielen, K.U. Leuven, Belgium

Efficient Spice-Netlist Representation of Reduced-Order Interconnect Model II-145
Yuya Matsumoto, Sophia University, Japan; *Yuichi Tanji*, Kagawa University, Japan; *Mamoru Tanaka*, Sophia University, Japan

Interconnect Model for Simulation of a Low-Voltage Integrated Power Amplifier II-149
Johan Sjöström, Ericsson Microelectronics AB, Sweden; *Christian Nyström*, Wireless Solutions Sweden; *Ted Johanson*, Ericsson Microelectronics AB, Sweden; *Torkel Arnborg*, Ericsson Microelectronics AB, Sweden

Faster Incremental VLSI Placement Optimization II-153
Chieh Lin, Eindhoven University of Technology, The Netherlands; *Domine Leenaerts*, Philips Research Labs, The Netherlands; *Arthur van Roermund*, Eindhoven University of Technology, The Netherlands

The Vector Network Approach to Inconsistent Initial Conditions in Linear and Nonlinear Switch-Mode Circuits II-157
Jan Ogrodzki, Warsaw University of Technology, Poland

A Rigorous Approach to Electro-Thermal Network Modeling II-161
Lorenzo Codecasa, Dario D'Amore, Paolo Maffezzoni, Politecnico di Milano - DEI, Italy



15:30 — 16:50

**SESSION S11: NONLINEAR CIRCUITS IN COMMUNICATION SYSTEMS (NCCS)
Session Room A**

Exploiting Chaos in Multibit Sigma Delta Modulation II-165
Joshua Reiss, Mark Sandler, King's College London, UK

Mode-Locking and Strange Nonchaotic Attractors in a Digital Phase-Locked Loop With FM Input II-169
Anna Vasylenko, Institute of Mathematics, Ukraine; *Orla Feely*, University College Dublin, Ireland; *Yuri Maistrenko*, Institute of Mathematics, Ukraine

Simplification of Nonlinear DAE Systems with Index Tracking II-173
Tim Wichmann, Fraunhofer Institute for Industrial Mathematics, Germany

About the Spectral Properties of Non-Linear Zero-Position Coding Algorithm II-177
Frank Felgenhauer, Martin Streitenberger, Wolfgang Mathis, University of Hannover, Germany

**SESSION S12: APPLICATIONS OF CHAOS I
Room B**

Chaos Based DS-CDMA Systems: Steps from Theory to Experiments II-181
Gianluca Mazzini, CEGDI - University of Ferrara, Italy; *Riccardo Rovatti*, CEGDEIS - University of Bologna, Italy; *Gianluca Setti*, CEGDI - University of Ferrara, Italy

<p>Comparison of Different Chaos Shift Keying Methods II-185 <i>Thomas Schimming, Martin Hasler</i>, EPFL, Switzerland</p>	<p>New Cost Evaluation Schemes in Graph-Based Memory Allocation Method for Indirect Addressing DSPs II-221 <i>Nobuhiko Sugino, Tomoyuki Matsuura, Akinori Nishihara</i>, Tokyo Institute of Technology, Japan</p>
<p>On the Spectrum of Signals Obtained by Driving FM Modulators with Chaotic Sequences II-189 <i>Sergio Callegari, Riccardo Rovatti</i>, DEIS, University of Bologna, Italy; <i>Gianluca Setti</i>, DI, University of Ferrara, Italy</p>	<p>An Algorithm for the Optimization of Pipelined Recursive Digital Filters II-225 <i>Juha Yli-Kaakinen, Tapio Saramäki</i>, Signal Processing Lab., Tampere University of Technology, Finland</p>
<p>Non-Redundant Error Correction in FM-DCSK Chaotic Communications Systems II-193 <i>Zoltan Jako</i>, Budapest University of Technology and Economics, Hungary; <i>Daniele Fournier-Prunaret, Veronique Guglielmi</i>, L.E.S.I.A., I.N.S.A., France; <i>Gabor Kis</i>, Budapest University of Technology and Economics, Hungary</p>	<p>SESSION R12: ANALYSIS AND DESIGN TOOLS I Session Room E</p>
<p>SESSION S13: ADVANCED NUMERICAL TECHNIQUES FOR TRANSIENT AND STEADY-STATE ANALYSIS OF NONLINEAR CIRCUITS Session Room C</p>	<p>A Combined Structural and Symbolic Method for Automatic Behavioral Modeling of Nonlinear Analog Circuits II-229 <i>Markus Olbrich, Ralf Popp, Lutz Näthke, Lars Hedrich, Erich Barke</i>, University of Hanover, Institute of Microelectronic Circuits and Systems, Germany</p>
<p>Analysis of Digitally Modulated Steady States in Nonlinear Circuits by Krylov-Subspace Harmonic Balance II-197 <i>Vittorio Rizzoli, Alessandra Costanzo</i>, DEIS, University of Bologna, Italy; <i>Franco Mastri</i>, DIE, University of Bologna, Italy</p>	<p>Optimal Zero Locations of Continuous-Time Systems Tracking Reference Step Responses II-233 <i>Anna Soffia Hauksdottir</i>, University of Iceland, Iceland</p>
<p>Advanced Analysis and Design Methods for RF and Millimeter Wave Mems II-201 <i>Katia Grenier</i>, LAAS CNRS, France; <i>Laurent Rabbia, Patrick Pons, A Takacs, T Parra, J Graffeuil, H Aubert</i>, LAAS, France; <i>Robert Plana</i>, LAAS CNRS, France</p>	<p>Efficient Methods for Reducing Register And Phase Requirements for Synchronous Circuits Derived Using Software Pipelining Techniques II-237 <i>Noureddine Chabini, El Mostapha Aboulhamid</i>, Universite de Montreal, Canada; <i>Yvon Savaria</i>, Ecole Polytechnique de Montreal, Canada</p>
<p>Generalized Circuit Formulation for the Transient Simulation of Circuits Using Wavelet, Convolution and Time-Marching Techniques II-205 <i>Michael Steer, Carlos Christoffersen</i>, North Carolina State University, USA</p>	<p>I.M.A.G.E A New Cad Tool for Device Modeling in Spice II-241 <i>Marco Zorzi, Francesco Franzè, Nicolò Speciale</i>, DEIS, University of Bologna, Italy</p>
<p>Combined State-Space and Convolution Techniques for Transient and Steady-State Simulation of RF/Microwave Circuits II-209 <i>Thomas Brazil</i>, University College Dublin, Ireland</p>	<p>SESSION R13: DIGITAL SYSTEMS Session Room Y228</p>
<p>SESSION S14: OPTIMIZATION OF DIGITAL FILTERS Session Room D</p>	<p>Optimized Design of Carry-Bypass Adders II-245 <i>Massimo Alioto, Gaetano Palumbo</i>, DEES - University of Catania, Italy</p>
<p>Express Coefficients in 13-ary radix-4 CSD to Create Computationally Efficient Multiplierless FIR Filters II-213 <i>Jeffrey Coleman</i>, Naval Research Laboratory, USA</p>	<p>A 200-MHz RNS Core II-249 <i>Haridimos Vergos</i>, Computer Engineering & Informatics Dept., Greece</p>
<p>An MILP Approach for the Design of Linear-Phase FIR Filters with Minimum Number of Signed-Power-Of-Two Terms II-217 <i>Oscar Gustafsson, Håkan Johansson, Lars Wanhammar</i>, Linköping University, Sweden</p>	<p>Minimizing Sensitivity to Clock Skew Variations Using Level Sensitive Latches II-253 <i>François-Raymond Boyer, El Mostapha Aboulhamid</i>, DIRO, Université de Montréal, Canada; <i>Yvon Savaria</i>, DGEGI, École Polytechnique de Montréal, Canada</p>

Color Filter Array and Color Correction for High Dynamic Range CMOS Image Sensors II-257
Thorsten Heimann, Markus Schwarz, Bedrich Hosticka, Fraunhofer Institute of Microelectronic Circuits and Systems, Germany

SESSION R14: CNN CIRCUIT DESIGN
Session Room Y307

Robust Multilayer DTCNN Design for B/W and Grayscale Input Applications II-261
Paula Lopez, David L. Vilarino, Victor M. Brea, Diego Cabello, Departamento de Electronica e Computacion, Universidade de Santiago de Compostela, Spain

2d Two-Channel IIR PRQMF Bank Design Using CNN II-265
Emir Tufan Akman, Koray Kayabol, University of Istanbul, Turkey

A DTCNN CMOS Implementation of a Pixel-Level Snake Algorithm II-269
Victor M. Brea, University of Santiago de Compostela, Spain; *Ari Paasio*, Helsinki University of Technology, ECDL, Finland; *David L. Vilarino, Diego Cabello*, University of Santiago de Compostela, Spain

CNNS, Intelligence and Synchronization Theory II-273
Johan Suykens, Joos Vandewalle, K.U. Leuven, ESAT-SISTA, Belgium

SESSION S15: SYSTEM ON A CHIP
Session Room Y227

Early Estimation of Interconnect Effects on the Operation of System-On-Chip Platforms II-277
Tero Nurmi, University of Turku, Finland; *Li-Rong Zheng*, Royal Institute of Technology, Sweden; *Jouni Isoaho*, University of Turku, Finland; *Hannu Tenhunen*, Royal Institute of Technology, Sweden

Interconnect IP for Gigascale System-On-Chip II-281
Ilkka Saastamoinen, TUT, Finland; *Teemu Suutari, Jouni Isoaho*, UTU, Finland; *Jari Nurmi*, TUT, Finland

Reed-Muller Transform Based Boolean Matching Filters II-285
Chip-Hong Chang, Bogdan Falkowski, School of Electrical & Electronic Engineering, Singapore

Generic Interface Block for System-on-a-Chip Designs II-289
Vesa Lahtinen, Kimmo Kuusilinna, Tampere University of Technology, Digital and Computer Systems Laboratory, Finland; *Timo Hämäläinen, Jukka Saarinen*, Tampere University of Technology, Digital and Comp, Finland

SESSION PS4: ANALOGUE AND DIGITAL SIGNAL PROCESSING. FAULT DETECTION

Reconstruction of Nonuniformly Sampled Bandlimited Signals Using Digital Fractional Delay Filters: Error and Quantization Noise Analysis II-293
Håkan Johansson, Per Löwenborg, Linköping University, Sweden

On Adjustable Fractional Delay FIR Filters and Their Design II-297
Håkan Johansson, Per Löwenborg, Linköping University, Sweden

VLSI Parallel Architecture for Low Density Parity Check Decoder II-301
Wai Leng Lee, Angus Wu, Ping Li, Department of Electronic Engineering, City University of Hong Kong, Hong Kong

Signal-Flow-Graph Identities for Structural Transformations in Multirate Systems II-305
Alexandra Groth, Heinz Göckler, Ruhr-Universitaet Bochum, Germany

Prototype Filter Design Techniques for Cosine-Modulated Transmultiplexers II-309
Pilar Martín-Martín, Fernando Cruz-Roldán, Pedro Amo-López, Francisco López-Ferreras, University of Alcalá, Spain

A Study of Distributed Algorithm for Network Optimization Problem Based on Tie-Set Graph Theory II-313
Takeshi Ishibashi, Toshio Koide, Hitoshi Watanabe, Soka University, Japan

A Novel Technique for the Estimation of Stability in Feedforward and Multiple-Feedback Oversampled Sigma-Delta A/D Converter Configurations II-317
Neil Fraser, Behrouz Nowrouzian, University of Alberta, Canada

Optimization of Chirp-Z and Truncated Shannon's Interpolation II-321
Djordje Babic, Markku Renfors, Tampere University of Technology, Telecommunications Lab., Finland

Fractional Signal Processing: Scale Conversion II-325
Manuel Ortigueira, UNINOVA, Portugal; *Carlos Matos*, Escola Superior de Tecnologia, Portugal; *Moisés Piedade*, INESC, Portugal

Rns-Fpl Merged Polyphase DWT Architectures **II-329**

Javier Ramirez, University of Granada, Spain; *Antonio García*, Universidad Autónoma de Madrid, Spain; *Pedro García Fernández*, University of Jaén, Spain; *Luis Parrilla*, *Antonio Lloris*, University of Granada, Spain

An Efficient Semi-Systolic Architecture for 2-D Discrete Wavelet Transform **II-333**

Kresimir Mihic, University of Zagreb, Croatia

Calculation of Dyadic Autocorrelation Through Decision Diagrams **II-337**

Radomir S. Stankovic, Dept. of Computer Science, Faculty of Electronics, University of Nis, Yugoslavia; *Mrinmoy Bhattacharaya*, *Jaakko Astola*, TICSP, Tampere University of Technology, Finland

Accelerated Analogue Fault Simulation by Concurrent Fault Detection **II-341**

Mustapha Dhifi, Institut of Electromagnetic Theory, Germany

New Reliability Indices for Multi-State System **II-345**

Elena Zaitseva, *Vitaly Levashenko*, Belarus State Economic Univ., Belarus

The Use of Correlation Technique Combined with $\Sigma\Delta$ -Modulation for Detection of Defective Sensor Elements **II-349**

Dirk Weiler, *Dirk Hammerschmidt*, *Niels Chritoffers*, *Bedrich J. Hosticka*, Fraunhofer IMS Duisburg, Germany

Friday, August 31



10:50 — 12:10

SESSION S16: ANALOG AND RF INTEGRATED CIRCUITS DESIGN
Session Room A

Integrated RF Front-End for WCDMA and GSM 900 **III-1**

Jussi Ryyänänen, *Kalle Kivekäs*, Helsinki University of Technology, ECDL, Finland; *Jari Heikkinen*, Nokia Networks, Finland; *Jarkko Jussila*, Helsinki University of Technology, ECDL, Finland; *Aarno Pärssinen*, Nokia Research Center, Finland; *Kari Halonen*, Helsinki University of Technology, ECDL, Finland

The Design of CMOS Cellular Transceiver Front-Ends **III-5**

Michiel Steyaert, *Bram de Muer*, *Johan Janssens*, *Marc Borremans*, *P. Leroux*, ESAT - MICAS K.U. Leuven, Belgium

An Integrated 110 MHz Bandpass Filter in Bipolar Technology **III-9**

Francesco Belfiore, STMicroelectronics, Italy; *Giuseppe Palmisano*, University of Catania, Italy

A CMOS 1.57 GHz Quadrature-VCO for a GPS Receiver Front-End **III-13**

Wouter De Cock, *Michiel Steyaert*, Katholieke Universiteit Leuven, Dept. ESAT-MICAS, Belgium

SESSION S17: APPLICATIONS OF CHAOS II
Session Room B

FM-DCSK Chaos Radio System **III-17**

Karol Krol, *Leonardo Azzinnari*, *Esa Korpela*, *Andras Mozsary*, *Mikko Talonen*, *Veikko Porra*, Helsinki University of Technology, ECDL, Finland

Mixed-Signal Map-Configurable IC Chaos Generator for Digital Communication Systems **III-21**

Manuel Delgado-Restituto, *Angel Rodriguez-Vazquez*, Instituto de Microelectronica de Sevilla, Spain

A Simple Digital FPGA Pseudo-Chaos Generator **III-25**

Leonardo Azzinnari, *Andras Mozsary*, *Karol Krol*, *Esa Korpela*, *Veikko Porra*, Helsinki University of Technology/ECDL, Finland

SESSION S18: RECENT TRENDS IN INTERCONNECTS MODELING AND SIMULATION
Session Room C

Asymptotic Equivalent Circuits of Interconnects Based on Complex Frequency Method **III-29**

Akio Ushida, Tokushima University, Japan; *Kouji Urabe*, Niihama National Technical College, Japan; *Yoshihiro Yamagami*, *Yoshifumi Nishio*, Tokushima University, Japan

Pspice Subcircuits for Passive Reduced Order Interconnect Models **III-33**

Murat Dinç, Istanbul Technical University, Turkey; *Izzet Cem Göknaar*, Dogus University, Turkey

Passive Time-Domain Model Order Reduction via Orthonormal Basis Functions **III-37**

Qingjian Yu, *Ernest S. Kuh*, University of California at Berkeley, USA

Passive Macromodels for Distributed High Speed Interconnects **III-41**

Anestis Dounavis, *Ramachandra Achar*, *Michel Nakhla*, Carleton University, Canada

SESSION S19: APPLICATIONS OF GABOR FILTERS AND TRANSFORMS IN IMAGE PROCESSING
Session Room D

Competitive Orientation Selective Arrays III-45
Bertram Shi, EEE/HKUST, Hong Kong;
Kwabena Boahen, UPenn Bioengineering, USA

Optimization of Gabor Filter Parameters for Pattern Recognition III-49
Shunji Uchimura, *Yoshihiko Hamamoto*, Yamaguchi University, Japan

Handwritten Character Recognition Using CNN Gabor-Type Filters III-53
Ertugrul Saatci, *Vedat Tavsanoglu*, South Bank University, UK

Multindow Gabor-Type Schemes and Their Application Late
Yehoshua Zeevi, Israel Institute of Technology, Israel

SESSION R15: ANALYSIS AND DESIGN TOOLS II
Session Room E

Mixed-Mode Simulation in APLAC III-57
Sami Marjoniemi, APLAC Solutions co., Finland; *Antti Kallio*, *Tuomo Kujanpää*, Helsinki University of Technology, Finland

Model Parameter Identification with Spice Opus: a Comparison Of Direct Search and Elitistic Genetic Algorithm III-61
Arpad Buermen, *Janez Puhon*, *Tadej Tuma*, *Iztok Fajfar*, *Andrej Nusssdorfer*, University of Ljubljana, Slovenia

Simulation of the Coupling of an External Electromagnetic Field to the PCB Traces in Spice Simulator III-65
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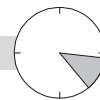
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Daniel Foty, David Binkley, Gilgamesh Associates, USA

T2: Phase Locked Loops in Communications

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Emanuel Gluskin, Ben-Gurion Univ., Israel

T4: Network Calculus: a System Theory for Communication Networks

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T5: Design Principles for Chaotic Oscillators

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Martinez Peiro, M.
Mastronardi, N.
Matei, R.
Matsueda, H.
Matsumoto, T.
Matsumoto, N.
Mawet, P.
McCarthy, K.
Mecklenbräuker, W.
Menegaz, G.
Mijail, A.
Milic, L.
Min, M.
Miyazaki, A.
Moonen, M.
Moschytz, G.
Mosin, S.
Mucha, I.
Männamaa, V.
Nagel, J.
Najim, M.
Nauta, B.
Ndagijimana, F.
Neikirk, D.
Neitola, M.
Ng, T.
Nguyen, T.
Nielsen, J.
Niemelä, I.
Niiranen, J.
Nikias, M.
Nishio, Y.
Njølsten, T.
Nouta, R.
Nunnari, G.
Nys, O.
Occhipinti, L.
O'Connor, I.
Ogrodzki, J.
Okumura, K.
Paasio, A.
Pahlke, K.
Pajunen, P.
Palumbo, G.
Pasero, E.
Pecora, L.
Perfetti, R.
Perri, A.
Piguet, C.
Pileggi, L.
Piller, B.
Plana, R.
Porod, W.
Prince, J.
Proakis, J.
Pyrhönen, J.
Rabaey, J.
Radvanyi, A.
Raik, J.
Raivio, K.
Ramirez-Angulo, J.
Ramstad, T.
Ravasi, M.
Reibiger, A.
Reich, S.
Reichel, J.
Reiszig, G.
Renfors, M.
Reyneri, L.
Rintamäki, M.
Rizzo, A.
Rochelle, J.
Rodanski, B.
Roermund, A.
Ronkainen, H.
Rovatti, R.
Rubio, A.
Ruck, B.
Rudberg, M.
Rüstern, E.
Salinari, S.
Salo, T.
Sandler, M.
Sargeni, F.
Sasada, I.
Sasao, T.
Savaci, A.
Sayed, A.
Scherpen, J.
Schimming, T.
Schindler, T.
Schmelcher, P.
Schmid, H.
Schreier, R.
Sekerikiran, B.
Setti, G.
Shah, P.
Shi, B.
Shi, R.
Shi, X.
Shi, C.
Sicard, E.
Silva-Martinez, J.
Silvén, O.
Skyttä, J.
Slump, C.
Sodini, C.
Sommariva, A.
Sommen, P.
Sommer, R.
Stadius, K.
Stankovic, R.
Stankovic, M.
Stasinski, R.
Steeb, W.
Steer, M.
Steyaert, M.
Stievano, I.
Storti Gaiani, G.
Straube, B.
Streitenberger, M.
Strzeszewski, B.
Sumanen, L.
Sundstrom, L.
Suntio, T.
Suszynski, Z.
Suykens, J.
Szatmari, I.
Szekely, V.
Szeto, A.
Sziranyi, T.
Szolgay, P.
Särelä, J.
Tabus, I.
Takagi, S.
Takagi, N.
Takahashi, N.
Takala, J.
Takebe, T.
Tamasevicius, A.
Tanner, S.
Tanskanen, J.
Taraglio, S.
Tchamov, N.
Tenhunen, H.
Tetzlaff, R.
Thao, N.
Thevenaz, P.
Thiele, L.
Tiiliharju, E.
Tiilikainen, M.
Tilmans, H.
Tong, L.
Toth, L.
Trajkovic, L.
Tse, M.
Tsimring, L.
Tufan, E.
Tuikkanen, T.
Tuomainen, V.
Ueda, Y.
Uster, M.
v.d. Vyver, J.
Vainio, O.
Wallinheimo, J.
Wallius, J.
Waltari, M.
Wambacq, P.
van der Kloet, P.
van der Meijs, N.
van der Meulen, E.
van der Schaft, A.
van der Veen, A.
van Staveren, A.
Vandenbergh, L.
Vandermeulen, E.
Watanabe, H.
Verhaegen, W.
Verleysen, M.
Werner, S.
Werner, R.
Vesanto, J.
Vesma, J.
Veszely, G.
Vidkjaer, J.
Wiehler, K.
Viitanen, T.
Viitanen, A.
Willson, A.
Wolf, W.
Vuolevi, J.
Vuori, J.
Välimäki, V.
Xibilia, M.
Yakovlev, A.
Yalcin, M.
Yang, W.
Yao, K.
Yli-Harja, O.
Yoshida, N.
Yoshifumi, N.
Yufera, A.
Zagurski, V.
Zhakor, A.
Zielinski, T.
Ziolko, M.
Zirath, H.
Zuberek, W.
Åberg, M.
Öktem, H.

ECCTD'01 Program Schedule

Day	Time	Room A	Room B	Room C	Room D	Room E	Y228	Y307	Y227	Posters	
T U E S D A Y	9:00 – 10:30	T1 MOS	T2 PLL		DAD						
	10:30 – 10:50	COFFEE BREAK									
	10:50 – 12:20	T1 MOS – contin.	T3 Grid		DAD						
	12:20 – 13:40	LUNCH									
	13:40 – 15:10	T4 Calculus	T5 Chaos I		DAD						
	15:10 – 15:30	COFFEE BREAK									
	15:30 – 17:00	T6 Genetic	T7 Chaos II	T8 CAD							
18:00 – 20:00	GET - TOGETHER HUT Main Lobby										
W E D N E S D A Y	8:50 – 9:00	OPENING SESSION, Room B									
	9:00 – 9:45	Plenary 1, Room B: <i>Self-Organizing Networks</i> , Teuvo Kohonen, Helsinki University of Technology									
	9:45 – 10:30	Plenary 2, Room B: <i>Digital Signal Processing: Road to the Future</i> , Sanjit Mitra, UC Santa Barbara									
	10:30 – 10:50	COFFEE BREAK									
	10:50 – 12:10	S1 Circuit Paradigm in Nanoelectronics I	S2 Applications of Symbolic Analysis	S3 Independent Component Analysis (ICA)	R1 Digital Filters I	R2 Simulation and Modelling I	R3 MOSFET Circuit Modelling	R4 CNN Applications		PS1 Mixed-Mode IC's. Filters.	
	12:10 – 13:40	LUNCH									
	13:40 – 15:10	Plenary 3, room B: <i>Molecular Devices and Circuits</i> , Leon Chua, UC Berkeley									
	15:10 – 15:30	COFFEE BREAK									
15:30 – 16:50	S4 Circuit Paradigm in Nanoelectronics II	S5 Techniques for Symbolic Analysis	S6 Bio-Inspired Novel Circuit Applications	R5 Digital Filters II	R6 Fault Analysis of Analogue Circuits	R7 Switched-Capacitor Circuits	R8 Frequency Synthesis		PS2 RF. Power. Σ - Δ applicat. LP Design		
19:00 – ...	ESPOO CITY RECEPTION, Buses to Espoo Cultural Centre leave at 18:30										
T H U R S D A Y	9:00 – 9:45	Plenary 4, Room B: <i>Belevitch Lecture</i> , J.O. Scanlan, University College Dublin									
	9:45 – 10:30	Plenary 5, Room B: <i>The Complexity of Analogic Computations</i> , Tamas Roska, Hungarian Academy of Sciences									
	10:30 – 10:50	COFFEE BREAK									
	10:50 – 12:10	S7 Speech and Audio Processing	S8 Analogic Wave Algorithms	S9 Memory Effects in RF PA's	S10 LP CMOS Camera Circuits	R9 Simulation and Modelling II	R10 Low-Voltage Analogue IC's	R11 Modelling of Chaotic Circuits		PS3 Design Tools. Modelling	
	12:10 – 13:40	LUNCH									
	13:40 – 14:25	Plenary 6, Room B: <i>Technologies, Architectures, CAD and Application of Complex Systems-on-Chip (SoC)</i> Manfred Glesner, Technical University Darmstadt									
	14:25 – 15:10	Plenary 7, Room B: <i>Circuit Theory for Computations</i> , Patrick Dewilde, Delft University of Technology									
	15:10 – 15:30	COFFEE BREAK									
15:30 – 16:50	S11 Nonlinear Communication Circuits (NCCS)	S12 Applications of Chaos I	S13 Numerical Analysis of Nonlinear ckts	S14 Optimisation of Digital Filters	R12 Analysis and Design Tools I	R13 Digital Systems	R14 CNN Circuit Design	S15 SoC	PS4 Signal Processing, Fault Detect.		
19:00 – ...	BANQUET, Buses to Casino Kulosaari Restaurant leave at 18:15										
F R I D A Y	9:00 – 9:45	Plenary 8, Room B: <i>Network Synthesis in Mobile Communications</i> , David Rhodes, Filtronic plc									
	9:45 – 10:30	Plenary 9, Room B: <i>Wave-Digital Approach to Numerical Integration of Electromagnetic PDEs</i> , Alfred Fettweis, Ruhr-Universität Bochum									
	10:30 – 10:50	COFFEE BREAK									
	10:50 – 12:10	S16 Analogue and RF Integrated Circuits Design	S17 Applications of Chaos II	S18 Interconnect Modeling / Simulation	S19 Gabor Filters in Image Proc.	R15 Analysis and Design Tools II	R16 Image Signal Processing	R17 CNN Analysis/Modelling		PS5 Circuit and System Theory.	
	12:10 – 13:40	LUNCH									
	13:40 – 15:00	S20 Electronics and Optics for Multigigabit C.	S21 Design and Testing of Digital Syst.	S22 Interconnect Chip/Packaging Design	R18 Nonlinear Circuit Dynamics	R19 Communication Systems	R20 RF & μ wave Communication Circuits	R21 Circuit Theory		PS6 CNN's. Neural Net's Mixed Design	
15:00 – 15:20	COFFEE BREAK										
15:20 – 16:40	R22 Low-Power Integrated Circuits	R23 Adaptive Signal Processing	R24 A/D and D/A Converters	R25 Microelectromechanical Systems	R26 Simulation and Modeling III	R27 Neural Networks	R28 Applications of Chaotic Circuits				