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Concurrent Reliability Testing as an Alternative for More Comprehensive and Efficient Reliability Testing of Electronic Assemblies

Master's thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Technology in the Degree Programme in Engineering Physics.

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Aalto University School of Science and Technology Faculty of Information and Natural Sciences	ABSTRACT OF THE MASTER'S THESIS
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Abstract: Traditionally the reliability and lifetime predictions of electronic assemblies have been conducted by employing single load accelerated life tests. This thesis aimed to develop a new concurrent reliability testing method that would offer a more realistic representation of actual use environments. Additionally, the combination of several loadings is expected to accelerate the damage accumulation, thus decreasing the associated testing times and costs. The focus was on the combination of thermomechanical and mechanical loads.

Accelerated life tests were analyzed in the literature part. The relevant conventional accelerated life tests utilizing a single loading parameter were discussed before addressing multiple loading tests by giving a literature review on the current status of the subject.

The experimental part combined power cycling and vibration loading into a single concurrent test method. To determine the actual test parameters and to clarify the failure modes and mechanisms in concurrent loading, single loading tests were conducted before the loads were combined. The experimental results were consistent with the previous results reported in literature with observed lifetimes considerably shorter than expected based on the single load test results. Observed failure modes in concurrent testing closely resembled those observed in pure mechanical loading, but the accelerated damage accumulation rate was attributed to the temperature related change of material properties.

It was concluded that when the loading parameters are carefully set, significant improvements in both the lifelikeness of the loading conditions and in effectiveness can be achieved with the new test method. The results indicated that even under relatively small magnitude single loads the interactions of the various loadings can have significant effects on reliability that cannot be accounted for with single load tests.

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Tiivistelmä: Perinteisesti elektroniikan kokoonpanojen luotettavuutta on testattu kiihdytetyillä elinaikatesteillä yhtä rasitusparametriä hyväksikäyttäen. Tässä diplomityössä pyrittiin kehittämään uusi rinnakkainen yhdistelmätestausmenetelmä, joka simuloisi tuotteiden todellisia käyttöolosuhteita todenmukaisemmin. Rasituksien yhdistämisen uskotaan myös nopeuttavan vauriomekanismejä ja täten lyhentävän testaukseen käytettyä aikaa. Työ keskittyi termomekaanisten ja mekaanisten rasitusten yhdistämiseen.

Työn kirjallisuusosa käsitteli kiihdytettyjä elinaikatestejä. Oleelliset yhden rasituksen testimenetelmät käytiin läpi ennen syventymistä useita rasitusparametrejä hyödyntäviin testeihin kirjallisuusselvityksen avulla.

Työn kokeellisessa osassa yhdistettiin tehosyklaus ja tärinätestaus yhdeksi testimenetelmäksi. Ennen rasitusten yhdistämistä suoritettiin yhden rasitusparametrin tehosykli- ja tärinätestit varsinaisten testiparametrien määrittämiseksi ja rinnakkaistestauksen vikaantumismekanismien selvittämiseksi. Tulokset olivat yhtäpitäviä aikaisempien asiasta suoritettujen tutkimusten kanssa, elinaikojen yhdistelmätestauksessa ollessa huomattavasti lyhyempiä kuin oli oletettu erillisten yhden rasitusparametrin testien tulosten perusteella. Yhdistelmätestauksessa havaitut vikaantumismoodit olivat hyvin samankaltaisia tärinätesteissä havaittujen moodien kanssa ja vaurioitumisnopeuden kasvun oletettiin johtuvan juoteliitoksien lämpötilasta aiheutuvien mekaanisten ominaisuuksien muutoksista.

Tulokset osoittivat, että testiparametrien huolellisella valinnalla voidaan uudella menetelmällä saavuttaa todellisia käyttöympäristöjä todenmukaisemmin edustava rasitusympäristö sekä lyhentää testiaikoja merkittävästi. On myös huomioitava, että yksittäin lähes merkitysettömillä rasituksilla saattaa olla merkittäviä yhteisvaikutuksia luotettavuuteen, joita ei voida huomioida perinteisillä yhden rasituksen testeillä.

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Preface

This thesis was carried out in the Department of Electronics at Aalto University School of Science and Technology as a part of a research project called Development of A Novel Reliability Testing Method of Consumer Electronics.

After finishing this thesis, I feel indebted to many people who have contributed to this project. I would like to thank all of you, albeit I can name here only a few.

First of all I would like to express my grattitude to professors Paulasto-Kröckel and Sepponen for providing the opportunity to undertake my Master's Thesis on this interesting topic. I would also like to thank my supervisor, Toni Mattila, for his advices and guidance during this thesis. Furthermore, I would like to express my sincere thanks to Juha Karppinen for his valuable insights and help related to this thesis.

I would like to thank all the people in the Electronics Integration and Reliability research unit for making my working experience enjoyable and for the inspiring and supporting atmosphere. Special thanks go to the technical support staff (Pirjo Kontio, Kimmo Rajala and Heikki Ruotoistenmäki) and secretary Pia Holmberg for their help with the countless practicall issues.

I would also like to express my sincere thanks to my parents, Lauri and Marja-Leena, and sisters, Taru and Mirva, for their patience and support during my studies. All of my friends also deserve a warm thank you for all the shared moments. Finally, my most sincere compliments go to Katja for her constant encouragement and support during the course of this work; you are my light at the end of the tunnel.

Espoo, 20.04.2010

Juha Tuomas Toivonen

Contents

Symbols and Abbreviations

Symbols

α	temperature coefficient of resistance [1/°C]
β	shape parameter of the Weibull distribution
η	scale parameter of the Weibull distribution
f	frequency
G	standard acceleration due to gravity ≈ 9.81 [m/s^2]
G_{rms}	root mean square average of the acceleration interval
γ	location parameter of the Weibull distribution
i_D	drain to source current
k	Boltzmann constant $\approx 1.380 \times 10^{-23}$ [J/°K]
σ	standard deviation
T	temperature
V_{th}	threshold voltage of a transistor
V_{DS}	voltage between the drain and source terminals
V_{GS}	voltage between the gate and source terminals

Abbreviations

ALT	Accelerated Life Test
ATC	Accelerated Thermal Cycle
BGA	Ball Grid Array
CCGA	Ceramic Column Grid Array
CDI	Cumulative Damage Index
CTE	Coefficient of Thermal Expansion
DFT	Discrete Fourier Transform
DL	Destruction Limit
EIR	Electronics Integration and Reliability research unit
ESS	Environmental Stress Screening
FEA	Finite Element Analysis
ENIG	Electroless Nickel (phosphorus)/Immersion Gold
HALT	Highly Accelerated Life Test
HASA	Highly Accelerated Stress Audit
HASS	Highly Accelerated Stress Screen
HAST	Highly Accelerated Stress Test
I/O	Input/Output
IC	Integrated Circuit
IDSA	Incremental Damage Superpostion Approach
IEC	International Electrotechnical Commision
ISO	International Organization for Standardization
JEDEC	Joint Electron Device Engineering Council
LDSA	Linear Damage Superposition Approach
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NI	National Instruments
NTF	No Trouble Found
OL	Operating Limit
OSP	Organic Solder Preservative
ppm	parts per million
PDF	Probability Density Function
PWB	Printed Wiring Board
RCA	Root Cause Analysis
SMT	Surface Mount Technology
STRIFE	Stress + Life
THB	Temperature, Humidity and Bias test
UBM	Under Bump Metallization

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Chapter 1

Introduction

Manufacturers and designers of electronic products are constantly facing new challenges while trying to cope with consumers and markets' continuous demands of new features and improved performance in a smaller size. The component sizes, I/O (input/output) pitches and line widths of the printed wiring boards (PWB) have been decreasing rapidly and the increasing packaging density is causing manufacturing and reliability challenges.

Higher operating speeds require shorter interconnection distances to minimize propagation delays. As the components are becoming smaller while the number of electric contacts is simultaneously increasing the size of electrical interconnections is decreasing. As a consequence, the components are brought even closer to the PWB with smaller interconnections, adding to the stresses and strains of the interconnections. Simultaneously the smaller and more versatile components increase current densities and the number of I/Os, while the enhanced performance creates thermal challenges due to the increased power densities.

It is a generally recognized fact that the reliability of electronics is to a large extent determined by the ability of electrical interconnections to withstand various loadings during products' operational lifetime. Reliability testing is needed to provide assurance that designs and products are reliable and durable in service, and due to modern day's tight time-to-market requirements and shortening product cycles, should be conducted in a timely fashion. The reliability testing of the interconnections has been traditionally carried out with accelerated reliability tests, where the test units are used more frequently than usual or are subjected to higher than usual levels of accelerating variables like temperature or voltage. These tests can be grouped under two categories, single load tests, where only one loading type is used, and multiple loading tests, where two or more different loading types are used. Today, the vast majority of accelerated tests are still conducted as single load tests, mainly because of simplicity and because the interaction effects of various combined loads are still not known or understood.

There are, however, various potential advantages in multiple loading tests. Most modern products are designed to operate without failure for years and it has become more difficult, even with an accelerated single load test, to obtain a sufficient amount of failure data within a reasonable amount of time. Multiple loading tests have

recently been employed as a means of overcoming such difficulties. Multiple loading tests can also offer a much better representation of the actual use-environment strains and stresses, since the components in actual products are rarely exposed to a single type of strain or stress.

This thesis focuses on multiple loading tests and, more specifically, on the combination of mechanical and thermomechanical loads. The theory part of the thesis gives a review on the current status of the subject, while the experimental part attempts to combine two separate loads (namely vibration and power cycling) into a single, more comprehensive and efficient concurrent reliability testing method.

Chapter 2

Reliability of Electronics

This chapter gives a brief overview on the history of reliability engineering as an introduction in section 2.1. The reasons for reliability engineering are established in section 2.2 before some basic concepts relating to reliability are defined and discussed in the final part (section 2.3) of the chapter.

2.1 History of Reliability Engineering

Reliability engineering emerged as a separate engineering discipline during the 1950s but traces its roots to the Second World War. At the onset of the war, the essential ingredients of reliability engineering, statistics (theory of sampling) and mass production were well established and reliability engineering was ripe to emerge. Electronics played a critical role in the war but the increasing complexity of military electronic systems was generating failure rates which originated in greatly reduced availability and increased costs. During the war, the availability of American naval and army electronic equipment was approximately 70% and less than 40% respectively, while over 60% of airborne equipment shipped to the Far East arrived damaged [DN02].

During the 1950s the gathering pace of electronic device technology meant that especially the developers of new military systems were making increasing use of large numbers of new component types and involving new manufacturing processes, with the inevitable consequences of low reliability. The increasing complexity of military electronic systems was generating intolerable failure rates and greatly influenced on the emergence of reliability engineering. As a consequence, several methods (such as the identification of root cause of field failure and determination of mitigating actions or the specification of quantitative reliability requirements) to achieve higher reliability were developed. A permanent committee (the Advisory Group on Reliability of Electronic Equipment, AGREE) was established to guide the emerging reliability discipline and the birth date of reliability engineering is often coincided with the committees foundational report, published in 1957, that provided assurance that reliability could be specified, allocated and demonstrated. [SM06]

The most widely known and used reliability prediction handbook, MIL-HDBK-217, was first published in 1961. Although originally developed for military and

aerospace applications, it became widely used for industrial and commercial electronic equipment applications throughout the world. The most recent revision, "Military Handbook, Reliability Prediction of Electronic Equipment", MIL-HDBK-217, Revision F, Notice 2, was released in February of 1995. The MIL-217 is an influential military standard by which reliability predictions are still performed.

The reliability development in the western world was driven to a large extent by the customers and particularly by the US military. In order to improve reliability, several standards and procedures were set up, whilst the suppliers saw little motivation to improve, since they were paid for spares and repairs. By contrast, the Japanese had a different view on improving reliability. Guided by the doctrines of the late W. Edwards Deming, the Japanese industry had learned the fundamental connections between quality, productivity and competitiveness and their basic philosophy was that quality provided the key to greatly increased productivity and competitiveness. [O'C94]

The inductive western approach on reliability leads to inventions, breakthroughs and to greater reliance on systems for control of people and processes as opposed to the more deductive approach applied by the Japanese. The effectiveness of the deductive approach was shown in the way that many products, such as Japanese cars, machine tools or consumer electronic products won dominant positions in world markets in the last 40 to 50 years. The deductive approach seeks to generate continuous improvements across a broad front, and new ideas are subjected to careful evaluation. Furthermore, it allows a clearer view, particularly in discriminating between sense and nonsense, but it is not conducive to the development of radical new ideas. Obviously these two philosophies are not exclusive, and elements of both can be seen in modern reliability engineering.

2.2 Why Is Reliability Important?

Today the reliability of electronics is an important factor of success in the highly competitive global markets. The modern consumer will not tolerate products that do not perform in a reliable fashion, or as promised or advertised and if the manufacturer does not design its products with reliability and quality in mind, someone else certainly will. In addition, customer dissatisfaction with a product's reliability can have disastrous financial consequences to the manufacturer. A company's reputation is very closely related to the reliability of their products and while it takes a long time to build up a reputation for reliability, only one malfunctioning product can brand the whole company as unreliable. Furthermore, if a product fails to perform its function within the warranty period, in addition to the unwanted attention the replacement and repair costs can be substantial. Thus it is of utmost importance that a manufacturer knows the reliability of its product and continual assessment of new product reliability and ongoing control of the reliability of everything shipped are critical necessities in today's competitive business arena.

Besides financial issues, reliability can be of paramount importance in some application areas. In today's technological world we depend upon the continued func-

tioning of a wide array of complex equipment and machinery. Constantly more and more important operations are performed with automated equipment, whose failures have varying effects from minor nuisances to catastrophic results. It is clear that in critical fields and key applications, such as medical devices or avionic electronics, where failures can lead to life threatening situations, reliability should be of highest priority to avoid the catastrophic consequences of failure.

2.3 Basic Reliability Concepts

This section introduces, defines and briefly discusses some basic concepts related to reliability.

Reliability

An illustrative description of the meaning of reliability today is ([Suh02], originally cited by an unknown reliability engineer): "Reliability—it is when the customer comes back not the product". More formally reliability is commonly defined as the ability of a product or a component to operate without failure under a set of predetermined conditions over a specified period of time [MIL81]. The definition contains several key requirements: functions of the products, their normal operation and stated operating conditions as well as anticipated lifetime expectations must be specified. Predetermining these conditions makes the designing easier and the reliability considerations are much easier to implement.

Quality

Reliability should not be confused with quality or quality control since the two concepts are quite different. Reliability grew out of the need for a time-based concept of quality and it is the distinction of time that marks the difference between the traditional quality control and the modern approach to reliability. International Organization for Standardization (ISO) defines quality as "the totality of features or characteristics of a product or service that bear on its ability to satisfy stated or implied needs" [ISO94]. The definition of quality refers to this totality at a particular instant of time, whereas reliability deals with the behavior of failure rate over a long period of performance. For a detailed discussion on the differences of quality and reliability the reader is referred to chapter 1.10 of [Kec91].

Failure

Failure is an important concept in reliability, since the measure of reliability is the infrequency in which failures occur in time. Especially for all life tests, some time-to-failure information for the product is required since the failure of a product is the event we want to understand. Failure is generally defined as "the non-performance or inability of a component or system to perform its intended function for a specified

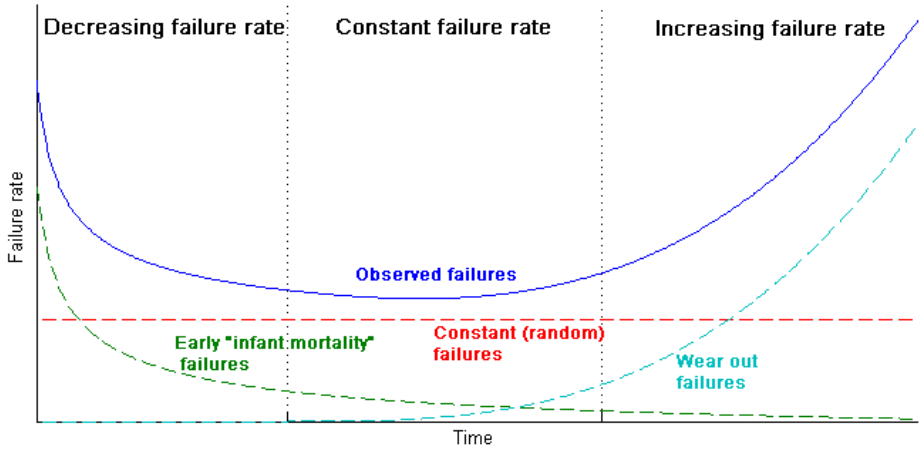


Figure 2.1: *The bathtub curve: hypothetical failure rate versus time. The product's life cycle can be divided into three distinct periods based on the dominant failure mode. The green, red and cyan curves represent the infant mortality, constant and wearout failures respectively, while the blue curve is a combined representation of the three individual failure rates.*

time under specified environmental conditions" [Fri06]. Once again, the intended function of the device and its operating conditions need to be specified.

Bathtub Curve

The so called bathtub curve (presented in Figure 2.1) is typically used to illustrate reliability over time and the three principal periods of product failure. The curve does not depict the failure rate of a single item, but describes the relative failure rate of an entire population of products over time. Although it is rare to have enough short- and long-term failure information to actually model a population of products with a calibrated bathtub curve, the curve is nonetheless a widely used concept in the industry.

The curve consists of the following three periods:

- **Infant mortality period** is characterized by a decreasing failure rate. These infant mortality failures are highly undesirable and are caused by defects and blunders.
- A constant and relatively low failure rate is a characteristic feature of the **normal-life period** (also known as "useful life"). The failures during this period are considered as random cases of stresses and strains exceeding the product strength.
- **Wear-out period** exhibits an increasing failure rate due to the fatigue or depletion of materials.

Weibull distribution

The versatile Weibull distribution is often used in reliability engineering and life-time data analysis. Depending on the values of the parameters, it can be used to represent many different time-to-failure characteristics and be made to fit many life distributions. However, the physical phenomena causing the failure must be clearly understood prior to using the distribution. The probability density function (PDF) of a three parameter Weibull random variable x is

$$f(x;\beta,\eta,\gamma) = \begin{cases} \frac{\beta}{\eta}\left(\frac{x-\gamma}{\eta}\right)^{\beta-1}\exp\left(-\left[\frac{x-\gamma}{\eta}\right]^{\beta}\right) & \text{x}\geq\gamma \\ 0 & \text{x}<\gamma \end{cases}, \tag{2.1}$$

where $\beta > 0$ is the shape parameter, $\eta > 0$ is the scale parameter and $\gamma \in]-\infty,\infty[$ is the location parameter. In reliability engineering the Weibull distribution is commonly used to model a variety of life behaviors with respect to time, and time to failure (t) is typically used as the random variable. The location parameter is only introduced if the data plots with a concave or convex trend and the fit of regression is therefore poor. Otherwise γ equals zero, and we speak of the two-parameter Weibull distribution. A change in the scale parameter has the same effect on the distribution as a change of the abscissa scale. Increasing the value of η stretches out the PDF while a decrease pushes the distribution towards the left. The scale parameter has the same unit as the random variable x. The dimensionless shape parameter, β, is also known as the slope, because the value of β is equal to the slope of the regressed line in a probability plot. Different values of the parameter can have marked effects on the behavior of the distribution, *e.g.* when $\beta = 1$, the PDF of the three-parameter Weibull reduces to two-parameter exponential distribution. [Rel02]

The PDF can be used to derive commonly used probability metrics such as the reliability function, cumulative probability function, failure rate, mean and median. The cumulative probability function is (with t used as the random variable)

$$F(t;\beta,\eta,\gamma) = 1 - \exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right] \tag{2.2}$$

and the failure rate (also referred as the hazard rate) is given by

$$h(t;\beta,\eta,\gamma) = \frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1}. \tag{2.3}$$

The two-parameter ($\gamma = 0$) Weibull PDF and the effect of the shape (β) and slope (η) parameters are illustrated graphically in Figure 2.2. The value of β has a marked effect on the failure rate of the Weibull distribution, and conclusions can be drawn about a population's failure characteristics just by considering the value of β. When $\beta < 1$ the failure rate decreases with time, when β equals one the failure rate is constant and when it is greater than one, the failure rate increases with time.

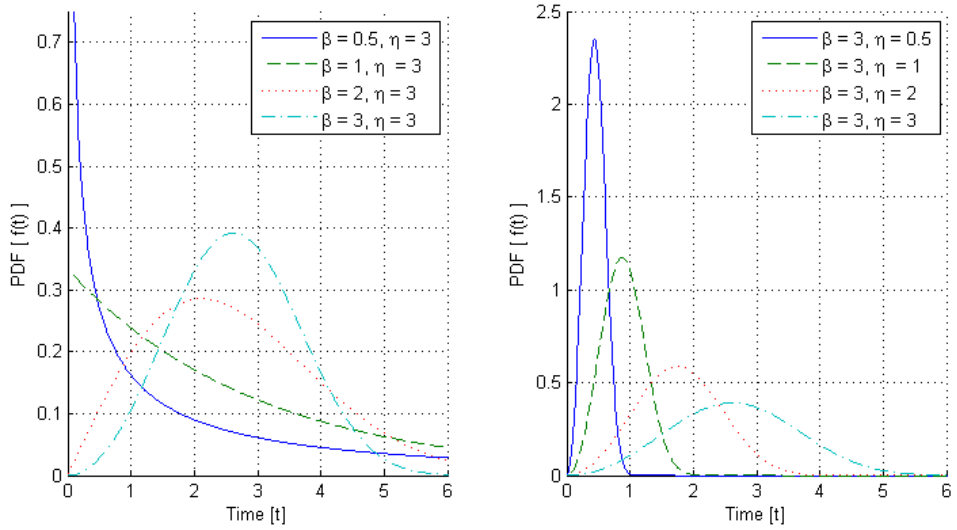


Figure 2.2: *The effect of varying shape parameter (β, on the left graph) and slope parameter (η, on the right graph) on the PDF of 2-parameter Weibull distribution.*

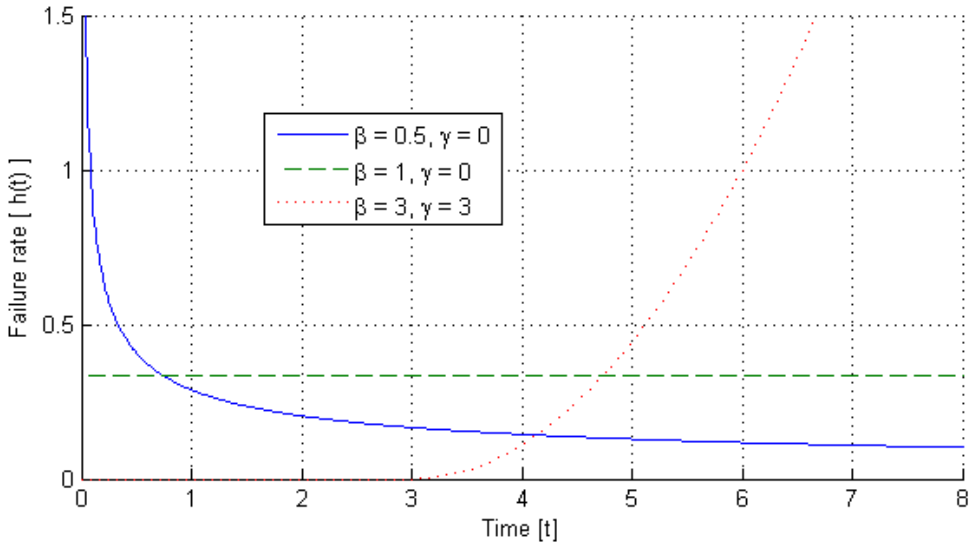


Figure 2.3: *The effect of shape parameter β and location parameter γ on the Weibull failure rate function. The slope parameter is kept constant (η=3).*

All three life-stages of the bathtub curve can thus be modeled with the Weibull distribution by varying the value of β. This is shown graphically in Figure 2.3.

Chapter 3

Reliability Testing

For all the aforementioned reasons, it is necessary for the manufacturer to have a clear understanding of its products expected lifetime and reliability. Reliability testing is needed to provide assurance that designs and products are reliable in service. Due to the long life times of today's products and the small time period between design and release, changes in current technologies can be such that some products (for example computer memory chips) may become obsolete before they are proven reliable. Therefore testing at 'representative' stresses in the hope that failures will not occur is very expensive, time consuming and a waste of resources.

The industry features a wide variety of methods to provide different information about the product and its failure mechanisms in a timely fashion. Different methods serve different purposes, and confusion surrounds the nomenclature as various test methods have multiple names and acronyms and, depending on the author, can have different definitions. Generally speaking these reliability testing methods can be divided into three categories: reliability verification tests, screening tests and accelerated lifetime tests. To avoid further confusion, the following three sections describe and distinguish the differences between the three test types.

3.1 Reliability Verification Tests

Reliability verification tests have various names, such as elephant tests, torture tests, qualitative tests or shake & bake tests and are primarily used to reveal probable failure modes and weaknesses in the least amount of time. A good reliability verification test quickly reveals the failure modes that will occur during the life of the product under normal use conditions. The tests are typically employed at the product's design phase with a small number of samples exposed to a single or to a number of severe loads until failure. Appropriate actions will be taken to improve the product's design and to eliminate the causes of failure, thus pushing the bottom of the bathtub curve down and the wear-out period as far to the right as possible. However, if not designed properly, reliability verification tests may cause products to fail by modes that would have never been encountered in actual use conditions.

The most commonly used reliability verification test philosophy is HALT (Highly Accelerated Lifetime Test), developed by Gregg K. Hobbs. The basic philosophy of

HALT has been used since 1969 on many products from various fields. It can be used for entire systems but can be performed on individual assemblies as well. Contrary to its name, HALT is not a lifetime test: it is not intended to estimate lifetimes or mean times to failure, but rather to find the weakest locations on the product with supreme time compression. In HALT the loadings are stepped up to well beyond the expected field environments of the test specimen. The loadings are not meant to stimulate the field environments at all but to find the weak links in the design in a very short timescale. Flaws and weaknesses are eliminated until the fundamental limit of technology is reached, but only those failures that are likely to occur in normal field conditions are addressed. The relevant flaws and weaknesses should be eliminated without unduly spending resources and not to overdo the process by making the product more robust than necessary and thus spending unnecessary money in the process. One should also note that in HALT weaknesses can be exposed with a different stress or strain than the one that would make the weakness show up in the field and therefore the focus should be on the failure mode and mechanisms instead of the margin for the particular stress in use. [Hob00]

There is no general HALT profile or procedure, since all the limits and used loadings are application specific. Only the HALT philosophy, to stimulate failures by any means necessary, is generic. However, there are six steps in HALT, five of which need to be covered in order for the method to function at all and long-term improvements can be gained by adding the sixth step. In sequential order the steps are: precipitation, detection, failure analysis, corrective action, verification of corrective action and documentation of knowledge gained.

HALT is a design aid tool and can be efficiently used, for example, to compare different designs (as early in the development cycle as possible) or to compare different components from various vendors. By enhancing reliability with supreme time compression a successful implementation of HALT promises significant return of investments that are extremely difficult to accomplish in any other way. The HALT philosophy is widely used in the industry, but most of the users are not publishing their results because they are unwilling to give away valuable technical advantages and knowledge gained in the process. The HALT approach is further discussed in section 5.1, where its applicability on the useful product life characterization is investigated and a detailed example of a typical HALT process is given in subsection 5.1.1.

Other reliability verification test methods include STRIFE (stress + life) and HAST, highly accelerated stress test. STRIFE, as used by Hewlett-Packard, is a subset of HALT while HAST is basically an accelerated version of THB (temperature, humidity, bias) test. HAST utilizes high pressure, high temperature and high humidity. Humidity is increased without formation of water droplets by utilizing pressure above atmospheric. HAST is recommended for the qualification of any change that can potentially affect the corrosion resistance of the product and for changes in the die glassivation, metallization or thin film resistors, as well as changes in the molding compound.

While reliability verification tests are generally designed to reveal failure modes and to provide information on how to make products more robust, they can also be

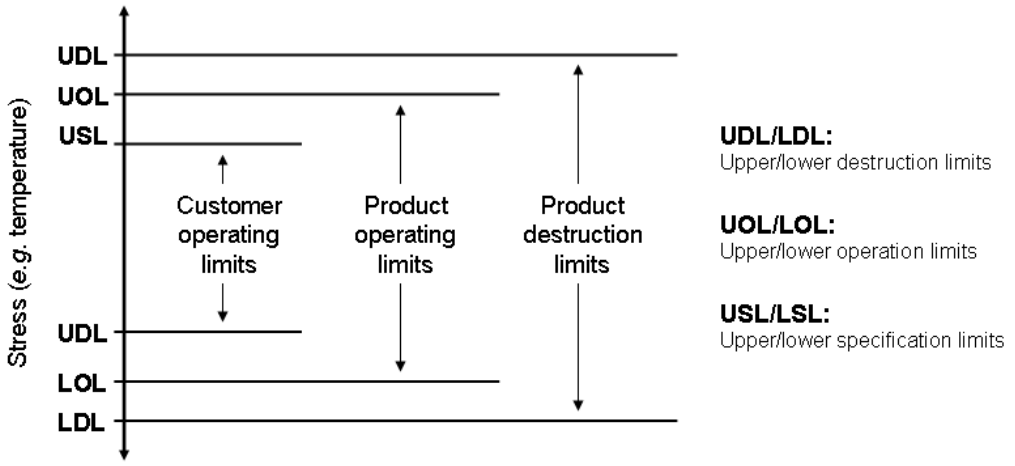


Figure 3.1: *Stress levels and the specification, operation and destruction limits.*

used to characterize products under test and to identify products specification, operation and endurance limits. The upper and lower specification limits are defined as the limiting stress levels or dimensions or other variables to which the manufacturer guarantees the operation of the product in question. The upper and lower operation limits indicate the stress levels in which the product ceases to function. However, if upper or lower destruction levels are not reached, the product can be restored to normal operation by decreasing the stress level to the specification limits. The upper and lower destruction limits (also referred as endurance limits) indicate the stress levels at which the product fails catastrophically and cannot be restored. These limits are illustrated graphically in Figure 3.1. This data can in turn be used as a basis for the design of an optimal screening test. However, it should be emphasized that reliability verification tests are not designed to yield life data, so they can not be used to quantify the life or reliability characteristics of the product under normal operating conditions.

3.2 Screening Tests

The objective of screening tests is to expose, identify and eliminate latent defects, which can not be detected by visual inspection or electrical testing but which will cause failures in the field *i.e.* to eliminate the infant mortality failures on the left side of the bathtub curve. Another objective is to minimize repair and maintenance costs. Since it is a generally accepted fact that the removal of defects from systems as early in the design or manufacturing process as possible is an economical approach, screening tests should be performed at the lowest level of assembly consistent with the types of flaws involved.

It should be emphasized that screening tests are not reliability tests, *i.e.* they are not intended to validate designs but rather screening processes to force out latent defects that may otherwise cause failures in the field. While a screening test may occasionally expose design inconsistencies, its intent and methodologies are different.

Screening tests are usually conducted on the entire population of manufactured items. A common practice in electronic equipment manufacturing has been a burn-in –test, where items are aged (baked) under normal operating conditions. Environmental Stress Screening (ESS) achieves more effective screening by introducing environmental stress conditions over shorter durations. Kececioglu and Sun [KS03], list the two important key factors for a proper implementation of ESS as follows:

1. An optimum level of stress must be applied to products to force latent defects into failure.

2. The stress environment must not exceed electrical or mechanical limits of products, forcing unintentional failures or reducing products useful life.

HASS (Highly Accelerated Stress Screen) is another popular screening technique. It is very similar to HALT, the reliability characterization technique developed by the same author. In HASS the loading levels imparted are lower than in HALT, and typically beyond the product's specification limits but within the established endurance limit. Like with HALT, there is actually no specific HASS test, but it should rather be seen as a general test philosophy. Hobbs [Hob00] lists the only two requirements based on the loading environments (or other methods) used as:

1. Precipitate and/or support the detection of relevant defects, *i.e.* the family of defects which would show up in normal use including shipping

2. Leave screened products with substantially more fatigue life left after screening than is required for survival in the expected field environments. (Note that this definition of screening is quite different from that used for classical environmental stress screening.)

The HASS procedure requires the same six steps as HALT and, like in HALT, the first five are required for the method to function at all. In HASS the loadings imparted are typically beyond operation specifications, but within the capacity of the design. As these limits are in most cases determined by HALT, HALT is, if not an obligatory requisite, then at least highly beneficial in successfully conducting HASS.

HASS is intended to find the products with latent flaws without needlessly reducing the lifetime of the screened products. In order to successfully implement HASS, its functionality needs to be demonstrated. The so called 'proof of HASS' needs to demonstrate the following two aspects:

1. Products which have been through the screen have sufficient lifetime left to survive a normal lifetime of field use (safety of HASS).

2. The chosen screen does find the latent defects in the product (proof of effectiveness).

The implementation, optimization and proof of HASS is very time and resource consuming process. The time and effort going into setting-up HASS is clarified in

subsection 5.1.2, where a detailed example of a HASS test process is given. The interested reader is further referred to the work of G. Hobbs [Hob00] for more information.

HASA (Highly Accelerated Stress Audit), another screening method, is simply HASS on a sample basis. Despite its costs, HASS is regarded as a cost effective method in its own right until the quality is such that HASA can be employed. HASA is a great opportunity to receive major savings in time and resources if only the pre-screened reliability of the product is good enough, since most units (*i.e.* the units not in the sample) will be shipped with no screen at all.

3.3 Accelerated Life Tests

Like the reliability verification tests, accelerated life tests (ALTs) have various names such as accelerated reliability tests, life data analysis, operating life tests and quantitative tests. ALTs are designed to quantify the life characteristics of the component under normal use conditions, and thereby provide reliability information. Reliability information can include the estimation of the probability of failure of the product under use conditions, mean life under use conditions, projected returns and warranty costs. It can also be used to assist in the performance of risk assessments, design comparisons and to assure that the right side of the bathtub curve is far enough.

When whole products are tested, the number of factors affecting the test is large, and many of the factors are independent of the properties of components. For example, when drop testing a product, the covers of the product, the mounting of the printed wiring boards to the body of the product, the mechanical properties of the boards and the orientation of the product as it hits the strike surface have a strong effect on the vibration of the printed wiring board and thus on the reliability of the components. Therefore, in order to reduce the number of factors, most reliability studies are conducted on component board level. Furthermore, in many cases component-level testing is undertaken to begin characterizing product's reliability even tough full system level test units are unavailable or prohibitively expensive. However, system-level reliability characterization can be achieved through component-level testing if sufficient understanding exists to characterize the interaction of the components. If this is the case, the system-level reliability can be modeled based on the configuration of components and the result of component reliability testing. The focus of this thesis is on component board level tests and all discussion on reliability testing from here on is on component board level tests unless otherwise specifically stated.

The basic idea of the component level electronics reliability tests is to generate similar failure modes in electric assemblies that would occur in products under normal operating conditions in a much shorter timescale. This is accomplished by subjecting the test units to higher than usual levels of accelerating variables like temperature or voltage. Thus obtained results are used, through an appropriate physically-based statistical model, to make predictions about product life or performance over time at more realistic use-conditions. Numerous testing methods have been developed to

gather for the different needs of the wide spectrum of products and components. The test subjects can be exposed to loadings that are chemical, mechanical, thermal or electrical in nature or to any combination of the aforementioned loads, all depending on the presumed normal operation conditions of the subjects. Thermomechanical and mechanical single load accelerated life test methods are presented in the following chapter before moving on to discuss the combination of thermomechanical and mechanical loads in the ensuing chapter.

Due to the wide range of modern electronic products, it is impossible to define a universal test method that would prove the reliability of each product in their own use environment. Thus when planning an accelerated life test to a new product, the following five assumptions should hold for the test to be a meaningful representation of the products actual use environment [VS98]:

1. There is a predictable relation between the applied loadings and the resulting life duration for the product under test.

2. The severity of the applied load(s) should not change the shape of the lifetime distribution, *i.e.* the distribution of failures should have a known relationship with the applied stress level.

3. Failure times observed at the completion of the test should be analyzed to determine the underlying statistical distribution. If no reasonable distribution can be fitted to the obtained data, *e.g.* due to large amount of scatter, drawing conclusions based on the test results is dubious. A probability plot of the life data provides a check on the validity of the data and the assumed distribution.

4. In order to explain the effect of loading(s) on the product's life time, the physical laws of failure that explain the reasons for the reduction of life must be known. Without this understanding of the failure mechanisms, it is very easy to misinterpret the results.

5. ALTs are typically run on prototypes or test vehicles. To interpret the results from prototypes to actual production units, it is important that no significant design changes are made between the two phases. If there are significant changes in design, parts or manufacturing, a new set of tests should be run and evaluated prior to production.

Besides the fore mentioned five assumptions, the accelerated life tests should be fast, economically efficient and repeatable to justify their use from a commercial standpoint. Modern manufacturing of electronic products is strongly based on purchasing various parts and whole sections straight from subcontractors and the demonstration of reliability of said parts and sections is often left to the subcontractors. In that case it is very important that both the purchaser and the subcontractor have a mutual understanding on the quality and quality control of the merchandise. The purchaser should necessitate the applicability of the parts and the sections to his purpose of use and the subcontractors should be able to verify the applicability of their own products to match these specific criteria.

It should be emphasized that testing times can not be reduced beyond a certain point by just increasing stress levels. This is due to the fact that increasing stress to certain level induces different failure modes than those encountered at usual operating conditions. In extreme cases, the new failure modes result from a fundamental change in the mechanism causing the material or component to degrade or fail. For example, instead of simply accelerating a failure causing chemical process, increased temperature can actually change certain material properties, *e.g.* cause melting. In less extreme cases, high levels of an accelerating variable still might induce different failure modes such that the assumed statistical regression model does not hold any more. Consequently one of the main difficulties in accelerated testing is choosing the correct level of acceleration: the imparted loading levels should be low enough to represent the actual use environments, but should simultaneously accelerate the failure mechanisms to reduce testing times from several years to more acceptable timescales.

Chapter 4

Single Load Tests

Conventionally the reliability of electronic components has been tested by loading component boards with a single type of stress or strain. The industry has a long standing history of single load tests and a wealth of different standards so test results are predictable and comparable. The test methods have been established and testing equipment is easily available and due to the long history, the damage mechanics are often well understood and modeling can yield good results.

Numerous testing methods have been developed to gather for the different needs of the wide spectrum of products and components. The test subjects can be exposed to loadings that are chemical, mechanical, thermal or electrical in nature, all depending on the presumed normal operation conditions of the subjects. Thermomechanical cycling tests are still the most widely used reliability testing methods while mechanical loading is gaining more popularity especially in portable consumer electronics, where products are likely to experience mechanical shock loads. This chapter provides an overview of the typical thermomechanical and mechanical loading tests used in the industry.

4.1 Thermomechanical Load Tests

Individual electronic component contains no moving parts and can often perform reliably for many years, especially when operating near room temperature. In practice, integrated circuits operate at substantially higher temperatures and undergo various thermal excursions for different durations in their use conditions, all depending on the operating profile at any given time. Temperature can be considered as the main single factor affecting the reliability of electronics, because it influences both directly and indirectly via other failure mechanisms.

The direct effects of temperature influence the material properties such as tensile strength, yield strength or ductility and thus have an impact on reliability. For example, high temperature can lead to softening, weakening or melting of materials, while low temperatures can result in embrittlement of plastics, condensation and freezing of condensation or coolants. Most of these effects are deterministic and are not cumulative unlike the indirect effects of temperature. Gaseous and liquid diffusion, chemical reactions and some other physical processes are accelerated by in-

creasing temperature. These phenomena are typically represented by the Arrhenius' Law,

$$R = K \cdot e^{-\frac{E}{kT}}, \tag{4.1}$$

where R is the process rate, K is a constant, E is the activation energy for the process, k is the Boltzmann's constant, and T is temperature in °K. [ONB02]

However, the major source of thermally induced reliability failures in electronic packages is the thermal expansion mismatch that occurs due to temperature changes. Thermally-induced stresses and strains are generated in various parts of the system due to the mismatch in the coefficient of thermal expansion (CTE) among different materials, thermal gradients in the system and geometric constraints. For example, for ceramics, the CTE is 6 parts per million (ppm)/°C, while for FR-4 laminate (most commonly used base material for printed wiring boards) it is 17–18 ppm/°C (in the X and Y directions), thus giving a differential expansion of more than 10 ppm/°C which can exert a high stress on the interconnection joints. With repeated thermal excursions, the strain damage accumulates causing the joint to fail. These failures are referred as thermomechanical failures and the three widely used testing methods (namely thermal cycle, thermal shock and power cycle) to simulate thermomechanical stresses experienced by their operational life span are presented in the following three subsections. [VS98, Tum01]

4.1.1 Thermal Cycle

Thermal cycle tests have been designed to simulate the thermal excursions experienced in regular operating conditions. The tests are conducted at wider temperature ranges and higher frequencies to induce failures in much shorter duration than in field use while still under the assumption that failure modes are identical to the ones observed in field use. Analytical equations are then developed to enable the extrapolation of test results to regular operating conditions.

The actual test process is straightforward: the test specimens are continuously exposed to alternating high- and low temperature extremes. The tests are typically conducted until a predetermined number of cycles are reached or a failure is detected. The test parameters are temperature range (maximum [T_{max}] and minimum [T_{min}] temperature), dwell time (time spent at both T_{max} and T_{min}) and ramp-time (how fast the temperature changes from T_{max} to T_{min} and from T_{min} to T_{max}). The tests are conducted in specially designed environmental test chambers, which are typically equipped with one, two or three zones. In one zone configuration the specimens are heated and cooled in one chamber according to test specifications. Two zone configuration features hot and cold zones, which can be controlled independently and a product carrier to move the test specimen between the zones. Three zone configuration utilizes a third, ambient zone between the hot and cold zones to enable a more constant change of temperature than in two zone chambers. Regardless of the configuration, the chambers are typically air filled and heating and cooling is achieved by convection.

The test parameters should be selected carefully according to the potential use conditions of the product and physical limitations of the test specimens. Typical values for testing interconnections for solder joint fatigue are ramp rate less than 15°C/min, T_{max} 125°C, T_{min} −40°C and a dwell time of 15 min. Two most widely used standards are JEDEC's JESD22-A104D [JES09] and IEC's 60749-25 [IEC03].

4.1.2 Thermal Shock

Thermal shock tests are performed to determine the reliability of the interconnections in sudden changes in temperature as experienced *e.g.* in hand or wave soldering, self-heating of power semiconductors or turn on of optical devices. Thermal shock tests are very similar to thermal cycle tests with the ramp rate being the main distinction between these two testing methods. As specified by the IPC-SM-785 standard [AS92], the ramp rate used in thermal cycling should be less than 20°C/min, while in thermal shock the ramp rate should exceed 30°C/min. The method has been standardized by JEDEC [JES04] and IEC [IEC09].

Test chambers employed in thermal shock tests use air or liquid as a medium to transfer thermal energy. Air-to-air chambers are similar to the ones used in thermal cycle tests but to achieve the high temperature change rate, two or three chamber systems are used. Air-to-air systems are more common for general product testing due to their easier maintainability and their ability to handle larger devices than in liquid filled systems. In liquid-to-liquid systems the heating and cooling is achieved by conduction, which is significantly faster than convection. Just like the two chamber air-to-air systems, liquid-to-liquid systems feature two chambers and a product carrier to move the samples from one chamber to the other. Besides the differences in size (chambers in liquid-to-liquid systems are typically small) and thermal medium, the process is basically the same as in air-to-air systems. Due to their smaller size, liquid-to-liquid systems are typically only used for component level tests.

De Vries *et al.* [dVJvDW07] studied the difference between thermal cycling and thermal shock testing with finite element analyses (FEA) and experiments done on ball grid array (BGA) packages. The experiments indicated that the products survived significantly longer in the thermal cycle test. It was concluded that in thermal cycle tests the stresses are mainly caused by CTE mismatches, depending on the combination of materials used, while in thermal shock tests additional stresses can be generated due to temperature gradients, which depend on the thermal behavior of the tested system. Additionally, thermal shock might even cause different types of failures than the thermal cycle test.

4.1.3 Power Cycling

The previously mentioned thermomechanical reliability testing methods correspond relatively well with real life (*i.e.* the worst case scenario) experienced by handheld consumer electronics moved from one ambient to another along the user. However, the internal heating of electronic devices is becoming increasingly non-uniform due to

their compact size, modular construction and novel cooling solutions. Furthermore, the increasing current and power densities impose another threat to interconnection reliability in the form of electromigration. In order to overcome the aforementioned shortcomings of thermal cycling and thermal shock, an alternative test method, power cycling, has been developed.

In power cycling the functional test specimens are electrically operated to function similarly to their estimated field use. The acceleration of the test is accomplished by using higher electrical power as compared with the specimens' normal operation, while still remaining within the manufacturer's operation limits. The heat of the test specimens is generated internally and is non-uniform by nature.

The loading in power cycling is achieved by an electric current and thus the test method is obviously not purely thermal or thermomechanical in nature. Furthermore, unlike thermal cycle and shock tests, power cycle tests are not accelerated environmental tests but rather they are accelerated in time relative to use operation. Nonetheless, in power cycling the test specimens are continuously subjected to rapid thermal cycles, which induce mechanical stresses within the assembly much like in thermal shock and cycle tests. Laurila *et al.*'s recent study [LMV+07] concluded that the failure mechanism of lead-free solder interconnections in power cycling and thermal shock tests are generally the same with experimental results indicating that the failures were induced by recrystallization-assisted crack nucleation and propagation. Thus power cycling can be employed as an alternative, power induced, temperature cycling method to simulate the non-uniform temperature distribution of the test specimen. [ZvDF06]

Due to its non-uniform temperature distribution within the package and the next level of assembly, power cycling offers several advantages when compared to thermal cycle and –shock tests. Power cycling can be utilized to better simulate the service operating conditions, to activate the field failure mechanisms and precipitate the field failure modes better than the traditional thermal cycling and thermal shock tests. Furthermore, in addition to the more realistic loading environment, power cycling seems to produce harsher loads than the more traditional methods. Power cycling is intended to simulate the range of usage conditions from the vicinity of ambient room temperature up to the maximum operating temperature of the test specimens. Despite the lower temperature change than in the thermal cycle and shock tests, and thus lower thermomechanical loads induced, both the progress of recrystallization and intermetallic layer growth were reported to be faster in a comparative study [KLK06]. The higher rate of recrystallization was suspected to result from the higher average temperature in power cycling which accelerates transformation kinetics exponentially. The increased growth of intermetallic layers was credited to the high density electric current through the interconnections. The method has only recently been standardized by JEDEC [JES07].

4.2 Mechanical Load Tests

The mechanical reliability of solder interconnections under shock loads is an important issue for the manufacturer of electronics. As modern portable devices are getting smaller and smaller they are more likely dropped during their day-to-day use, while automotive electronics are constantly exposed to vibration originating from the cars engine. These and various other types of mechanical shocks are transmitted to the PWB and the IC component mounted on the PWB, affecting the integrity of the components and their interconnections. Mechanical loading is becoming more and more popular in reliability research and it is gradually replacing the traditional thermomechanical cycling tests in some fields. Some of the industry's standard mechanical loading methods are presented in the following two subsections.

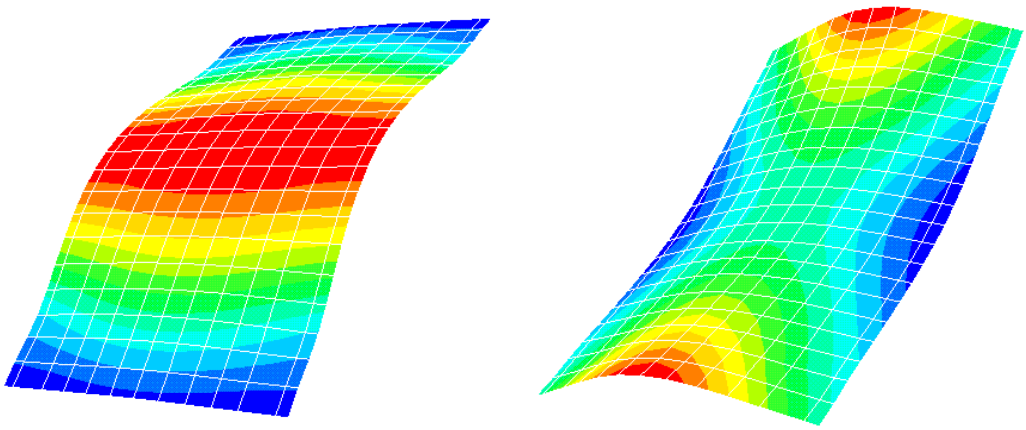
4.2.1 Drop Test

There are currently two different standards for board level drop testing: IEC's 62137-1-3 [IEC08] and JEDEC's JESD22-B111 [JB03]. The IEC standard is rather recent while the JEDEC standard was developed in 2003 to make the drop test reliability from different component manufactures comparable and is widely adopted in microelectronic industry.

JEDEC's board level drop test is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment. The standardized test method provides reproducible assessment of the drop test performance while aiming to duplicate the failure modes normally observed after product level tests. The test procedure is more appropriate for relative component performance than to serve as a component qualification test. It is not meant to replace any system level drop test that may be needed to qualify a specific electronic product.

The primary failure mode observed in drop tests is the cracking of the reaction layer between the bulk solder and the component or PWB metallization. This is due to the strain rate hardening of the bulk solder that forces the cracks to propagate in the brittle reaction layer(s). It should be noted that this failure mode differs from that typically observed in thermally cycled test assemblies, where the nucleation and propagation of cracks is strongly enhanced by recrystallization of the solder interconnections. Other observed failure modes during drop testing include the cracking of the circuit board, trace cracking on the board and cracks in the components. [ALK05]

Drop tests are typically conducted by attaching the component boards into a test apparatus, where the drop test table is allowed to slide down on guide rods to hit the strike surface. The drop table is raised to a specified height and the strike surface material is specified to achieve the required G level, pulse duration and pulse shape. According to JEDEC's specifications, the test board should be mounted to the base plate standoffs in horizontal orientation with the components facing downward using four screws, one at each corner of the board, to achieve maximum PWB flexure.



(a) (b)

Figure 4.1: *The first (a) and second (b) natural modes of a JEDEC drop test compliant test board after drop impact. Contour represents vertical displacement. Images taken from [MMK06].*

As the test table hits the strike surface, the PWB starts bending due to the impact forces transmitted through the mounting screws. After the impact, the vibration of the test board can be considered as a sum of natural modes of vibration. The natural mode of the component board describes the shape where the board bends and depends on the geometry of the assembly (board geometry, supports, and the distribution of components) while the natural frequency describes how fast the bending takes place and is dependent on the mode, the thickness and the elastic module of the structure and the mass. Most of the bending occurs by the first and the second modes (illustrated in Figure 4.1) with the lowest frequencies. In general, the higher the frequency of the mode, the smaller the effect on bending. [Mar07, ALK05]

The JEDEC standard specifies the test procedure and preferred test specifications in much detail but only a few most important details are briefly mentioned here. The test procedure requires all components to be daisy chained and the electrical resistance of each daisy chain should be measured in-situ during each drop. The board layout, presented in Figure 4.2, allows up to 15 locations for component mounting. The mounting and simultaneous testing of 1, 5, or 15 components is enabled with 15 being the preferred number. When using the 1-component configuration, the component should be placed at location U8 (see Figure 4.2), and when using the 5-component configuration the components should be mounted at locations U2, U4, U8, U12 and U14.

4.2.2 Vibration

Vibration testing is a process where a controlled amount of vibration is applied to the test specimen. The car and aeroplane industry have long been employing vibration testing in qualifying electronic components. Usually the magnitude of

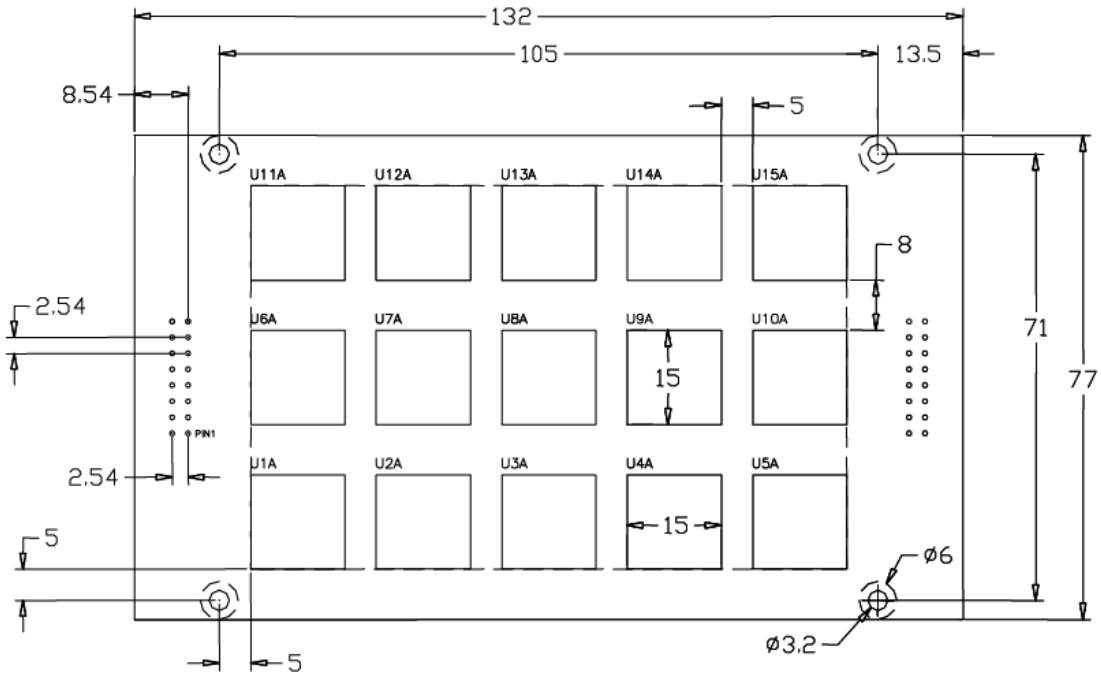
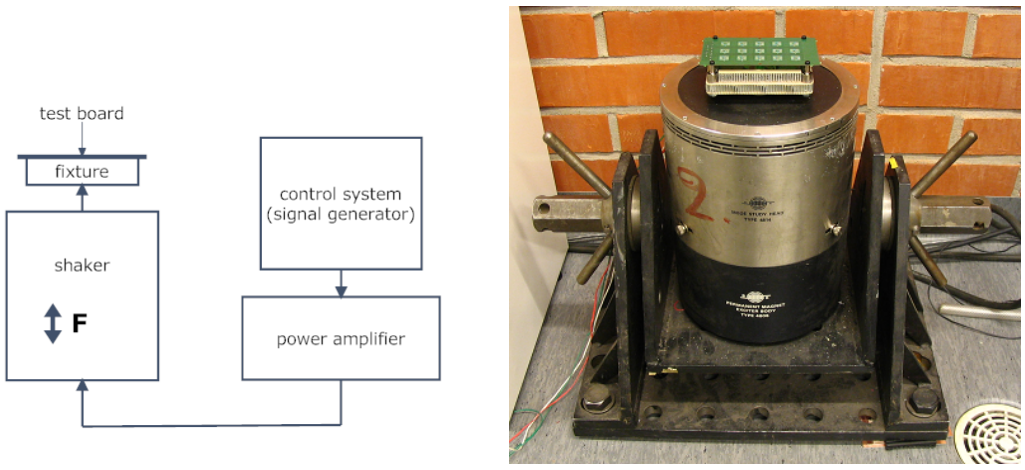


Figure 4.2: *Preferred test board size and layout with measures (in mm) as specified by the JEDEC standard [JB03].*

loading has been significantly lower than in drop testing. The vibration tests have been conventionally conducted with an electrodynamic vibration system, where the operation of the shaker is based on the electromagnetic forces of two interacting magnetic fields. One of the magnetic fields is static (generated either by permanent magnet or a direct current in a field coil), while the armature coil has a magnetic field proportional to the applied voltage. The armature is coupled to the fixation table where the test specimen is attached. Figure 4.3 presents a schematic graph of a typical vibration system along with the electromagnetic shaker used in the Electronics Integration and Reliability (EIR) –research unit. [GdSGdSFT08]

Modern electrodynamic vibration systems are capable of performing three basic tests broadly characterized as sine, random and shock. In sine testing the energy is output either at a single frequency or by sweeping the predetermined frequency range back and forth. Sweeping the frequency range can also be utilized to locate the natural frequencies of the test setup. Random vibration, where a wide range of frequencies are excited simultaneously at closely controlled energy levels, is conventionally used to closely approximate real world application environments. Variable vibration frequency tests have been standardized by JEDEC [JB06] and IEC [IEC07]. Modern electrodynamic vibration systems have also the capability of performing shocks, where the armature is given an initial displacement and a pulse of energy is delivered by the amplifier which translates into a particular waveform. Other more complex waveforms can be generated such as sine-on-random, random-on-random and it is even possible to replicate data collected from real life situations. [The06]



(a) (b)

Figure 4.3: *(a): Schematic graph of a typical vibration system. (b): EIRs electromagnetic shaker.*

To overcome the drawbacks related to drop testing, the use of large amplitude single frequency vibration test has been investigated recently [Mar07, Suo07] as a method for studying the reliability of electronic assemblies under shock loadings. In drop testing the primary source of stresses in the interconnections is the bending of the PWB, so by adjusting the amplitude and frequency of vibration similar stresses and failure modes can be produced. In drop testing the bending is the sum of all the natural modes of the test specimen and even tough the first natural mode dominates, the bending can be quite complex. When only the lowest natural mode is excited in vibration testing, the bending is less complex and analyzing stresses is easier. Furthermore, vibration testing has several other advantages: the test structure does not move much so more accurate contact free component board behavior measurements are possible. Significantly less strain is placed on the measurement cables, so faulty signals are not as common as in drop testing and the system needs less maintaining. The vibration testing is also much faster, since the typical lowest natural frequency of a test board designed according to JEDEC's specifications [JB03] is in the range of 200 Hz. Assuming that three to five vibration cycles correspond to one drop in drop testing, the testing time for say 200 drops can be reduced from half an hour (further assuming that the cables don't break during testing) in drop testing to mere seconds. Furthermore, the implementing of other loads such as temperature is much easier. However, it should be stressed that the bending behavior during vibration testing is highly dependant on the properties of the test assembly, so whenever utilizing the vibration test system the bending amplitude of the component board should be specified and the excitation signal (amplitude and frequency) should be adjusted accordingly. The comparison of the two test methods is presented in numerical form in Table 4.1 and for more details on the subject the reader is directed towards the excellent work of Marjamäki. [Mar07].

Table 4.1: *Numerical evaluation of drop and large amplitude single frequency vibration test methods (1=bad, 4=very good) according to [Mar07].*

	repeatability	speed	versatility	loading type	reliability
drop test	2	3	1	3	2
vibration test	3	4	3	2	3

4.3 Other Single Load Tests

In addition to the aforementioned test methods, the industry features various other standardized single load tests and innumerable amount of nonstandardized methods to represent the wide area of operating conditions that modern electronic devices are exposed to. Besides the fore mentioned thermomechanical (section 4.1) and mechanical load tests (section 4.2), there are various other test methods employing thermal and mechanical loads. In addition to the previously discussed thermomechanical tests, where the failures are induced by temperature changes, thermal loadings can be imparted in a steady manner. Examples of steady state temperature tests are high and low temperature operating life tests to determine the reliability of the test specimen at high or low temperature conditions over an extended period of time or high temperature storage test to determine the effects of long term storage at elevated temperatures. Besides the vibration and drop tests, typical mechanical loading tests include such tests as solder ball shear test to assess the ability of solder balls to withstand mechanical shear forces or flip chip tensile pull and solder ball pull tests to asses the interconnections ability to withstand pull forces. In addition to the mechanical and thermal loading methods, the test specimen can be exposed to loads that are chemical (*e.g.* salt atmosphere test to determine solid state devices resistance to corrosion) or electrical in nature. However, all these test methods are beyond the scope of this thesis, and are not discussed further here.

Chapter 5

Multiple Loading Tests

Electronic products are very seldom exposed only to a single type of stress or strain. For example portable products might be dropped during their operation (*i.e.* when their components are running hot) while automotive, avionic and military products can be constantly exposed to concurrent vibrations and thermal excursions. Multiple loading tests have, therefore, been developed to simulate the real operational loadings as realistically as possible and to address all relevant failure mechanisms as in the use environment. The combining of several loadings is also expected to increase the rate of damage accumulation and thus decreasing the associated testing time and costs. The combination of loadings can be implemented in two different ways. In sequential loading only a single load is applied at a time and the combining of the loads is achieved by applying several loadings either consecutively or alternately while in concurrent loading the separate loads are applied simultaneously. [Qi06]

Despite the various advantages associated with multiple loading tests, the methods are still seldom utilized. Although extensive research results have been documented for product failures due to single load tests, limited research has been conducted on failures caused by combined loads and disagreement still surrounds the complex interactions between combined loadings. It is often unclear how to choose and set up test parameters in the most cost effective way and how to extrapolate the test results to actual use environments. Different loading frequencies (such as the low frequency loading in thermal cycling and the high frequencies in vibration testing) and loading amplitudes between the loads confuse the matters even more. To combine separate loadings in a meaningful way a thorough understanding of the failure modes and mechanisms taking place independently under the stated loading conditions is needed. Thus it is clear that innovative testing methodologies and approaches with a thorough understanding of the associated phenomena are required for reaping the benefits of multiple loading tests.

It is mentioned here that various standardized accelerated life testing methods that can be considered as multiple loading tests are used in the industry. For example, temperature, humidity and bias (THB) test, a reliability test designed to accelerate corrosion, features three different loadings: temperature (85 °C) and humidity (relative humidity of 85 %) to promote corrosion of metals in the presence

of contaminants and an applied bias to maximize the variations in the potential levels of the different metallization areas. However, as previously stated, the focus of this thesis is on the combination of mechanical and thermomechanical loads and all other multiple loading test methods are thus omitted.

Linear damage super-position rule is used in practice as a first-order approximation for damage calculation and fatigue-life prediction under multiple loadings. The rule, popularized in 1945 by M. A Miner [Min45], was first proposed by A. Palmgren in 1924 [Pal24] and is also known as Miner's rule or the Palmgren-Miner linear damage hypothesis. The name of the rule is slightly misleading since the term linear does not refer to the linearity of the damage process. Instead, the hypothesis of the rule is that the normalized damage fractions of the total consumed life can be superposed linearly. The rule states that the damage fraction (D_i) at any stress level S_i is linearly proportional to the ratio of the number of cycles of operation (n_i) to the total number of cycles that would produce failure (N_i) at that level. In other words:

$$D_i = \frac{n_i}{N_i}, \tag{5.1}$$

and failure is predicted to occur if the sum of the damage fractions (also referred as the cumulative damage index, CDI) at k levels surpasses the pre-determined critical value $\mathrm{CDI}_{critical}$:

$$CDI = \sum_{i=1}^{k} D_i = \sum_{i=1}^{k} \frac{n_i}{N_i} \geq CDI_{critical}. \tag{5.2}$$

CDI ranges from 0 to 1.0 with 0 being the undamaged state and 1.0 being the fully damaged state. Although failure is classically predicted to occur when the critical value ($\mathrm{CDI}_{critical}$) equals one, commonly more conservative values such as 0.7 for electronic equipment or lower when loss of life is at stake, are used. [Ste00]

The linear damage super-position rule has several recognized shortcomings. The rule is insensitive to the sequence of load steps, although several studies have shown that the effect of sequence can be important. Only the damage caused by stresses above the fatigue limit (overstress) is accounted for. Fatigue limit is an expression used to describe a property of materials and is generally defined as the amplitude (or range) of cyclic stress that a material can tolerate for an infinite number of cycles without breaking. Most metals do not have a distinct limit and will eventually fail even from small stress amplitudes. In these cases, a number of cycles (usually 10^7) is chosen to represent the fatigue life of the material. For a stress level lower than the fatigue limit, the number of cycles to failure N_i is assumed to be infinity, meaning that the stress fluctuation below the fatigue limit gives no damage. Furthermore, the rate of damage accumulation is independent of the stress level which does not correspond to observed behavior. Cracks will initiate in a few cycles at high loading amplitudes whereas at low loading amplitudes almost all the life is spent initiating a crack. Despite these shortcomings the rule is still widely used due to its simplicity,

wide applicability and due to the fact that more sophisticated methods do not always result in better predictions. [PS08, Sin03, BJ92]

This chapter aims to give a review on the current status on multiple loading tests. The relevant articles on the subject are first summarized in section 5.2 before conclusions on the subject are drawn in section 5.3. However, before going into detail with multiple loading tests, the most commonly used multiple loading reliability characterization and screening methods, HALT and HASS, and their applicability on accelerated reliability testing are discussed.

5.1 HALT And HASS

HALT and HASS are by far the most used reliability verification and screening methods and are probably the first things associated with multiple loading tests in the industry. These methods have been previously presented and discussed in sections 3.1 and 3.2, but to further illustrate the test procedures, examples of typical HALT and HASS test processes are presented in the following subsections before discussing why the test methods are inapplicable to life testing.

As previously stated, since all the limits and used loadings are application specific, there is no general HALT or HASS procedure and only the test philosophies are generic. Although the types of loadings used in HALT and HASS should be application specific and chosen on the basis of the presumed operating environments, the combination of thermal and multi-axial vibration loads is an unofficial industry norm. The combination is by far the most common type of loading used in HALT and HASS, and this is reflected on the chosen test process examples.

Qualmark's guidelines for HALT [Qua07] and HASS [Qua04] both require equipment capable of performing thermal and vibration loadings. It should be noted that Qualmark is the largest global manufacturer of HALT and HASS test systems, and the guidelines are obviously written with their own equipment (*i.e.* test chambers) in mind. However, the combination of thermal and vibration loads is so common in HALT and HASS testing, that these guidelines can be considered representative of the industry. Furthermore, since many manufacturers are reluctant to give away valuable technical advantages and knowledge for free, the Qualmark guidelines are one of the few guidelines publicly available and are thus chosen for examples to illustrate the HALT and HAST test processes.

Because certain failures will only occur during operation, it is also stressed here that the test units should be operational and monitored during testing. Furthermore, part of the HALT process is to identify the operating limits of the test units and these limits can only be accurately determined when a monitored test unit begins to malfunction during testing.

5.1.1 HALT Test Process

Qualmark's HALT Guidelines [Qua07] test procedure consists of four phases (temperature step stress, rapid temperature transition, vibration step stress and combined environment stress test) that are clarified in the following.

Temperature Step Stress

During the thermal step stress the temperature is raised up with increments less than or equal to 10°C. The test should be started at ambient temperature (which can be defined anywhere between 20°C and 30°C) and the dwell time on each temperature is a minimum of ten minutes as determined by the sample thermocouple response. The loading is continued until either the operational limit (OL) of the sample is determined or the chamber maximum is achieved. If the OL can be determined, the test process should continue to the destruct limit (DL) or chamber maximum. However, since the sample will most likely not be operational beyond its OL, it will become necessary to return to a lower temperature (i.e. below the OL) after each additional dwell to determine whether the sample is still operational.

Rapid Temperature Transition

Rapid temperature transition phase consists of a minimum of five thermal cycles (performed at the maximum attainable rate of change) that shall be performed unless a destructive failure is encountered prior to completion. The minimum thermal cycle temperature range should be within 10°C of both the lower and upper thermal OLs as discovered during the previous phase. The minimum dwell time is five minutes following stabilization of the sample at the setpoint as determined by the sample thermocouple response. The dwell time is increased to allow higher mass components to reach at least 80 percent of the thermal range.

Vibration Step Stress

Vibration step stress test begins at a chamber setpoint of 5 to 10 G_{rms} (or lowest stable chamber control setpoint), as measured over a 2 Hz to 2,000 Hz or greater bandwidth and is then increased in 2 to 5 G_{rms} increments (5 G_{rms} recommended) upon completion of the dwell period and subsequent functional test. The minimum dwell time is ten minutes, with functional testing performed at the very least at the conclusion of the dwell. In the same way as in temperature step stress, the loading is increased until either the operational and destruction limits of the sample are determined or the chamber maximum is achieved.

Combined Environment Stress Test

A minimum of five combined environment cycles are required unless a destructive failure is encountered prior to completion of the five cycles. The combined environment test is performed with thermally cycling between the thermal OLs (with a minimum dwell period of 10 minutes at each thermal extreme). The starting level

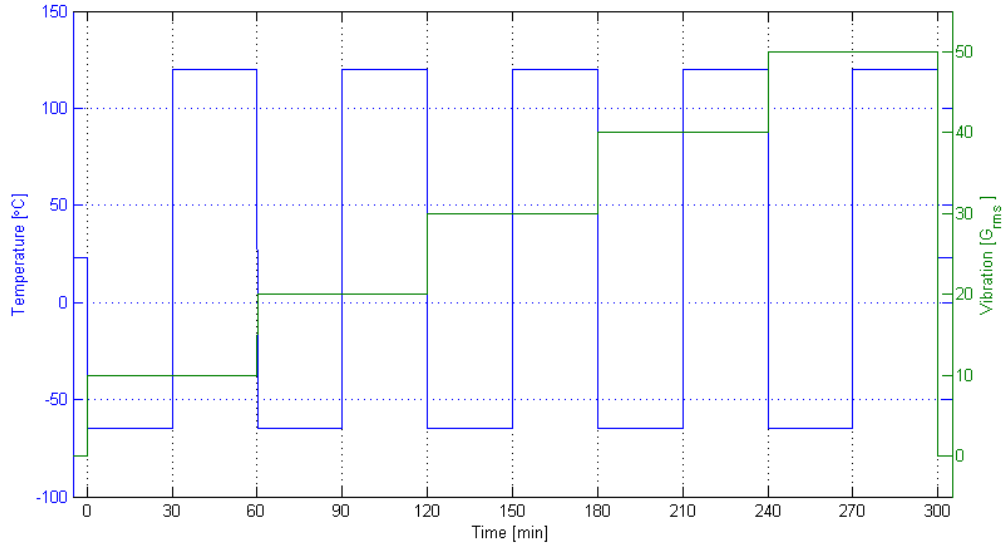


Figure 5.1: *An example of a combined environment stress HALT profile. The temperature profile is plotted in blue and the vibration profile in green.*

for the vibration is determined by dividing the maximum vibration level applied during the vibration step stress by five, and the vibration level is then increased by the same amount during each subsequent thermal cycle. However, smaller starting vibration and increment levels may also be used. Functional testing is recommended throughout the test, but should at the very least be performed at the conclusion of each step. To further illustrate the test process, an example of a combined environment stress test profile for a fictional product (maximum vibration level of 50 G_{rms} and thermal OLs of T_{high}=120°C and T_{low}=−65°C) is presented in Figure 5.1.

5.1.2 HASS Test Process

HASS is used to find the products with latent flaws and should not initiate additional failures like HALT. HASS is a living process that needs modifications and adjustments over time. As more and more is learned about the product over time, including the HASS results, the profile may change and evolve into a better screen. Therefore the profiles offered in various guidelines serve only as starting points and usually require modifications to specify the types of loadings to fit to the specific use environments of the products and to uncover defects without removing significant life on the products. Once a test profile has been set up, it is essential that it is audited on a continual basis throughout the life of the product. This ensures that screen remains effective and that subtle changes in the product are not causing the screen levels to move into the damage area.

HASS testing is usually begun by designing a test profile based on HALT results, product specific criteria and functional test considerations. Qualmark [Qua04] presents two approaches to developing the test profile in its HASS guidelines, the standard profile and the precipitation/detection profile. Additionally, when setting

up a HASS profile, its functionality needs to be assessed. The proof of HASS needs to determine how effective the screen is in detecting manufacturing flaws (screen effectiveness) and to prove that the screened products have sufficient life left in them (product life valuation). The HASS test profiles (standard and the precipitation / detection profile) and the proof of screen (screen effectiveness and product life valuation) according to Qualmarks guidelines are presented in the following.

Standard Profile

The standard profile is a traditional approach to screening in the sense that the repeated cycles (two or more) are performed within the OLs of the product. Typical chosen levels are 80% of the cumulative range of the upper and lower OL for thermal loadings while vibration setpoint levels should be set up to obtain a product response equal to 50% of the DL product response, but within the OL of the product as measured by HALT. If the vibration level exceeds the OL, then a level of approximately 80% of the OL should be used as a setpoint.

Vibration should be modulated throughout the profile, beginning at 5–10 G_{rms} and slowly ramped to the maximum level followed by a minimum dwell of 5 minutes. This process is then repeated in reverse, from the maximum level to the minimum level with no dwell on the minimum level. Vibration maximum levels should be applied at the temperature extremes and during the temperature ramps, if possible and the vibration modulation ramps should be as slow as possible.

Dwell times at each temperature extreme depend on the product attaining the desired temperature with a minimum dwell of 5 minutes. The length of the dwell is also affected by the length of the functional test as the test should be completed at the least at each temperature extreme.

Precipitation / Detection Profile

This profile subjects the product beyond its OLs for the first cycle (precipitation) followed by subsequent cycle(s) within the OLs (detection). The precipitation cycle aims to precipitate the dormant or latent defects as quickly as possible and the detection cycle seeks then to detect the precipitated defects. The units are usually non-functional but may be powered during the precipitation cycle and are powered and functionally tested during the detection cycle(s). If there is sufficient margin between the temperature OL and DL, then precipitation / detection margin should be used.

Thermal precipitation cycle levels are performed between the OLs and DLs and typically levels equal to half the difference between the OL and DL are chosen. Detection cycle levels are within the OL, typically from 5°C to 10°C within the OLs. Minimum dwell time at each temperature extreme is 5 minutes, with the length of the dwell depending on the units attaining the desired temperature and the length of the functional test on the detection cycle(s), as the functional test should be completed at the very least at each temperature extreme.

Vibration levels for the precipitation cycle should be 50% of the DL, and levels for the detection cycle should be 80% of the OL. Vibration should be modulated

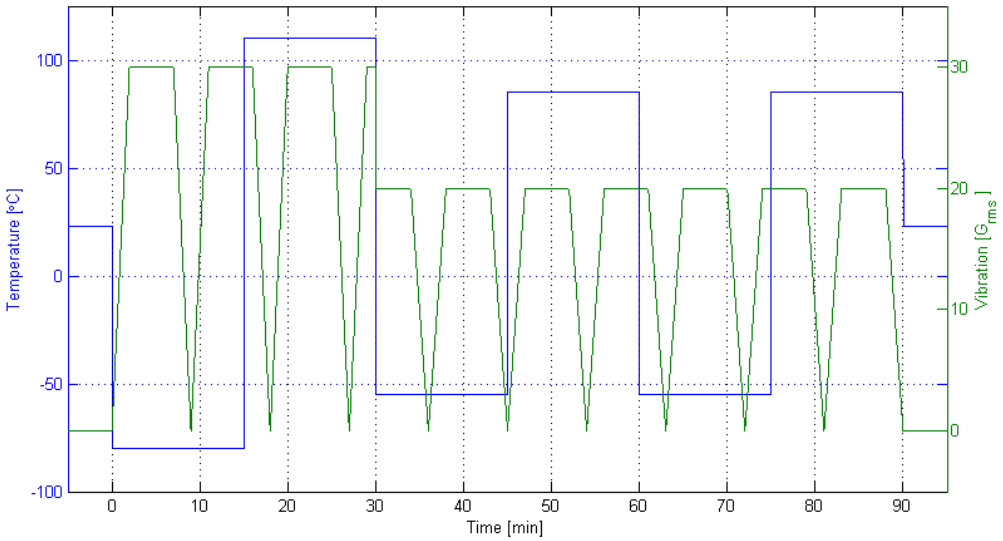


Figure 5.2: *An example of a precipitation / detection HASS profile with two detection cycles. The temperature profile is plotted in blue and the vibration profile in green.*

throughout the cycles, beginning at 5 to 10 G_{rms} and slowly ramping to the maximum level and back to starting level after a dwelling minimum of 5 minutes. The vibration modulation ramps should be as slow as possible based on the aforementioned variables.

An example precipitation / detection profile for a fictional product (with upper and lower thermal DLs of 130°C and −100°C and OLs of 90°C and −60°C and vibration DL and OL of 60 and 25 G_{rms}, respectively) is presented in Figure 5.2. The example profile features the precipitation cycle and two subsequent detection cycles. Thermal and vibration levels are set according to the guideline and are 110°C – −80°C and 30 G_{rms} for the precipitation cycle and 85°C – −55°C and 20 G_{rms} for the detection cycles.

Screen Effectiveness

The effectiveness of a screen is measured by its ability to precipitate latent defects. For this process, units classified as no trouble found (NTF) or units that are determined to be marginal from parametric functionality testing should be used. If these units are not available, then production units should be seeded with defects in a manner that they are representative of the manufacturing process going out of control. All of these units should fail during the HASS profile.

The initial profile shall be performed and the result analyzed. If a failure occurs at any point during the profile execution, the profile should be stopped and the failure should be analyzed. Root cause analysis (RCA) should be performed on the failed unit to determine whether the failure was the result of overstress or wear-out, or due to a manufacturing process flaw. If the failure resulted from overstress or wear-out, the profile levels should be reduced and the profile re-executed using previously

non-tested units. If no defects are detected, the screen severity is increased (either by expanding the profile levels or increasing the number of cycles) and the process is repeated. Note that increasing the cycle count extends the total production HASS duration and therefore should be done only when the level severity cannot be increased.

Product Life Valuation

This process estimates the degree of appreciable life remaining in the product(s) after exposure to the HASS screening profile. The product life validation is conducted with production level units exposed to the HASS screening profile a minimum of ten times. If no failures are detected, it is demonstrated that the units exposed to only one pass of the profile, will still have 90% minimum of the useful life remaining or 10% maximum of life removed. For greater confidence, it is recommended that the profile is repeated from 30 to 50 times.

If a failure occurs during execution at any point of the profile, the test should be stopped and RCA performed to determine if the failure was the result of overstress or wear-out, or due to manufacturing process flaw. If failures that were the result of overstress or wear-out are detected, the profile levels shall be reduced and the profile re-executed using previously non-tested units. Units with no failures observed upon the completion of the product life valuation process may be subjected to the normal qualification process or other accelerated life tests. The purpose of this would be to gain even greater confidence that products have not been degraded significantly and that minimal life has been removed in the product life valuation.

5.1.3 Applicability on Life Testing

Both HALT and HASS have their own pros and cons. HALT is a design aid tool and is very effective in precipitating failures in a very short timescale. It can be used *e.g.* to compare different designs (as early in the development cycle as possible) or to compare different components form various vendors. HASS, if properly implemented, is very effective in finding products with latent flaws but the implementation of HASS is a resource and time consuming process. Due to complex loading conditions typically used in HALT and HASS, the failures observed may not always be relevant from the operational environment point of view. Thus, the arguable increased reliability of the product after HALT and/or HASS testing can (in worst cases) mean only that the product is more reliable in HALT and HASS tests.

HALT and HASS have several drawbacks which illustrate why the methods are not suited for life testing. These are [Suh02, Sil04]:

- Due to the very complex nature of the stress state (especially combined tri-axis vibration and temperature cycling) during HALT and HASS the root cause analysis of failure modes and mechanisms is very difficult. Without the understanding of failure mechanisms, explaining the effects of loadings on product's lifetimes is very difficult and thus the results are often misinterpreted.

- The loadings applied in HALT (and HASS) are designed to stress the test unit until failure rather than simulate use environments. As different failure modes are characterized by different activation energies, the types and order of failures observed during HALT (and HASS) might differ significantly from the ones observed in typical use environments, making life time predictions and the calculation of acceleration factors challenging. Furthermore, a simple superposition of the effects of two or more failure mechanisms can be misleading and result in erroneous reliability projections.

- Albeit the failures that occur during HALT can be partly the same as the ones observed in field use, the frequency of occurrence is usually very different and the determining of the underlying statistical distribution is difficult. Furthermore, HALT testing is usually conducted with only a few test units, making the statistical or probability considerations nearly impossible.

As there are no standards concerning HALT and HASS, and the differences how the test methods are perceived in the industry can be quite substantial. There have been several attempts to use HALT or the results obtained with HALT to predict useful product life [BKRD06, LF06, PMTM00, PFP+00, MSCA88] but none have been particularly successful. It should be, once again, emphasized that the purpose of HALT (and HASS) is to stimulate failures but not to simulate reliability. To conclude, HALT and HASS are not designed as accelerated life tests and should not be used as such.

5.2 Literature Review on Multiple Loading Tests

Due to the limited amount of results published on the combining of mechanical and thermomechanical loadings, the order of this review is such that the relevant papers on the subject are summarized in this section, and the conclusions on the current status of the subject are drawn in the following section. The publications are summarized in alphabetical order, and the order is in no way related to the significance of the publication.

Albeit limited research has been conducted on the subject, multiple loading tests seem to attract more and more attention. It is worthy to note that in addition to the publications discussed here, two doctoral dissertations [Qi06, Per07] on the topic have been published during the recent years. However, as the results and conclusions presented in the dissertations have been discussed and analyzed further in the following papers [QOP08, QOP09, PS08] published by the respective authors, the dissertations are only mentioned here to serve as a very extensive and detailed introduction on the subject for the interested reader.

Barker *et al.*: Combined Vibrational and Thermal Solder Joint Fatigue—A Generalized Strain Versus Life Approach [BVDP90]

In one of the early publications on the matter, Barker *et al.* investigated the combined effects of elastic and inelastic strains on solder joint reliability. The purpose of the paper was to present a generic unified method to properly account for the thermal as well as the vibrational strains, with the focus on lifetime prediction. To develop a better understanding on the solder joint behavior from low cycle (from 1 to 10^4 cycles) to high cycle (between 10^3 to 10^8 cycles) fatigue, the transition region from 10^3 to 10^4 cycles was explored in detail.

The analysis was begun by discussing that most thermal reliability models assume that the elastic strains have a minimal effect and only utilize the inelastic strains. However, the assumption is not valid in combined vibration and thermal loading where both strain components have comparable magnitudes and must be accounted for. It was emphasized that the elastic strains, caused by vibration must be included in any reliability prediction model, especially if the strain amplitudes are in the transition region.

Two approaches were then used to determine how the high frequency vibration strain can influence the predicted solder joint life in concurrent loading. In the first approach, the thermal induced strains were assumed completely inelastic and vibrational strain completely elastic. In the second approach, referred as the total strain approach, both strains were recognized to contain elastic and inelastic components and the fatigue lives were calculated accordingly. The effects of subjecting a surface mounted component to combined vibration and thermal loading was then studied with these approaches. The used thermal load had a frequency of one cycle per day and three different loading levels (with shear strains of 6, 3 and 1.5 percent) were employed. Vibration loading was executed with random vibration and variable strain levels.

The two different lifetime approaches to predict the fatigue life produced dramatically different results. It was noticed that the first approach significantly underestimates the life predictions made by the more general, total strain approach. It was concluded that high frequency vibrations will shorten the life of solder joints and should not be neglected in a solder joint reliability prediction. Albeit some valid points were made regarding vibration loading, no experimental data was given to support the results and the conclusions should thus be regarded as speculative.

Basaran *et al.*: Damage Mechanics of Microelectronics Solder Joints Under Concurrent Vibration and Thermal Loading [BZC01]

In an attempt to understand the solder joint material under realistic thermal and vibration loading conditions, Basaran *et al.* conducted concurrent thermal cycling and vibration tests. The purpose of the study was to provide a solid basis for more accurate material modeling and fatigue life prediction. It is also noted here that the same ideas and results have been utilized in other publications by the same research group [BZCD00, ZBCD00]. However, as the publications present very little new information compared to this article, only this article is discussed here.

The concurrent tests were conducted with an actual BGA package and Moiré interferometry was utilized to measure the inelastic deformation field of solder joints

with submicron resolution. Thermal cycling was conducted with a temperature range from −55°C to 155°C, ramping rate of 20°C/min and dwell times of 12 min at temperature extremes. Vibration was conducted with a frequency of 100Hz and acceleration of 50G. In addition to the concurrent tests, pure thermal cycle tests were conducted as a reference. The effect of pure vibration loading was not investigated.

The results indicated that vibration loading has a significant effect on the behavior of the solder joints during concurrent loading. Although thermal fatigue was the dominant failure mode, vibration was observed to significantly modify the total behavior of solder joints. Smaller irreversible shear strains were observed in concurrent loading than in pure thermal cycling. The cyclic behavior of solder joints was reflected in the stabilization of cyclic inelastic strain. This behavior was possibly attributed to the microstructure evolution process of eutectic solder joints, where vibration contributes by straining the material in a faster pace.

Test results furthermore indicate that Miner's rule is not accurate for concurrent environments due to its lack of consideration of thermal and vibration interaction and scale effect. The effects of concurrent loading on product lifetimes were not discussed.

Eckert *et al.*: A Solder Joint Fatigue Life Model for Combined Vibration and Temperature Environments [EMFH09]

Eckert *et al.* discussed the lifetime prediction for lead-free soldered flip chips under vibration load in different temperature environments. Since the vibration was considered only at constant temperature, the discussion is not on multiple loading tests *per se* but the authors raise interesting points regarding multiple loading tests and the inclusion of this paper is thus justified.

The discussion is begun by noting that the temperature-dependence on vibration loading is not accounted for in most investigations on the matter. To investigate temperature effects on the vibration fatigue life the authors first subjected test assemblies to vibration at various constant temperatures. The PWBs were mounted with fixed boundary conditions on the short sides and free boundary conditions on the long sides and precisely controllable, easy-to-model harmonic excitation was used. To account for variations due to manufacturing and mounting the fundamental frequency of each PWB was determined individually. Prior to the lifetime testing experiments were run with various PWB deflections to determine the failure mechanism with respect to the board deflection. A failure mechanism shift from solder joint fatigue to a delamination of UBM from the chip metallization from 300 μm on was observed and thus deflections under 300 μm were used. The test parameters and results are summarized in Table 5.1. The observed failure mode was cracking of the bulk solder (no failures at the intermetallic phases were found). Furthermore, despite the differences in the shape parameter β between different temperatures, no differences in the failure type were observed.

Non-linear, temperature dependent FEA was then performed to investigate the elastic-plastic behavior of the solder joints. For this purpose a strip of PWB along with the test specimen was modeled. The deflection was raised stepwise and

Table 5.1: *Test parameters and results. [EMFH09]*

Group	Temperature [°C]	f_n [Hz]	Average deflection [μm]	η [cycles]	β	Coefficient of correlation
1	27	415	218	$5.06 * 10^9$	0.43	0.984
2	27	419	258	$1.00 * 10^8$	0.39	0.943
3	65	467	158	$3.46 * 10^8$	0.50	0.993
4	65	509	207	$8.13 * 10^6$	0.61	0.881
5	100	342	162	$2.34 * 10^6$	1.05	0.975
6	100	330	193	$1.01 * 10^6$	0.97	0.939

temperature-dependant material models were used to mimic the experimental testing conditions. From these simulations, the relevant failure parameters (maximum stress σ_a and plastic strain ϵ_{pl}) were extracted.

In the final part of the paper, data from experimental and simulation work was compiled in order to obtain a solder joint fatigue life model in form of the temperature-dependent Coffin-Manson-Basquin relationship. Linear accumulation of damage during the experiment was assumed and a strong trend to shorter lifetime at higher temperatures was derived.

Mattila and Kivilahti: Reliability of Lead-free Interconnections Under Consecutive Thermal And Mechanical Loadings [MK06]

In an attempt to simulate the effects of strains and stresses on the reliability of portable electronic products more realistically Mattila and Kivilahti thermally cycled (−45°C/+125°C, 15-min. dwell time, 750 cycles) or isothermally annealed (125°C, 500 h) lead-free test assemblies before a standard ([JB03], condition B: 1500G, 0.5 millisecond duration, half-sine pulse) drop test. The tests were conducted with chip-scale packed BGA components.

A reliability comparison between two different under bump metallization (UBM) materials on the component-side bump attachment pads was conducted first by drop testing the as-soldered assemblies. Electrochemical copper was found out to be more reliable than electrochemical Ni with a very thin layer of Au, and was used for the multiple loading tests. The multiple loading tests were conducted with two different PWB coatings, Ni(P)|Au or organic solder preservative (OSP). After the initial thermal loading (thermal cycle or isothermal annealing) the test assemblies were drop tested until failure. The test results are presented in Table 5.2.

The primary failure mode of assemblies drop tested in the as-soldered state was cracking of the reaction layers on either side of the interconnection. When drop testing thermally cycled assemblies the failure mechanism was observed to change

Table 5.2: *Estimated Weibull parameters. [MK06]*

PWB coating	UBM material	Pretreatment	η	β
Ni(P)|Au	Ni	-	6	1.7
Ni(P)|Au	Cu	-	10	1.5
Ni(P)|Au	Cu	thermal cycling	16	1.3
Ni(P)|Au	Cu	isothermal annealing	4	3.1
Cu|OSP	Ni	-	12	1.9
Cu|OSP	Cu	-	16	3.7
Cu|OSP	Cu	thermal cycling	18	1.8
Cu|OSP	Cu	isothermal annealing	4	3.7

from brittle facture through the intemetallic layers to intergranular fracture through the bulk of the solder. The change in the failure mode was attributed to recrystallization during thermal cycling. The recrystallization occurs first near the corner region of the interconnections, where the structure is most heavily deformed plastically and also where the cracks were typically observed to locate after drop testing. The local recrystallization of solder interconnection enhances cracks to nucleate in and propagate through the recrystallized regions and can explain the increase in the average drops to failure and the large deviation.

The assemblies isothermally annealed before the drop test exhibited yet another failure mode, the cracking of Cu_3Sn layer on the component side of the interconnection, in addition to performing significantly weaker than the other test assemblies. Detailed microscopic studies revealed that a great amount of voids had formed inside the Cu_3Sn layer. These voids provide almost continuous paths for crack propagation and explained the observed decrease in the average drops to failure.

The type of PWB coating was observed to affect the drop test reliability only in the as-soldered state, where Cu|OSP was found out to be more reliable than Ni(P)|Au. It was concluded that both pretreatments affected the drop test reliability, but due to the large dispersion of drops to failure of the thermally cycled boards the difference between the average drops to failure of the thermally cycled and the as-soldered assemblies was not statistically significant.

Perkins and Sitaraman: A Study into the Sequencing of Thermal Cycling and Vibration Tests [PS08]

Perkins and Sitaraman investigated solder joint reliability under sequential application of accelerated thermal cycling (ATC, −25°C/+105°C, two cycles per hour) and (sinusoidal out-of-plane) vibration tests. The experiments were conducted using

daisy chained ceramic column grid array (CCGA) components, popular in high I/O applications in harsh environments, and high melting point 90Pb10Sn solder.

The testing was begun with single load tests where only one type of loading was applied until failure was observed. The mean number of ATC to failure was 1640 cycles (σ=134) and significant deformation of the solder columns was observed. It was further discussed that crack initiation occurs very quickly in thermo-mechanical loading (in the first 10% of the fatigue life according to Darveaux [Dar93]) and the majority of life is spent in crack propagation. Vibration testing was conducted by clamping the test assembly boards on their shorter edges and then characterizing the natural frequency f_n of each assembly. After characterization each assembly was subjected to 1G input acceleration at f_n until failure. The mean of f_n was 308 Hz (σ=14.2) and the mean number of cycles to failure was 1.83E6 (σ=1.06E6). The high variations in the number of vibration cycles were attributed to variations in G_{out} (mean 47.3G, σ=8.4) due to potential variations in the clamping of the test assemblies. The observed failure mode was the cracking of bulk solder, with the cracks predominantly on the PWB side of the solder column.

The multiple loading conditions were then studied by sequential two step loading. In T-V sequence the assemblies were first subjected to ATC (such that approximately one half of the expected fatigue life N_T was consumed, *i.e.* $n_T/N_T \approx 0.5$) followed by vibration to solder joint failure. In V-T loading vibration (so that approximately one quarter of fatigue life N_V was consumed, *i.e.* $n_V/N_V \approx 0.25$) was followed by ATC to solder joint failure. Since the loading in both sequences was carried to out to solder joint failure, the expected CDIs of the sequences should be same if the sequence of loading has no effect. Based on the results, median CDI values for the T-V (0.66) and V-T (0.96) sequences were calculated and it was concluded that the T-V sequence is harsher than the V-T sequence. The difference was attributed to the severe deformation and microstructural changes that occur in thermal cycling which initiate cracks quickly and thus quicken the subsequent vibration loadings. The failures that occurred during the two step loadings were not analyzed.

As Miner's Rule (equation 5.2) clearly proved inadequate to predict the fatigue-life, a nonlinear cumulative damage law was developed to account for the sequence affect and the differences in damage mechanisms. The only requirements for the model were simplicity and its applicability for sequential loading. The model was developed according to Marco and Starkey [MS54] by incorporating an exponent m_i that varies for each load type and on the sequence of loads into each fatigue life ratio. Fitting the exponents for T-V and V-T sequences respectively, the following equations were attained:

$$CDI_{T-V} = \left(\frac{n_T}{N_T}\right)^{0.47} + \left(\frac{n_V}{N_V}\right)^{0.70} \tag{5.3}$$

$$CDI_{V-T} = \left(\frac{n_V}{N_V}\right)^{0.91} + \left(\frac{n_T}{N_T}\right)^{0.93}. \tag{5.4}$$

Qi *et al.*: Modeling of Combined Temperature Cycling and Vibration Loading on PBGA Solder Joints Using an Incremental Damage Superposition Approach [QOP08]

Qi *et al.* explored the effects of concurrent temperature cycling and vibration loadings using both experimentation and simulation. A plastic BGA was subjected to thermal cycling (−50°C/150°C, 24 min ramp time and 15 min dwell time), random vibration (25°C/0.1 G^2/Hz, frequency from 100 to 1000 Hz) and combined temperature cycling and random vibration loading. The reliability of the test assemblies was also assessed by linear damage superposition and incremental damage superposition simulations.

The experimental results obtained by Qi *et al.* are presented in Table 5.3. It is apparent from the test results that combined loading has a much higher damage rate than either one of the single loadings. The time to 50% failure in concurrent loading was observed to be only 3.8% compared to pure thermal cycling and 5.6% to pure vibration loading. Albeit the differences observed in the shape parameter β that might suggest different failure modes and mechanisms under different loading conditions, the failure modes and mechanisms were not discussed.

Table 5.3: *Estimated lifetimes and Weibull parameters. [QOP08]*

Loading	time to 50% failure [h]	β	γ [h]
thermal cycling	3346	1.32	1793
vibration	2242	2.60	693
concurrent	126	0.82	8

In linear damage superposition approach (LDSA, eq. 5.2) it was assumed that the failure site and mechanisms are the same regardless of the loading applied and that the damage rate is constant over the stress application. With these assumptions and the experimental results, the time to 50% failure in concurrent loading was estimated as 1438 h. The value is over eleven times higher than the experimental result and demonstrates that the approach is not suitable for these conditions.

The more complex incremental damage superposition approach (IDSA) also assumes a constant damage rate over the stress application. However, the loadings are simulated separately with vibration damage partitioned in fixed increments and the impact on temperature induced mean stress incorporated on the vibration induced damage segments. The approach is based on detailed FEA and in-time experimental strain measurements. Using this model, the life expectancy under combined loadings is calculated as 351 h. The result was a significant improvement over the classical LDSA, but still nearly triple the value obtained in experimental results.

Qi *et al.*: A Rapid Life-Prediction Approach for PBGA Solder Joints Under Combined Thermal Cycling and Vibration Loading Conditions [QOP09]

In their previous article [QOP08], Qi *et al.* found the IDSA more representative for the concurrent temperature cycling and vibration loading than the classical LDSA. However, due to its complexity and costs (both in time and resources), the method was not considered an efficient tool for industrial engineers and thus a new rapid prediction approach was developed. The rapid prediction approach presented in this paper aimed to assess the life expectancy of solder joints under concurrent thermal cycling and vibration loads. The same concurrent test results as in the authors previous article were utilized to provide comparison with experimental data.

The rapid life prediction method includes three major parts: first the damages under single loadings are assessed and then superposed. To assess the temperature cycle a strain range based damage was used while a generalized Manson-Coffin damage model was used for the vibration damage. The vibration damage was calculated at three different temperature levels, high (150°C), mean (50°C) and low (−50°C). The accumulated vibration damage was then computed by incrementally adding the damages due to vibration loads at each discrete temperature level. The overall damage was then estimated by combining the normalized single damage fractions. A predicted lifetime expectancy of 730h was calculated with this method. The results obtained experimentally and by the three models (LDSA and IDSA in the previous article and rapid life prediction in this article) are summarized in Table 5.4. Although the rapid life prediction method provides better results than the classical LDSA, it is clearly seen that the method overestimates the fatigue lifetimes of solder joints under concurrent loading, estimating lifetimes over five times higher than the experimental results indicate.

Table 5.4: *Estimated experimental lifetimes and calculated lifetime expectancies for concurrent temperature cycling and vibration loading. [QOP08, QOP09]*

Loading	time to 50% failure [h]	Model	time to 50% failure [h]
thermal cycling	3346	LDSA	1438
vibration	2242	IDSA	351
concurrent	126	Rapid life prediction	730

Further observations were made based on the developed rapid life prediction model. The total damage under combined loading is predicted to be greater and the life shorter than with vibration loading at room temperature alone, if:

- damage caused by thermal cycling is equal or greater than the damage caused by vibration loading or

- the vibration response at high temperature significantly increases and the tensile mean stress effect is significant (*e.g.* longer low temperature dwell and larger tensile mean stress).

However, if the vibration response at low temperature significantly decreases and the compressive mean stress effect is significant (*e.g.* longer temperature dwell and larger compressive mean stress), the total damage under combined loading is predicted to be less and the life longer than with pure vibration loading at room temperature.

Xu *et al.*: Impact of Thermal Cycling on Sn-Ag-Cu Solder Joints and Board-Level Drop Reliability [XPC08]

Xu *et al.* studied the effect of thermal cycling on drop reliability by using lead free Sn-3.0Ag-0.5Cu (SAC) soldered daisy chained fine-pitch BGA assemblies. Standard [JB03] drop impact tests were conducted before and after thermal cycling (500, 1000 and 1500 thermal cycles). A half-sine 690G shock pulse with a 2ms period was used in drop testing and the thermal cycling was conducted with temperature profile of $-40°C$ to $+125°C$ with 1h cycle time and dwell times of 15 minutes at each temperature extreme. Two types of surface finish, electroless nickel (phosphorus)/immersion gold (ENIG) and Cu-OSP, were used on the test assemblies.

Table 5.5: *Drop lifetimes after temperature cycling. [XPC08]*

Number of thermal cycles	Lifetimes	
	Cu-OSP	ENIG
0	29	21
500	5	13
1000	2	9
1500	2	8

The drop test results are summarized in Table 5.5, and it is clearly seen that the drop test reliability of both assembly types was significantly reduced by thermal cycling. While being initially more reliable, the drop test reliability of Cu-OSP surface finish collapsed after thermal cycling. This result was explained by the observed growth of Kirkendall voids between the intermetallic and the Cu pad after thermal cycling. The void formation changed the crack path from the Cu_6Sn_5 layer to Cu_3Sn, significantly lowering the drop test reliability. With the ENIG surface finish, the consumption of Ni for the formation of NiCuSn intermetallics induced vertical voids in the Ni(P) layer, leading to crack propagation through the Ni(P) layer after 1000 and 1500 cycles. It was concluded that the effect of thermal cycling aging on interfacial voiding process and subsequently drop impact lifetime is crucial.

5.3 Summary of the Current Status of Multiple Loading Tests

The previous section summarized the relevant articles on multiple loading tests. Based on the published results it is clear that the combined interactions of thermomechanical and mechanical loads are not completely understood and more research on the subject is required before exploiting the various benefits associated with multiple loading tests. However, there are some issues on which all the associated seem to agree upon.

A general consensus is that the lifetimes under multiple loads are shorter than the respective lifetimes under single loads. This is further verified by experimental results: only Mattila & Kivilahti [MK06] reported an increase in lifetimes under multiple loads. Albeit a slight increase in the average number of drops to failure was observed when thermal cycling was performed before the drop test, the difference was not statistically significant due to large dispersion in the number of drops failure.

It is further agreed that the linear damage super-position rule (equation 5.2) is inaccurate for fatigue life prediction under multiple loads. Especially under concurrent loading conditions the rule is found to overpredict product lifetimes, with reported results [QOP08] predicting solder joint life even eleven times higher than the experimental results indicate. To overcome the shortcomings of the rule, some authors have tried to simply lower the value of $CDI_{critical}$. However, the lowering of $CDI_{critical}$ is deemed as arbitrary and inconsistent for different loadings.

As the linear damage super-position rule has been deemed insufficient, several different nonlinear damage models have been proposed and developed for fatigue life prediction. These include the IDSA [QOP08], rapid life prediction approach [QOP09] and the nonlinear cumulative damage law employed by Perkins and Sitaraman [PS08]. Despite the complexity of and the effort put into the methods the results can only be considered as indicative. This further proves that the complex interactions between different loadings are not completely understood.

When drop tests were employed with thermomechanical loading methods, the authors conducted detailed failure analyses with the results and the failure modes were extensively discussed in their publications [MK06, XPC08]. However, when vibration loading was used as the mechanical loading method, no detailed failure and root cause analyses were conducted or the results were not discussed in the publications. Perkins & Sitaraman [PS08] provided detailed solder joint failure mechanism and microstructural analyses for the single load tests, but the failure modes and analyses for the sequential tests results were omitted. Qi *et al.* [QOP08] only mention that failure analysis was performed and the failure sites were identified at the interface of the solder joint and PWB with the observed failure mode identified as solder joint fatigue caused by environmental stress conditions. Albeit the authors have been keener on predicting fatigue lifetimes under multiple loads than performing failure analysis, significant information might be gained from detailed failure analysis considerations. This is clearly one aspect, where more research is needed.

To summarize, compared to single load tests, multiple loading tests are more complicated and laborious and slight differences in test setup or structure might lead to totally unpredicted results. How the failure mechanisms are accelerated and what are the causes that eventually lead to failure during multiple loadings depend on a number of reasons such as the applied loads, loading frequency and order, test parameters and structure or the material of the test assemblies. It is still not clear how to choose and combine separate loading methods in a meaningful way. Furthermore, the complex interactions between different loads are currently not completely understood and thus more research on the topic is needed before the various benefits that are associated with multiple loading tests can be reaped.

Chapter 6

Purpose of the Thesis

This work was carried out in the Electronics Integration and Reliability (EIR) unit at Department of Electronics at the Aalto University School of Science and Technology. It is a part of a research project called Development of A Novel Reliability Testing Method of Consumer Electronics. The project is jointly funded by Finish funding agency for technology and innovation (TEKES), Nokia, Efore, National Semiconductor Corporation (NSC) and NXP Semiconductors.

The project was divided to three work packages. The first work package aimed to develop a new test system capable of producing discrete shock impacts with higher accuracy and better repeatability than the currently commercially available methods. The objective of the second work package was to establish a new cost-efficient testing method based on the concept of concurrent reliability testing that simulates the operational loadings of electronic products as realistically as possible. In the third work package a new lifetime prediction model was pursued that would take into account, for the first time, the microstructural evolution of components' solder interconnections that occurs during the operation of products.

The purpose of this thesis is closely related to the second work package. Two different test cases were implemented to account for a wide range of applications:

1. The high-density test setup was designed to closely simulate the operation of a real portable multimedia device.

2. The high-power test setup was designed to represent the stresses and strains experienced by an advanced high power unit (such as an advanced power supply unit).

This thesis covers the second (high-power) case. The main objective of the case is to develop a new concurrent reliability testing method as an alternative for more comprehensive and efficient reliability testing of high power electronic assemblies. The goal is to produce more realistic failure modes and mechanisms in a substantially accelerated fashion for lifetime prediction. The main objective of this thesis is to clarify the failure modes and mechanisms taking place independently under single loads and to find out how the concurrent combination of the loads affects the lifetimes, failure modes and mechanisms.

Chapter 7

Materials and Methods

In the experimental part of this thesis a concurrent testing method was developed. This chapter introduces the methods and materials used and the results and conclusions are presented in the following chapters. The order of this chapter is such that the selected component and loading conditions are discussed first in section 7.1, the test assembly is presented in section 7.2 and the methods required for the pre-test characterization of the test assemblies are discussed in section 7.3. The single load reference tests methods are then presented in section 7.4 before introducing concurrent testing methods (7.5) and the final section (7.6) of the chapter describes the failure analysis methods used.

7.1 Component and Loading Conditions

The tests were conducted with Infineon's OptiMOS 3 SuperSO8 Power-Transistor. The component, presented in Figure 7.1, is a surface mounted power metal-oxide-semiconductor field-effect transistor (MOSFET) with a low conduction loss and fast switching speeds. It is suitable for low conduction loss applications (like motor control and hot swap), and particularly to those that need to be optimized for very high switching (such as power supplies or class D audio equipment).

The operation of MOSFET can be separated into three different operation modes, each of which has a special function in the following experiments. The operation modes are dependent on the voltages at the terminals (gate, source and drain) of the transistor. A very simplified description of the operation modes and their prerequisites is given here.

- **Cutoff mode** ($V_{GS} < V_{th}$): The transistor is turned off and there is no conduction between the drain and source.
- **Triode mode** ($V_{GS} > V_{th}$ and $V_{DS} < [V_{GS} - V_{th}]$): The transistor operates like a resistor (also referred as the ohmic mode), allowing current flow between the drain and source.

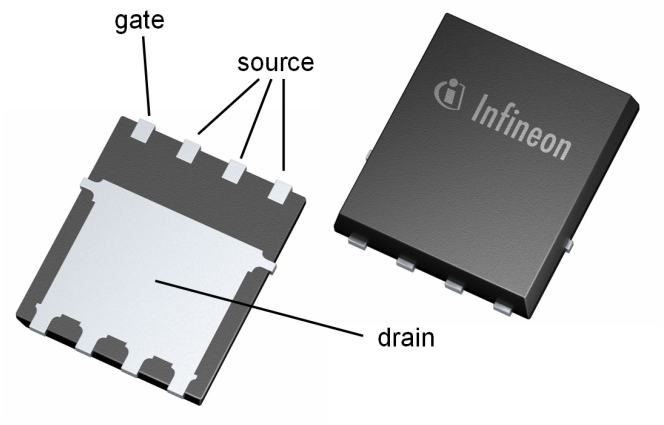


Figure 7.1: *Bottom and top view of Infineon OptiMOS 3 SuperSO8 power transistor. Image adapted from [Inf].*

- **Saturation mode** ($V_{GS} > V_{th}$ and $V_{DS} > [V_{GS} - V_{th}]$): The transistor allows current flow between the drain and the source with a negligible resistance (also known as the active mode).

V_{th} is the threshold voltage of the transistor, V_{GS} is the voltage between the gate and source terminals and V_{DS} is the voltage between the drain and source terminals. For Infineon's OptiMOS 3 SuperSO8, $1V \leq V_{th} \leq 2.2V$, when $V_{DS} = V_{GS}$ and i_D (current from drain to source) $= 250\mu A$ [Inf06].

Many electronic devices are mainly thermally stressed owing to their internal heat dissipation. Especially in power electronic components, such as the component used in this study, local heating of components can lead to drastic changes in the microstructures of materials, for example in solder interconnections. In these cases the thermo-mechanical stress of solder interconnections is related to varying temperature levels caused by the components themselves. As opposed to the more traditional thermomechanical testing methods (temperature shock and cycling), where the effect of thermal gradients is disregarded, power cycling offers a better representation of the actual use loading conditions. Furthermore, power cycling incorporates the effect of electrical current into the test structure and the implementation of other loads is more convenient than in thermal shock and cycle tests. For these reasons, power cycling was chosen as one reliability test method. In an attempt to portray the actual use environment more realistically and to accelerate the tests a mechanical loading parameter in the form of vibration was incorporated to the test procedure. The purpose of the vibration loading is to stimulate the various mechanical loadings experienced by components during their product life. The chosen components are common in automotive electronics, where they are more often exposed to various vibrations originating from their surroundings than discrete shock impacts. Thus vibration loading can be considered as a good representation of the mechanical loads experienced in typical field use environments.

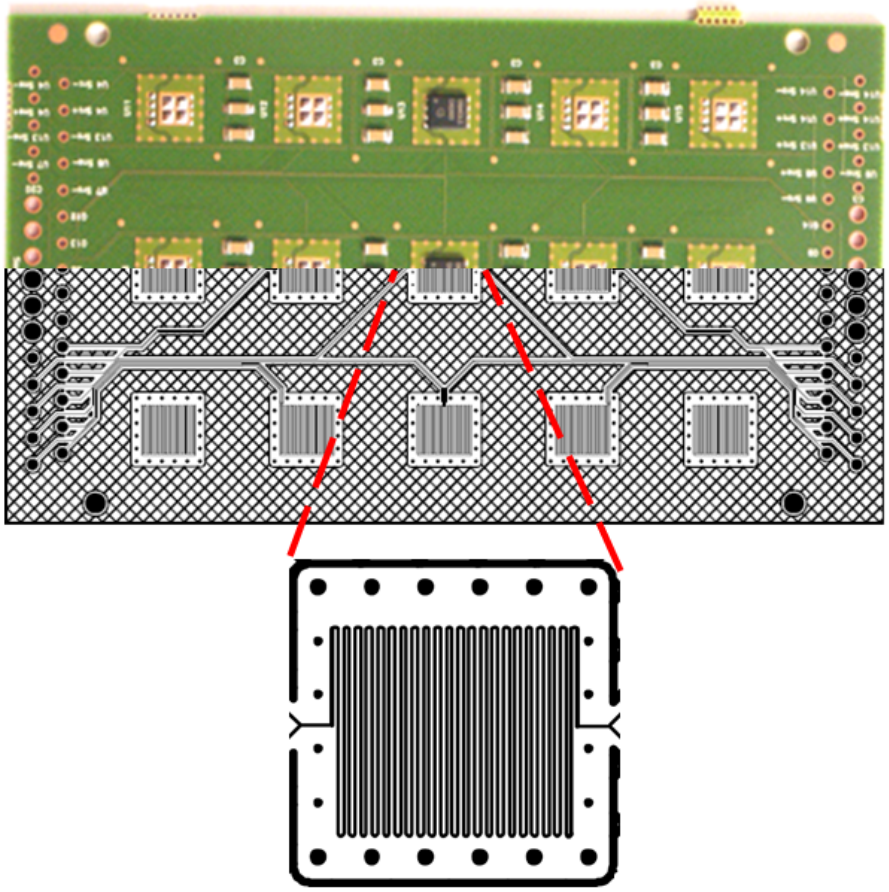


Figure 7.2: *Test assembly and its layout with a magnification of the resistor network for temperature measurements.*

7.2 Test Assembly

A 132 x 77 x 2 mm JEDEC drop test derived [JB03] eight-layer FR-4 printed wiring board (PWB), one for each component type, was specifically designed for this project. The PWBs were manufactured by Austria Technologie & Systemtechnik. The components were mounted on the PWBs at the laboratory's SMT assembly facility by using Multicore's Sn3.8Ag0.7Cu (wt.-%) solder paste. Due to the limited amount of components, the boards were mounted with three components (at component locations U3, U8 and U13). A picture of the test assembly and its layout is presented in the upper part of Figure 7.2.

It should also be noted that besides the 15 transistor locations, the test board features 36 possible locations for multilayer ceramic capacitors and some test assemblies were further mounted with 36 capacitors. The capacitors, visible in the top part of Figure 7.2, are situated between each transistor column, with three locations between each two transistors. However, the capacitors have no role in this thesis and are not discussed further here.

The testboard incorporates a thin copper resistor network below the used component interconnection areas for temperature measurement. The temperature measurement is based on the resistance-temperature (R-T) relationship of copper: within the operating specification temperatures of the components the R-T relationship is almost linear [Gri99]. Within the linear range, $T_1 < T < T_2$, the R-T relationship can be expressed as

$$R = R_{Ref}[1 + \alpha(T - T_{Ref})], \tag{7.1}$$

where R_{Ref} is resistance in reference temperature, α is the temperature coefficient of resistance (1/°C) and T_{Ref} is the reference temperature. Rearranging for temperature gives

$$T = T_{Ref} + \frac{(R/R_{Ref}) + 1}{\alpha}. \tag{7.2}$$

Thus, by measuring the resistance of the resistor network, the network temperature can be determined with the help of equation 7.2 providing that the resistance (R_{Ref}) at a reference temperature, for example room temperature, (T_{Ref}) is known. Since the resistance of the resistor network is relatively low (in the scale of few ohms), to accurately measure the resistance changes induced by temperature (milliohms/°C), terminals for four-point resistance measurement were integrated onto the test boards. A magnification of the resistor network layout is presented in the lower part of Figure 7.2.

The test board features individual terminals for the component gates, while the drain and source connections are common for all the mounted components. In practice, this means that while the operation mode of each transistor can be individually controlled by its gate voltage, the board allows only parallel health monitoring when operating the transistors in the saturation mode.

7.3 Pre-testing

The objective of pre-testing was to characterize the test board properties for optimal design of the actual tests, as well as design and assemble all the equipment required for actual testing.

Due to PWB manufacturing tolerances, the performance of the resistor networks on the test boards is susceptible to variations. To measure the level of discrepancy between the specimens and to verify the temperature-response of the resistor networks a series of (four point) resistance measurements were conducted in different ambient temperatures. The resistance measurements were conducted by placing the specimens in to an oven (Heraeus UT 6) and measuring the resistance with the help of a data logging unit (Agilent 34970A) and a measurement card (Agilent 34901A) from room temperature up to 125°C in steps of 5°C. The tests were conducted with eight boards and using five component locations each (locations U3, U7, U8, U9 and U13, see Figure 4.2). The measurement results for the centermost component locations (U8) are presented graphically in Figure 7.3. Albeit small deviations in the initial resistance value (for the 40 measured resistance networks, the average resistance measured at room temperature was 4.24Ω with a standard deviation of

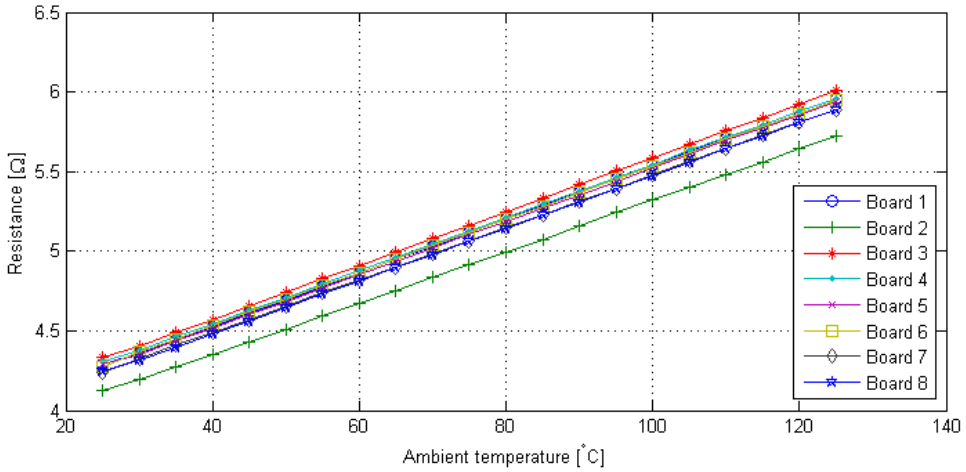


Figure 7.3: *The temperature response of the centermost resistor networks (beneath component location U8).*

0.057Ω), a linear temperature response in accordance with equation 7.1 was observed. It was concluded that by knowing the initial resistance the temperature of the resistor network can be determined with an accuracy of ±2°C.

To characterize the mechanical properties of the test assemblies, several boards were equipped with Kyowa's biaxial strain gauges (KFG-2-120-D16-11L3M2S). The principle of resistive strain gauges is based on the change of a materials specific resistance due to elongation or contraction. As an external tensile force is applied to the strain gauge, its resistance increases due to elongation and decreases when a compressive force contracts it. Typically a grid shaped sensing element (see Figure 7.4) is tightly glued to a measured object so that it may elongate or contract according to the strain borne by the measuring object. The strain is then directly proportional to the change in resistance and if the properties of the strain gauge are known the strain can be calculated. [Kyo06]

The natural frequencies of the test boards were determined with strain gauges before actual testing. The mechanical properties were first characterized with unassembled boards, where the strain gauges were glued directly on top of the component locations. As external wires glued to the board were observed to skew the strain measurement results, the strain gauge wires were cut and bonded to the capacitor pads and the capacitor terminals on the edges of the boards were then utilized to minimize the effect. The strains were then measured with National Instruments (NI) data acquisition system (NI PXI-6052E/SCXI-1520/SCXI-1314 with sampling frequencies up to 100000 Hz) while additional data processing (if required) was conducted with Matlab software. A first order approximation of the natural frequency was gained by drop testing a test board equipped with strain gauges and taking a discrete Fourier transform (DFT) of the strains. The results were then verified with the vibration tester by measuring the strains at various frequencies.

When characterizing the temperature dependence of the strains, due to the chosen heating method (covered in subsection 7.4.2), the characterization had to be con-

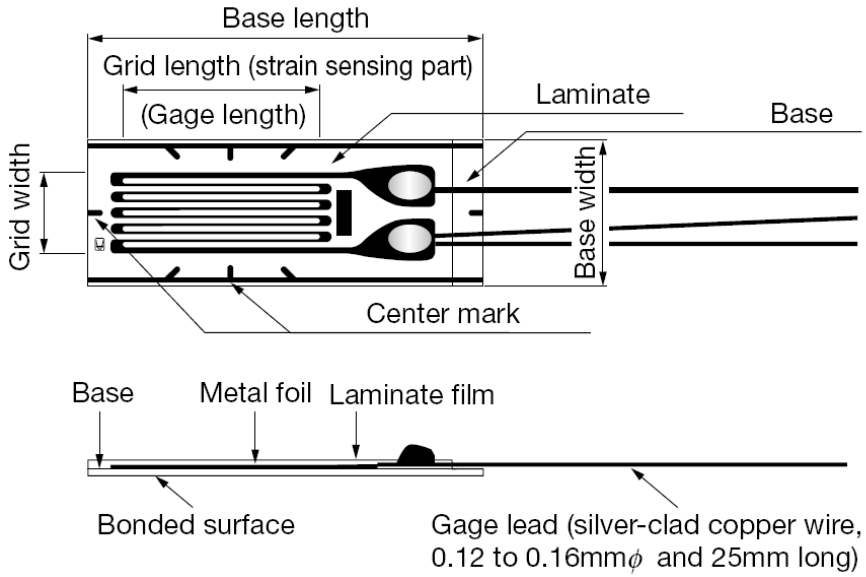


Figure 7.4: *The structure of a typical resistive strain gauge pictured from the top (upper picture) and from the side (lower picture). Image taken from [Kyo06].*

ducted with assembled boards. The strain gauges were thus glued directly beneath the component locations on the back side of the board. Because the capacitor pads were only routed on the top side of the boards, the gauge wires were glued to the boards. The temperature dependence was studied by heating the components with the chosen method and measuring the strains on various amplitudes and frequencies.

Although the strain gauges employed in this study were biaxial, mostly longitudinal strain data (*i.e.* strains parallel to the long side of the test assembly) was used and all further discussion refers to longitudinal strains unless otherwise specifically stated. Furthermore, due to reasons clarified in the next section, only the centermost component (location U8) was chosen for monitoring and, thus, the strain behavior was mostly characterized at that location.

When analyzing the results (in subsection 8.1.2), the gluing of strain gauges and external gauge wires to the board was observed to affect the measured strains. To overcome this effect in the future, the idea of internal integrated strain gauges was contemplated. By implementing a strain gauge pattern (see Figure 7.4) into a test boards conductive copper layers several possible advantages could be gained. Most importantly, the integrated strain gauges would efficiently minimize the changes in human errors in attaching the strain gauges. As the wiring would be routed internally to board perimeter, the effect of external wiring and gluing would be minimized and thus more comparable results between different boards would be gained. However, to accurately measure the changes in resistance, relatively large (in the scale of centimeters) resistive elements have to be used and the spatial resolution of these gauges would thus be limited. Nonetheless, these integrated gauges would efficiently eliminate the need for separate external strain gauges in general strain measurements and characterization, and cost savings could thus be gained. Furthermore, especially in large amplitude vibration the lifetime of external strain gauges

was very limited. The lifetimes of the internal gauges are assumed to be comparable to the boards copper conductor lifetimes, and the gauges are expected to remain operational significantly longer than the external gauges. As every board would be equipped with a strain gauge and due to the long assumed lifetimes of the gauges, the strain amplitude of each board under test could be constantly monitored, allowing for better control of the mechanical loading conditions and the test procedure.

The test boards utilized in this study were already designed, manufactured and assembled, and the idea could not be explored further within this project. However, the idea is not limited to this particular study and might be worthy of more research in the future. For future considerations, if the internal strain gauges are not feasible and strain characterizations of the test boards are needed, it is recommended that the test board is designed with several contact pads for strain gauges. These contact pads should be then routed internally to the board perimeter to minimize the effect of external wiring and gluing when strain gauges are attached.

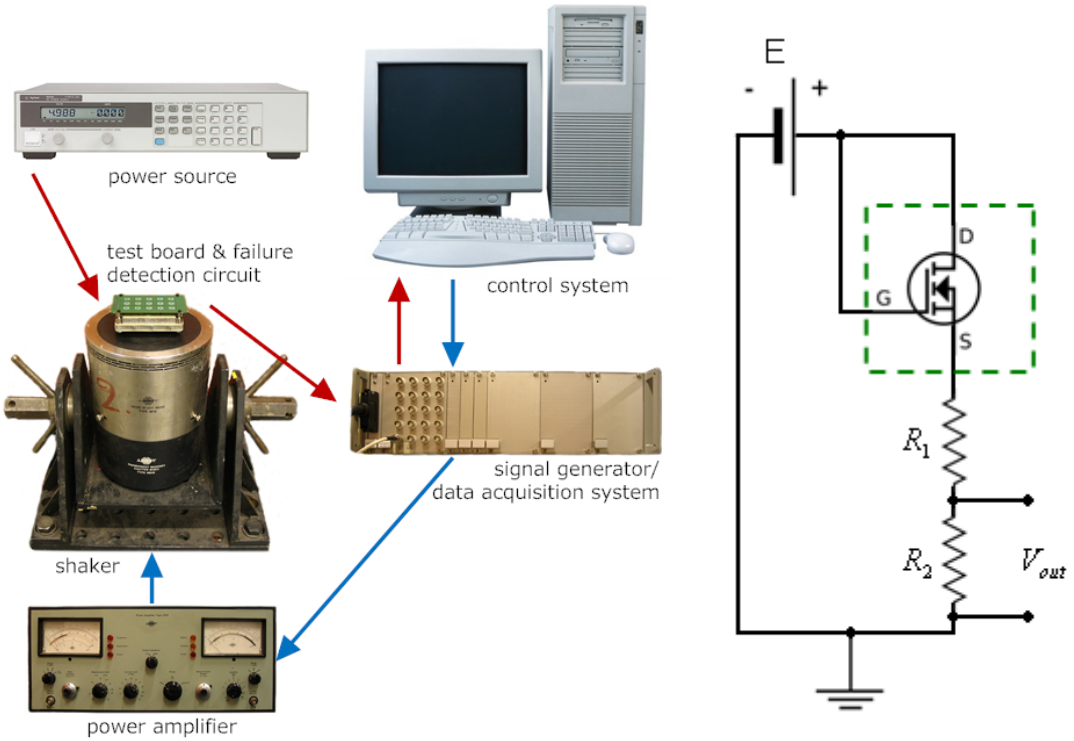
7.4 Single Load Testing

In order to fully understand the loadings and failure mechanisms in concurrent testing, separate vibration and power cycling tests were conducted as a baseline measurement.

7.4.1 Mechanical Loading

A schematic illustration of the measurement system used in pure mechanical loading is presented in Figure 7.5(a). The test equipment consists of Brüel & Kjær's electromagnetic shaker (Permanent Magnet Type 4805, Mode Study Head Type 4814) and power amplifier (700W Power Amplifier Type 2707), high speed data acquisition system (Microstar DAP 5200a), which was also used as a signal generator, and a computer with a specifically created NI Labview program to control the system. A single frequency sine signal was used with the output amplitude of the signal generator set to 5 V. The actual excitation amplitude was then manually adjusted by setting the amplification of the power amplifier to a desired level. The fixation table on top of the electromagnetic shaker unit features four base plate standoffs, where the test boards were mounted using four screws, one at each corner of the board. The boards were attached with three millimeters thick hexagonal head shoulder screws using a torque of 1 Nm.

The design of the test board only enables parallel component health monitoring, *i.e.* when operating multiple components in saturation mode, only the failure of all components selected for health monitoring is detected. Due to this limitation, only the center component (component location U8) on each board was selected for monitoring. A schematic representation of the health monitoring circuit is presented in Figure 7.5(b). The health monitoring is carried out by setting the measured component in saturation mode (and the other components in cutoff mode) and applying a voltage difference (power source E: Agilent 6642A) of 5 V between its



(a) (b)

Figure 7.5: *(a): Schematic illustration of the measurement system used in pure mechanical loading. The blue arrows represent the controlling signals while the red arrows represent the failure detection signals. (b): The schematic presentation of the circuit used for failure detection in pure mechanical loading. The dashed green square indicates the test assembly.*

drain and source. Two external resistors (R_1 and R_2) were connected in series with the source and the voltage over the resistor R_2 (V_{out}) was constantly monitored with the data acquisition system that has a sampling frequency of 40000 Hz. If the measured voltage (V_{out}) was observed to drop from a steady state value of 1.5 V to beneath the threshold value of 1 V the test was automatically stopped and the failure time logged. If a consecutive undershoot of the voltage was observed within ten seconds of restarting the test, the component was classified as failed and removed from the test.

As the interconnection damaging caused by power cycling was expected to be relatively slow compared to mechanical loading and cannot be considerably accelerated, special attention was paid to the severity of the vibration loading. It was estimated that in order to see any effects on the interconnections from power cycling on concurrent tests, the tests should last at least one full calendar week. To characterize the vibration lifetimes and to discover suitable amplitude levels for concurrent testing, vibration lifetime measurements were first conducted with relatively high amplitudes. Then consecutive lifetime measurements were conducted with gradually

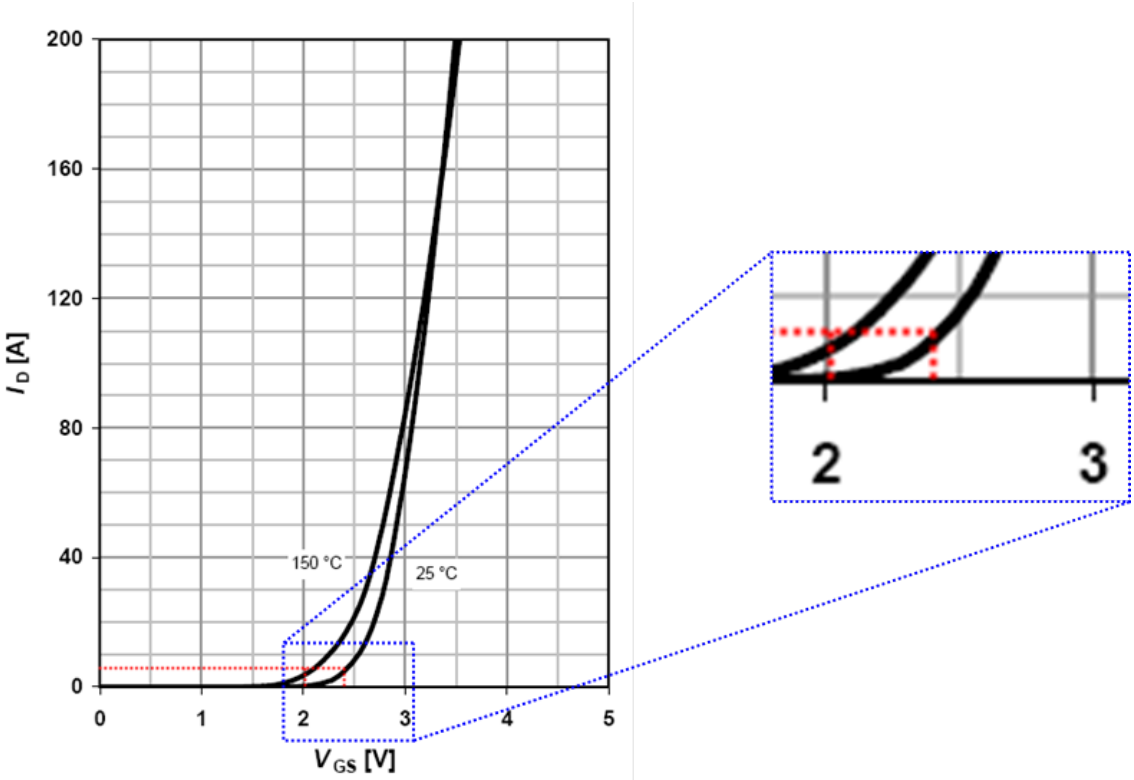


Figure 7.6: *The typical temperature dependant transfer characteristics of Infineon's OptiMOS 3 power transistor, with the approximated operating range highlighted in red and a magnification of the operating area. Image adapted from [Inf06].*

smaller vibration levels to create a trend line graph of the lifetimes. Based on this data suitable amplitude levels for concurrent testing were then extrapolated and experimentally verified.

7.4.2 Power Cycling

The power cycle tests were conducted with a square on/off cycle. A 15 minute on / 15 minute off –cycle profile was decided upon with targeted interconnection temperature ranges of 120°C during the power on –period.

In power cycling the heating of the components is by definition achieved by an electric current. In this study, the transistors were locked to the triode mode by their gate voltage and a voltage difference was then applied between the drain and the source. As the transistor operates like a resistor in triode mode, the voltage difference resulted in a current flowing through the transistor and consequently heating up the component.

The test parameters were determined experimentally. In addition to the gate voltage the operation of the transistor at the triode mode is affected by temperature (see Figure 7.6), especially when operating with relatively low (in the scale of few amperes) currents. As the transistor heats up, it allows more and more current to flow through, heating the transistor even more. To stabilize the current flow

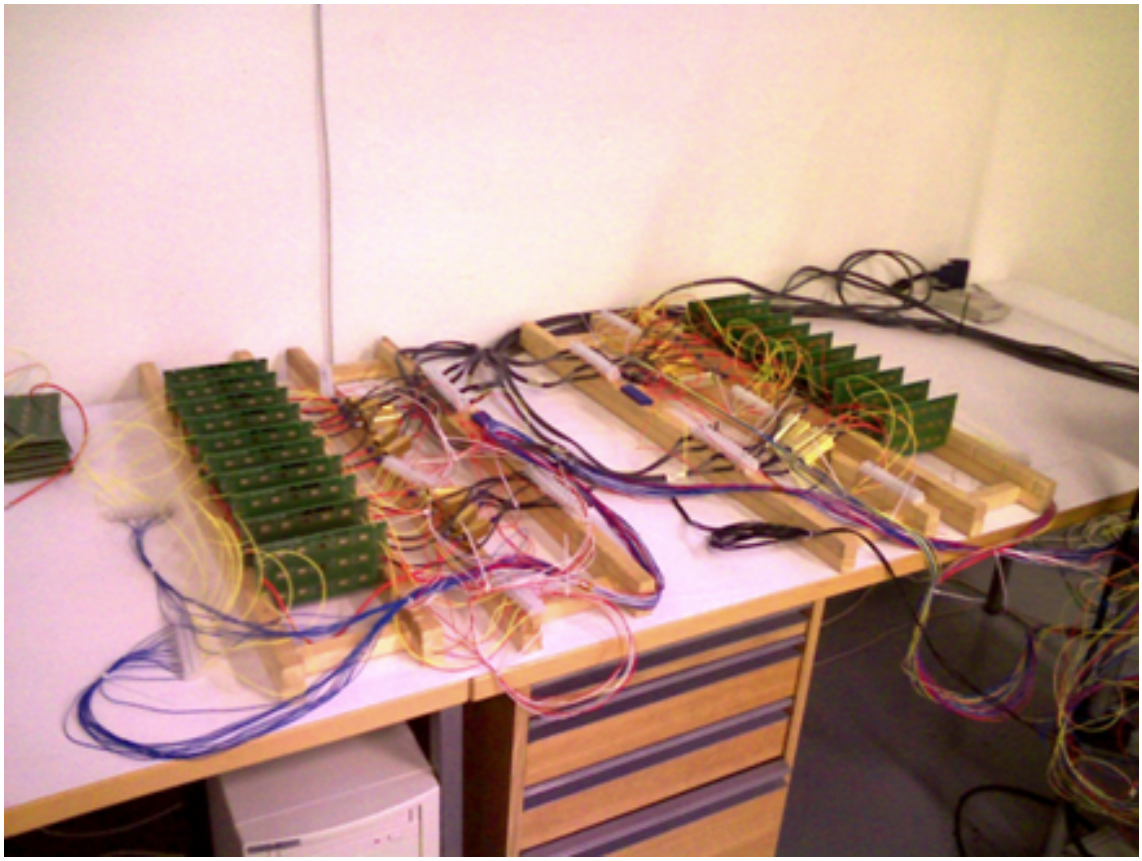


Figure 7.7: *The power cycling test bench.*

and to avoid overheating the transistor, a high power bias resistor was connected in series with the drain. The resistance of the bias resistor (1Ω) is large compared to the resistance of the transistor in triode mode (in the scale of milliohms) and the temperature effects on current flow are thus significantly decreased. The test parameters were then determined by first seeking out a current level on which the temperature response of the transistor was controllable. Then the gate voltage was set to reach the targeted temperature levels. Due to component variances, this had to be done individually for each component with the help of a potentiometer. This procedure resulted in a voltage of 6 V between the drain and the source, a drain to source current of approximately 4.4 A and gate voltage of approximately 2.1 V.

A customized test bench was constructed for the simultaneous power cycling of multiple test boards. The core of the test bench (Figure 7.7) is a PC workstation with NI Labview environment. In addition to the fore mentioned workstation and components, the test bench consists of:

- One high power laboratory power supply (Agilent 6671A) to power the test assemblies
- One data logging unit (Agilent 34970A) with three 20-channel measurement cards (Agilent 34901A) for continuous temperature monitoring of the test samples via four-point resistance measurements

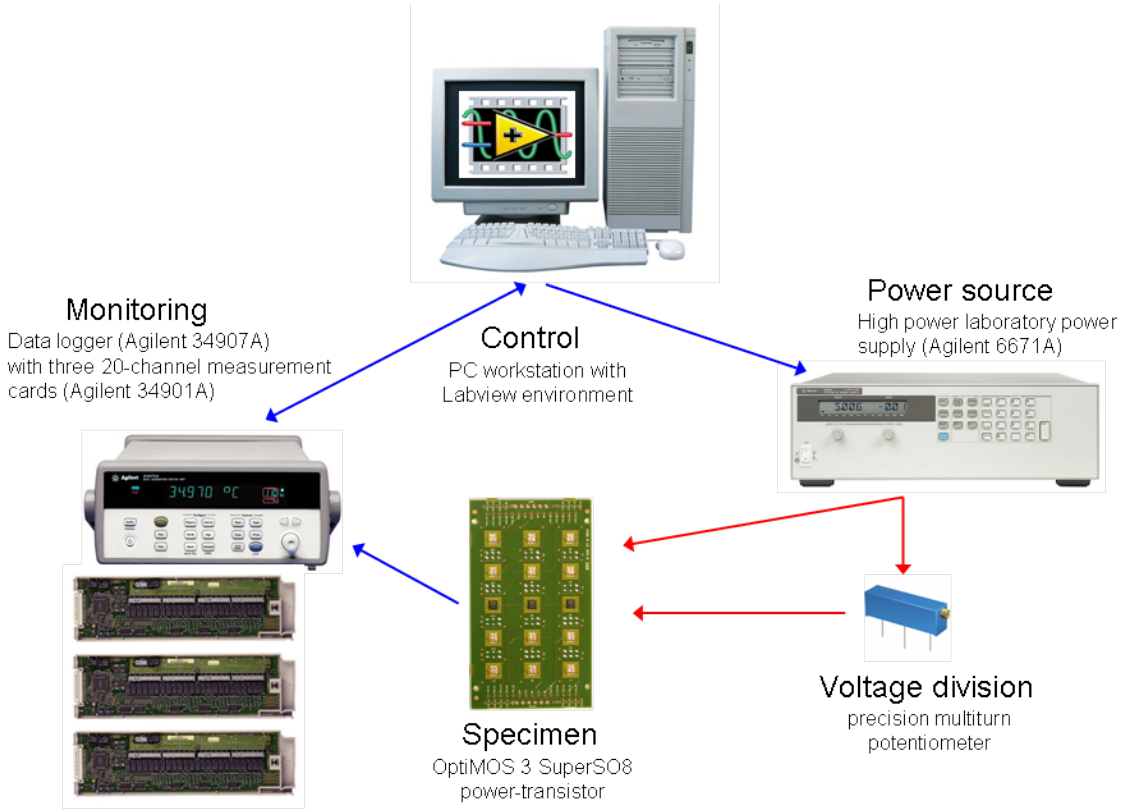


Figure 7.8: *Schematic illustration of the measurement system used in power cycling. The blue arrows represent the control and measurement signals while the red arrows indicate the power flow.*

- One GPIB-USB interface (Agilent 82357A) to connect the power source, data logging unit and workstation

A specifically created NI Labview program is then used to drive the power supply according to the predetermined power cycle parameters. Furthermore, the program simultaneously enables the continuous electrical monitoring of the test specimen by measuring and saving the four-point resistance of the test boards every two minutes. The data from these four-point resistance measurements is then converted to temperature and displayed in real time as a graph. The conversion of resistance was calculated with a user defined linear correction formula (equation 7.2) with independent correction coefficients for each board. It was estimated that the temperature at the resistor networks beneath the component is approximately 10°C lower than the temperature of the interconnections directly beneath the component during the power on –period. Thus resistor network temperatures of 110°C during the power on –period were targeted. A schematic representation of the power cycling bench is presented in Figure 7.8.

Typically ALTs are conducted until all or a predetermined number of test samples have failed. To investigate the failure mechanisms and the progress of failure in the interconnections (*i.e.* crack propagation), the power cycling tests were conducted with a predetermined number of samples. Instead of testing to failure, boards were

removed from the test structure at specified intervals and no separate arrangements for failure detection were devised. However, if significant deviation in the temperature response was observed, the sample in question was removed at the next scheduled interval. After removal cross sectional samples were made of the components and the interconnections were analyzed.

Based on the previous power cycling studies conducted, estimated lifetimes in the range of several thousand cycles were expected, and the initial removal schedule was determined based on this estimate. As the object was to investigate the progress of failure in the interconnections, it was decided that the first samples were to be removed after 500 cycles with further samples removed every 250 cycles. Modifications and adjustments on the number of samples removed and on the removal interval were then made based on the observed results at the sample removal point. All the removed samples are collected up in Table 7.1, where the number of samples removed at each interval is presented along with the number of power cycles experienced. In total, 32 samples were used for the power cycling characterization. The results of these tests are discussed in detail in section 8.3.

Table 7.1: *Power cycling samples.*

Number of		Number of		Number of		Number of	
cycles	samples	cycles	samples	cycles	samples	cycles	samples
500	2	2000	2	4500	1	7500	1
750	2	2250	2	5000	1	8000	1
1000	1	2500	2	5500	1	8500	1
1250	2	2750	2	6000	1	9000	1
1500	2	3000	2	6500	1		
1750	2	4000	1	7000	1		

7.5 Concurrent Loading

For concurrent loading a combination of the two previous single load setups was used. The samples were simultaneously subjected to continuous constant single frequency vibration and power cycling. However, due to the long expected lifetimes under power cycling, a method to test multiple boards simultaneously was developed in order to gain results within the timescale of the project. This was achieved by stacking: four boards were mounted on top of each other with the help of copper spacers. The cylindrical copper spacers (with outer and inner diameter of 5 mm and 3 mm and a height of 5 mm) were inserted between the boards and on top of the topmost board. The boards were then attached using the same torque (1 Nm) and with the same type of three mm thick hexagonal head shoulder screws as in pure

Figure 7.9: *Schematic presentation of the stacking procedure.*

mechanical loading. The stacking process is illustrated in Figure 7.9. The effects of board stacking on the mounting point rigidity and maximum achievable vibration amplitude were investigated by measuring the strains experienced by the stacked boards with strain gauges. These results are discussed in section 8.1.2.

The power cycling procedure in the concurrent test setup was nearly identical to the one used in pure power cycling. The only two differences in the test setup were that a different power source (Kepco KLP36-60-1200) was used and to compensate for the cooling effect due to vibration the voltage difference between the components drain and a source interconnections was brought up to 7 V (resulting in drain to source currents of approximately 5.75 A).

The mechanical loading procedure was the same as in pure mechanical loading with the exception of health monitoring. As a considerable current is driven through the component during the power on –period and no current flow during the power off –period, the health monitoring utilized in mechanical loading was deemed unpractical and an alternative failure detection method based on temperature was devised. As the interconnections start to fail, the resistance increases. This increase in resistance (and the resistance of the component) is relatively small compared to the high power resistor (1 Ω) and has thus a negligible effect on the current flowing through the circuit. It has, however, a marked effect on the component, causing a significant increase in temperature. This is utilized in failure monitoring: the temperature is periodically monitored and if it is observed to surpass a critical threshold value (120°C), the test is automatically stopped. To accelerate the failure detection and to avoid excessive temperature overshoots the temperature logging interval was changed from two minutes used in pure power cycling to 30 seconds. The chosen failure detection method only enables the failure detection during the power on –cycle, but since lifetimes in the range of several hundred power cycles were aimed at, the failure detection accuracy was deemed sufficient.

Four stacked boards were tested simultaneously and the concurrent tests were conducted in such a manner that a component was classified as failed after two consecutive threshold temperature surpasses. After failure the board was disconnected and the test continued. The tests were terminated after two of the four boards in the stack had failed and cross sectional samples of all the four boards were then made for failure analysis purposes. The drawback of the chosen procedure is that the time-to-failure data is obtained only from two of the four tested components and the component that has failed first is exposed to additional mechanical load-

ing that might affect the failure analysis considerations. In addition to testing four boards simultaneously, the benefit of the chosen procedure is that it enables the indirect examination of crack nucleation during concurrent loading. The benefits and drawbacks of the chosen test methods are discussed further in the next section.

7.6 Failure Analysis

After failure or if the test was otherwise terminated the test samples were analyzed. Failure analysis was conducted by taking a cross sectional sample of the component and examining the interconnections by an optical microscope. The sample preparation process and optical microscopy is discussed in the following two subsections.

Due to the structure of the component, the outermost source interconnection experiences higher stresses and strains during the various loads than the two centermost source interconnections. Furthermore, the separate relatively small source interconnections will certainly experience higher strains and stresses than the one, relatively large drain interconnection. Thus the failure analyses were mostly conducted by analyzing only the outermost source interconnection. However, this assumption was verified separately for each applied loading type (mechanical, power cycling and concurrent) by analyzing all the source interconnections and the drain interconnections of several samples subjected to the particular type of loading.

Together with the aforementioned test methods the chosen failure analysis method enables the indirect examination of crack nucleation as a function of time during the power cycling (and to a lesser degree concurrent) tests. As samples were removed periodically from the test structure, insights on the failure mechanisms and the progress of failure can be gained when comparing the samples taken out at different intervals. However, the chosen methods have several weaknesses which need to be taken into consideration when analyzing the results and drawing conclusions:

1. Due to the limited amount of samples taken out at each reference point in power cycling, the individual deviations of the assemblies (*e.g.* manufacturing defects) might be significant. Furthermore, due to the limited amount of samples at each reference point, the requirements for statistical validity are not fulfilled.

2. Due to the random nature of the crack propagation each sample is unique and there can be significant deviations between single samples. The comparisons between samples with different loading levels should thus be conducted in a general level.

3. Due to the destructive nature of the test method special care should be taken when cutting, molding, grinding and polishing the sample. Once cut and molded, the sample cannot be remade and soiled or damaged samples cannot be repaired.

The first and most important step in failure analysis and sample preparation is selecting and defining the appropriate research methods. The preparation of cross

sectional samples is a destructive process and a sample once cut and molded cannot be remade. The research subject, cutting direction and the inspection methods should thus be carefully defined before the sample preparation process. In this study, cross sectional samples and optical microscopy were used.

7.6.1 Cross-Sectional Sample Preparation

During the sample preparation process, the sample is first carefully cut out from the rest of the assembly according to the predefined cutting direction. It is then molded to facilitate the continued handling. In this study epoxy was used; other common casting materials include various acryls and polyesters. If a sample is to be inspected with an electron microscope, the casting material should have current-carrying capabilities or the polished surface should be coated with a current-carrying material. After hardening the sample is detached from the casting mold and the surface under examination is first grinded and then polished. The aim is to create an artifact free, clear surface, on which all the structural details can be observed. The grinding process is begun with a coarse (80 or 220 grit) grinding paper and moving gradually to more fine-grained grinding papers and continued at the very least until grinding paper coarseness of 1200 grit and the surface under examination is reached. Afterwards the surface is further worked with the help of polishing cloths and abrasives until a sufficient level of smoothness is achieved.

The process of successfully preparing a cross sectional sample requires time, carefulness and handiwork. A failure in any of the many phases of the sample preparation process might lead to unnecessary artifacts or in worst cases render the sample completely useless and special care should be paid during the sample preparation process.

7.6.2 Optical Microscopy

Despite the wide range of available inspection techniques and the enhanced resolution of the more advanced techniques (such as scanning electron microscopy), optical microscopy is still the first choice in most cases. This is due to ease of use, numerous contrast enhancement techniques and the variety of samples that it can accommodate.

Optical microscopy is based on visible light transmitted through or reflected from the sample through a single or multiple lenses to allow a magnified view of the sample. Typical resolution and magnification levels for optical microscopes are in the range of 1μm and 2000x, respectively.

In optical microscopy the samples can be inspected with several different manners, all depending on the features to be highlighted. In bright field mode the image is formed on the light reflected from the sample and the illumination provides contrast between surface features that are normal to incident light and those that are oblique to it. In dark field illumination, the oblique light is collected and the incident blocked. The method provides a significant improvement in contrast as compared to bright field illumination and is typically used when inspecting for fine features

like voids, cracks and delaminations. In addition the incident light can be polarized to highlight the structures consisting of unsymmetrical crystals. The asymmetric tin crystal structures have different refraction indices in different crystal directions and the grains in different orientations can be seen in different shades when the reflected plane polarized light is cross-polarized. This is particularly useful when inspecting microstructural changes, such as recrystallization, in the interconnections. [SG96, Mat05]

Chapter 8

Results

This chapter presents and discusses the experimental test results obtained. The order follows the previous chapter, with the results from pre-testing presented first, then followed by the single load reference test results and concurrent loading results. When presenting the results for single load reference tests and concurrent loading tests, the numerical results are presented and discussed first, followed by the results and discussion on failure analysis. The test procedures and methods are presented in detail in the previous chapter and are not discussed here.

8.1 Pre-testing Results

Pre-testing was conducted first to characterize and verify the properties of the test assemblies. Based on the results presented in the following two subsections, actual test parameters for single loading and concurrent loading were determined.

8.1.1 Temperature Response of the Test Assembly

To illustrate the temperature response of the test assemblies during power cycling and concurrent loading, the temperature response of four stacked boards during concurrent loading is plotted in Figure 8.1. To create the plot, the data sampling interval was temporarily changed from 30 seconds to 5 seconds. Due to the cooling effect of vibration during concurrent loading, slight fluctuations in temperature during the power on –period and slightly faster cooling when the power was switched off were observed when compared to the temperature response in pure power cycling. The difference in cooling rates was also observed when comparing the temperature responses of the various boards in the stack. From Figure 8.1 it can be seen that the outermost boards cool down slightly faster when the power is switched off than the boards in the middle of the stack. However, the observed differences were minor, and the temperature responses are considered identical during both tests.

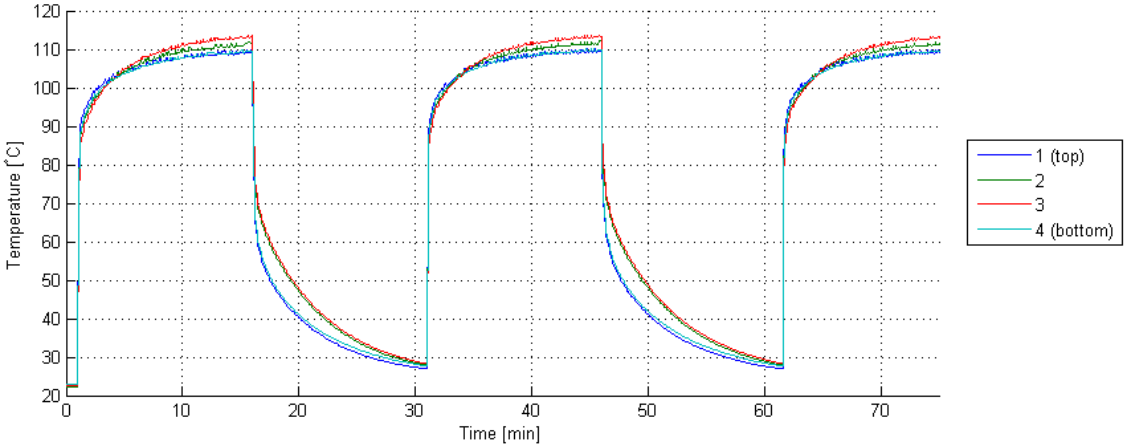
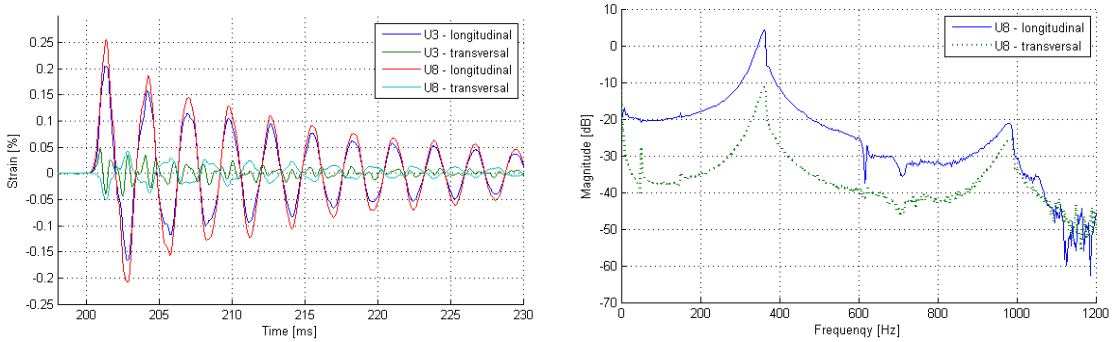


Figure 8.1: *The measured temperature response of the test assemblies during concurrent loading. The number in the legend indicates the board's position in the stack (1=top, 4=bottom).*



(a) (b)

Figure 8.2: *(a): Measured strains after drop impact. (b): DFT of strain data after drop impact.*

8.1.2 Mechanical Characterization Results

The mechanical characterization of the test assemblies was begun by drop testing a unassembled test board equipped with two strain gauges at component locations U3 and U8 (see Figure 4.2 for the layout of the component locations). The strain data after impact (1500 G) is plotted in Figure 8.2(a). The discrete Fourier transform (DFT) taken from the data after impact for the strain gauge located at the center of the board (U8) is plotted in Figure 8.2(b). Based on the DFT of the data, first estimates for the first (*ca.* 360 Hz) and second (*ca.* 975 Hz) natural modes are obtained. When using vibration base plate standoffs that were constructed to correspond to the fixation table standoffs, the first natural frequency was experimentally verified as 357 Hz by measuring the strain at different vibration frequencies. However, due to the rigidity of the test assemblies and to further account for the increased loadings on the standoffs during stack testing, a more rigid aluminum base plate with

Figure 8.3: *The vibration table base plates and their standoffs. The old, lightweight base plate on the left and the more rigid base plate utilized in this study on the right.*

thicker standoffs was employed in this study. The differences of the two base plates and their standoffs are illustrated in Figure 8.3.

As the natural frequency of the test system is affected among other things on the board fixation, a change in the natural frequency was observed. The natural frequency of the test system was determined to be 400±3 Hz when using unassembled test boards. The variations in the natural frequency were attributed to variations in manufacturing and to the slight differences in the bonding of the strain gauges and gauge wires. However, when using assembled boards further equipped with thick wires for power cycling purposes, changes in the natural frequency and strain amplitudes were observed. This is illustrated in Figure 8.4 where the strain amplitudes of two unassembled and two assembled boards are plotted as a function of frequency using a constant excitation voltage of 1V. The data obtained from the two assembled boards highlights the observed differences in the strain behavior. The natural frequency of the assembled test boards equipped with strain gauges and measurement wires was determined to be in the range of 390 Hz, with variances considerably larger than when using unassembled boards.

The effect of heating and stacking of the boards was studied in order to understand the strain behavior of the boards during concurrent loading. The effect of heating the component on the resonant frequency of the system and strain is illustrated in Figure 8.5, where the strains of a single board have been measured at room temperature and when the component is heated. The strain response of the stacked boards at different vibration frequencies was also studied and is illustrated in Figure 8.6. The frequency range of 360 Hz to 390 Hz was observed to be highly non-linear, with phase differences between the individual boards. Outside this non-linear frequency range the vibration behavior was stable with all the boards vibrating in phase. Different strain levels were measured between different stack locations and furthermore, due

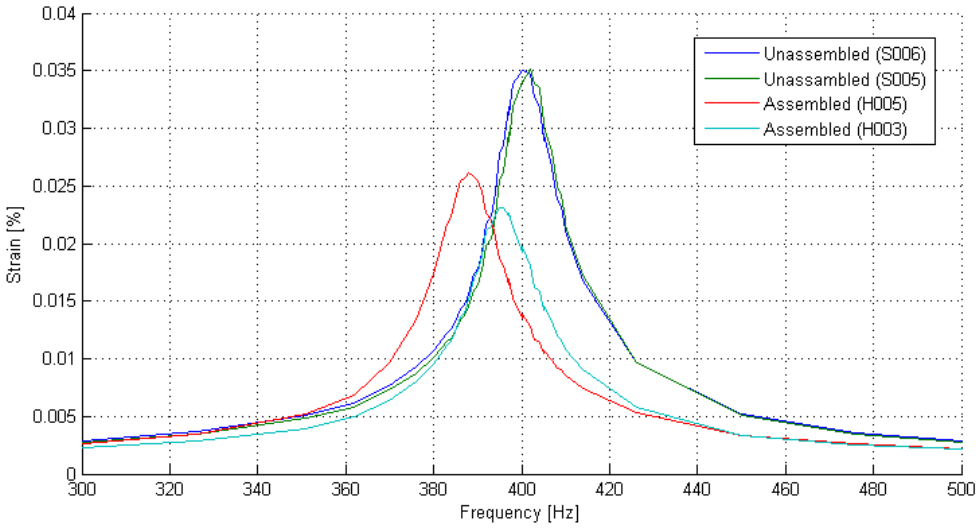


Figure 8.4: *Strains of the test boards as a function of frequency. Strains were measured with the new, more rigid base plate and at component location U8 with a constant excitation amplitude of 1V.*

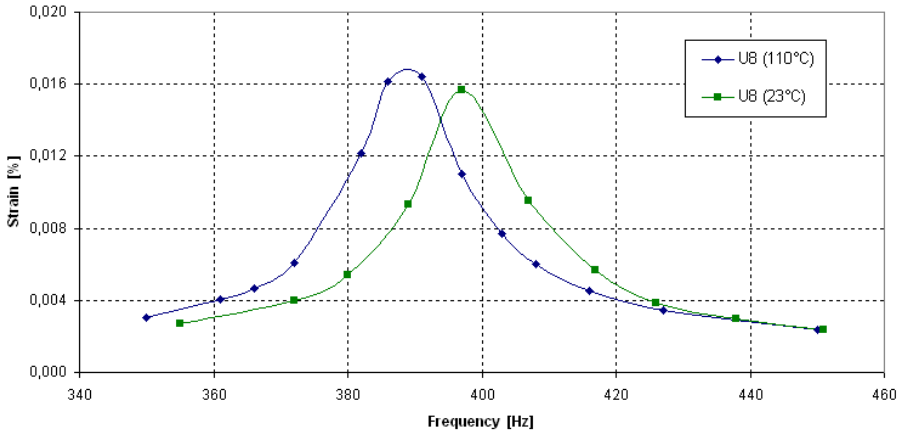


Figure 8.5: *The effect of heating the component on the strains and the natural frequency. The strains were measured with a constant excitation amplitude of 1V.*

to the increased mass of the structure, the total strain amplitudes were observed to decrease.

The combined effect of heating the components and stacking the boards on the strains measured at various vibration frequencies is illustrated in Figure 8.7. To compensate for the individual variances between the boards equipped with strain gauges, the data presented in the figure was collected by using a single strain gauge. As the heating of the other boards in the stack was observed to significantly alter the strain behavior, the measurements were conducted in a manner in which all the boards in the stack were heated when measuring strains at the high temperature level.

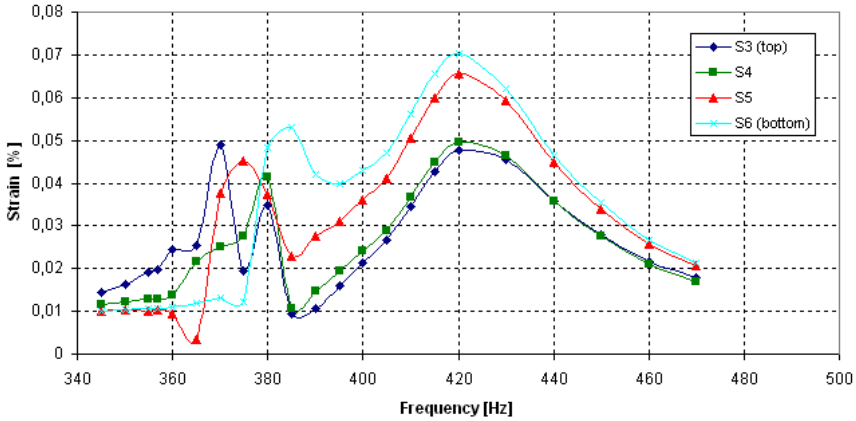


Figure 8.6: *The effect of stacking the boards on the strains and the natural frequency. The strains were measured with a constant excitation amplitude of 5V.*

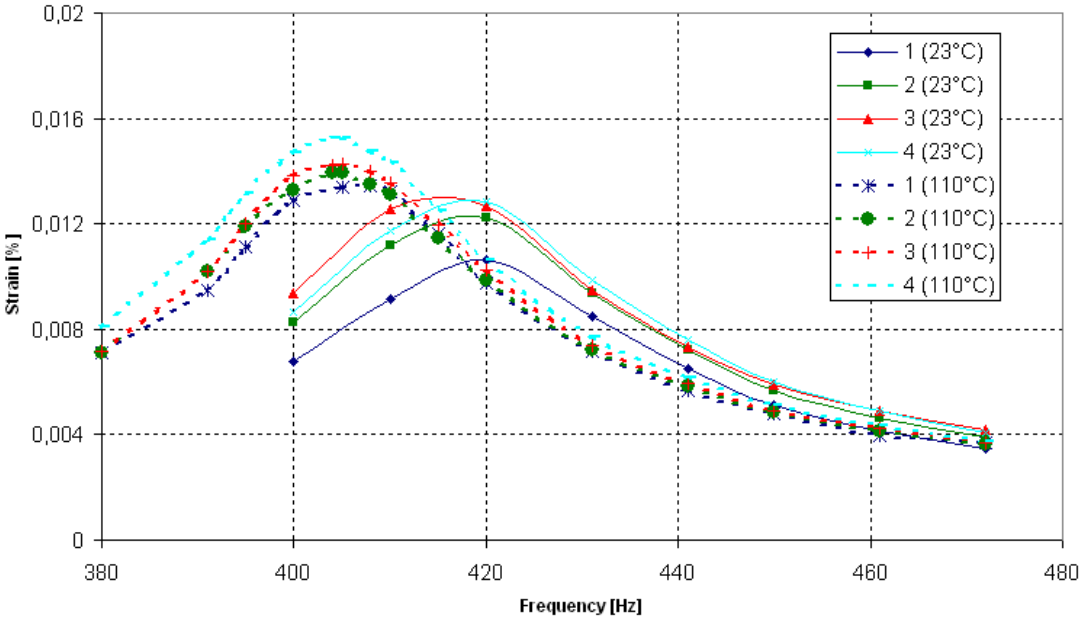


Figure 8.7: *The effect of temperature and stacking of the boards on the strains and the natural frequency. The strains were measured with a constant excitation amplitude of 5V. The first number in the legend indicates the board's position in the stack (1=top, 4=bottom) and the number in parentheses indicates the measured temperature beneath the component.*

The mechanical characterization was performed to determine the optimal parameters for the actual tests. The mechanical loading was conducted with two different setups. The preliminary lifetime characterization tests were conducted with a single board at a time. To minimize the effect of natural frequency variations on the strain levels, the single board test frequency was chosen outside the natural frequency range. As no significant differences in the strain levels between different

boards were observed and high enough strains could be achieved with the frequency of 357 Hz, the single board tests were conducted with that frequency.

The concurrent tests and some mechanical verification tests were conducted with four stacked boards. Based on the mechanical single board lifetime characterizations (the results are discussed in section 8.2), it was estimated that high enough strain levels and stable vibration behavior on the current setup could only be achieved on the frequency range of 390 Hz to 460 Hz. On the available frequency range the heating of the boards was observed to influence the strain levels the more the lower the employed vibration frequency was (see Figure 8.7). To minimize the effect of heating in concurrent loading as well as the variations in natural frequencies between individual boards on the strain levels, the frequency of 460 Hz was chosen for the stacked tests (both pure mechanical and concurrent), providing that no changes in the failure mode are observed. The results of the comprehensive failure analyses indicated that the change of frequency does not affect the failure mode. The effect of the change in frequency is further analyzed and discussed in subsection 8.2.2.

8.2 Mechanical Loading Results

This section presents the results obtained from mechanical loading tests. The numerical results are presented first in subsection 8.2.1 and are followed by failure analysis results in subsection 8.2.2. In the first two subsections the results of the single board tests are discussed, while the final subsection 8.2.3 focuses on the stacked tests by presenting the results of the stack verification tests.

8.2.1 Numerical Results of the Mechanical Loading Tests

The mechanical lifetime characterization results measured with one board and a vibration frequency of 357 Hz are presented graphically in Figure 8.8. The results seem to follow a logical trend, *i.e.* when the strain amplitude decreases, the lifetime increases. To gain a first order estimation on the lifetimes, a simple two term power series model ($y = a + b \cdot x^c$) was fitted to the data using the method of least squares. The fitted curve is also included in the figure. The parameters for the curve were $a = 0.01948$, $b = 0.04622$ and $c = -0.1265$. However, due to the limited data points available and the methods used, the lifetime-estimation curve can only be considered tentative.

The failure detection worked when the strain amplitudes presented in Figure 8.8 were employed. However, when the strain amplitude was lowered beneath 0.0448% (the lowest data points in Figure 8.8), no failures were observed within reasonable timeframes. When the lifetimes of the test samples subjected to low amplitudes significantly exceeded the preliminary predicted lifetimes, the samples were taken off and analyzed. Failure analyses revealed that although no failures were observed, all the source interconnections had failed. In an attempt to catch these failures, the failure detection system was changed from the previously mentioned (subsection 7.4.1) to an event detector (Analysis Tech model 128/256 STD Event Detector),

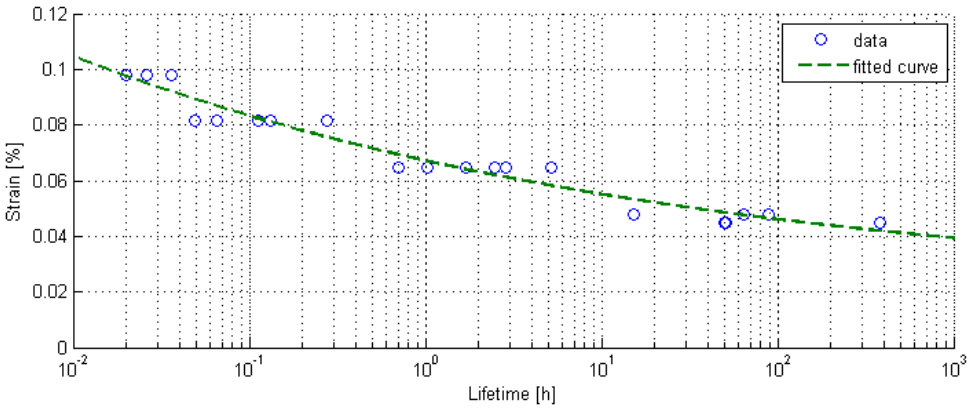


Figure 8.8: *Test assembly lifetimes under mechanical loading. Measurements conducted with a single board and a vibration frequency of 357 Hz.*

which had an event duration sensitivity of 200 (±10) ns. Albeit the test unit sampling rate was brought up from 40 kHz to 500 kHz, no significant enhancements in failure detection were observed.

The difficulties in failure detection were attributed to the structure of the component and the relatively low loading levels used. The failures in mechanical loading are typically observed as short intermittent failures during the loads. Albeit completely cracked through, the interconnection can still be electrically operational due to spring contact in a static case. As the mechanical loading is applied (*i.e.* vibration in this case), the bending of the PWB causes brief intermittent electrical shorts in the circuit that are observed as failures if the bending amplitude is high enough. If the amplitude is not high enough, the interconnections remain electrically operational and no failures are detected. To give an indication on how low the employed strain levels were, it is noted that the measured maximum strain amplitude of the test assembly on a standard 1500G drop test was 0.25% (see Figure 8.2), while a drop impact of 520G resulted in a maximum strain amplitude of 0.14%.

The failure detection is further complicated by the structure of the component. The three, relatively small source connections are predicted to be much weaker mechanically than the continuous, rather large drain interconnection. However, since the source interconnections are parallel, all of the three separate interconnections need to fail simultaneously in order to detect a failure. Due to the intermittent nature of the failures, there can be a significant time difference between failure and the time when the failure is actually detected.

It is recognized that the difficulties in the failure detection are not restricted to loading levels where the achieved strain amplitudes are beneath 0.0448%. Albeit the difficulties are highlighted when operating below the mentioned level, the same issues still exists at higher strain levels. Thus it is concluded that the lifetimes presented in Figure 8.8 may overestimate the actual lifetimes of the interconnections. In retrospect, the failure detection could have been enhanced by designing separate routings for each one of the three source interconnections. Then the failures of the

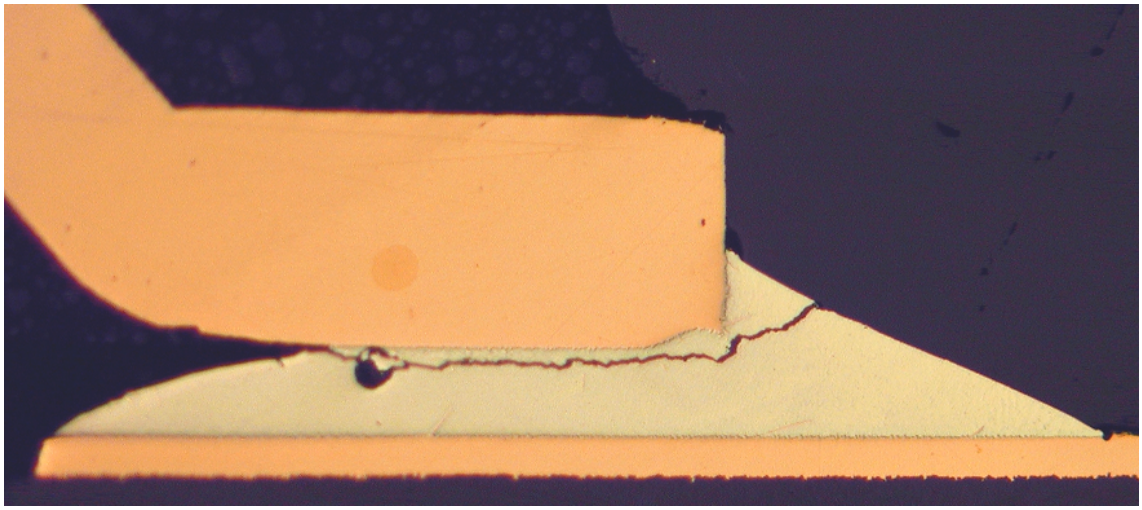


Figure 8.9: *The typical failure mode observed during mechanical loading.*

three interconnections could have been detected separately and thus the failures would probably have been caught earlier.

8.2.2 Failure Analyses of the Mechanical Loading Tests

Due to the structure of the package (see Figure 7.1) all the observed failures were localized in the source interconnections. As presumed, the three relatively small source interconnections proved to be mechanically weaker than the one relatively large continuous drain interconnection.

The observed failure mode in mechanical loading was a crack through the bulk solder. This is illustrated in Figure 8.9, where the cross-sectional view of a component's source interconnection is presented. The component in Figure 8.9 was subjected to vibration with a strain amplitude of 0.098% until a failure was observed after 131.4 seconds.

When the strain amplitude was lowered, the main failure mode stayed the same (crack through the bulk solder), but the crack was observed to move closer to the interface between the solder and the component. The differences in failure modes are illustrated in Figure 8.10, where the cross sectional views of the source interconnections loaded with various strain amplitudes are presented. With the lowest measured strain amplitudes, the crack was observed to propagate partly through the interface between the component and bulk solder, or in some single cases, as illustrated in image c) of Figure 8.10, even nearly completely along the interface.

Besides the slight differences in the crack paths, Figure 8.10 also illustrates the difficulties in the failure monitoring. When operating at relatively high strain amplitudes (see *e.g.* Figure 8.9 or images a) and b) of Figure 8.10), only a single crack is observed and it is evident that the failure has been detected and the test stopped shortly after the mechanical failure has occurred. However, when operating at lower strain levels, the cross sections reveal multiple cracks and crack paths, as illustrated in image c) of Figure 8.10. The additional damage is suspected to originate from the

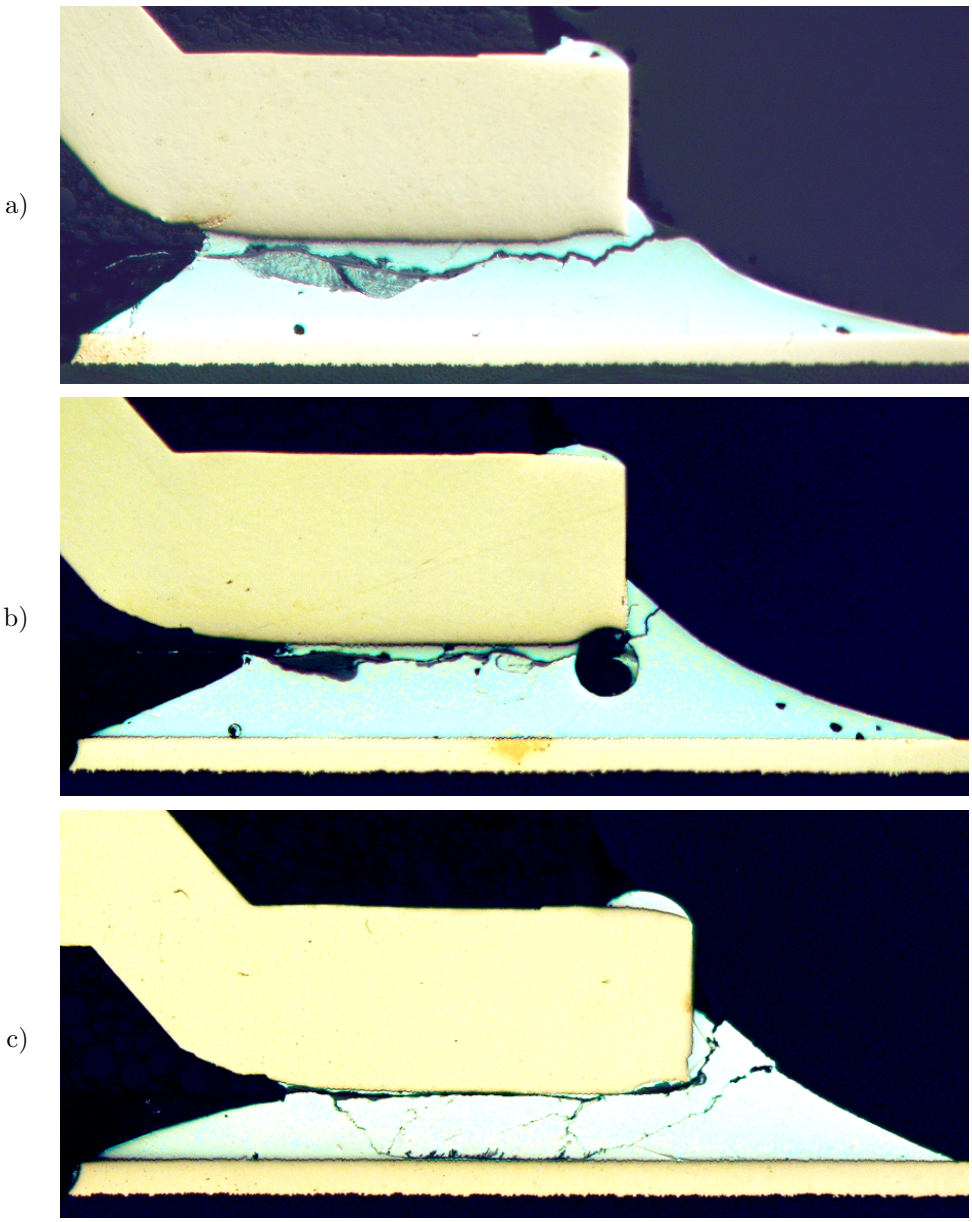


Figure 8.10: *Failure modes of single boards vibrated with different amplitudes. Applied strain amplitudes: a) 0.082%, b) 0.065%, and c) 0.045%.*

subsequent loading cycles experienced after the occurrence of the mechanical failure and before the failure was electrically detected.

8.2.3 Stack Verification Results

The stacked tests were conducted with four boards stacked on top of each other and a vibration frequency of 460 Hz. In addition to the low amplitude single board tests, the aforementioned difficulties in failure monitoring were also evident when determining the lifetimes of the stacked boards. Due to the limitations of hardware,

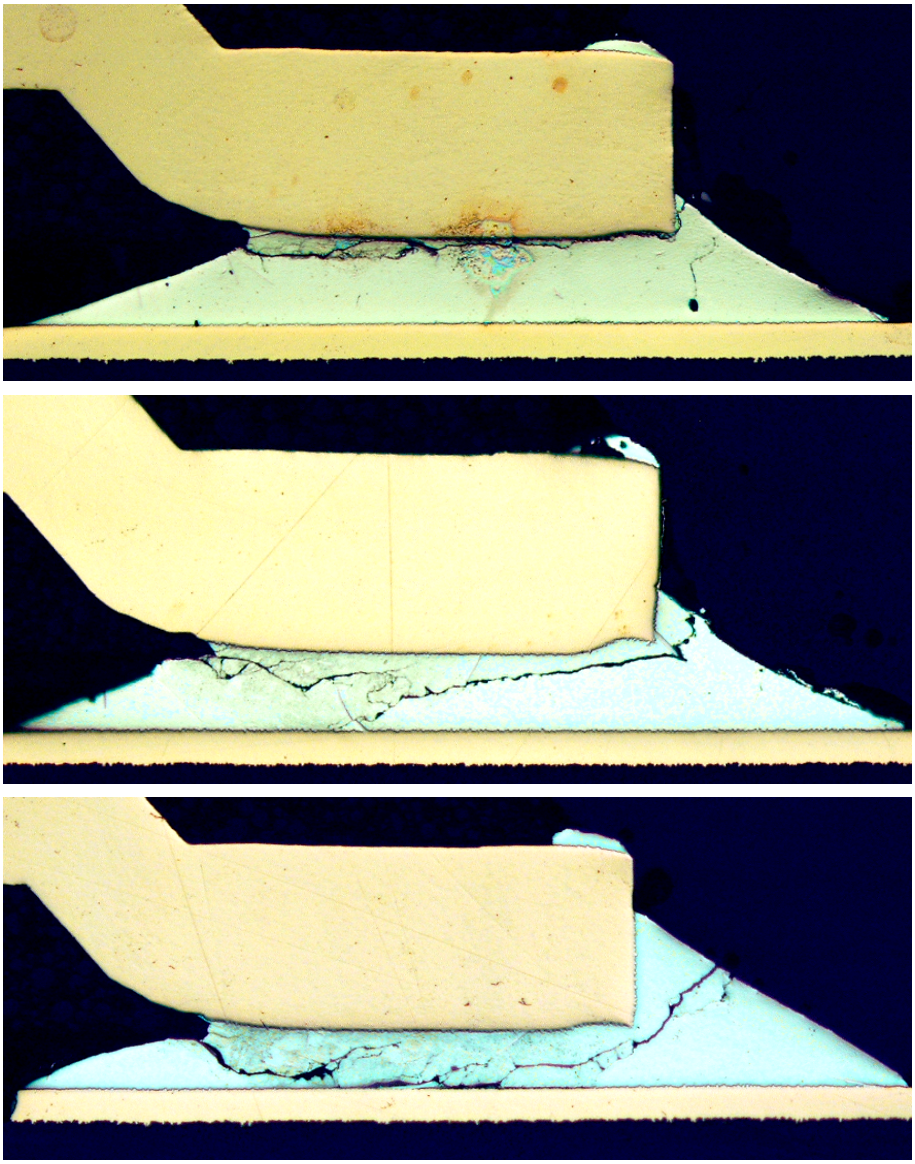


Figure 8.11: *Observed failure modes of stacked boards under mechanical loading.*

the maximum attainable strain amplitudes were much lower than in the single board –case, and no failures were reliably observed in a reasonable timescale.

The fundamental prerequisite for the chosen stacking procedure and frequency was that it should not affect to the failure mode, *i.e.* the failure mode should be the same as in the single board tests. The failures in the stacked tests were analyzed, and it was concluded that the main failure mode, the cracking of the bulk solder, was the same as in the single board tests.

The typical failure modes in the stacked tests are illustrated in Figure 8.11, where the cross-sectional views of the source interconnections are presented. As illustrated image c) in Figure 8.11, in some single cases the crack was observed to propagate partly through the interface between the PWB and bulk solder.

Several tests were conducted with stacked boards and albeit the exact failure times could not be determined, the lifetimes seemed to correspond with the lifetime prediction curve obtained with the single board tests (see Figure 8.8). As no failures were detected electrically, the samples were removed from the test and analyzed to find if they had mechanically failed. The analyzed samples revealed that the boards removed before their expected lifetime were still mechanically intact while the boards removed after their expected lifetime had failed mechanically. However, due to the limited amount of samples and inoperativeness of the electrical failure detection, these results can only be considered as indicative.

8.3 Power Cycling Results

This section presents the results obtained from the power cycling tests. Due to the relatively small size of the source interconnections (when compared to the one, continuous drain interconnection), higher thermomechanical stresses are induced to the source interconnections than in the drain interconnection. Furthermore, the different interconnection geometries cause much higher current densities in the source interconnections that might lead to electromigration. Thus the effects of power cycling were expected to concentrate on the source interconnections and this was verified with failure analyses. However, before the results of failure analyses are discussed in subsection 8.3.2, the numerical results of the power cycling tests are discussed first in subsection 8.3.1.

8.3.1 Numerical Results of the Power Cycling Tests

The temperature of the power cycled samples was periodically monitored. No additional failure detection systems were devised for the power cycle tests and only total failures, where the sample fails to heat up or overheats could be detected. Instead of testing the components until failure, samples were periodically removed from the test structure according to a predetermined schedule, and all the removed test samples are collected in Table 7.1.

To characterize the crack propagation, the crack length in the source interconnections was studied. Based on the crack lengths observed at cross-sectional analyses of each sample, the samples were divided into five rough categories (crack length of 0%, 25%, 50%, 75% or 100% of the source interconnection). To illustrate the crack propagation as a function of experienced power cycles, the data is plotted in Figure 8.12. However, as discussed in section 7.6, due to the random nature of crack propagation and a maximum of only two samples per reference point, these results can only be considered as indicative.

The results indicate that the first incipient crack was observed at 1000 cycles. However, as no further incipient cracks were observed until 2000 cycles, this observation was classified as deviant. A sharp increase in crack length was observed at 3000 cycles, where a total interconnection failure was found in all the six interconnections (three source interconnections / sample) analyzed. Based on these results,

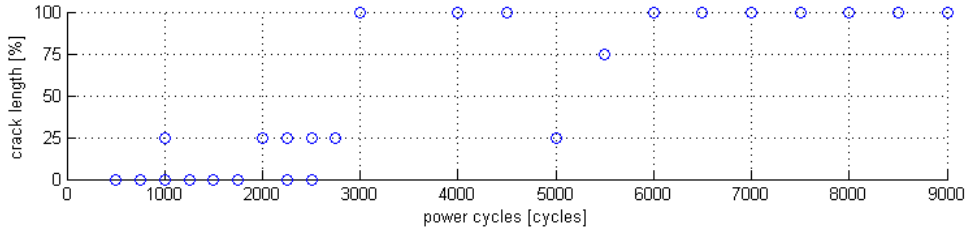


Figure 8.12: *The crack lengths observed in the source interconnections in power cycled samples as a function of experienced power cycles.*

the average interconnection lifetime during power cycling was estimated as 3000 cycles.

To investigate the component behavior and to find out if any electrical failures could be observed, the removal schedule was adjusted after 3000 cycles. Due to the limited number of boards left, only one board was removed at each reference point and the removal interval was changed to 500 cycles starting from 4000 cycles. Furthermore, no samples were removed between 3000 and 4000 cycles.

Two electrical failures were observed with the remaining samples. The failures manifested when the components failed to heat up despite the voltage applied. The first total failure was observed at 6500 cycles, while the last sample removed was still electrically operational at 9000 cycles. If a failure was observed, the board in question was removed at the next scheduled interval and analyzed. The results from the analyses are discussed in the next subsection.

8.3.2 Failure Analyses of the Power Cycling Tests

In the power cycling tests, the main cause for failures was thermomechanical stress induced by different thermal expansion rates of materials.

The first samples analyzed after 500 power cycles closely resembled the as-soldered –state and no effects of power cycling could be seen. However, the first effects of power cycling were observed after 750 cycles in the form of incipient recrystallization. This is illustrated in Figure 8.13, where the cross-sectional view of the source interconnection is presented after 1000 cycles. Polarized light was utilized to highlight the microstructural changes, such as recrystallization, in the interconnections. The nucleation and propagation of cracks is strongly enhanced by recrystallization of the solder interconnections, and the newly formed grain boundaries provide favorable paths for cracks to propagate. As the test progressed, these recrystallized areas grew in size and cracks began nucleate and propagate at the boundaries of the recrystallized grains. [Mat05]

Besides the evident recrystallization, the growth of intermetallic layers at the PWB side was observed both at the source and at the drain interconnections. This growth was distinctly nonuniform, not only between the source and drain connections, but between different samples as well. The differences in the thicknesses of the intermetallic layers is illustrated in Figures 8.13, 8.14 and 8.15. The growth of the intermetallic layers is highlighted in Figure 8.14, where the cross-sectional view

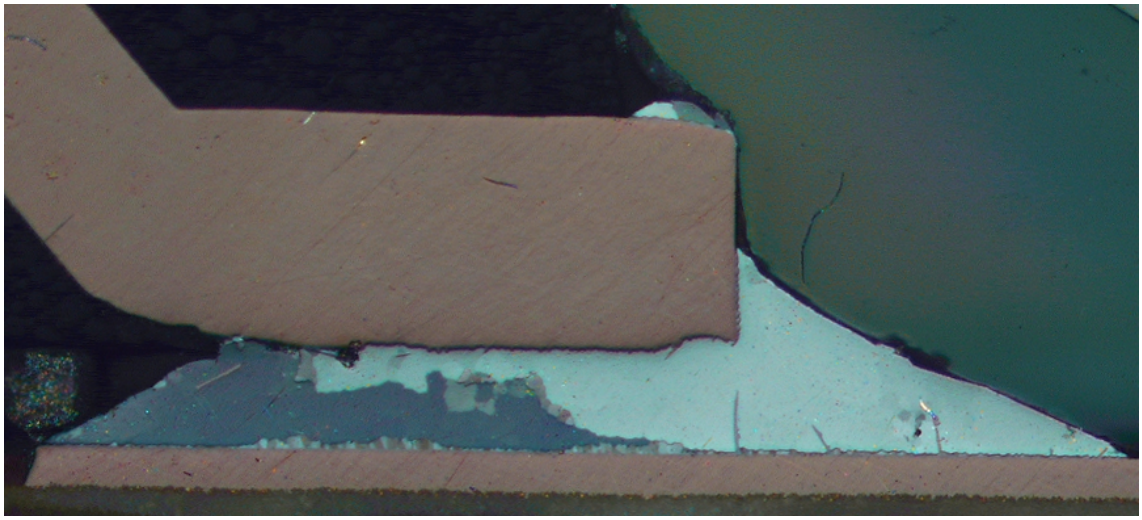


Figure 8.13: *Cross-sectional view of a source interconnection after 1000 power cycles.*

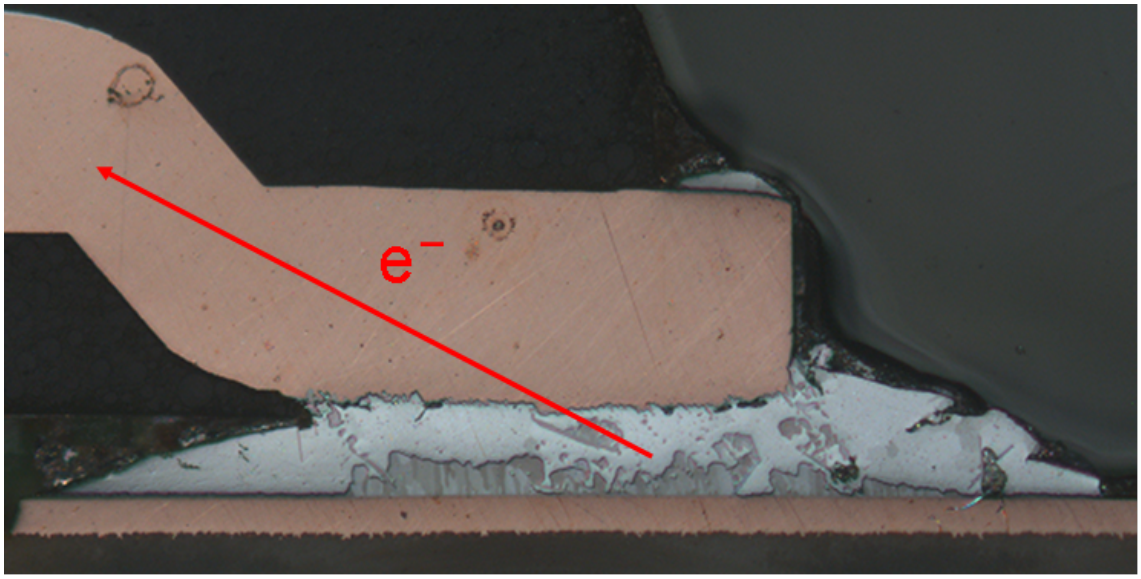


Figure 8.14: *Cross-sectional view of a source interconnection after 2750 power cycles and the direction of electron flux.*

of the source interconnection after 2750 cycles and the direction of the electron flux is presented. Typically the biased growth of the intermetallic layers is explained as a result of electromigration phenomena. As electric current flows through the interconnection, it enhances the diffusion of atoms to the direction of the electron flux (from cathode to anode) [GT05], and in this case the growth is expected to occur on the component side of the source interconnection. Evidently this is not the case here. However, as the phenomena is beyond this thesis and as the growth of intermetallic layers was not observed in any other loading conditions or to affect the failure mode, it is thus not discussed further here.

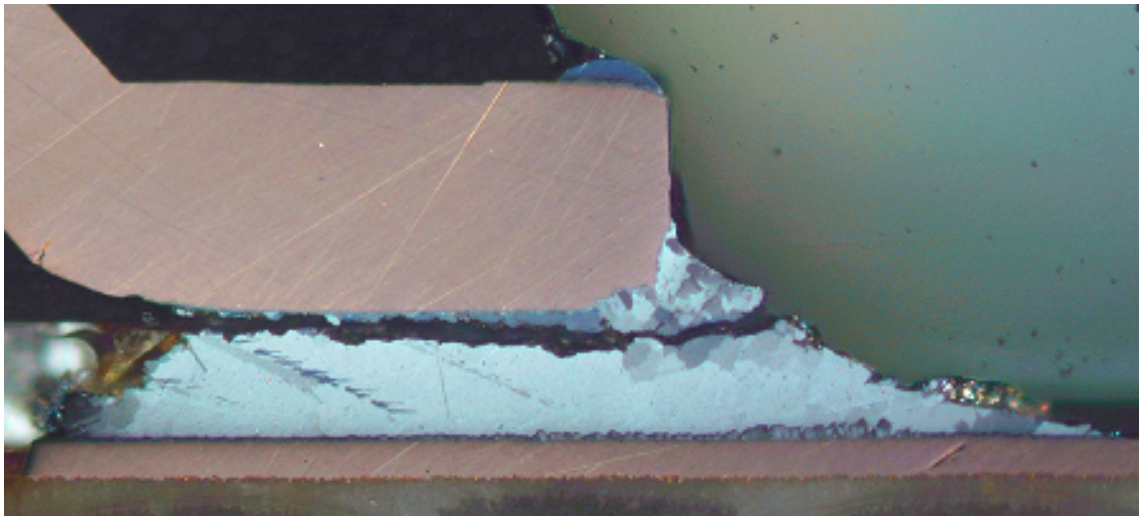


Figure 8.15: *Cross-sectional view of a source interconnection after 3000 power cycles.*

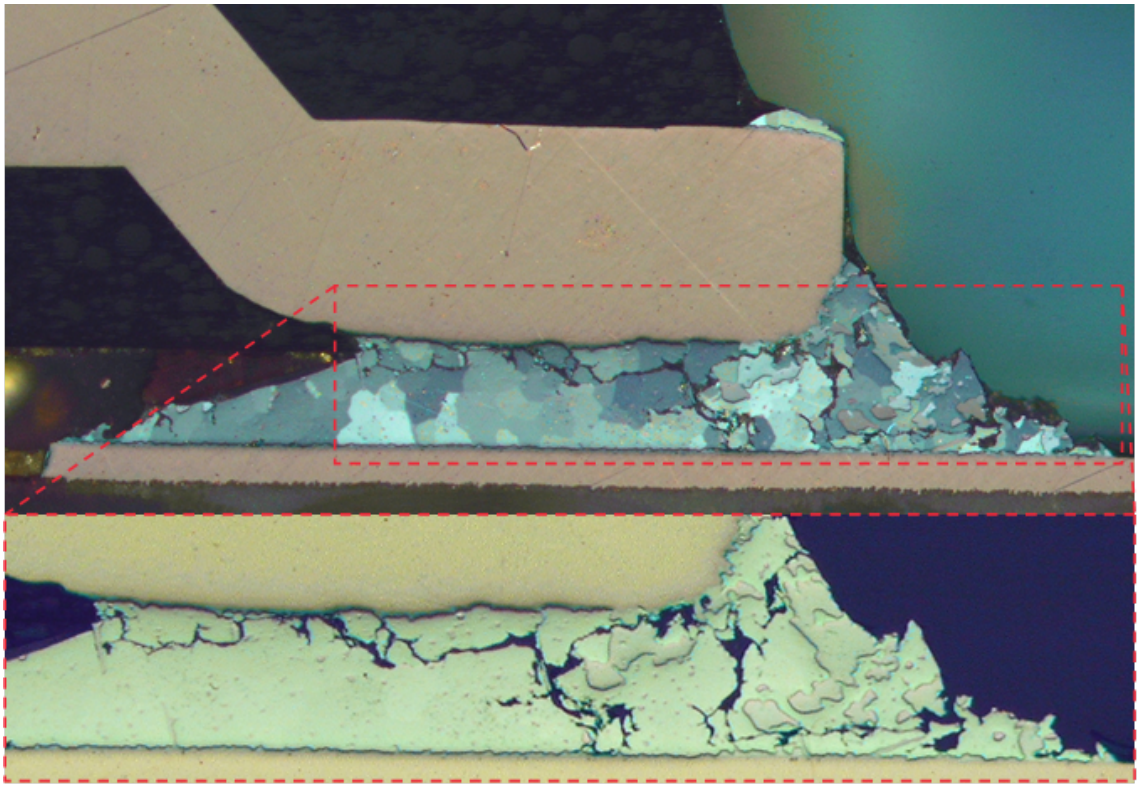


Figure 8.16: *Cross-sectional view of a source interconnection after 4000 power cycles and a bright light magnification of the damaged interconnection area to highlight the crack propagation.*

Besides the thick intermetallic layer, incipient cracks can be observed at the top part of Figure 8.14. Cracks were observed to nucleate after 2000 cycles, and by 3000 cycles they had propagated all the way through the interconnection, as presented in Figure 8.15. Albeit all the three source interconnections of the component presented

in Figure 8.15 were cracked all the way through, the component was still electrically operational due to spring contact. It is suspected that if the component would be subjected to mechanical loads, the failures would be detected.

When compared to the samples taken out after 3000 cycles, only minute changes were observed in the final samples. Figure 8.16 presents the typical failure mode observed and clearly illustrates how the cracks propagate through the grain boundaries.

8.4 Concurrent Loading Results

This section presents the results obtained from the concurrent tests. To shorten the overall testing times, the mechanical loading was implemented by stacking four boards on top of each other and with a frequency of 460 Hz. Thermomechanical loading was applied simultaneously in the form of power cycling with the same test parameters as in the single loading case (15 min. on / 15 min. off –cycle and targeted interconnection temperatures of 120°C). The numerical results are presented first in subsection 8.4.1 and are followed by the failure analysis in subsection 8.4.2.

As previously mentioned, the concurrent tests were conducted in a manner that all four boards in the stack were removed after two of the four boards had failed. This was due to several reasons. Firstly, due to the difficulties in failure detection in the mechanical loading, the method was chosen to confirm the functionality of the chosen failure detection method and to see if the two electrically operational boards had failed mechanically. Temperature differences between different boards were observed to affect the strain behavior of the stack during the power on –cycle. To keep the strain levels as stable as possible, the tests were finished after two of the boards had failed. Furthermore, the chosen test procedure also enables the indirect examination of crack nucleation and propagation during concurrent loading. The drawback of the method was that actual time-to-failure data was obtained only from two of the four boards in the stack.

8.4.1 Numerical Results of the Concurrent Loading Tests

The measured time-to-failure data under concurrent loading is plotted in Figure 8.17. When comparing the results, the effect of temperature on the strain levels presented in concurrent loading should also be noted. As already discussed, one of the main reasons for choosing the frequency of 460 Hz for the stacked tests was to minimize the effects of increased temperature on the strains. Although the effect of temperature on the strain was minimized, the measured strains during the power on –period were approximately 5 to 15 percent (depending on the boards' location in the stack) lower as compared to those measured during the power off –period (see Figure 8.7). The average experienced strain level is indicated with a circle in Figure 8.17, and the error bars indicate the maximum and minimum strain levels. However, the data seems to follow a logical trend just like in the pure mechanical loading case, *i.e.* when the strain amplitude decreases, the lifetime increases.

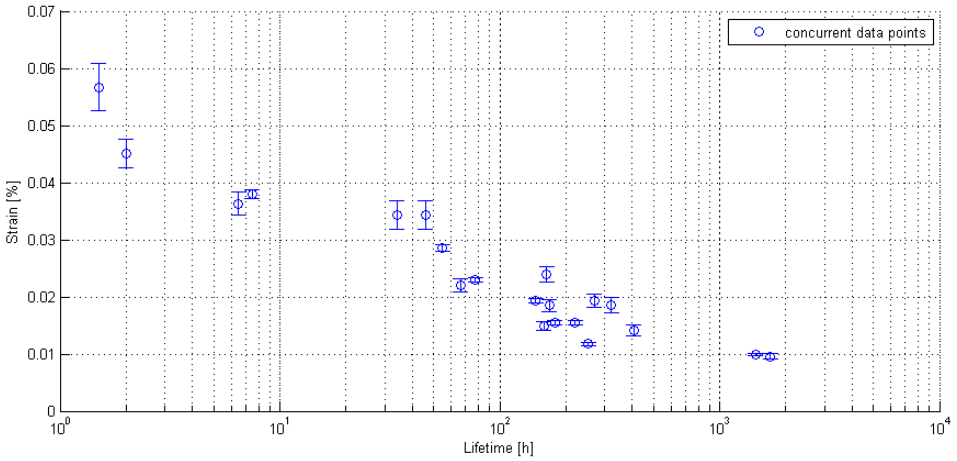


Figure 8.17: *Test assembly lifetimes under concurrent loading. Measurements conducted with four stacked boards and a vibration frequency of 460 Hz.*

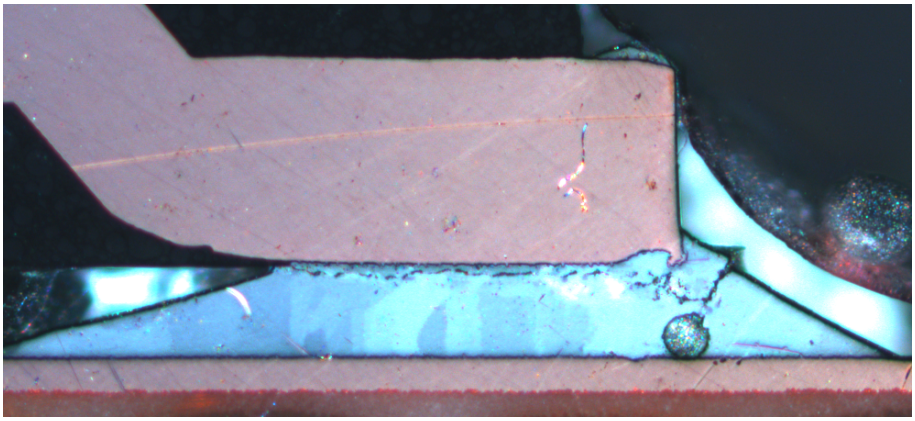
The chosen failure detection method was functional with considerably lower strain levels than the method employed in pure mechanical loading. While no failures were detected in pure mechanical loading with strain levels lower than 0.0448%, failures in concurrent loading were detected even with strains of 0.01%. Furthermore, the failure analysis results revealed that albeit some single interconnections had failed, the electrically operational components were also generally mechanically operational. Thus it was concluded that the failures were detected faster and more reliably than with the method employed in mechanical loading.

8.4.2 Failure Analyses of the Concurrent Loading Tests

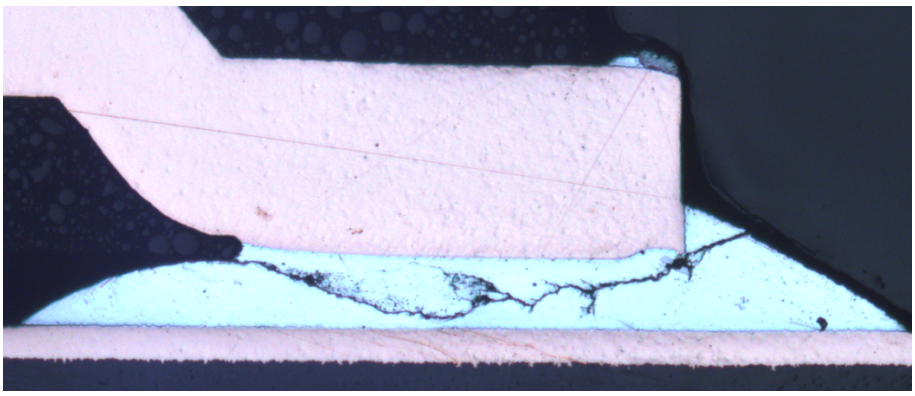
The observed failure mode under concurrent loading, the cracking of the bulk solder, was the same as in the single load reference tests. The observed failure modes are illustrated in Figure 8.18. Images a) and b) of the figure present the typically observed failure mode, where the crack propagates through the bulk solder. As in the stacked mechanical setup, some single cracks were observed to propagate partly through the interface between the bulk solder and the PWB: this is illustrated in image c) of Figure 8.18.

Despite the rather wide strain range used (strains from 0.061% to 0.010%), no apparent changes in the failure mode relating to the strain amplitude were observed. Furthermore, despite the rather long lifetimes (up to 1700h), no recrystallization or growth of intermetallic layers were observed and the faster damage accumulation rate in concurrent loading was thus attributed to the temperature related change of material properties rather than the recrystallization-assisted crack nucleation and propagation observed in the power cycling tests.

a)



b)



c)

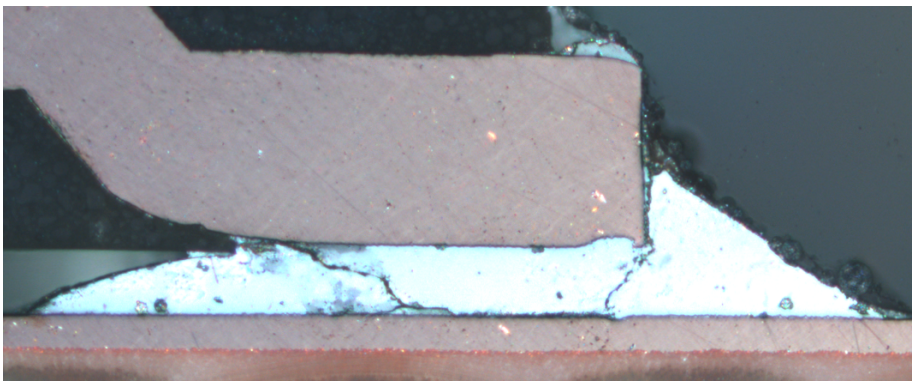


Figure 8.18: *Observed failure modes under concurrent loading.*

8.5 Comparison of Results

This final section compares the obtained results. The results with the two individual loading methods and the combination of the two loadings are compared first. As in the previous sections, the numerical results are discussed and compared first in subsection 8.5.1 before comparing the results from the failure analyses in subsection 8.5.2. The final subsection (8.5.3) compares the results obtained in this study with other published multiple load test results.

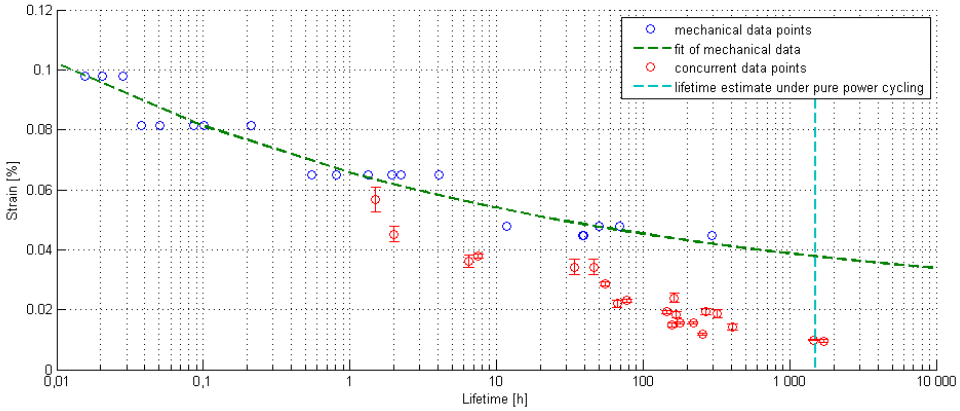


Figure 8.19: *Test assembly lifetimes under pure mechanical and concurrent loading and the expected lifetimes under single loads.*

8.5.1 Comparison of Numerical Results

The measured time-to-failure data from the pure mechanical single board tests and concurrent tests is plotted in Figure 8.19. To illustrate the estimated lifetime under pure loadings, the lifetime-estimation curve for pure mechanical loading (obtained in subsection 8.2.1) and the estimated lifetime under power cycling (1500h) are also included in the figure.

Due to the difficulties in failure monitoring in mechanical loading, the mechanical single board lifetime characterization tests were conducted with a different frequency (357 Hz) than the stacked concurrent tests (460 Hz). To account for the different loading frequency, and thus different number of vibration cycles experienced per unit of time, the timescale of the mechanical data points and the mechanical fit was adjusted to allow the comparison of results. This adjustment was done by first calculating the total number of vibration cycles experienced, and then dividing this number with the frequency used in the stacked loading, or in other words

$$t_{adj} = \frac{t \cdot f_{single}}{f_{stacked}} = \frac{t \cdot 357Hz}{460Hz}, \tag{8.1}$$

where t_{adj} is the adjusted time. Albeit the change of frequency was not observed to affect the failure mode, it is recognized that the different loading frequency can have an impact on the damage accumulation rate. However, the analyses performed on the few pure mechanical test batches conducted with the stacked setup indicated that the lifetimes were in line with the lifetime prediction obtained with single boards. It is thus suspected that if the change of frequency affects the lifetimes, the effect is minor.

When comparing the results, the effect of temperature on the strain levels in concurrent loading should also be taken into account. The calculated average strain levels for the concurrent data points are presented with red circles in Figure 8.19, and the maximum and minimum strain levels are indicated with error bars.

The results indicate that at relatively high strain levels mechanical loading dominates and power cycling has very little effect on the lifetimes. As the strain levels are lowered to more moderate levels (below 0.05%), the results clearly indicate shorter lifetimes than based on the expected lifetimes of the single load test results. Even when the scatter and the other previously mentioned factors affecting the results are taken into account, the results indicate that lifetimes under concurrent loading at moderate strain levels are over a decade shorter than the expected lifetimes under single loads. When the strain levels were further lowered the lifetimes were observed to approach the lifetimes expected at pure power cycle tests.

8.5.2 Comparison of Failure Analyses

The main observed failure mode in all tests was the cracking of the bulk solder. In pure mechanical loading the solder joint fatigue was caused by the environmental stress conditions. In pure power cycling, the main cause for failure was the thermomechanical stress induced by different thermal expansion rates of materials and the failures were induced by recrystallization-assisted crack nucleation and propagation. In concurrent loading, the observed failures were very similar to the ones observed in pure mechanical loading. As no recrystallization was observed, it was concluded that the failures were caused by the applied mechanical loading rather than the thermomechanical stresses that originate from power cycling.

However, despite similar failure modes, very different damage accumulation rates and lifetimes were observed when moderate strain levels (strains from 0.05% to 0.015%) were applied. This is illustrated in Figure 8.20, where the cross-sectional views of samples subjected to concurrent loading (upper row) and pure mechanical loading (lower row) are presented. The applied strain levels are the same within both columns. Polarized light was utilized to illustrate that no recrystallization was observed in the samples subjected to concurrent loading, but to highlight the failures an additional close-up of the failed interconnections taken with bright light is enclosed. The pictured samples failed after 253.5 and 407.5 hours with respective strain levels of 0.024% and 0.030%. No failures were detected on the control samples subjected only to mechanical loading, and the samples were removed from the test and analyzed after 1500 hours. Although the imparted mechanical loading levels were the same in both cases, the mechanical control samples were completely operational despite being subjected to mechanical loading over three times longer than the concurrent samples. The cross-sectional views of two of the mechanical control samples are presented in the lower row of Figure 8.20. The cross-sectional analyses revealed only a single incipient crack that is highlighted in the image on the left-hand side.

The differences in damage accumulation rates are also evident when comparing the pure power cycling results with the results from the concurrent tests. The concurrent samples presented in Figure 8.20 failed after 253.5 and 407.5 hours, *i.e.* 507 and 815 powercycles. To illustrate the differences in damage accumulation rate and failure mode, a cross-sectional view of the source interconnection subjected to 750 power cycles (375h) is presented in Figure 8.21. The sample closely resembles

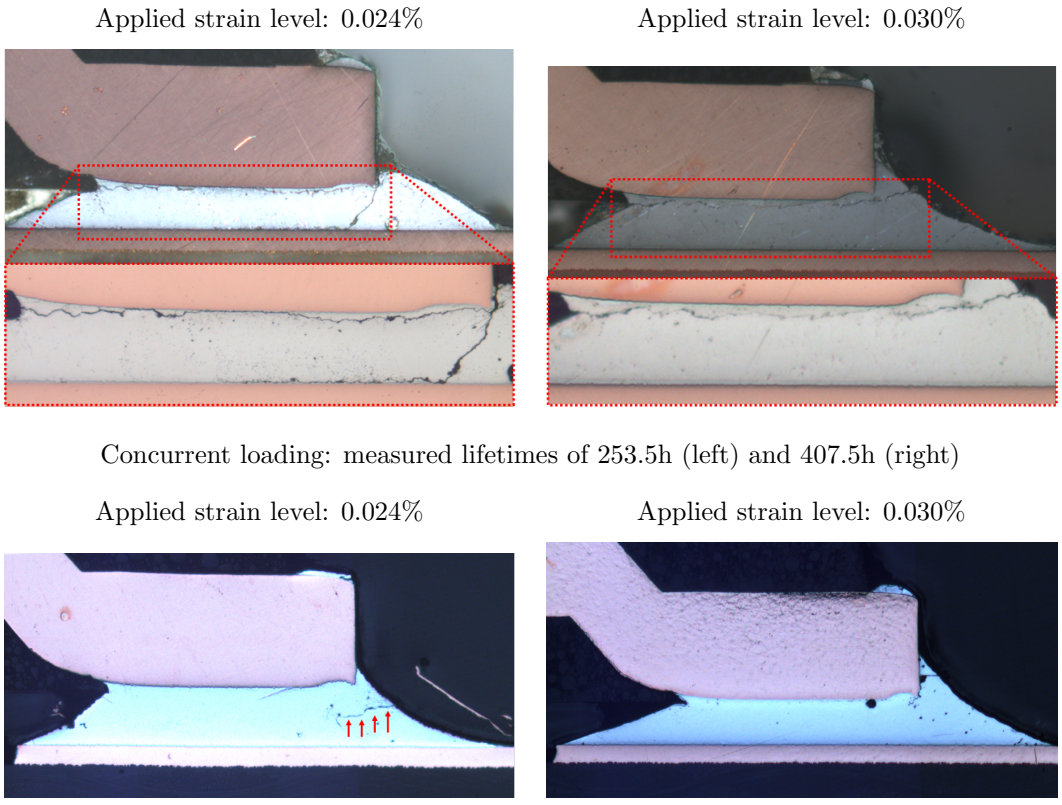


Figure 8.20: *Comparison of damage accumulation rate between concurrent and mechanical loading. The applied mechanical strain levels are the same within both columns.*

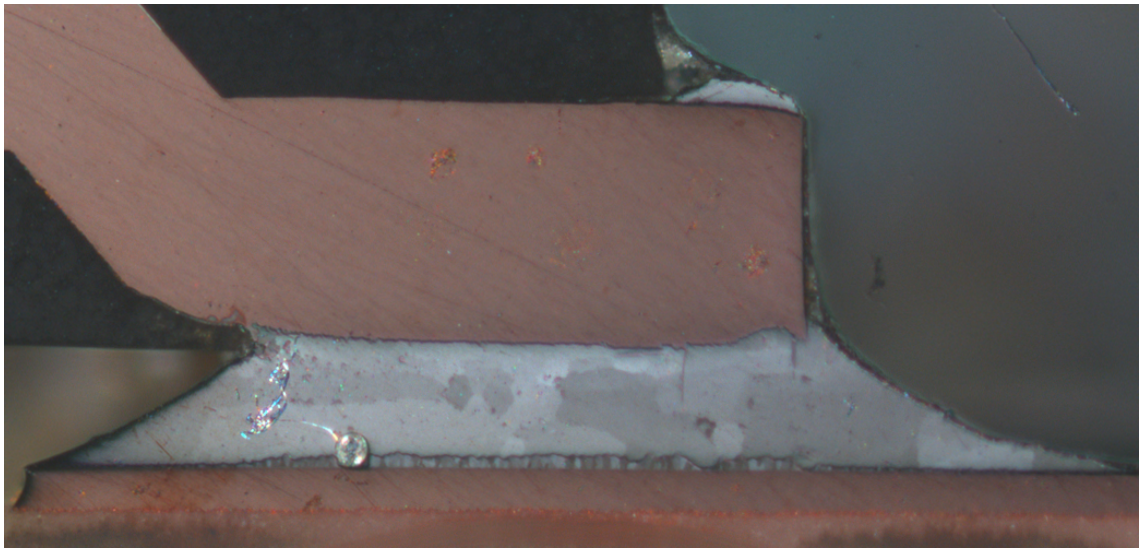


Figure 8.21: *Cross-sectional view of a source interconnection after 750 power cycles (375 hours).*

the as soldered –state with no evident recrystallization or damage. In power cycling the first signs of cracks were typically observed after 2000 power cycles, and failure is predicted to occur at 3000 cycles, so the damage accumulation rate is considerably slower than in the concurrent tests.

No recyrstallization was observed in any of the samples subjected to concurrent loading and it is thus suspected that the faster damage accumulation rate in concurrent loading is attributed to temperature related change of material properties rather than the recrystallization-assisted crack nucleation and propagation observed in the power cycling tests.

8.5.3 Comparison with Other Multiple Loading Studies

The relevant other publications on multiple loading tests and their results were summarized in section 5.2, and conclusions on the current status of multiple loading tests based on these publications were then drawn in section 5.3. The experimental results obtained in this study correspond with the results presented in the previously discussed other publications on the topic.

It should be noted that the failure mechanisms and their acceleration during concurrent loading depend on a variety of reasons. In addition to the tested components, the test assemblies, set-ups, materials, various parameters and chosen loads all affect the test results and complicate the comparisons between different studies. The component and the loadings utilized in this study all differ from the ones used in other publications. The component was a high power MOSFET transistor that proved out to be very robust. A more advanced thermomechanical loading method, power cycling, was used to better simulate the actual use conditions of the transistor. Furthermore, the other multiple loading studies involving vibration have been conducted either with random vibration loading [QOP08] or with the natural frequency of the test assembly [PS08]. In order to keep the vibration loading levels as stable as possible, a vibration frequency outside the natural frequency ranges of the various temperatures was employed in this study.

Despite these differences, similar results as in the other studies were obtained. As the separate loadings were combined, a significant decrease in lifetimes was observed. The observed decrease in lifetimes can not be explained by simply superposing the damage fractions as suggested by the linear damage super-position rule (equation 5.2). The rule neglects the interaction effects of the different loads and is not applicable for concurrent load conditions as demonstrated by [QOP08].

The other multiple loading test publications discussing the combination of vibration and thermomechanical loads [QOP08, PS08] have been focusing on the prediction of fatigue lifetimes under combined loads. In this study, however, a different approach was taken. It is evident that the complex interactions of the different loads are not understood. In order to gain more knowledge on the interactions of the loads and the failure modes and mechanisms under concurrent loads, detailed failure analyses for the single load and concurrent loading conditions were conducted.

Chapter 9

Conclusions

In order to develop a new concurrent reliability testing method as an alternative for more comprehensive and efficient reliability testing of high power electronic assemblies, this thesis aimed to clarify the failure modes and mechanisms under concurrent loading and how the combination of the loads affects the lifetimes of the test assemblies. To assess this, separate single loading tests were first conducted as baseline measurements before the single loads, namely power cycling and vibration loading, were combined into a single concurrent test method.

The comprehensiveness of the concurrent testing method is achieved with more realistic loading conditions. When compared to the traditional accelerated life tests where only a single loading parameter is employed, the new concurrent test setup clearly offers a more realistic representation of actual use environments involving local heating and vibration. Although one particular loading might be more significant than the others in actual use environments, electronic products, assemblies and components are certainly subjected to several different loadings during their field life. This is particularly true to products operating at harsh environments (such as some military, space or automotive products), where several different loadings can have comparable effects on product reliability. Besides the individual effects of the various loadings, the interactions between different loads can have significant effects on reliability. Furthermore, the interaction effects are often poorly understood and experimental tests are thus needed to verify the reliability of products. Multiple loading tests offer more realistic representations of the actual use environments than the traditional single load tests. However, to address the relevant failure mechanisms as in the use environment, the applied loads have to be chosen accordingly and care should be paid when setting the various test parameters.

The effectiveness of a test method is highly dependent on the chosen test parameters. In this study, the effectiveness of concurrent power cycling and vibration loading was studied by varying the vibration amplitude and keeping the other parameters constant. The results were then compared to single loading tests conducted with the same test parameters. The experimental results obtained in concurrent loading can be divided into three groups based on the applied strain level.

- At relatively **high strain levels** (strain amplitudes higher than 0.06%) the vibration loading dominates. Power cycling has no effect and the observed lifetimes correspond to pure vibration loading.
- At **moderate strain levels** (strain amplitudes from 0.015% to 0.06%) the experimental results clearly indicated shorter lifetimes than expected based on the single parameter test results.
- At relatively **low strain levels** (strain amplitudes lower than 0.015%) the lifetimes were observed to approach the lifetimes expected in pure power cycling.

The results thus indicate that when combined with thermomechanical loads, even relatively low mechanical loads can have significant effects on product reliability. It should be emphasized that the mechanical loading levels imparted in this study during concurrent loading were relatively low (strains ranging from 0.06% to 0.01%) when compared to typical mechanical ALTs. For example, when characterizing the test assembly, a maximum strain of 0.25% was measured during a standard [JB03] 1500G drop test. In worst cases, the effect of these relatively low mechanical loads on product lifetimes can be several decades greater when interacting with thermomechanical loads. It is thus evident that lifetime prediction based on single load tests alone can lead to erroneous results if products are exposed to various loadings and the interaction effects are not taken into account. Multiple loading tests as such offer a straightforward way to account for these interaction effects.

Regardless of the different vibration amplitude levels used in concurrent loading, no differences in the failure modes were observed. The failures were very similar to those observed under pure mechanical loading, and no recrystallization was observed in any of the samples. It was thus concluded that the failures under concurrent loading were caused by the applied mechanical loading and the faster damage accumulation rate was attributed to temperature related change of material properties. The main objectives of this thesis, to clarify the failure modes and mechanisms under concurrent loading and to find out how the combination of two loads affects the lifetimes of test assemblies, can thus be considered as fulfilled.

The results further indicate that significant improvements in both the lifelikeness of the loading conditions and in effectiveness can be achieved with the new test method. As the field life conditions can be represented more realistically and the testing times of long tests are reduced considerably, the developed concurrent loading test method can be successfully employed for studying the reliability of electronic assemblies. However, as the emphasis of this study was in the development of the new test method, no statistically valid data was obtained. It is thus suggested that the research of the developed method is further continued with an increased number of samples to gain more statistical validity. As the acceleration of damage accumulation rate was accredited to temperature related change of material properties, it might further be worthwhile to verify and quantify the effects of temperature on vibration loading. This could be done with vibration tests either with constantly powered samples or at elevated ambient temperatures.

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