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Structure and Electrical Characteristics of Graphene Field Effect Transistors

School of Electrical Engineering

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Työn tavoitteena oli tehdä kirjallisuuskatsaus grafeeni-transistoreista ja mallintaa Aalto Yliopiston Nanoteknologian tutkimusryhmän valmistamia grafeeni-kanavatransistoreja (engl. field-effect transistor).

Työn alkuvaiheessa havaittiin, että kirjallisuudesta löytyy muutamia grafeeni-kanavatransistorimalleja, jotka pohjautuvat puolijohdekanavatransistoreihin. Työssä mitattiin grafeeni-kanavatransistorien DC-käyttäytymistä ja tarkoituksena oli tehdä radiotaajuusmittauksia SiC-grafeenitransistoreista sekä CVD grafeenitransistoreista. Radiotaajuusmittauksia ei kuitenkaan kyetty tekemään SiC-transistoreista, koska transistorien kontaktiresistanssi oli liian suuri ja näin ollen katkotaajuus liian alhainen. CVD-grafeenitransitoreille tehtiin S-parametrimittaukset ja laskettiin piensignaalimallin parametrit. CVD grafeenikanavatransistorien katkotaajuudeksi saatiin 80 MHz, joka on samaa suuruusluokkaa laskennallisen katkotaajuuden kanssa.

Työssä käytettiin jo olemassaolevaa mallia transistorin DC-parametrien, varauksenkuljettajien liikkuvuus, jäännösvarauksenkuljettajatiheys ja kontaktiresistanssi, selvittämiseksi. Mallille suoritettiin validointi (engl. k-fold crossvalidation).

Avainsanat:	Grafeeni, GFET, SiC grafeeni, CVD grafeeni MOSFET, piensignaalimalli

AALTO SCHOOL OF ELECTRICAL ENGINEERING

ABSTRACT OF THE MASTER'S THESIS

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The goal of this master's thesis was to write a literature survey of graphene transistors, and to measure and model the graphene field-effect transistors (GFET) fabricated by Nanotechnology research group at Aalto University.

Direct current (DC) and radio frequency (RF) measurements were performed on graphene field-effect transistors to find out the DC and RF properties. Two sets of GFETs were measured, first chip was fabricated with SiC process and the second with CVD process. The SiC GFET impedance levels were too high to measure RF properties. RF-measurements were performed on CVD GFETs. The CVD GFET cut-off frequency was found to be approximately 80 MHz, which is in the same range as the calculated cut-off frequency. MOSFET small-signal model was used for GFETs and the model parameters are presented.

The results of the DC measurements were analyzed and the data was fitted according to an existing device resistance model. The curve-fit to total device resistance gives estimations on parameters such as contact resistance, residual charge carrier concentration and conductivity mobility. The model was validated using k-fold cross validation.

Keywords: Graphene, GFET, SiC, graphene electrical models S-parameter measurement, CVD graphene

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Preface

This thesis was written at Electronic Circuit Design group as a part of Nokia and Tekes funded Nanoradio project. I'd like to thank my instructors D.Sc. Kari Stadius and Prof. Jussi Ryynänen for the opportunity to work in this project. I'd like to thank Wonjae Kim and Juha Riikonen, and my supervisor Prof. Harri Lipsanen for collaboration. A great big thank you should also go to everyone in our lab who have helped me to get Labview and measurement setups running. A very special thanks to my home team, especially Sami Salonen whose Matlab and machine learning advice has been invaluable.

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Symbols and Abbreviations

Symbols

μ	Conductivity mobility [cm^2/ Vs]
μ_{FE}	Field-effect mobility [cm^2/ Vs]
μ_{eff}	Effective mobility [cm^2/ Vs]
ρ	Resistivity, sheet [Ohm]
Ω	Optical phonon frequency [Hz]
$\hat{R}$	Model predicted resistance [Ohm]
$\hbar$	Reduced Planck constant 1.05457$\cdot 10^{-34}$ m^{2}kg/s
C_q	Quantum capacitance [F]
C_{ox}	Oxide layer capacitance [F]
C_{TG}	Top-gate capacitance [F]
E	Electric field strength [V/m]
f_t	Cut-off frequency [Hz]
f_{max}	Maximum frequency of oscillation [Hz]
g_d	Drain conductance [S]
g_m	Terminal transconductance [S]
I_{on}/I_{off}	Current on-off ratio
k_B	Boltzmann constant 1.3806503 $\cdot 10^{-23}$ m^2 kg s^{-2} K^{-1}
L	Gate length [m]
n	Charge density/doping concentration [cm^{-2}]
n_0	Residual carrier concentration [cm^{-2}]
N_{sq}	Number of squares: L/W

n_{tot}	Total charge carrier density [cm^{-2}]
q	Elementary charge, $1.602 \cdot 10^{-19}$ [C]
Q_n	Charge density [$\mathrm{C/m}^2$]
$R_{channel}$	Channel resistance [Ohm]
$R_{contact}$	Contact resistance [Ohm]
R_{total}	Total resistance [Ohm]
T	Temperature [K]
v_F	Fermi velocity, 1/300 of the speed of light [m/s]
V_{ch}	Voltage over the quantum capacitance [V]
V_{DRC}	Top gate voltage at minimum conductance point [V]
v_{drift}	Drift velocity [m/s]
v_{sat}	Saturation velocity [m/s]
V_{TG}	Top-gate voltage [V]
W	Gate width [m]

Abbreviations

ALD	Atomic Layer Deposition
CMOS	Complementary-metal-oxide semiconductor
CVD	Chemical Vapor Deposition
DC	Direct Current
DLC	Diamond-like carbon
DOS	Density of States
GFET	Graphene Field Effect Transistor
GNR	Graphene nanoribbon
IQR	Interquartile range
ITO	Indium Tin Oxide
LCAO	Linear Combination of Atomic Orbitals
MSE	Mean squared error
NEMS	Nanoelectromechanical System

QHE	Quantum Hall Effect
RF	Radio frequency
SiC	Silicon carbide
SSE	Sum of squared error
TBA	Tight Binding Approximation
TLM	Transmission Line Model
VNA	Vector Network Analyzer

Chapter 1

Introduction

Graphene has been a purely theoretical form of carbon for decades. It wasn't until the year 2004 that Andre Geim and Konstantin Novoselov managed to produce graphene flakes with a technique called mechanical exfoliation. Geim and Novoselov were awarded the Nobel Prize in Physics in 2010 for their discovery of graphene. It is, therefore, easy to claim that 2010 has been the year of graphene. In 2010, around 3000 graphene related articles were published and roughly 400 patent applications filed. According to a recent news article in Nature [1], South-Korea is planning to put 300 million US dollars in commercializing graphene. New graphene related discoveries are in nanotechnology news almost every other day. Keeping up with the pace of progress in the graphene research field is getting quite exhausting, and the pace of new discoveries shows only slight saturation.

Graphene is a single layer of sp^2-bonded carbon atoms, that are packed in a honeycomb lattice [2]. The name graphene is sometimes misleadingly used with multiple layers, even though the variation in properties is quite significant when going from one layer to several. It should be noted that multilayer graphene can have up to ten layers, and still be called graphene. Few layer graphene (FLG) has three to nine layers. The limit where graphene becomes graphite is ten layers.

The atomic structure of graphene gives rise to exceptional electrical, optical, mechanical and thermal properties [2]. The most interesting electrical properties are high electron mobility and ballistic transport of charge carriers. However, these properties come with a twist; graphene is zero-bandgap semiconductor, or semimetal. The lack of bandgap in intrinsic graphene is perhaps, together with large scale manufacturing, the most difficult engineering issue. The zero-bandgap means that graphene cannot be switched from conductive state to non-conductive state. The lack of a band gap is a problem, if graphene is to be used in logic circuits in much the same way as silicon is used today as the material in complementary metal-oxide semiconductor logic circuits [3]. Nonetheless, the zero band gap of large area graphene is not an issue in all applications. One such example is radio frequency (RF) ap-

plications, where having no energy gap is not an issue. Transistors are not the only field, in which graphene can be used; other applications include graphene thin film electrodes, using graphene as sensing material or as photodetector to name a few.

The most studied graphene transistor today is the graphene field-effect transistor (GFET). The operation principle of a GFET is based on the ambipolar electric field effect in single- and few-layer graphene [4]. The ambipolar field effect is due to a small overlap in the valence and conductance bands. The structure of a GFET resembles that of silicon FETs. The electric current through the device is controlled by the electric field.

The aim of this thesis is to provide a literature review of graphene devices and to measure the DC- and radio frequency behaviour of top-gated graphene field effect transistors. Two batches of graphene FETs were studied, both of which were fabricated by the Nanotechnology research group located at Micronova in Otaniemi campus area. The first chip was fabricated with SiC evaporation and the second with chemical vapour deposition. DC measurements were performed for both chips and a simple AC-model was made.

The thesis is divided into four chapters. First, a literature survey is given. The electrical properties and synthetization of graphene are briefly discussed. Then the design metrics of graphene field effect transistors and the previous research in the field is considered. The experimental methods and the measurement results as well as curve-fitting results will be presented and analyzed.

Chapter 2

Background

Graphene is a purely two dimensional material. If graphene is stacked vertically to hundreds of layers, it would form three dimensional graphite. When rolled into a tube, graphene forms 1D carbon nanotubes, and when in a ball shape it forms 0D fullerenes. Different allotropes of carbon are shown in Figure 2.1.

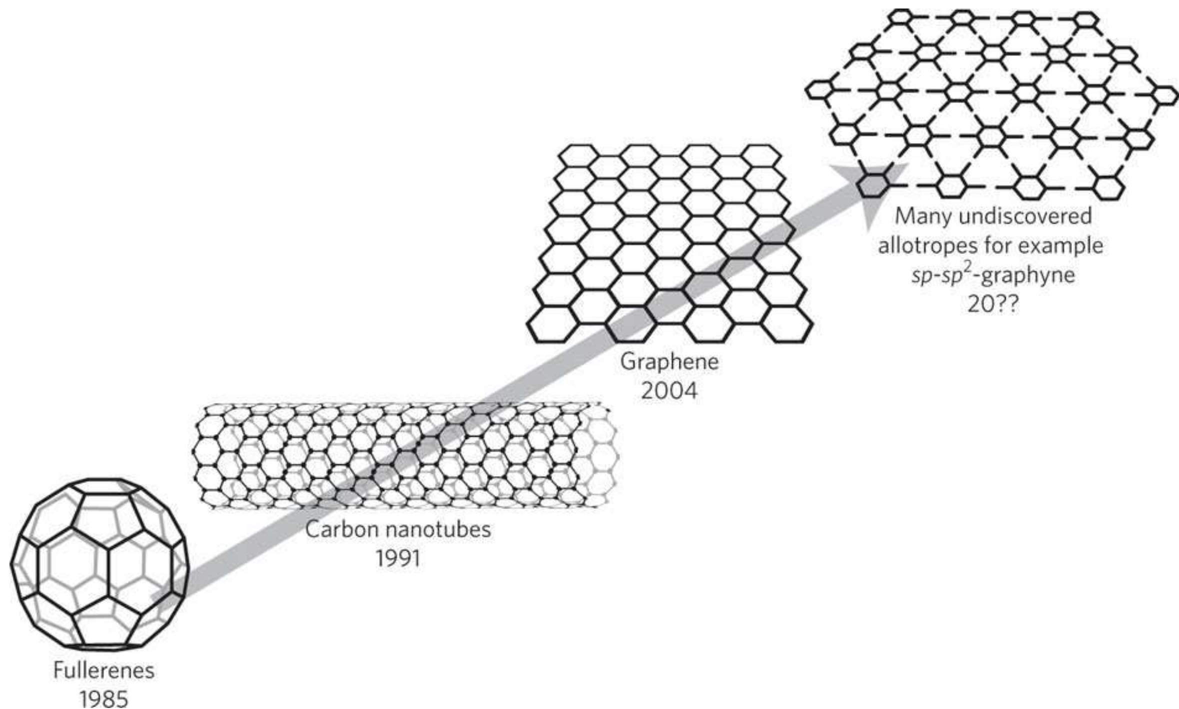


Figure 2.1: Some carbon allotropes. Adapted from reference [5]

Since the discovery of graphene in 2004, graphene has been claimed as the saviour of Moore's law. Moore's law states that the number of transistors in integrated circuits doubles every two years [6]. The consensus in the scientific community is that transistor linewidth cannot be reduced for much longer without increasing fabrication costs to such a level that the cost of a single transistor would be too high [7].

Graphene research has been focused on transistors and thin film applications, but the interest in different applications of graphene is growing rapidly [8]. Some articles have been published about graphene photodetectors and sensors. It has been suggested that graphene sensors could be used to detect gas molecules through the change in conductivity that the gas molecule causes by doping the graphene layer [9]. Another interesting application of graphene is as a material for nanoelectromechanical systems (NEMS) [10]. A piece of graphene suspended on source and drain electrodes with the gate below the graphene layer can act as a RF NEMS. The NEMS can be used as radio frequency electrical transducer with oscillation frequency in the mega Hertz range. Graphene optoelectronic research is gathering speed with the recent discovery that graphene opacity is dictated only by the fine structure constant $\alpha = 1/137$ [11].

Of all of the suggested applications of graphene, the use of graphene as a thin electrode seems the one most closest to emerge [1]. Graphene has excellent properties in the visible region of light, because the transparency is higher than 80%. The currently used material for optically transparent thin film electrodes is indium tin oxide (ITO). ITO is expensive, brittle and has relatively large sheet resistance. The need for another material to replace ITO comes mainly from the limited indium resources and hence its price. Carbon nanotubes (CNT) are at the moment the most promising technology along with graphene to replace ITO. CNT sheet large scale production is being developed by several companies, such as Finnish Canatu. Transparent electrodes are required in a large variety of applications, such as touch screen and liquid crystal displays.

2.1 Electronic Band Structure

Graphene has a honeycomb (hexagonal) structure of sp^2-bonded atoms. The electronic band structure of graphene can be solved with tight binding approximation (TBA) or the similar linear-combination of atomic orbitals (LCAO), which is more commonly used in chemistry. The honeycomb lattice has 2 atoms per unit cell, hence the π bands of graphene have 2 x 2 Hamiltonian. The diagonal elements of the Hamiltonian describe the nearest neighbour interactions, while the off-diagonal elements describe the three nearest neighbour interactions in different sublattices. The derivation of the electronic band structure is omitted here, but a detailed derivation can be found in [12].

Graphene is a 2D material, but distinctions can be made between bi-layer graphene and few-layer graphene (FLG) [2]. Bilayer graphene has two layers, but the electronic band structure is already quite different from single layer graphene. Band gaps of some hundreds of millielectron volts have been achieved with bilayer graphene by applying a perpendicular electric field to the bilayer [13]. The gap in Bernal stacked bilayer graphene arises from the forming of pseudospins between the layers, thus making it possible to electrically induce a

band gap [14].

There are still many properties of graphene that have not been thoroughly investigated. Even the existence of a band gap in large area graphene is controversial. In addition to band gap opening in bilayer graphene by applying an electric field, it is possible to create band gap by quantum confinement, i.e. by fabricating graphene nanoribbons [2]. Edges may have significant influence on electrical properties, especially with GNRs [15]. The edge effects are still being actively researched. Numerical modelling shows that strain induced band opening is also a possibility, though there is no experimental verification of strain induced band opening [16]. Band engineering of graphene is essential if graphene is ever to compete with silicon CMOS technology [14]. The energy gap is important for logic gate purposes to keep the power consumption at minimum i.e. going to a non-conductive state.

The band-structure of graphene differs from the band-structures of semiconductors in that the energy dispersion around the band edges is linear instead of quadratic [17]. The mobility of charge carriers is limited by defects in the supporting material or defects in graphene. The previous claim is backed up by the much higher mobilities achieved with suspended graphene sheets. Electronic transport that is limited by scattering is called ballistic transport. Ballistic transport is possible in very pure and defect free graphene. Naturally, obtaining clean and defect free graphene is difficult and is often not achieved. The linearity of band dispersion in graphene means that the velocity of electrons is independent of energy or momentum. Furthermore, the velocity of electrons in graphene is at maximum the Fermi velocity, which is 1/300 of the speed of light. Another intriguing property is that backscattering through phonons or charged impurities is forbidden and the mean free path is in the range of hundreds of nanometres.

Figure 2.2 shows the electronic band-structure of graphene. The Figure was plotted with Matlab using the equation and values given in [12]. The linear dispersion around the Dirac point, the part where the conductance and valence bands meet, can be seen from the band diagram.

The electrical properties of graphene have been studied extensively, but much is still unknown about the mechanical and thermal properties [8]. Mechanical and thermal properties of graphene are similar to those of carbon nanotubes. Measurements show that the breaking strength of graphene is around 40 N/m, and thermal conductivity in the range of 5000 W/mK, and yet the thermodynamic properties of graphene are largely unknown [8]. The chemistry of graphene is in early phases, but shows much promise. Graphene can absorb and desorb different atoms and molecules, such as K and OH. Adsorbates can affect the electronic properties of graphene. There is even the possibility of localized doping. In addition, the stability of graphene under various circumstances has not received much attention.

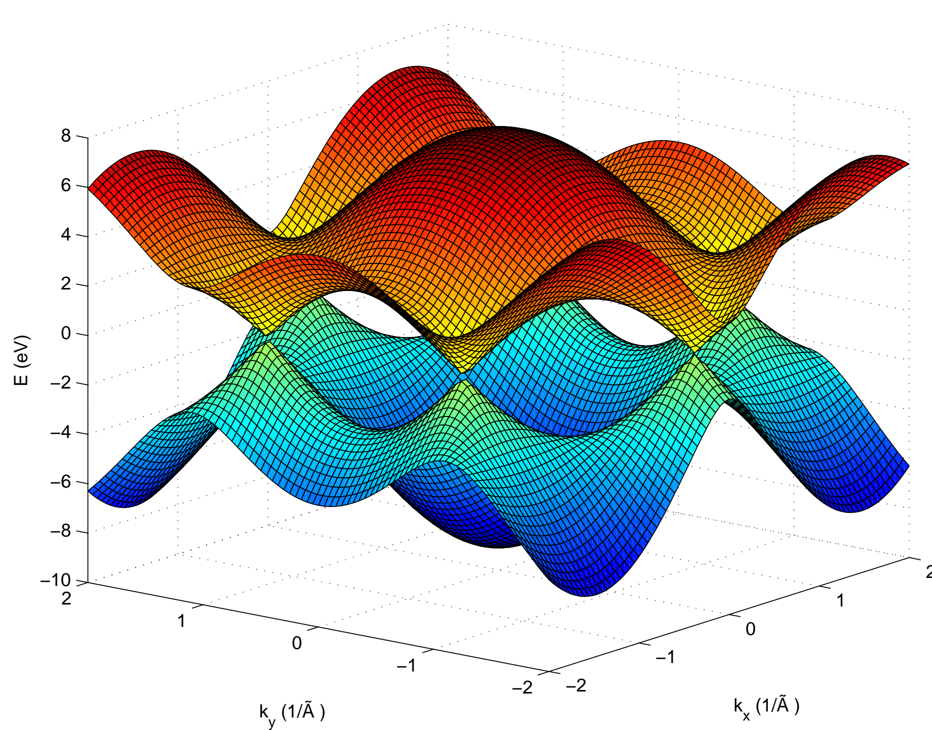


Figure 2.2: The electronic dispersion in graphene.

2.2 Graphene Synthesis

Though the synthetization of graphene is not the focus of this thesis, it may be beneficial to briefly discuss the most commonly used synthetization methods in order to understand the challenges in fabricating graphene transistors. After the discovery of graphene by mechanical exfoliation, often called the 'Scotch tape method', serious attempts have been made to produce large areas of top quality graphene [14]. The importance of high quality graphene with few or no defects can not be emphasized enough. The investigations into electron transport in graphene and current saturation show, that defects are the most important factor in hindering the transport of electrons (holes). In 2010, the time of writing this thesis, the best graphene quality is still achieved with mechanical exfoliation. However, two synthetization methods with great potential for large scale manufacturing of graphene have been developed, namely graphene grown with chemical vapor deposition (CVD) and silicon carbide (SiC) desorption method [14].

Mechanical exfoliation works, to a large extent, as the name suggests. First, a piece of bulk graphite is repeatedly peeled with tape to separate layers of graphene, which is then transferred onto a substrate, usually silicon dioxide SiO_2 [2]. This technique has become a form of art. The problem is in finding those single layer graphene samples and finding one with the right size for further studies. Novoselov and Geim discovered in 2004 that the invisible graphene flakes become visible on (SiO_2) substrate that is of a certain thickness. The phenomenon is due to optical interference at the graphene-substrate interface. Raman

spectroscopy can be used to find out if the graphene flakes are single, few- or multilayer.

Graphene can be synthetized by sublimation of silicon from SiC in high temperature (1200°C) in ultra high vacuum [18]. The benefit of this method is that the SiC provides an insulating substrate and no transfer of the graphene layer is needed in order to fabricate top gated FETs. Yet, the disadvantage of this method may outweigh its advantages; the high temperature is cost-ineffective, and thus may not be suitable for large scale manufacturing. The graphene layer has different properties depending on the crystal growth face [8]. Graphene grown on Si-terminated face has poor homogeneity and crystal quality and is subject to unintentional doping. Graphene grown on C-terminated SiC is often called 'turbostatic' graphene, because of the rotatiotal disorder. Graphene grown on C-face has higher mobility than on Si-face and has less doping.

Growing graphene with CVD is an attractive solution, because it is compatible with existing semiconductor industry processes [14]. Graphene has been grown with CVD on metal substrates, such as nickel (Ni) and copper (Cu). With CVD, the graphene layer needs to be transferred to a substrate, which is somewhat difficult and may degrade the quality of the layer and lead to folding of the layer. However, CVD synthetized graphene has larger grain size. Researchers are optimistic about extending CVD growth to silicon wafer sizes.

Other suggested methods of large scale graphene synthetization are direct chemical synthetization [8], ion implantation [19], crystal sonification [8] and even unzipping carbon nanotubes to form graphene sheets [20].

2.3 Graphene Field-Effect Transistor Structure

Graphene FET research was fueled by the discovery of the ambipolar electric field effect in graphene by nobelists Novoselov and Geim in 2004. Novoselov and Geim showed that the electronic properties of few layer graphene (FLG) greatly differed from those of bulk graphite, a 3D structure.

The sheet resistivity of graphene was found to have a peak of a few kOhms and decays to some hundreds of Ohms with changing the gate voltage [4]. The resistivity peak, often called dirac point or minimum conductance point, is located approximately at zero gate voltage in pure graphene. The location of the Dirac point depends on the difference between the work functions of the gate and the graphene, doping (electrical or chemical), and type and density of charges at the interfaces at the top and bottom of the channel. The Dirac point changes with adsorbed water or other ambient adsorbing molecules [21]. Positive gate voltages promote n-type, electron, conduction and negative voltages give rise to p-type channel (hole conduction). Figure 2.3 shows an example of a measured gate- voltage drain-current curve for a SiC GFET fabricated at Micronova. This particular transistor has the Dirac point

quite far from zero gate bias, which is most likely due to unintentional doping during the fabrication and storage in room temperature. The transport curve in Figure 2.3 is quite symmetric, but often the transport is asymmetric due to charged impurities or graphene-electrode contact. Asymmetry in this case means that electrons and holes have different mobilities [3].

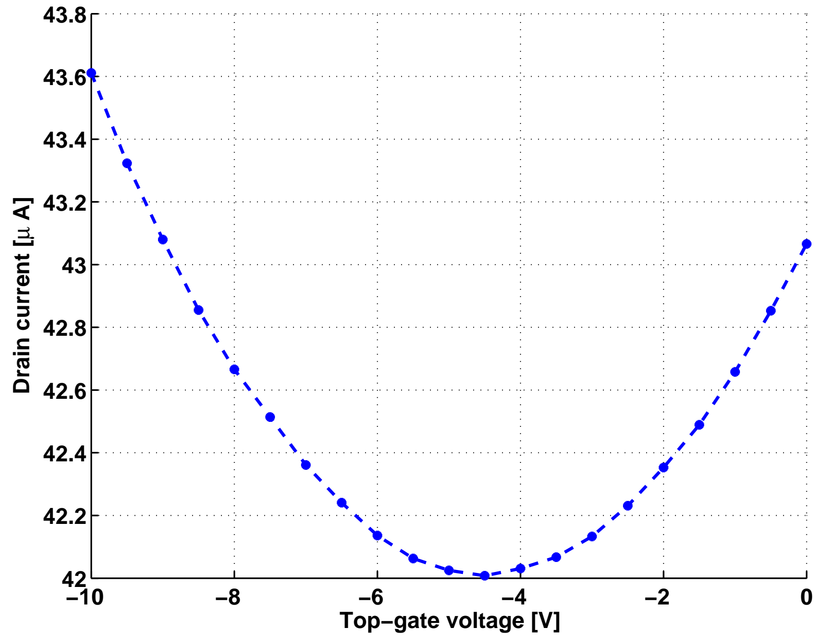


Figure 2.3: The Dirac point of a SiC GFET with 0.5 V drain-source voltage and W=10 μm and L=4 μm

Novoselov and Geim explain the ambipolar field effect by a 2D metal with a small overlap between valence and conductance bands [4]. The electric field induces doping in graphene by changing the Fermi energy, which should not be confused with the context of doping in semiconductors e.g. silicon.

Graphene is unique as a channel material, because unlike other semiconductors, graphene does not require impurity doping to conduct electricity. Graphene displays a phenomenon that is often called self-doping. Self-doping refers to the electric field effect in graphene, which allows the charge carrier type and concentration to be controlled with an outside electric field, or rather gate voltage.

The doping levels of graphene can be monitored with Raman scattering [22]. The raman peak intensity and displacement varies according to the applied gate voltage. The ambipolarity of graphene makes it possible to operate a graphene transistor with either electrons, holes or both simultaneously.The graphene bandstructure allows the conduction to shift from electrons to holes by changing the Fermi level. Das et al. [22] estimated the doping concentration in an electrochemically top gated GFET as

$$V_{TG} = \frac{\hbar|\nu_F|\sqrt{\pi n}}{e} + \frac{ne}{C_{TG}} \tag{2.1}$$

where ν_F is the Fermi velocity, n the doping concentration, and C_{TG} is the top gate capacitance calculated as a parallel plate capacitor.

The Hall coefficient R_H changes sign at dirac point [4]. The resistivity ρ of graphene is described by the classical equation

$$\rho^{-1} = \sigma = ne\mu \tag{2.2}$$

where n is the doping concentration, σ conductivity and μ the mobility of graphene.

According to Banerjee et al. [14], the transport properties of graphene are affected by the quality of the graphene layer, the interface with insulators and the metal contacts. The quality of the graphene is mostly affected by the fabrication process [23].

A graphene field effect structure is constructed from bottom to top as follows: substrate, graphene layer as the channel, dielectric layer and source-drain electrodes and top gate electrode. An example of a GFET is shown in Figure 2.4. Figure 2.4 shows a two gate-finger structure that is used when making S-parameter measurements. It is common that in physics journals GFETs are often misleadingly referred to as dual-gate transistors, when the devices have both a top gate and a heavily doped bulk substrate working as a back gate, whereas dual-gate transistor commonly means a transistor with two top gates.

A structure with substrate contact and a top gate is used to allow more control in electronic properties [24]. The reason for using both back gate and top gate, is that it allows more freedom in adjusting the doping by gate voltage, thus allowing more precise control in device resistance. The idea is that when the channel resistance is minimized, the transconductance is maximized. SiC substrate is insulating, and therefore SiC GFETs must naturally have a top gate. It is often simpler to fabricate a transistor with only a back gate for research purposes, because the layer under the substrate is often chosen as heavily doped silicon, that can be directly used as a back gate.

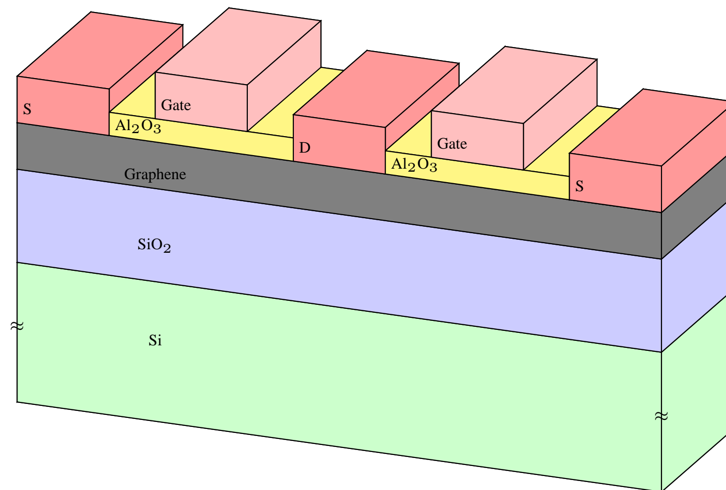


Figure 2.4: 3D view of a GFET with two top gates.

GFET channel material, graphene, can be either monolayer, bilayer or few-layer graphene. The operation of the transistor is affected by the number of graphene layers in the channel, because the electrical properties change when going from single layers to few layers. The number of layers can be deduced from Raman measurements [22].

Specific contact resistance is important for graphene transistor operation, because high specific contact resistivity may degrade the overall device performance and thus lose the edge that graphene properties offer, such as high mobility and ballistic transport of graphene [14]. The contact between graphene and metal is most often ohmic, but the low density of states (DOS) in graphene may hinder current injection [25]. Typical metals used for contacts are Ti/AU, Cr/Au and Cr/Pt.

A general guideline for choosing contact metals is to ensure that the contact is ohmic, and secondly to choose such a metal that its work function is as close to the semiconductor band gap as possible. Contacts can be deposited with e.g. electron beam lithography [26].

A recent study by Liu et al. [23] shows that contact resistance is affected by the processes used in fabrication. For example, sputtering leads to larger contact resistance than electron beam (EBM). The higher contact resistance caused by sputtering is possibly due to carbon vacancies in the graphene lattice. Liu et al. propose that the sometimes perceived asymmetry between hole and electron transport may be due to the contacts changing from p-p-p junction to p-n-p under gate modulation. Interestingly, the contact resistance decreases as the number of graphene layer increases when using sputtering process. The same does not apply for electron beam.

Contact resistance can be measured with a setup, in which the channel length is varied. One such measurement for graphene FETs has been performed by Nagashio et al. [25]. A similar measurement was performed for GNRs and is explained in [15]. The contact resistivity measurement is based on transmission line model (TLM), in which the metal-semiconductor interface is expected to be ohmic. In the setup a sequence of metal contacts is patterned on graphene with increasing channel width. The resistances are measured and contact resistivity can then be calculated according to TLM. The sheet resistance of graphene is needed to calculate the conduction length.

According to [25], the current enters graphene preferentially at the edge of the contact metal instead of from the whole contact area between metal and graphene. For contact lengths shorter than the calculated conduction length, the conduction becomes area conduction. Typical values for graphene sheet resistance is 250 Ω at $\mu = 5000$ cm^2/Vs and n = $5 \cdot 10^{12}$ cm^{-2}. The result of [25] is that it is preferable to choose a metal with higher work function than that of graphene to increase the graphene DOS and reduce contact resitivity.

Choosing the insulating material for a graphene FET is crucial. The gate dielectric should be very thin and uniform with high dielectric constant, often denoted with the symbol κ

[14]. Contrary to choosing metal contacts, the density of states at the interface should be low. High-κ materials are important in designing ever smaller transistors. Common high-κ materials are HfO_2 and Al_2O_3, which can be deposited with atomic layer deposition (ALD) [27]. Graphene is chemically very inert, and this poses difficulties for the deposition of dielectrics. The dielectrics do not stick well to graphene and the use of ALD is challenging because graphene is hydrophobic. The hydrophobic nature of graphene can be circumvented by depositing nucleation centers of aluminium.

2.4 State of the Art GFETs

There's plenty of room at the bottom. This may be true, but the semiconductor industry is investing heavily in the so-called 'More-than-Moore' or 'beyond-CMOS' technologies [7]. For decades the semiconductor industry has been leaning forward trusting that the Moore's law will hold.

Beyond-CMOS is an umbrella term for technologies that might replace CMOS one day, whereas More-than-Moore is used to describe the incorporation of new functionalities in devices [7]. The consensus among the semiconductor industry is that CMOS technology, that is the ruling logic technology in use, cannot be scaled down much longer. The limitations come from the fabrication technology and the material properties of silicon. Photolithography, that is the fabrication technology today, is a top-down process, and is becoming all the more expensive the smaller the feature size. Yet, Beyond-CMOS devices may never replace CMOS completely, but gain market share in niche applications.

The research on graphene transistors so far can be divided into two groups: logic devices and RF devices. The design goals in these two categories are quite different. Logic devices need to have low energy consumption when in static state, in which case the graphene channel has to be switched to a non-conductive state, i.e. graphene needs a band gap [14]. Graphene room temperature on-off current ratios are not yet good enough for logic circuits. The important metrics that must be met in order for graphene logic devices to replace CMOS are room temperature operation, higher speed, scalability and size, device gain and cost. CMOS technology excels in all of the metrics mentioned, and it remains to be seen if graphene logic devices can mature to replace CMOS.

In RF devices, it is not so important that the device can be turned off, but the high speed and low noise are the design goals [3]. Graphene, a semimetal, or a semiconductor with zero bandgap, may not be ideal for logic devices, but the required characteristics are different for RF devices. RF devices commonly suffer from short-channel effects and the series resistances between the drain, channel and the source. Graphene offers an edge here; as graphene is only one atom layer thick, it offers the thinnest possible channel, thus improving the electrostatics of the device.

2.4.1 Graphene RF Devices

Radiofrequency transistors are a key component in wireless communication devices. RF transistors amplify signals and provide gain at very high frequencies. The high mobilities achieved with graphene FETs have shown much promise for RF transistor development. Let us define cut-off frequency as the frequency f_t at which the device current gain drops to unity, and the maximum frequency of oscillation as the frequency f_{max} at which the power gain becomes unity. The recent progress in RF-GFETs is mapped in Figure 2.5 by F. Schwierz [28]. Figure 2.5 shows that though there has been progress in RF GFETs these past few years, the GFETs are still outperformed by InP and GaAs mHEMTs. Graphene FETs show quite high cut-off frequencies, but the maximum frequency of oscillation is another interesting parameter that is often disappointingly low. Unfortunately GFETs have low value of f_{max}. It should be noted that in Figure 2.5 the Wu et al. GFETs are made by CVD process and not by the 'Scoth-tape'-method.

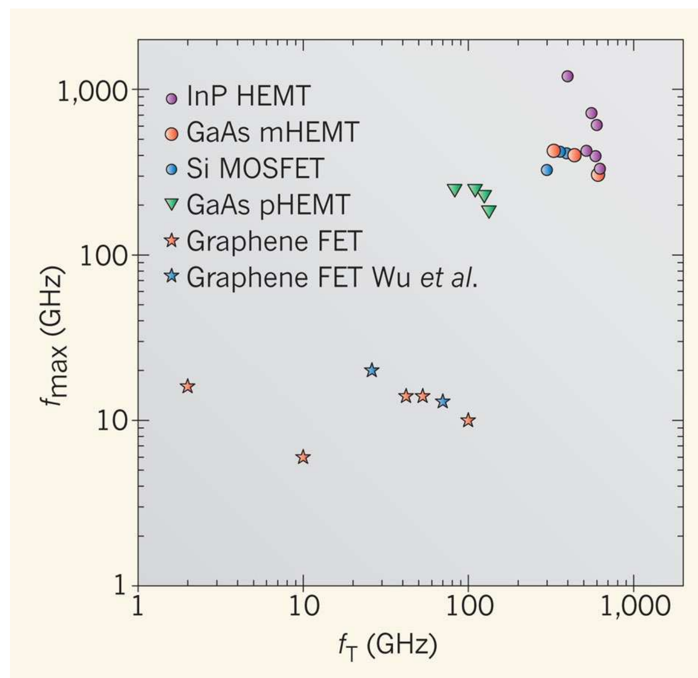


Figure 2.5: The maximum frequency of oscillation as a function of cut-off frequency. Figure adapted from [28].

Currently, the fastest reported GFET has the cut-off frequency of 170 GHz with 90 nm channel length [29]. For perspective, cut-off frequency of around 600 GHz, has been achieved with GaAs metamorphic high electron mobility transistor (mHEMT) with a 20 nm gate or InP HEMT [28]. Graphene as a large area sheet may offer higher mobility than semiconductor crystals, but the very weak or non-existent current saturation of GFETs limit the highest achievable cut-off frequency, intrinsic gain and other properties of interest in RF devices [3]. Constant progress has been made in improving GFET cut-off frequency, and the devices are limited by the series resistances. GFET cut-off frequency could be improved to 350 GHz, if

the series resistances can be minimized and a self-aligned gate structure is used [29].

Lin et al. from IBM demonstrated a 100-GHz GFET using epitaxial SiC process [30]. GFETs were fabricated on a 2 inch graphene wafer. For perspective, current silicon processes allow wafer sizes up to 16 inch. The gate dielectric was a spin-on dielectric poly-hydroxystyrene and HfO_2 on top. Lin et al. had promising results with the uniformity of the graphene; the dirac point was consistently at -3.5V gate bias. Despite the extrapolated 100 GHz cut-off frequency, the devices failed to show current saturation.

The improved performance of Lin et al. [30] transistors can be attributed to reduction in access resistances and enhanced mobility due to better dielectric deposition and high-κ material. The significance of access resistance grows as the channel length shrinks. Lin et al. report that they used a back-gate to modulate the access resistance through electrostatic doping. The back-gate was used to provide electrostatic doping in areas where the top gate does not reach, and thus lower access resistance. The total resistance of the graphene device was modelled by Lin et al. [24] as the sum of ideal graphene channel resistance modulated by the top gate, and a series resistance R_s

$$R_{total} = R_s + \left[\frac{e\mu W}{L_G} \sqrt{n_0^2 + \left(\frac{C_{tot}}{e} \cdot (V_{TG} - V_{DRC}) \right)^2} \right]^{-1} \tag{2.3}$$

C_{tot} is the total capacitance of the top gate consisting of top gate capacitance and graphene channel quantum capacitance. The top gate dirac voltage is denoted as V_{DRC} and n_0 is the minimum sheet carrier density, determined by disorder and thermal excitation.

Graphene based FETs have been found to operate much the same way as their MOSFET counterparts. The GFET intrinsic current gain follows the $1/f$ frequency dependence and the cut-off frequency f_T is dependent on the dc transconductance g_m of the device and is given by

$$f_T = g_m/(2\pi C_g) \tag{2.4}$$

where C_g is the gate capacitance [31]. The cut-off frequency was deduced from S-parameter measurements by Lin et al. [31]. The cut-off frequency is also found to be inversely proportional to the square of the gate length.

2.4.1.1 IBM GFET with 155 GHz Cut-Off Frequency

The fastest GFET made with CVD process at the time of writing this thesis has the cut-off frequency of 155 GHz with 40 nm gate length, which is also the shortest gate length so far [32]. The result is quite remarkable considering that the CVD process is IC-compatible.

The high cut-off frequency was achieved by using diamond-like carbon (DLC) instead of SiO_2 as the dielectric layer [32]. DLC has a higher phonon energy and lower surface trap

density than SiO_2. The single layer graphene was grown on copper foil at 1000 Celsius degrees and was then transferred on to the DLC using a PMMA as protecting layer and dissolving the Cu with $FeCl_3$. A transistor array was fabricated with a conventional top-down process.

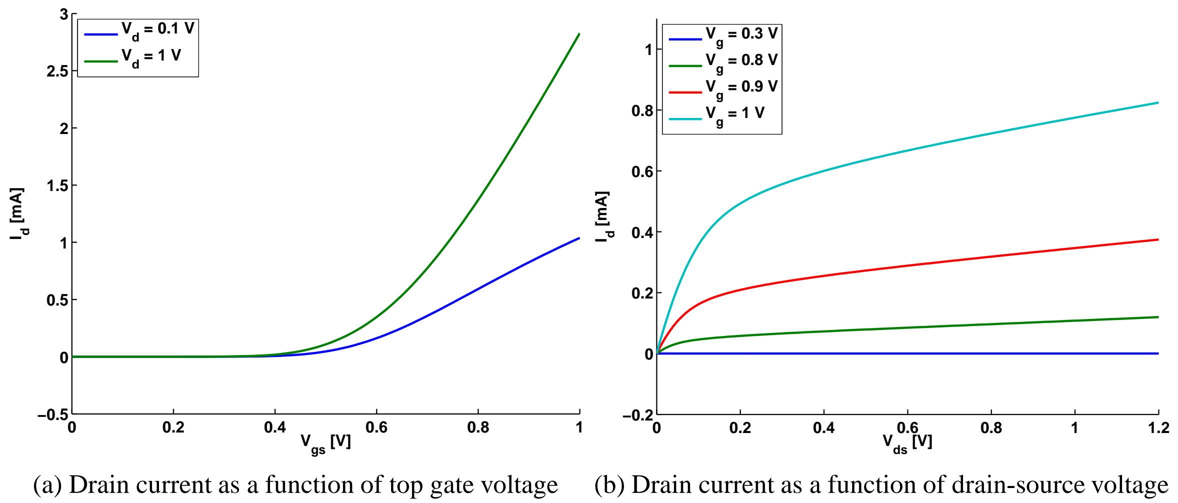
The 40 nm GFET has the Dirac point at -7V, and is due to impurity doping [32]. The GFET has lower gate modulation than longer transistors because the contact resistance has larger role in short channel FETs. The modulation is adversely affected by 'short-channel effects', i.e. the electrostatic control efficiency of the top gate is reduced by the drain voltage. The short-channel effects are not yet well understood in graphene transistors. The transconductance of the 40 nm GFET suffers from these short-channel effects and is at maximum roughly 35μS/μm with V_{ds}=0.4 V. The transconductance is expected to decrease when scaling down the GFETs due to Klein tunneling and graphene p-n-junctions. It is claimed in [32], that there will be a trade-off between device size and performance when it comes to scaling down GFETs. Future efforts on improving GFET RF performance should focus on reducing contact resistance and optimizing the FET structure to achieve higher f_{max}.

Graphene FETs have a surprising advantage in low temperatures, the operation of the DLC substrate GFETs is not affected by low temperature [32]. This feature is useful in specialised applications, for example outer-space applications.

2.4.1.2 A 65 nm Silicon NMOSFET

The competing and currently most used technology is silicon MOSFET. Silicon based MOS-technology is used in a wide range of applications from smart phones to cars, and sets the milestones for competing technologies. Silicon MOSFETS are similar to GFETs; the basic structure is the same, but some material choices may differ. Important figures of merit of silicon 65 nm MOSFET are shortly reviewed in this section, so that comparison between graphene and silicon technology can be made.

Figures 2.6a-2.6b show a the current-voltage graphs of a typical 65 nm slicon NMOSFET. Figure 2.6a shows the drain current plotted against top gate voltage with two drain-source voltages. The lower curve is in the linear transistor operation region and the upper in saturation region. Figure 2.6b shows the drain current as a function of drain-source voltage with different top gate voltages. The transistor shows a clear current saturation after approximately 0.1 V (drain-source). The transistor turns completely off. Table 2.4.1.2 summarizes the performance of the NMOSFET.



(a) Drain current as a function of top gate voltage (b) Drain current as a function of drain-source voltage

Figure 2.6: For a 10 μm/0.1 μm NMOSFET, the current on-off ratio is in the range of $\approx 10^7$. The transconductance in 2.6a is 2 mS in the lower curve and 8 mS in the upper.

Table 2.1: NMOSFET with W/L 10/0.1 (μm).

g_m	V_{ds}	I_{ds}
2 mS	0.1 V	0.5 mA
8 mS	1 V	2 mA

2.4.2 Graphene Digital Devices

Digital graphene devices have been intensily researched ever since graphene was first discovered. Alas, graphene's lack of band gap has turned out to be an issue that is yet to overcome. The results in graphene digital devices have been so disappointing, that IBM, the company leading the graphene research, has already stated that it is unlikely that graphene would ever replace silicon technology [33]. Nonetheless, two interesting proof of concept papers have been published and will be briefly reviewed in this section.

Yang et al. [34], proposed a triple mode single-transistor graphene amplifier in 2010. The operation is made possible by the ambipolarity of graphene, which enables different points of operation. This device can be considered as proof of concept, though the properties of the proposed graphene amplifier are yet inferior to conventional MOSFET technology. Single-transistor graphene amplifiers have several advantages over the current technology. Single-transistor amplifiers take less space, and thus use less components and materials. In addition, it is beneficial that the transistor can be configured in-field, which in infeasible with MOSFETs. It has also been suggested that the $1/f$ noise is quite low in graphene transistors. At the moment, the small transconductance and very low current saturation limit the operation.

Sordan et al. [35], have demostrated four basic input logic gates with a single graphene transistor. Needless to say, it is desirable to have fewer transistors. Their idea is similar to the triple mode transistor of Yang et al. Sordan et al. graphene logic gate uses the charge

neutrality point to implement boolean logic. The gate values are decoded with resistance values as shown in Figure 2.7.

The logic gates demonstrated, showed promise in the possibility of a configurable logic gate [35]. Alas, there are issues with the proposed design. The fact that graphene cannot be turned off, makes the power consumption unacceptably high. Sordan et al. suggest that the transistor resistance could be increased to lower the static power usage. Then again, a higher resistance would slow the response time of the transistor. Furthermore as the the input and output logic voltage levels are not the same, cascading the gates would require additional transistors.

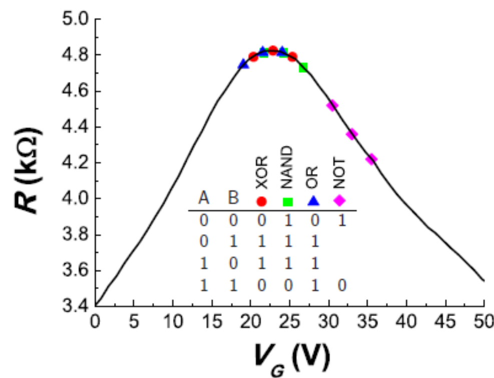


Figure 2.7: The four logic gates. Adapted from [35].

2.5 GFET Circuit Models and Characterization

Graphene field-effect transistor modelling and characterization methods develop alongside the fabrication technology; the better the quality of the GFETs, the better models can be made for the transistors. One of the issues in empirical modelling of GFETs is the variation in GFETs due to fabrication.

The interesting parameters of GFETs are mobility, system capacitances, contact and channel resistance, current saturation velocity and conductances, such as transconductance. Quantum capacitance and mobility parameters will be reviewed in the following sections.

The existing graphene FET circuit models and small signal models, all rely on the observation that GFETs behave similarly to MOSFETs. The operation of GFETs near the minimum conductance point has not been thoroughly analyzed yet as the operation near the Dirac point is not completely understood. For example, the exact mechanisms leading to widening of the Dirac point to a plateau have not been throughly studied.

2.5.1 Quantum Capacitance

Graphene shows a capacitive behaviour under electric field, that is referred to as quantum capacitance. Quantum capacitance in graphene is due to the peculiar linear energy dispersion. In graphene field-effect transistors, the graphene/insulator/semiconductor interface the graphene layer adds a capacitor in series with the insulator and semiconductor capacitance contributions. Graphene quantum capacitance is in series with the gate oxide capacitance and must be taken into calculations. The quantum capacitance of the graphene channel has to be taken into account when the gate dielectric thickness is reduced. The quantum capacitance is derived from the density of states (DOS) of graphene assuming the Fermi-Dirac distribution for charge carriers [36].

The quantum capacitance of graphene is approximately linearly dependent on the channel voltage and has a minimum value around the minimum conductance point [37]. Furthermore, the capacitance is symmetric with respect to the Dirac point [38]. Quantum capacitance is expressed in reference [37] as

$$C_q = \frac{2q^2 k_B T}{\pi(\hbar v_F)^2} \ln\left[2\left(1 + \cosh\frac{qV_{ch}}{k_B T}\right)\right] \tag{2.5}$$

where k_B is the Boltzmann constant, $\hbar$ the Planck constant and V_{ch} is the voltage over the graphene channel. Equation (2.5) can be simplified to

$$C_q \approx q^2 \frac{2qV_{ch}}{\pi(\hbar v_F)^2} = \frac{2q^2\sqrt{n}}{\hbar v_F \sqrt{\pi}} \tag{2.6}$$

when $qV_{ch} >> k_BT$. According to reference [37], the quantum capacitance is influenced by impurities and defects.

Since the quantum capacitance of graphene is linear with respect to the applied top gate voltage, the quantum capacitance could be used in sensor applications. The challenge is in measuring the very small changes in the quantum capacitance.

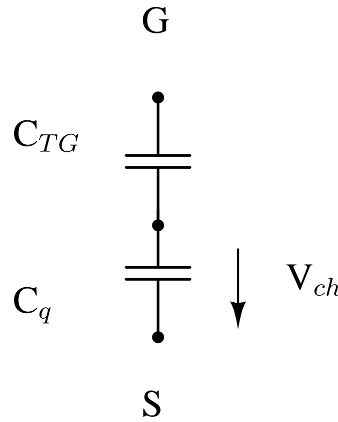


Figure 2.8: Quantum capacitance equivalent circuit.

2.5.2 Mobility

Charge carrier mobility is often used as a figure of merit when investigating the transistor properties. A high mobility value means a fast transistor. Mobility is restricted by scattering caused by perturbations in the periodic lattice and by impurities [26]. Unlike semiconductor materials, such as silicon, graphene doesn't have to be doped with impurities, which is in part the reason why graphene devices show very high mobilities. Different definitions and ways to calculate mobilty values for GFETs will be presented in this section.

Drude model of electrical conduction can be used to calculate the conductivity mobility if the sample length is much larger than the transport mean free path [39]. The transport mean free path for graphene is estimated to be around 100 nm, therefore the Drude model is applicable for samples in the micrometer range [22].

There are three types of mobilities that can be defined for a metal-oxide-semiconductor FET; field-effect mobility, effective mobility and saturation mobility [26]. In addition to the previous, Hall mobility can be measured and calculated, but obtaining Hall mobility value requires that a Hall-bar device is fabricated. Effective mobility is defined with the help of drain conductance g_d and mobile charge density Q_n.

$$\mu_{eff} = \frac{g_d L}{W Q_n} \tag{2.7}$$

The field-effect mobility is usually lower than the effective mobility. The difference between these mobilities is that the the electric field dependence of the mobility is neglected in Equation (2.8).

The field-effect mobility is given as

$$\mu_{FE} = \frac{L_{ch} g_m}{W_{ch} C_G V_{DS}} \tag{2.8}$$

where V_{DS} is the drain-source voltage. The use of Equation (2.8) requires that the influence of the series resistance is removed. The gate capacitance C_G should include the quantum capacitance of the graphene layer.

Saturation mobility is often not as interesting a parameter as saturation velocity. Most of the current GFETs show no current saturation, with the exception of Meric et al. top gated GFETs [40].

Table 2.5.2 shows some reported graphene FET mobilities. The purpose of the table is to show the ambiguity of reported mobility types and the divergence of the measured values. The conductivity mobilities are as expected, but the carrier mobilities are hard to interpret due to lack of information about the used formulae and measurement setup.

Table 2.2: A collected table of reported mobilities of GFETs.

Layers	Mobility type	Growth method	Reference
1-2	Conductivity mobility for holes 710 cm^2/Vs and 530 cm^2/Vs for electrons	Mechanical exfoliation	[41]
1-2	Hall mobility 1575 cm^2/Vs Field-effect mobility 1400 cm^2/Vs	SiC	[42]
1-2	Field-effect mobility 800-1500 cm^2/Vs	SiC	[30]
1	Field-effect mobility 2700 cm^2/Vs	Mechanical exfoliation	[24]
2	Carrier mobility 1000 cm^2/Vs	Mechanical exfoliation	[13]
1 ?	Low field field-effect mobility 1200 cm^2/Vs	Mechanical exfoliation	[40]
1?	Low field field effect mobility 10000 cm^2/Vs	Mechanical exfoliation (h-BN dielectric)	[43]

It should be mentioned, that the mobility of graphene transistors is not so well defined figure of merit. It is not always clear which definition for mobility has been used in the previous studies on GFETs. Sometimes the inadequate reporting of the definition used for mobility may lead to confusion [3]. In [3] it is reported that the whole concept of low-field mobility

in the case of 2D graphene is misguided. The electric field strengths in short channels are high even with relatively low drain-source voltages. At high electric fields, the velocity of charge carriers is expected to saturate. The vague defitions and differing measurement methods make the comparison of reported mobility values of FETs difficult. Furthermore, the reported high mobility values are for gapless large area graphene, which is expected to have higher mobility than graphene with band gap, either bilayer or band engineered [3]. Nonetheless, even the meagre mobility values for bilayer graphene are considerably higher than for silicon. For a more detailed description about different definitions for mobility, see [26].

There are three common methods in literature to extract the mobility from measurements [44]. The first one is to measure the transport curve σ-V_g and use the Equation $\mu = \Delta\sigma/(C_g \Delta V_g)$ to fit mobility in a linear regime. This methods suffers from the fact that the transport curve is nonlinear, and choosing a linear regime is somewhat arbitrary. The second method is to calculate the conductivity mobility with the equation below

$$\mu = \frac{\sigma}{nq} = \frac{\sigma}{C_g(V_g - V_{drc})} \tag{2.9}$$

Equation (2.9) depends on charge carrier density or gate voltage. The problem with the second method is that it doesn't apply near the Dirac point because the carrier density is not well-defined. The third method is to use curve fitting to total resistance vs. gate voltage measurement. The third method is used in this thesis and the equations (4.3) that are used to fit the curve are shown in Chapter 4. Xia et al. [44] studied the effect of top dielectric medium on back gate capacitance. The observation is that the gate capacitance can increase by 2 orders of magnitude when the top gate dielectric size is varied, while the mobility stays constant. This could enable new types of GFET based sensors.

2.5.3 Drain Current and Current Saturation

Most graphene FETs have been studied in low temperature, because researchers fear that charged impurities will affect the measurements. Still, in order for the GFETs to compete with existing technologies, they need to operate in room temperature. The room temperature measurements on GFETs so far have not been very promising. If the lack of band gap is acceptable for RF devices, the other important phenomenon that is needed for transistor operation is current saturation.

Current saturation in graphene is almost as much debated topic as the existence of a band gap in single layer graphene. In order for the electron velocity to saturate, all electrons would need to move in the same direction in graphene [14]. This requires a driving voltage, that is greater than the Fermi energy, but electron-electron interactions in graphene may make velocity saturation impossible. Furthermore, hot spots emerge when under high current bias

[45]. These hot spots show that current tansport in an irregular shaped graphene sheet is non-uniform. Chen et al. [21], claim to have observed conductance saturation. Their view is that in low carrier densities (low electric field strength) the long-range Coulomb scattering dominates and gives rise to the linear regime, whereas at high carrier densities the transport is dominated by short-range scattering [21].

Meric et al. [40] demonstrated in 2008 a graphene FET with current saturation. The current saturation demonstrated was incomplete, which raises the question, is it even possible to have complete saturation in graphene. The exact mechanisms of current saturation in graphene are a topic of speculation. Meric et. al suggest that current saturation depends on charge carrier concentration influenced by interfacial phonon scattering in the SiO_2 layer supporting the graphene channels. Current saturation in graphene shown in Figure 2.9, has three regions. In the first region, the charge is carried by holes in the whole channel length. The second region shows a pinch-off region at the drain when the carrier minimal density point is reached. In the third section electrons start to form the channel.

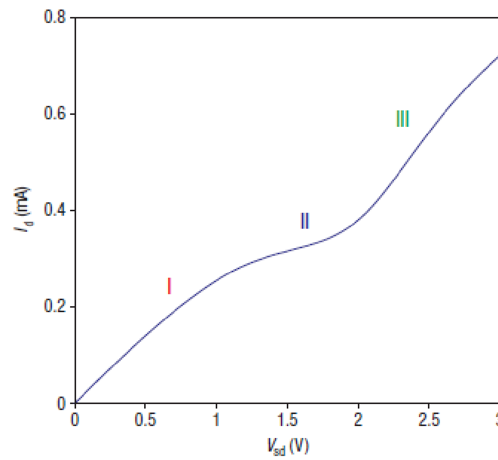


Figure 2.9: Current saturation and 'kink-effect' in a GFET at room temperature. Adapted from reference [40].

Despite the lack of bandgap and low I_{on}/I_{off}, the device shows current saturation and has 150 μSm^{-1} transconductance [40]. The device was studied in 1.7 K temperature to freeze out trapped charges.

For high-field regime unipolar channel, Meric et. al find that the carrier drift velocity saturates due to optical-phonon scattering. The current becomes independent of the drain-source voltage

$$I_d = \frac{W}{L} \int_0^L qn(x) v_{drift}(x) \, \mathrm{d}x \tag{2.10}$$

where W is the channel width and L the channel length. The carrier drift velocity can be

modelled as

$$v_{drift} = \frac{\mu E}{1 + \mu E / v_{sat}} \tag{2.11}$$

where E is the electric field and μ is the carrier mobility. The saturation velocity v_{sat} can be expressed as

$$v_{sat} = \frac{v_F \hbar \Omega}{E_F} \tag{2.12}$$

where $\hbar\Omega$ is the optical phonon energy.

Meric et al. [40] approximated the carrier concentration in the channel with a field effect model

$$n(x) = \sqrt{n_0^2 + [C_{top}(V_{gs-top} - V(x) - V_0)/q]^2} \tag{2.13}$$

where V_0 is the device threshold voltage, $V(x)$ is the potential in the channel, C_{top} is the top gate capacitance consisting of electrostatic capacitance and quantum capacitance in series and V_{gs-top} is the top gate voltage. There are naturally other ways to calculate the carrier concentration, such as using the Fermi-Dirac distribution, as in [36].

Thiele et al. [36] used the same formulae as Meric et al. [40] to qualitatively investigate the operation of GFETs. Thiele et al. improved the formula for saturation velocity from Equation (2.12) to

$$v_{sat} = \frac{\Omega}{(\pi \rho_{sh})^{0.5 + AV^2(x)}} \tag{2.14}$$

where A is a dimensionless empirical factor of the order of 10^{-3}. The previous equation is an empirical equation aimed to correct the overestimation of carrier-phonon interactions [36].

Both Meric et al. and Thiele et al. modelling of GFETs is based on the observation that a FET with large area single layer graphene channel operates much like a metal-oxide-semiconductor transistor. Meric et al. model does not accurately produce the peculiar kink-effect seen in Figure 2.9, but using the Equation (2.14) will predict the aforementioned effect [36].

Barreiro et al. [46] studied a Hall-bar device, with a four-point configuration for measuring. The four-point configuration is employed to minimize the contribution of contact resistance at the graphene-electrode interface. Barreiro et al. report that their device has a tencency to saturate, but that complete saturation was not observed. Barreiro et al. explain that in low-field, elastic scattering is the dominating process, and with higher fields, the optical phonon emission is activated leading to current saturation. Elastic scattering is caused by crystal defects in graphene.

Barreiro et al. claim that in order to have full saturation of current, the phonon emission would have to be instantaneous and elastic scattering processes would have to be negligible, which is impossible. Thus, current saturation is never complete at high fields. The high-field transport is sensitive to elastic scattering. Hot-phonon processes are expected to have a very

small impact on the high-field transport. Barreiro et al. claim that the mobility would need to be increased by at least one order of magnitude to achieve high field current saturation [46].

2.5.4 DC circuit model and MOSFET small-signal model

Small-signal model is a common concept in electronics. It is a linear approximation of a nonlinear device that is accurate when the signal range is small. The device DC operation point is first calculated and then the linearization is formed around that point. Small-signal model assumes that the components, such as capacitances and gain, don't change because the change in signals is so small that the operating point does not change.

Figure 2.10 shows the small-signal equivalent circuit for a two-gate-finger graphene FET. Figure 2.10 is similar to MOSFET small-signal equivalent circuits. The equivalent circuit includes the source and drain series resistances which have to be taken into account when calculating the internal voltages. The small-signal equivalent circuit in Figure 2.10 is expected to work in both electron and hole conduction, but not in hybrid conduction mode. Furthermore, the small signal model is almost exactly the same for a regular silicon MOSFET.

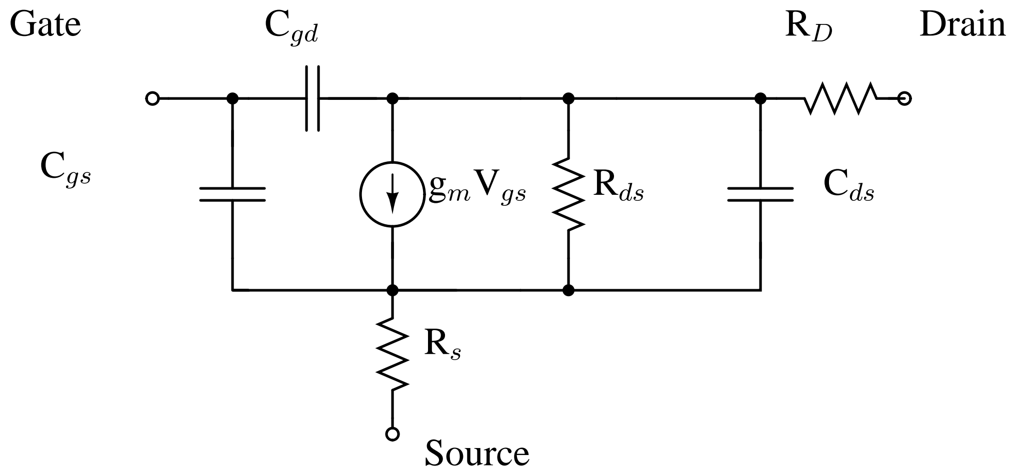


Figure 2.10: Typical small-signal equivalent circuit for a FET.

Figure 2.11 shows the conceptual model of a GFET on the left and the improved version on the rigth. GFET comprises of relatively large contact resistances with the channel resistance in between. The channel resistance can be adjusted with the top gate voltage. In the improved version, on the right in Figure 2.11, the current is a function of V_{ds}, V_g, V_{bg}.

The small-signal definitions are presented in table 2.3. All the voltages in the formulae are internal. The small-signal parameters can be extracted from scattering parameter (S-parameter) measurements assuming the model in 2.10.

The S-parameters can be transformed to other 2-port network parameters by simple calculus.

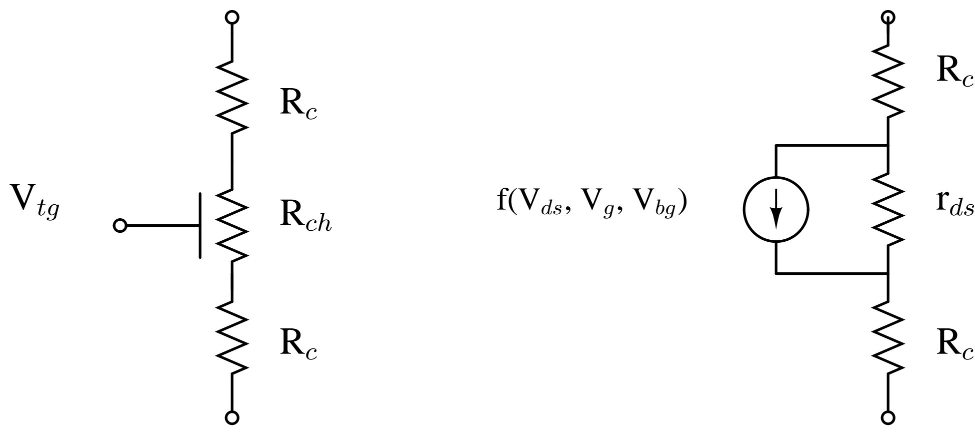


Figure 2.11: Conceptual DC-model of a GFET on the left and an improved circuit model on the right.

Table 2.3: Small-signal model definitions.

Transconductance	$g_m = \frac{dI_D}{dV_{gs}}\vert V_{ds} = const.$
Drain conductance	$g_{ds} = \frac{dI_D}{dV_{ds}}\vert V_{gs} = const.$
Drain capacitance	$C_{gd} = \frac{-dQ_{ch}}{dV_{ds}}\vert V_{gs} = const.$
Gate-source capacitance	$C_{gs} = \frac{-dQ_{ch}}{dV_{gs}}\vert V_{ds} = const.$

The exact equations are omitted here. Usually S-parameters are converted to admittance parameters (Y-parameters) to extract the small-signal parameters.

The small-signal model parameters were calculated using the following formulae assuming that R_S and R_D are both zero,

$$g_m = \Re(y(2{,}1)) \tag{2.15}$$

$$g_{ds} = \Re(y(2{,}2)) \tag{2.16}$$

$$C_{gd} = -\Im\frac{y(1{,}2)}{\omega} \tag{2.17}$$

$$C_{gs} = \Im\frac{y(1{,}1)}{\omega} - C_{gd} \tag{2.18}$$

$$C_{ds} = \Im\frac{y(2{,}2)}{\omega} - C_{gd} \tag{2.19}$$

Chapter 3

Experimental Methods

The measurements were performed with a measurement setup shown in Figure 3.1. The measurement procedure is shown in Figure 3.5. Two types of measurements can be performed with the setup in Figure 3.1: DC (direct current) sweeps and S-parameter measurements. The measurement setup consists of a Advantest R6243 combined DC source and ammeter, RC-filter with time constant of 300 ms, an Agilent 8722ES vector network analyzer (VNA), a HP 34401A voltmeter, LC-filter with time constant of 0.1 ms, an Agilent 3458A ammeter and a HP 3245A dc source. The sample was probed with Cascade Microtech RF ACP40-GSG probes with 100 μm pitch. Labview was used to control the measurement equipment and collect data.

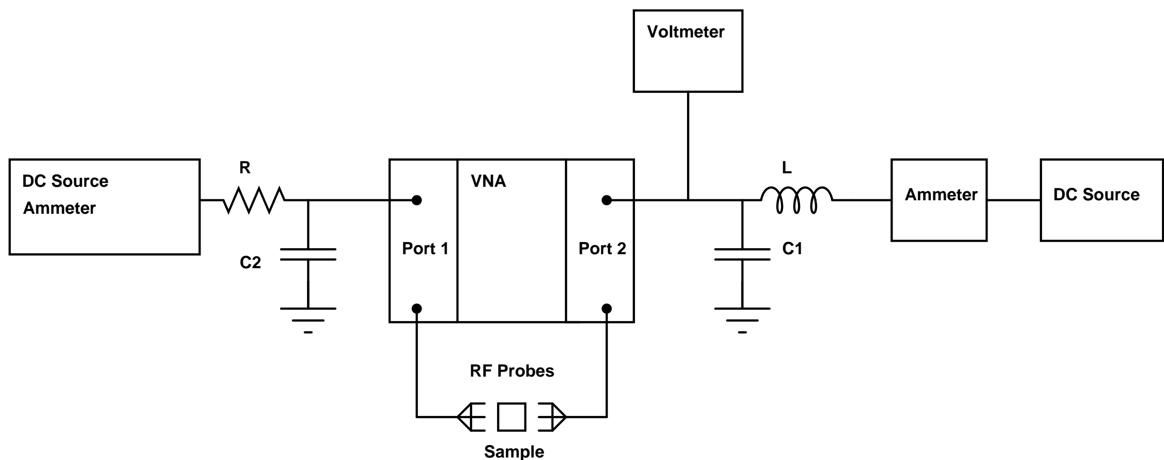


Figure 3.1: Measurement setup.

The measurements were performed in a ESD-shielded laboratory. The samples were placed in a vibration damped Cascade Microtech probestation. The RC- and LC-filters were used to prevent the sample from being destroyed by switching transients from the measurement equipment. Port 1 in Figure 3.1 is connected to the GFET gate pad and port 2 is connected to drain and source pads. The GFETs have two gate-fingers, which means that the GFETs

actually consist of two transistors with the same drain and the top-gate fingers are controlled simultaneously.

DC-sweeps were carried out for both SiC and CVD GFETs. First, the Dirac point was located by sweeping the gate voltage with constant drain-source voltage. Next, the drain-source voltage and current were measured at several constant gate voltages.

The RF probes were difficult to place on the golden contact pads of the GFETs, because the gold would easily wrinkle when the probe tips would slide on the pad surface. Often, it would not be possible to contact the pads more than twice. This restraint made it hard to evaluate if the contact to the gate was sufficient. In many cases the drain-source pads would be connected, which can be verified by applying a drain-source voltage, but the gate side pads would be poorly connected which can only be verified by either lifting the pads or by looking at the drain source voltage as a function of gate voltage. Due to the low field-effect, especially in SiC GFETs, it was not always clear if the gate was contacted or not. Another issue with the pads was that the gold would stick to one of the probe tips and make the tips different height. A SiC GFET with very damaged contact pads on the right side is shown in Figure 3.3.

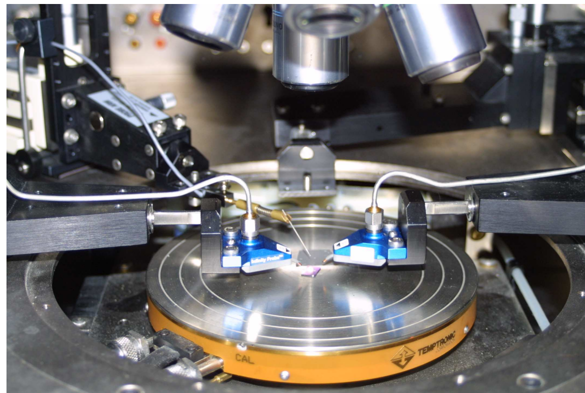


Figure 3.2: Photograph of the probes.

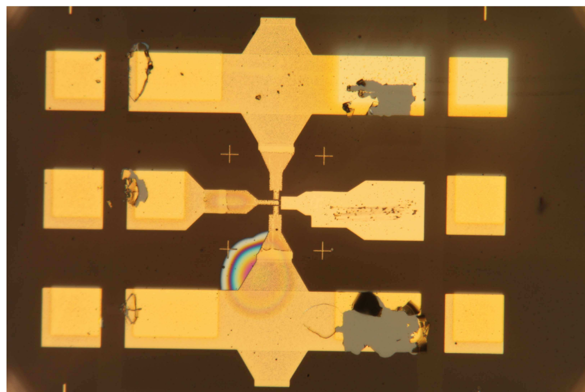


Figure 3.3: SiC GFET with damaged contact pads. The gate is on the right.

A 1/50 micron GFET was measured with HP 85047A 300kHz-6GHz S-parameter test set. Device calibration is an important step in the measurement process, and is done to remove

the influence of the cables and connectors. Calibration performed in the beginning of measurements is assumed to be valid for one day. The VNA was calibrated using Short-Open-Load-Thru (SOLT) method. An impedance standard substrate provided by the manufacturer was used as calibration reference. The measurement range was from a few MHz to 1 GHz. A broad frequency range was chosen because the cut-off frequency of the GFETs was unknown. Three operation points were chosen for S-parameter measurements, so that one point is from hole conduction, one at Dirac point and one in the electron conduction side. The point in the electron (hole) conduction regime was chosen in the maximum transconductance area, i.e. steepest slope in drain current vs. top gate voltage curve. A top gate-drain current sweep was always performed before the S-parameter measurement to ensure that the GFET properties have not changed during storage. The Dirac point of the four GFET samples was in the vicinity of -10 V (top gate) with around 0.7-1 mA drain current at 0.1 V drain source voltage. The drain current was found to drop slowly (in seconds) when a high negative top gate voltage was applied. This phenomenon is suspected to be caused by degrading contacts or dielectric layer, because the drain current was stable at lower top gate voltages. The dropping drain current may have effected also the S-parameter measurements.

A well-known de-embedding procedure using a open structure was used to substract the influence of the pads. The admittance equation for de-embedding is $\mathbf{Y}_{FET} = \mathbf{Y}_{DUT} - \mathbf{Y}_{Pad}$ The de-embedding is shown in Figure 3.4. DUT stands for Device Under Test. The crosstalk capacitance represents the influence of crosstalk through the substrate and crosstalk between the probes that are close to each other.

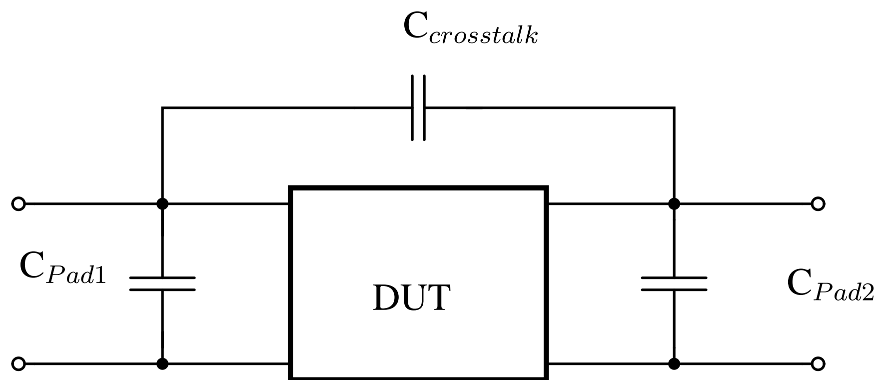


Figure 3.4: De-embedding of the device.

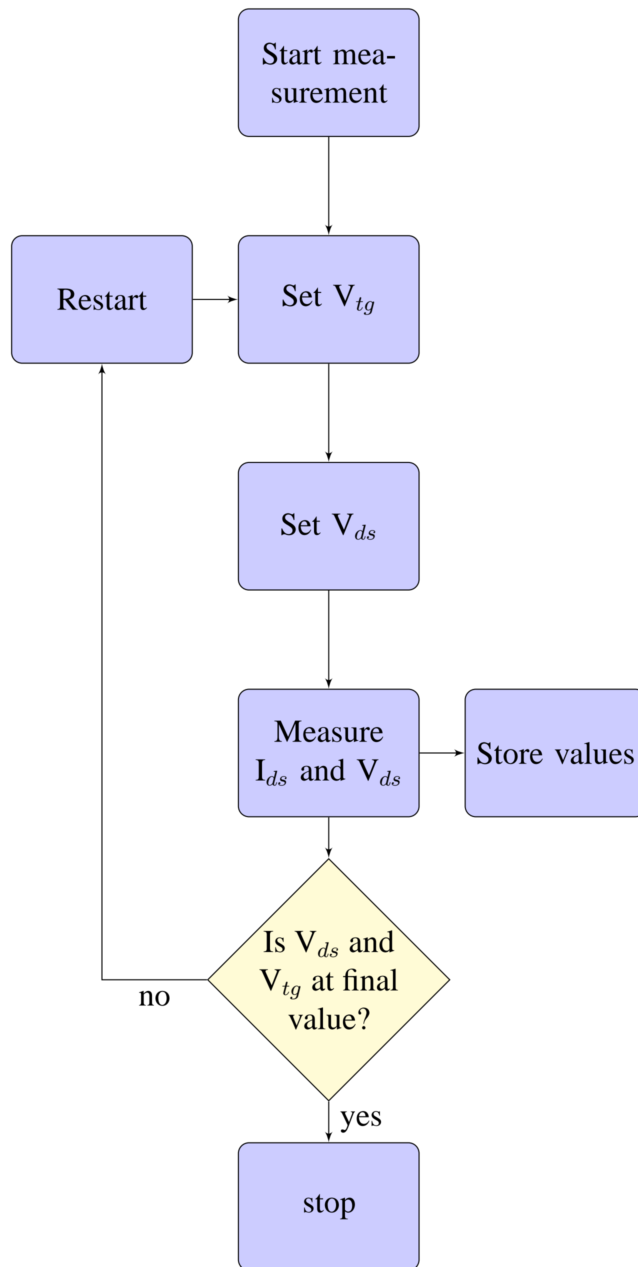


Figure 3.5: Measurement procedure.

Chapter 4

Results

In the first section, the experimental results of the SiC graphene field effect transistors are discussed. In the second section, the results of the CVD fabricated GFETs are presented and discussed. Last, the curve-fitting and validation method is presented and the results are analyzed.

To summarize, in the UI-measurements the SiC GFETs were found to be of very non-uniform quality with very low terminal transconductance. Due to the low transconductance of the GFETs, it was not possible to measure radio frequency characteristics with S-parameter measurement of the SiC GFETS. The CVD GFETs were found to give much higher currents with lower drain-source voltage than the SiC GFETs. Also, the CVD GFETs had much less unintentional doping than the SiC GFETs, meaning that the Dirac points were usually found in the region of 0 to -10 V. S-parameters measurements were performed on the CVD GFETs.

4.1 SiC GFETs

The SiC GFET structure is as follows from bottom of the device: 500 nm of SiC, FLG graphene and 40 nm Al_2O_3 as top gate dielectric. The electrodes are 5nm of titanium with 40 nm of gold on top. The GFETs were prepared by SiC evaporation process by Nanotechnology group at Micronova facilities by Wonjae Kim. The transistors were found to have 2-5 layer graphene in Raman spectroscopy performed by W. Kim. Figure 4.1 shows a photograph taken of the chip. The top-gate in Figure 4.1 is on the right of each transistor and the source-drain electrodes are on the left with drain as the middle electrode. The SiC GFETs don't have a back gate due to the thick insulating substrate. The GFETs are in two gate-configuration, so that RF-measurements could be performed if the components would exhibit high enough transconductance values.

There were 80 structures altogether on the chip, of which 52 were working and measured.

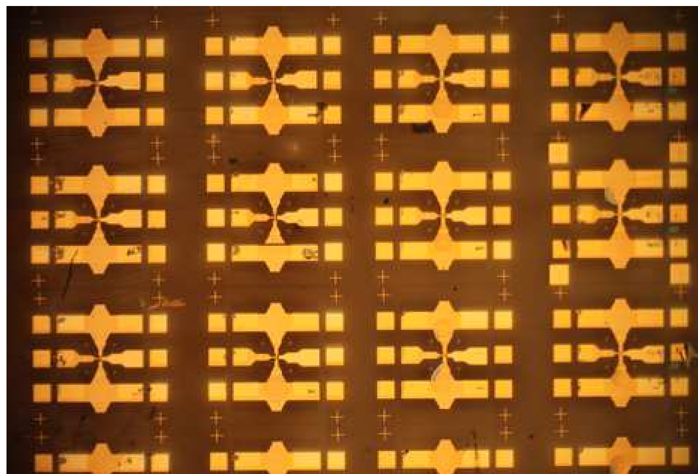


Figure 4.1: SiC GFET

There were four different size transistors (in microns, L/W): 4/10, 2/5, 1/1 and 0.5/1. The GFET substrate is 500 nm of SiC with 2-5 layers of graphene on top. The top-gate dielectric is 40 nm thick Al_2O_3. The electrodes are formed with 5 nm of Ti with 40 nm of gold (Au) on top of the titanium.

In Figure 4.3, the measured Dirac points are plotted against their original coordinates in the chip. See Figure 4.2 for the chip layout. The source to drain voltage in these measurements was 0.5 V. Some of the components were left out of the Figure, either because the components were defective or could not withstand the 0.5 V. The same data as in Figure 4.3 is shown as a scatterplot in Figure 4.5. Two different colours in each scatterplot are used to differentiate between transistor rows of the same L/W (left and right). It is evident from these two figures that the uniformity of the transistors is very poor. Figures 4.3 and 4.5 show that the SiC GFET process variation is high. The random locations of Dirac points may be due to unintentional doping, poor gate dielectric or defects in the graphene layer.

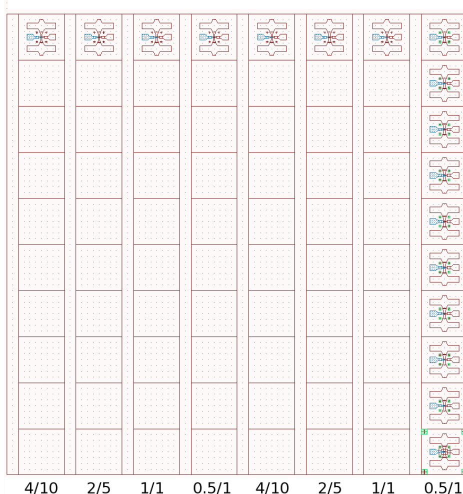


Figure 4.2: Each column has transistors of the same size, for example the first column contains transistors with L/W = 4/10. The original figure is loaned from W. Kim.

Figure 4.4 shows the SiC GFET current densities at Dirac point. Each coloured square represents the location of the transistor on the chip. Interestingly, the dirac point of these transistors vary greatly as can be seen from Figure 4.3, but the current densities at the Dirac point is quite similar with GFETs of the same size. The only exception in Figure 4.4 is the fourth and the last row from the left, these two rows are transistors with the same L/W. It is likely, that the processing of these transistors had difficulties resulting in very dissimilar devices.

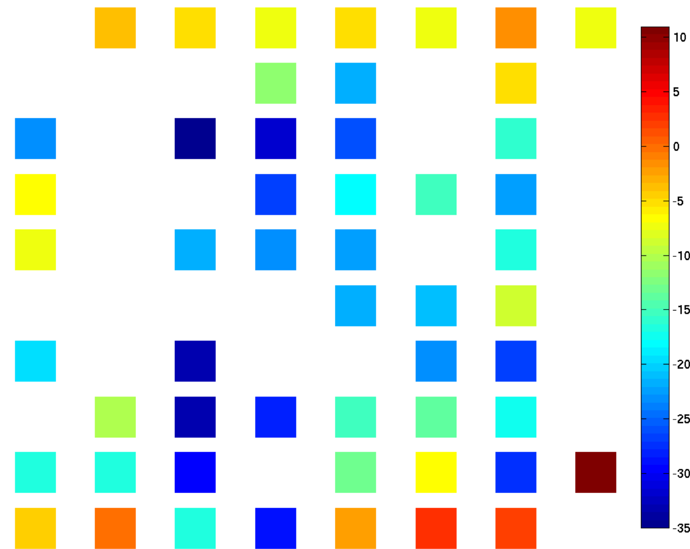


Figure 4.3: The SiC GFET Dirac points represented with colours in the same layout as the chip.

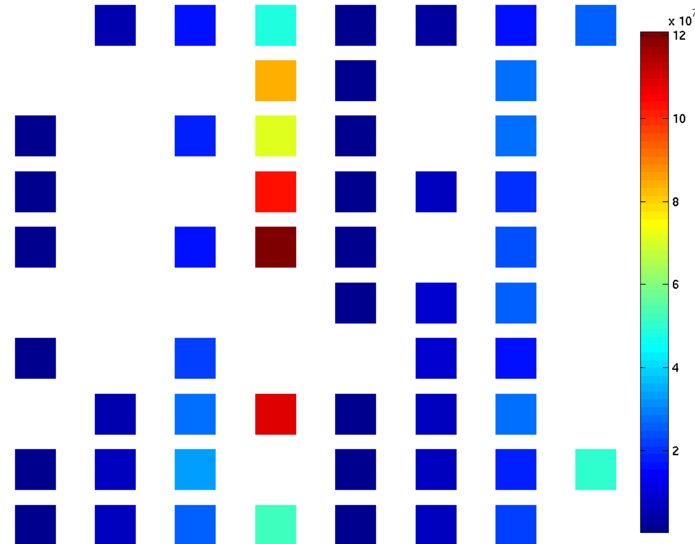


Figure 4.4: The SiC GFET current densities at Dirac points represented with colours in the same layout as the chip.

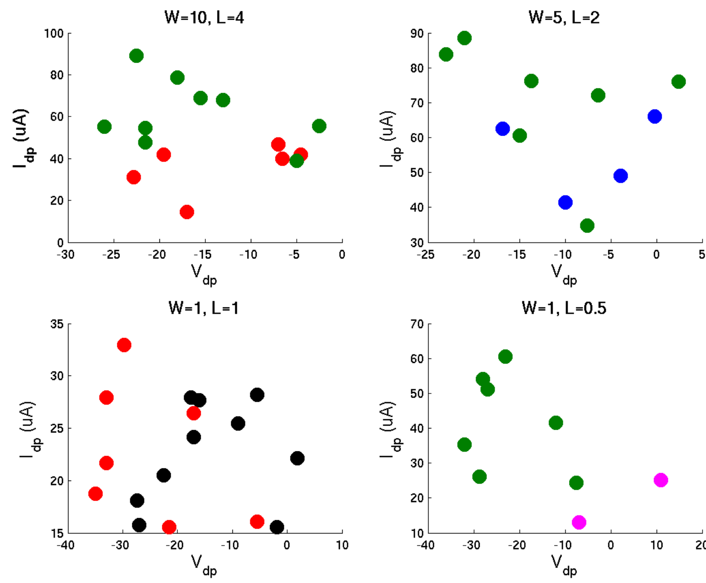


Figure 4.5: The SiC GFET Dirac points presented as scatter plot. The colours represent the location of the components, either left or right.

As mentioned, RF-measurements couldn't be performed for SiC GFETs due to too high impedance level. However, it is possible to estimate the cut-off frequency of the transistors using Equation (2.4) and calculating the top-gate oxide capacitance as parallel plate capacitor. For example, let us consider a transistor with W=5 μm and L=2 μm. The transconductance maximum value for this particular transistor can be approximated to be 2×10^{-7} S. Assuming the gate area as W*L, dielectric Al_2O_3 to have $\kappa = 9$ and thickness 40 nm, and quantum capacitance C_q of graphene as 2 μF/cm^2 [40]. The total top gate capacitance is the gate capacitance C_e and quantum capacitance C_q in series. The total top-gate capacitance C_{top} is then $1.81{\cdot}10^{-14}$. The cut-off frequency is

$$f_t = \frac{g_m}{2\pi C_g} = \frac{2 \cdot 10^{-7}}{2 \cdot \pi \cdot 1.81 \cdot 10^{-14}} = 1.76 \cdot 10^6 \text{Hz} \approx 2\text{MHz} \tag{4.1}$$

The relatively low cut-off frequency can be attributed to the poor transconductance value and possibly high contact resistance. Also, the graphene quantum capacitance becomes quite significant when the top-gate dielectric thickness is reduced [24]. The calculated cut-off frequency of the SiC GFETs is so low that the VNA would not have been able to measure it.

Figure 4.6a shows the Dirac point of the SiC GFET. The transistor is heavily doped as the Dirac point is approximately in -37 V. The graph ends before -40 V, because of limitations of the measurement equipment. Surprisingly, the device top-gates could often withstand very high voltages without breaking. Figure 4.6b shows the drain current as a function of drain-source voltage. The device shows no sign of current saturation, though with GFETs the reported current saturation is found at higher drain-source voltages (>1 V).

Figure 4.7a shows the calculated terminal transconductance of a 2/5 SiC GFET and 4.7b shows the terminal conductance calculated from a polynomial fit to the data. The transconductances are calculated from Figure 4.8. Figure 4.7 may give the impression that the transconductance would rise, but that is not the case as the growth in current would reach a deflection point.

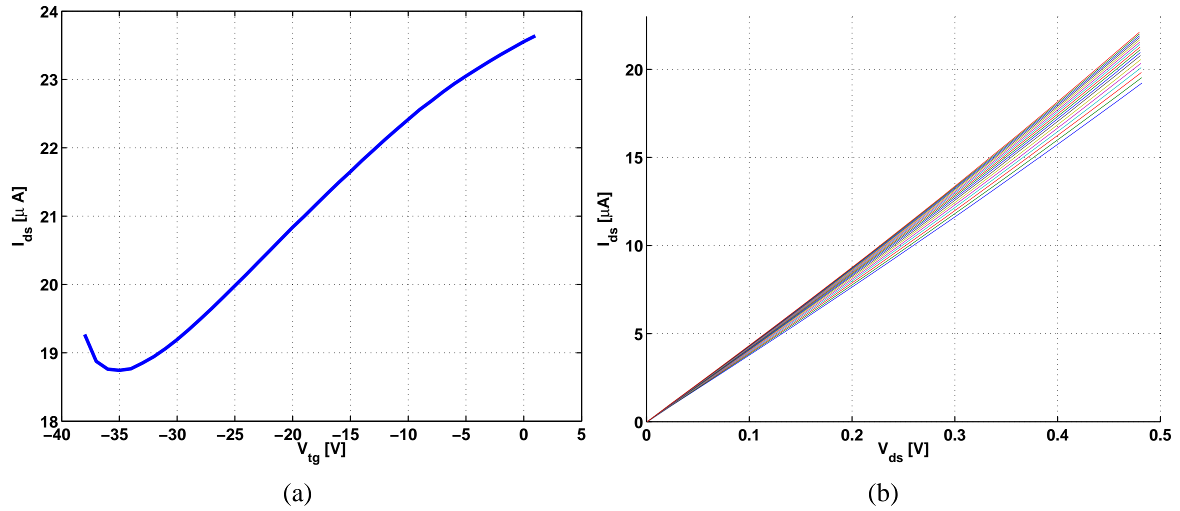


Figure 4.6: Figure a) shows the drain current as a function of top gate voltage with 0.5 V_{ds} and b) shows the IV-graph. The GFET L/W ratio is 1/1.

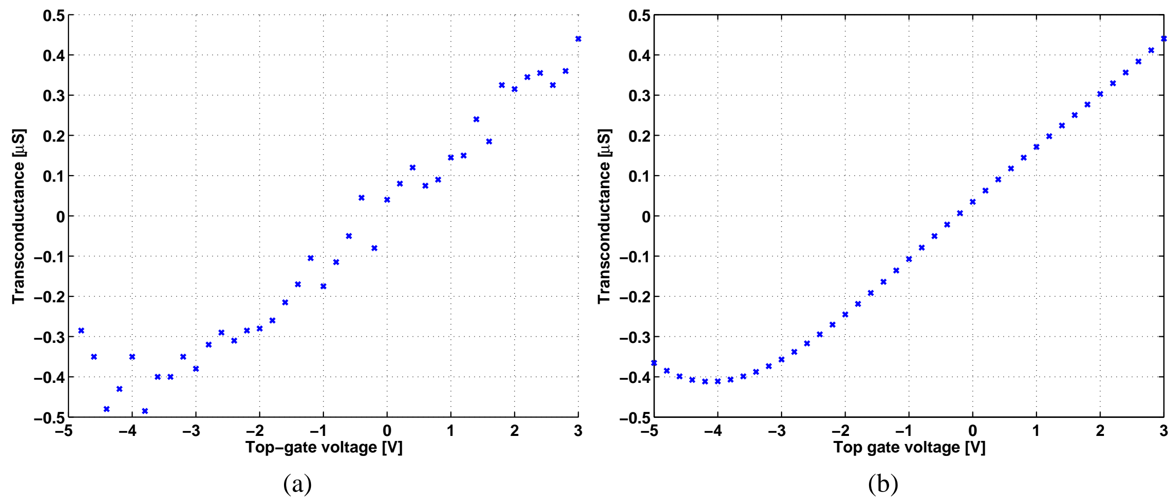


Figure 4.7: Figure a) shows the calculated transconductance and b) the transconductance values calculated from a polynomial fit to the data. The GFET L/W ratio is 2/5. The V_{ds} is 0.5 V in both figures.

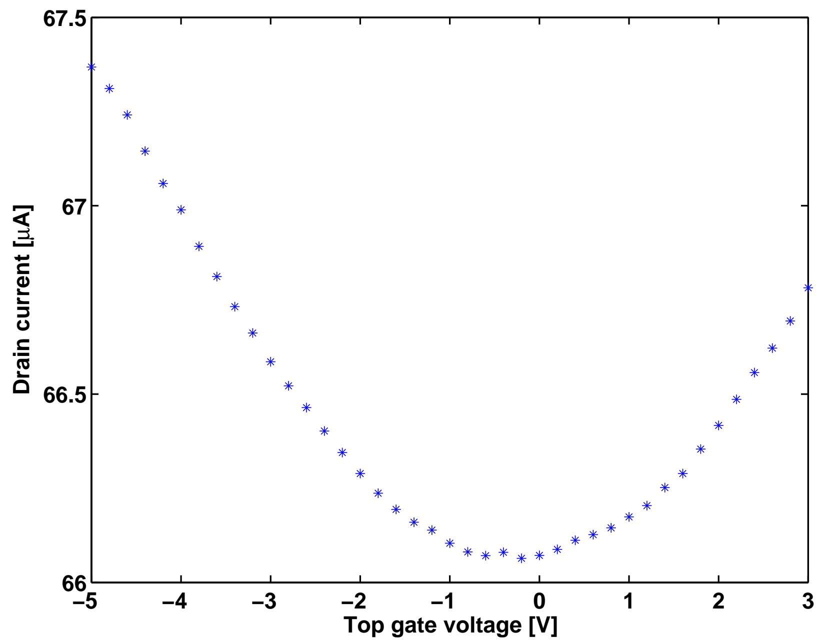


Figure 4.8: The minimum conductance point of a GFET with 2/5 L/W ratio. The V_{ds} is 0.5 V.

4.2 CVD GFETs

The second measured batch consisted of GFETs with CVD fabricated FLG graphene. The GFET structure is as follows from bottom of the device: back gate, 300 nm layer of SiO_2, FLG graphene and 25 nm Al_2O_3 as top gate dielectric. The electrodes are similar to the ones in SiC GFETs, but the thickness of the gold layer on top of titanium layer was increased, because the probe tips damage the gold layer.

There were 8 working CVD GFET transistors on the chip that was measured. There were three different sizes (in micron, L/W): 1/50, 2/50 and 4/50. The shortest gate length transistors were found to operate similarly to the longer gate length transistors, which is a good sign for further dimension downscaling. However, the gate effect is much weaker in the short gate length devices. It is possible that short-channel effects are the cause for diminished gate effect.

Figure 4.9 shows a photograph of the transistors on the chip. Figure 4.10 shows a close-up of one of the transistors. The top-gate is on the rigth and source and drain electrodes are on the left side. The brown smudges on the electrodes is gold that has scratched of when placing the probe tips.

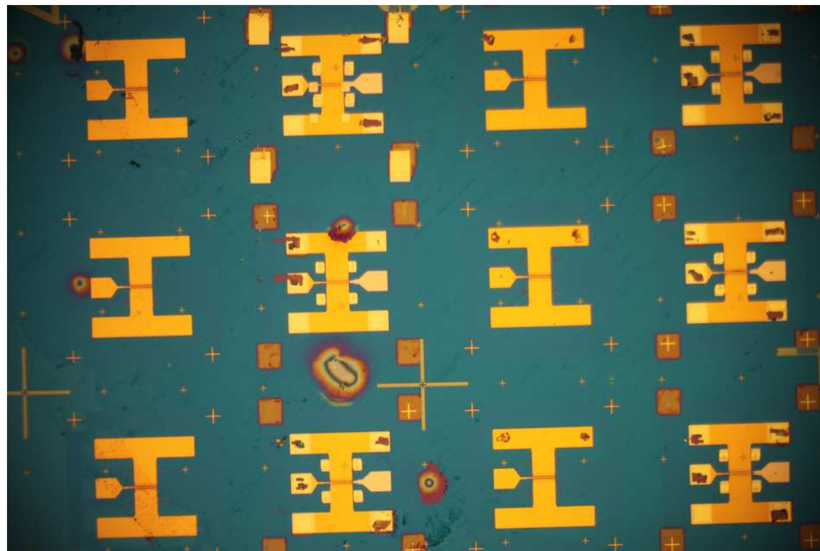


Figure 4.9: A photograph showing some of the two gate-finger CVD GFETs.

Figure 4.11 shows the current and the current density at top-gate Dirac point with back-gate voltage as zero. Naturally, the short gate length GFETs have the highest current and current density. The components have quite dissimilar Dirac point locations, especially the 2/50 and 1/50 GFETs.

Figures 4.12 and 4.13 show the results of the DC-measurements of a CVD GFET with L/W = 2/50. Figure 4.12 shows the drain current as a function of top-gate voltage with different back gate voltages. In hindsight, the back gate voltages should have been much higher for

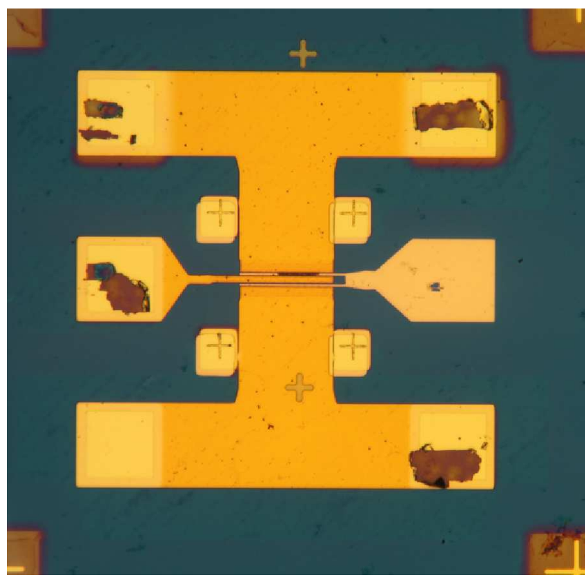


Figure 4.10: A photograph showing a single two gate-finger CVD GFET.

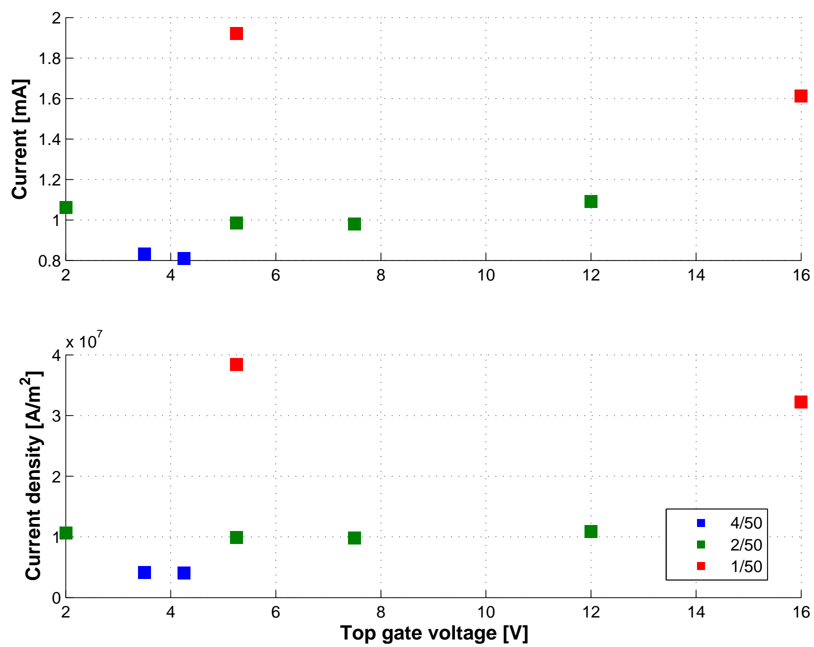


Figure 4.11: The current and current density at Dirac point.

the back gate to have effect on the drain current. The location of the Dirac point was found to change with the first few DC-sweeps after which it would stay roughly at the same location. Figure 4.13 shows the IV-characteristics of the GFET with the top gate ranging from 8-14 volts. It is clear that the drain voltage is not high enough for current saturation to show, but because of the small amount of samples the drain voltage was not raised above 0.2 so that the GFETs would not break.

Figure 4.14 shows the terminal transconductance calculated from the top-gate voltage vs. drain current graph. Terminal transconductance is defined as $g_{mt} = \frac{dI_d}{dV_g}$ at a constant drain source voltage.

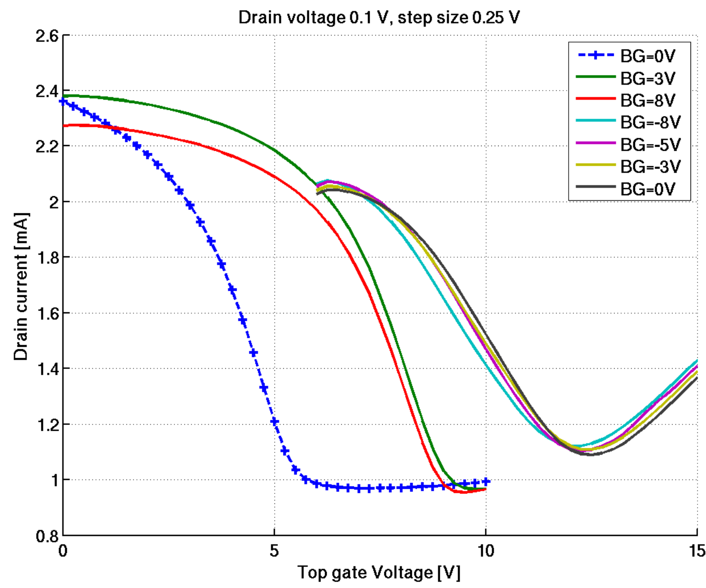


Figure 4.12: Drain-source current as a function of top gate voltage. GFET size is L/W=2/50.

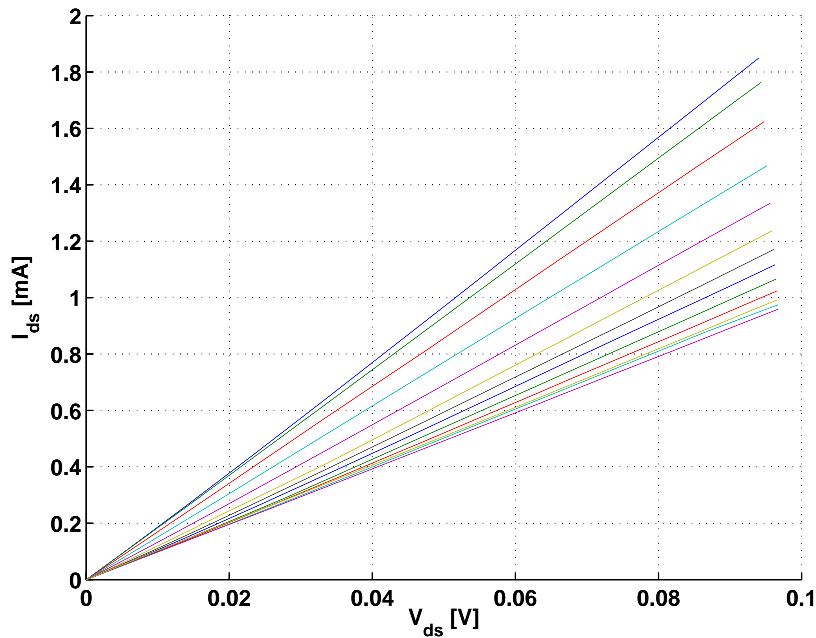


Figure 4.13: The drain-source current as a function of drain voltage. The top-gate is varied from 8 to 14 V with 0.5 V step size. The back gate voltage is zero. The transistor size is L/W=2/50.

Let us estimate the cut-off frequency of the CVD GFETs using the Equation (2.4). Assuming that the highest frequency is achieved with the CVD GFET that has the shortest gate, then L=1 μm and W=50 μm. Let us further assume that the quantum capacitance has the same value as in previous SiC GFET calculations, i.e. 2 μF/cm^2. The CVD GFET gate dielectric is Al_2O_3 with dielectric constant 9 and thickness 25 nm. The total gate capacitance is again the quantum capacitance and gate oxide capacitance in series, giving total gate capacitance of $1.37 \cdot 10^{-13}$ F. Estimating the maximum terminal transconductance from I_{ds}-V_g graphs as

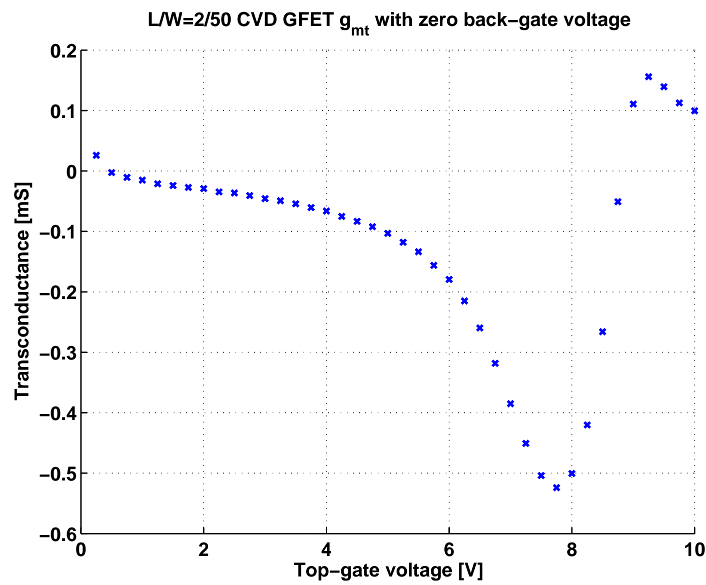


Figure 4.14: Top-gate voltage vs. terminal transconductance. V_{ds} = 0.1 V. L/W=2/50.

$1.2{\cdot}10^{-4}$ we can calculate an approximation for the cut-off frequency as

$$f_t = \frac{g_m}{2\pi C_g} = \frac{1.2 \cdot 10^{-4}}{2 \cdot \pi \cdot 1.37 \cdot 10^{-13}} = 1.389 \cdot 10^8 \text{Hz} \approx 140 \text{MHz} \tag{4.2}$$

The cut-off frequency is much improved when compared to the SiC GFET cut-off frequency estimates. The back-gate gives more freedom in adjusting the terminal transconductance [24].

The amplification of the CVD GFETs was tested by seeding a sine signal from a signal generator together with a DC top gate voltage. A back-gate voltage was also applied. The input and output signals were analyzed with an oscilloscope. The input and output waveforms are plotted in Figure 4.15. The output signal is in the range of millivolts when the input signal is several volts, which means that the GFET is unable to provide amplification.

Figure 4.16 shows the cut-off frequency of a GFET with 1/50 W/L ratio in three different operating points. The top gate values in Figure 4.16 are 0, -5 and -10 V with zero back gate voltage and 0.1 V drain-source voltage.

The GFETs studied showed cut-off frequencies between 30-80 MHz. Figure 4.16 shows that the highest cut-off frequency is achieved with -10 V at top gate. The relatively low field-effect and quite high contact resistance limit the operation. Figure 4.17 shows the result of a drain current measurement as a function of time with constant top gate and drain-source voltage. Top gate voltage was chosen as -18 V and drain-source as 0.1 V to investigate device drain current under high electric field. It is possible that the continuously dropping current, as seen in Figure 4.17, may hinder the operation.

Small-signal model parameters are calculated based on the S-parameters. Currently, the

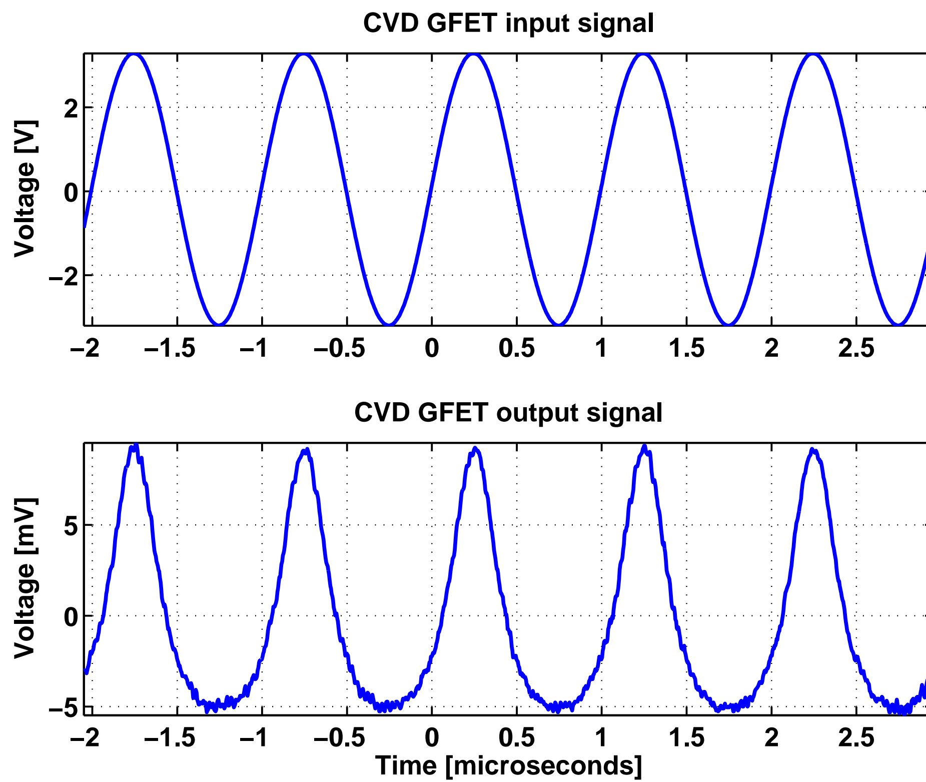


Figure 4.15: The upper plot shows the input signal to the GFET and the plot below shows the output signal.

small-signal parameters are calculated with extrinsic values and the effects of R_s and R_d are neglected. Figures 4.18a and 4.18b show the calculated small-signal capacitances as a function of frequency. The capacitances fluctuate in the beginning of the frequency range, but fall into line. The C_{ds} is negative, which may be due to measurement error or a discrepancy in the model. Figures 4.19a and 4.19b show the calculated drain conductance and transconductance at zero top gate voltage with 0.1 drain source voltage.

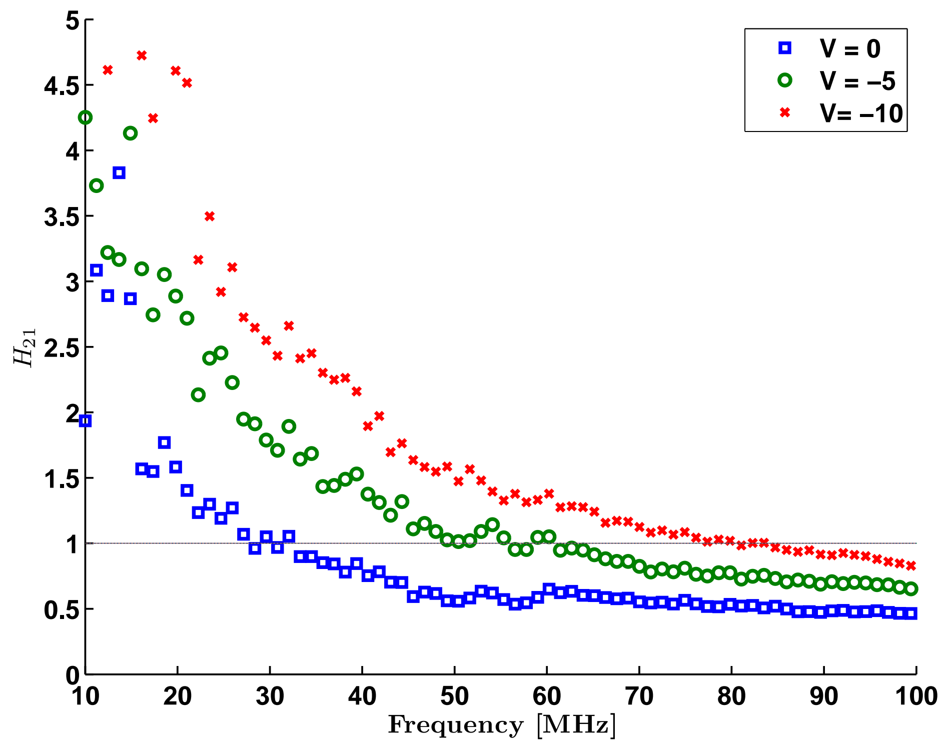


Figure 4.16: The cut-off frequency of a 1/50 micron CVD GFET at three top gate voltages 0, -5 and -10 V. The drain-source voltage is 0.1 V and back gate voltage is zero in all three cases.

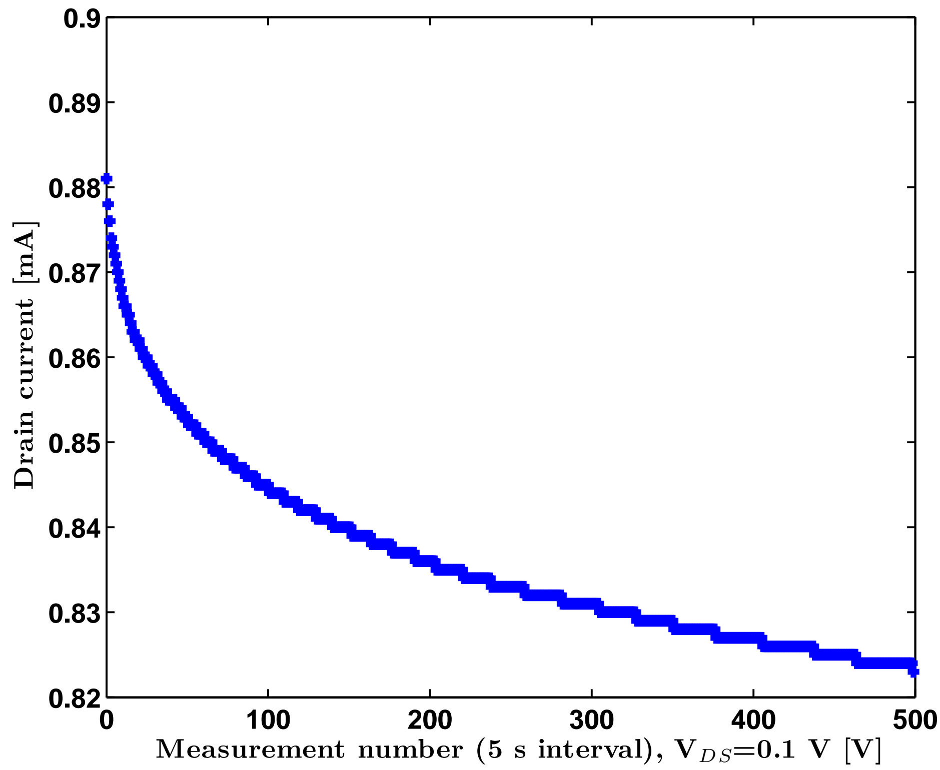


Figure 4.17: The measured drain-source current with -18 V top gate with 5 second waiting time between measurement points.

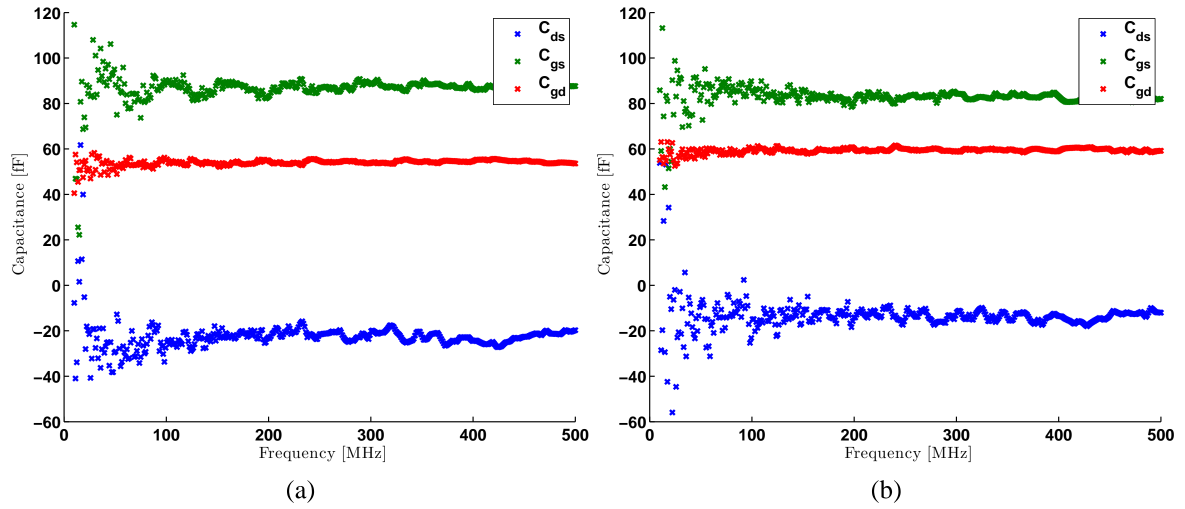


Figure 4.18: The small-signal model calculated capacitances at a) zero top gate and b) -10 V top gate.

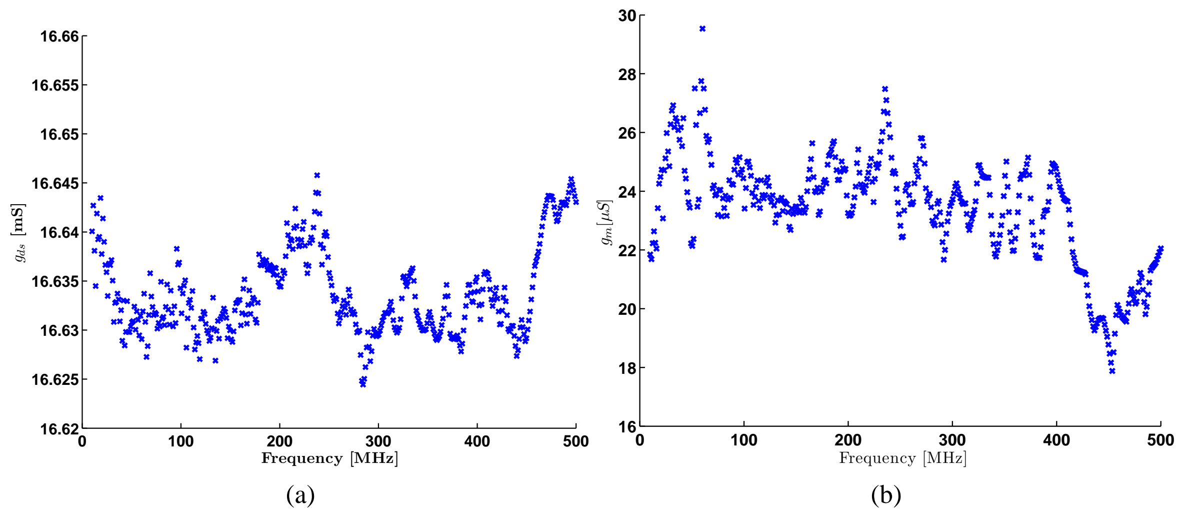


Figure 4.19: The small-signal model calculated a) drain conductance and b) transconductance at zero top gate voltage.

4.3 Curve-fitting

Curve-fitting is needed to gain more insight to the GFET electrical characteristics and to approximate the contact resistance. Contact resistance is needed to calculate the small-signal model. An effort was made to fit the measurements to the model described by Kim et al. [27]. The model consists of three equations describing how the total device resistance changes with applied top-gate voltage:

$$\begin{aligned} n_{tot} &= \sqrt{n_0^2 + n[(V_{TG} - V_{DRC})]^2} \\ V_{TG} - V_{DRC} &= \frac{qn}{C_{ox}} + \frac{\hbar v_F \sqrt{\pi n}}{q} \\ \hat{R} &= R_{contact} + R_{channel} = R_{contact} + \frac{N_{sq}}{n_{tot} q \mu} \end{aligned} \tag{4.3}$$

where $\hat{R}$ is the predicted total device resistance and N_{sq} is the number of squares.

The model was fit to the VI-measurement data with nonlinear least squares curve fitting algorithm in Matlab Optimization Toolbox (lsqcurvefit). Optimization algorithm tries to find parameters that minimize the following cost function

$$J(x) = \sum_i (\hat{R}(x, V_{TG,i}) - R(V_{TG,i}))^2 \tag{4.4}$$

where x is a vector containing the three unknown parameters: contact resistance $R_{contact}$, residual carrier density n_0 and mobility μ. $\hat{R}(x, V_{TG,i})$ is the total device resistance predicted by the model with parameters x and applied top-gate voltage $V_{TG,i}$). The actual measured resistances are denoted with $R(V_{TG,i})$.

The model described by equations (4.3) agrees well with the data if the total device resistance is symmetric with respect to V_{DRC}, implying that the electron and hole mobilities are equal. The top-gate capacitance was calculated from the geometry of the device, i.e. parallel plate capacitor, but it would have been more accurate to measure it directly or determine from the top-gate voltage vs. back-gate voltage slope. This top-gate capacitance measurement would not have been possible for SiC GFETs, because there is no back-gate. However, the measurements with the CVD GFETs were done with relatively small back-gate voltages and thus it was impossible to calculate the slope with any accuracy.

The model for total device resistance assumes that Drude model for electrical conduction applies. The Drude model is a classical model, and can be extended to semi-classical systems. The model assumes a free-electron gas and long-range interactions are taken into account. Also, electron-electron collisions are not taken into account.

K-fold cross validation was used to get a better idea of the validity of the model parameters than just by looking at residuals. Additionally, k-fold cross validation reveals the possible case of overfitting. The downside of k-fold cross validation is that it takes a lot of time even

with Matlab's parallel computing. In k-fold cross validation, the data set is divided randomly into k equal-sized parts [47]. Then $(k-1)$ parts are picked to form the training set, and the remaining part is the test set. Then the model is fitted using only the training data. The performance of the fitted model is evaluated using the test data. Since there are k different ways to pick the test set, the model is fitted k times. Additionally, the split into k subsets is repeated thrice to compensate the relatively small size of the data sets.

For each repetition of the k-fold cross validation there are k sets of different parameters. Using appropriate statistics an estimate of the sensitivity of each of the parameters can be acquired. Here, the interquartile range is used to measure sensitivity. If the interquartile range is 'large', the model is not able to predict the physical phenomenon well. Mean of squared errors (MSE) over the test set is used to measure how well the model performs against new data. If the MSE in test set is very different from the MSE from the training set MSE, it indicates a possible case of overfitting. The interquartile ranges and mean parameters are presented in Appendix B.

In this work, the number of folds k is ten with three repetitions. Matlab crossval-function in Statistics-toolbox was used. The matlab-code used for the optimization can be found in Appendix A.

A practical approach to get better fit between data and model is to determine the total device resistance function piecewise [48]. The method in all simplicity is to fit the electron and hole conduction branches separately. This will naturally result in different electron and hole mobilities and different contact resistances depending on carrier type. The cause for transport asymmetry is considered to be PN-junctions resulting from electrode doping. Both contact resistance and carrier mobility is claimed to contribute to transport asymmetry [48]. However, the grounds for mobility contributing to transport asymmetry are wanting and would require further investigation. Another improvement to the model would be to integrate an impurity doping profile to the calculation of carrier concentration.

An example of one of the curve-fits for CVD GFET is shown in Figure 4.20. Figure 4.20 shows that in this particular case the fit looks good; there is only a bit of undershooting in the 'tail' and some overshooting in the top of the curve.

The curve-fitting results for the SiC GFETs are shown in tables 4.1-4.4. Each table shows the model parameters for devices with certain L/W ratio. Mean of squared errors of the model using the whole data set as the training set, is denoted with 'MSE'. Mean of MSEs over all the test sets (30) of the repeated k-fold cross validation is denoted with 'MSE (k-fold)' in tables. Additionally, the parameters shown in tables have been acquired using the whole data.

The model predicted values for contact resistance, residual charge carrier concentration and mobility vary significantly within each transistor size. This is probably due to the observed

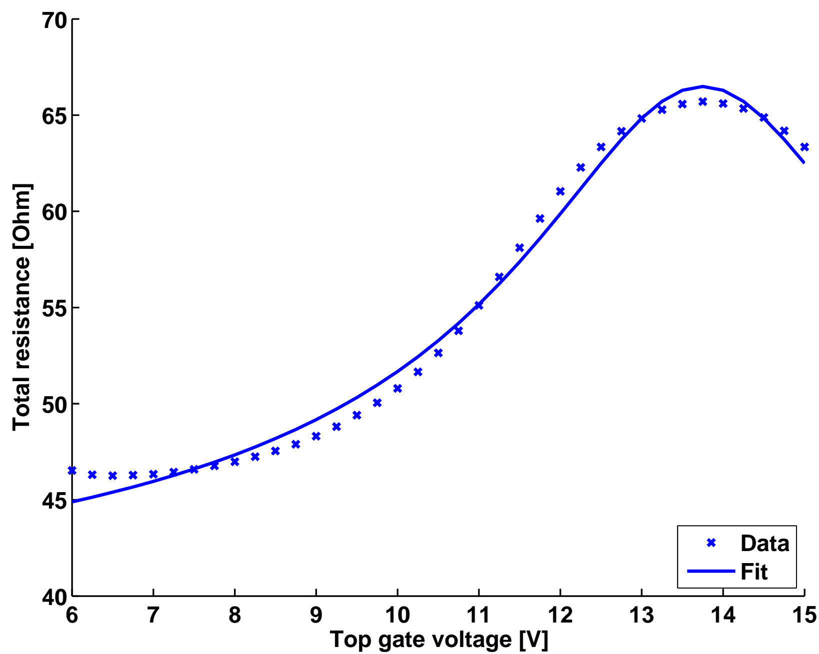


Figure 4.20: Curve-fit for a L/W = 2/50 transistor with zero back gate voltage. SSE=20.0571.

variation between transistors of the same size, and the fact that the SiC GFETs showed electron hole asymmetry. The MSE values for both full optimization and k-fold validation are in the same range for each type of GFET in all tables, excepting Table 4.2 in which the MSE values for k-fold validation are much greater than for optimization with all data. The transistors in question were not originally expected to function at all because of an error in fabrication process, and it is possible that this shows in the transistor behaviour and thus in the curve fit. The MSE values in Table 4.1 are the smallest and the parameter values are quite reasonable, though the contact resistance is quite high and the mobility values somewhat low, e.g. less than 100 cm^2/Vs. The optimization results in tables 4.2-4.4 are likely inaccurate because of the high MSE values when compared to Table 4.1 and should be regarded with reservations.

The curve-fitting results for the CVD GFETs are shown in Table 4.5. Of the eight working transistors, six could be fit with parameters that are reasonable. Large (small) MSE-values mean large (small) error in the fit. The MSE-values in Table 4.5 vary between samples indicating that the model could not predict the data well in all cases. The k-fold validation MSE values are presented in Table 4.5. The MSE values for both the curve-fit with all data points and with k-fold cross validation are similar. This would indicate that the model is not sensitive to number of data points. Also, a large difference between the MSE values and parameter values would indicate that the model is trying to overfit the data, i.e. too many parameters.

Most of the measured CVD GFETs had varying degrees of electron-hole asymmetry. Furthermore, the GFETs Dirac points were found to change with each measurement until after

several measurements it would stay put. This behaviour was found halfway through the measurements. Then the measurements were repeated until the $V_{tg} - I_{ds}$-graphs stabilized. The repeated measurements would also remove some of the asymmetry between electron and hole conduction with several GFETs.

Table 4.1: Curve-fitting results for SiC GFET with 2/5 L/W ratio.

$R_{contact}$ [Ω]	n_0 [cm^{-2}]	μ [cm^2/ Vs]	MSE	mean MSE (k-fold)
5852	$0.8347{\cdot}10^{13}$	375.7171	2.2747	2.9000
12316	$0.8100{\cdot}10^{13}$	263.4235	45.5417	50.5000
4590	$1.0179{\cdot}10^{13}$	230.9923	40.8060	42.900
760	$3.1100{\cdot}10^{13}$	12.2328	628.9936	$14688{\cdot}10^3$
4128	$1.6935{\cdot}10^{13}$	241.8939	3.8118	5.2000
4247	$1.7100{\cdot}10^{13}$	182.4155	12.7785	13.5000
2515	$3.4100{\cdot}10^{13}$	23.4033	3.3298	3.5000
4247	$1.5751{\cdot}10^{13}$	89.5042	25.2531	25.8000

Table 4.2: Curve-fitting results for SiC GFET with 4/10 L/W ratio.

$R_{contact}$ [Ω]	n_0 [cm^{-2}]	μ [cm^2/ Vs]	MSE	mean MSE (k-fold)
9.0	$2.3680{\cdot}10^{13}$	9.6122	$0.0057{\cdot}10^3$	$0.0011{\cdot}10^4$
458	$3.1101{\cdot}10^{13}$	5.4368	$1.4391{\cdot}10^3$	$0.1622{\cdot}10^4$
0	$2.1228{\cdot}10^{13}$	10.1389	$0.0266{\cdot}10^3$	$0.0033{\cdot}10^4$
0.3267	$2.5455{\cdot}10^{13}$	10.0619	$0.0233{\cdot}10^3$	$0.0029{\cdot}10^4$
7827	$1.3100{\cdot}10^{13}$	60.1661	$0.5582{\cdot}10^3$	$0.0697{\cdot}10^4$
20449	$1.6100{\cdot}10^{13}$	11.7592	$8.7789 \cdot 10^3$	$1.0427 \cdot 10^4$
1203	$2.3210{\cdot}10^{13}$	10.0870	$1.5777{\cdot}10^3$	$0.1915{\cdot}10^4$
137	$1.8693{\cdot}10^{13}$	16.8367	$0.0992{\cdot}10^3$	$0.0115 \cdot 10^4$
4615	$2.2052 \cdot 10^{13}$	23.0965	$0.3709{\cdot}10^3$	$0.0429 \cdot 10^4$
3256	$2.6340{\cdot}10^{13}$	19.5447	$0.4471{\cdot}10^3$	$0.0495{\cdot}10^4$
4552	$1.2734{\cdot}10^{13}$	221.6210	$0.0019{\cdot}10^3$	$0.0003{\cdot}10^4$
2323	$3.3100{\cdot}10^{13}$	31.8193	$0.0049{\cdot}10^3$	$0.0005{\cdot}10^4$
7493	$1.2100{\cdot}10^{13}$	267.7412	$0.0367 \cdot 10^3$	$0.0048{\cdot}10^4$
5730	$0.8752{\cdot}10^{13}$	465.1963	$0.0750{\cdot}10^3$	$0.0099{\cdot}10^4$
4509	$1.3201{\cdot}10^{13}$	97.8169	$0.0535{\cdot}10^3$	$0.0073{\cdot}10^4$

It should be noted, that the contact resistance here is *not* scaled with W/L, but is the resistance per square. For example, $R_{contact} = 19.1\Omega$ for a 1/50 CVD GFET is the resistance value per square, and to get the total resistance value at a certain top gate voltage, one should use Equation (4.3). The contact resistance in this case would be $R_{contact} = \frac{50}{1} \cdot 19.1\Omega = 955\Omega$.

4.3.1 CVD GFET measurement uncertainty

Graphene transistors are generally known to exhibit instability in the location of the Dirac point. In top-gate sweep measurements, the location and, at times also the magnitude of the Dirac point would change with each sweep. In the CVD GFET top-gate sweeps, the location

Table 4.3: Curve-fitting results for SiC GFET with 1/1 L/W ratio.

$R_{contact}$ [Ω]	n_0 [cm^{-2}]	μ [cm^2/ Vs]	MSE	mean MSE (k-fold)
10999	$2.0101 \cdot 10^{13}$	$0.04471 \cdot 10^{3}$	$0.3255 \cdot 10^{4}$	$0.4390 \cdot 10^{4}$
16868	$1.8719 \cdot 10^{13}$	$0.0382 \cdot 10^{3}$	$0.6923 \cdot 10^{4}$	$0.8825 \cdot 10^{4}$
10217	$1.4100 \cdot 10^{13}$	$0.1103 \cdot 10^{3}$	$0.0327 \cdot 10^{4}$	$0.0335 \cdot 10^{4}$
29971	$0.4100 \cdot 10^{13}$	$1.2813 \cdot 10^{3}$	$0.1008 \cdot 10^{4}$	$0.1121 \cdot 10^{4}$
17095	$1.0100 \cdot 10^{13}$	$0.1355 \cdot 10^{3}$	$0.0031 \cdot 10^{4}$	$0.0037 \cdot 10^{4}$
0	$2.6832 \cdot 10^{13}$	$0.0138 \cdot 10^{3}$	$0.0016 \cdot 10^{4}$	$0.0022 \cdot 10^{4}$
16206	$0.5100 \cdot 10^{13}$	$1.2726 \cdot 10^{3}$	$0.4367 \cdot 10^{4}$	$0.5873 \cdot 10^{4}$
18805	$1.1063 \cdot 10^{13}$	$0.1221 \cdot 10^{3}$	$0.2356 \cdot 10^{4}$	$0.2390 \cdot 10^{4}$
15807	$1.4100 \cdot 10^{13}$	$0.1119 \cdot 10^{3}$	$0.0240 \cdot 10^{4}$	$0.0758 \cdot 10^{4}$
131	$3.7284 \cdot 10^{13}$	$0.0090 \cdot 10^{3}$	$0.0004 \cdot 10^{4}$	$0.0005 \cdot 10^{4}$
0	$3.7782 \cdot 10^{13}$	$0.0088 \cdot 10^{3}$	$0.1429 \cdot 10^{4}$	$0.1776 \cdot 10^{4}$
29759	$0.5097 \cdot 10^{13}$	$1.1337 \cdot 10^{3}$	$1.5329 \cdot 10^{4}$	$2.9441 \cdot 10^{4}$

Table 4.4: Curve-fitting results for SiC GFET with 0.5/1 L/W ratio.

$R_{contact}$ [Ω]	n_0 [cm^{-2}]	μ [cm^2/ Vs]	MSE	mean MSE (k-fold)
0.0257	$3.4052 \cdot 10^{13}$	4.6606	$0.1208 \cdot 10^{3}$	$0.1227 \cdot 10^{3}$
17187	$0.4100 \cdot 10^{13}$	705.4117	$0.1143 \cdot 10^{3}$	$0.1251 \cdot 10^{3}$
5980	$2.3840 \cdot 10^{13}$	25.6775	$0.0277 \cdot 10^{3}$	$0.0406 \cdot 10^{3}$
1	$4.4066 \cdot 10^{13}$	5.3303	$0.2271 \cdot 10^{3}$	$0.3876 \cdot 10^{3}$
3492	$4.9318 \cdot 10^{13}$	11.7472	$0.1518 \cdot 10^{3}$	$0.1764 \cdot 10^{3}$
3510	$4.9104 \cdot 10^{13}$	16.5585	$0.0143 \cdot 10^{3}$	$0.0162 \cdot 10^{3}$
4409	$2.8984 \cdot 10^{13}$	31.6841	$0.0380 \cdot 10^{3}$	$0.0527 \cdot 10^{3}$
5505	$2.8918 \cdot 10^{13}$	148.4276	$0.0148 \cdot 10^{3}$	$0.0176 \cdot 10^{3}$
1762	$4.9100 \cdot 10^{13}$	9.6897	$0.0942 \cdot 10^{3}$	$0.1277 \cdot 10^{3}$
4484	$3.8970 \cdot 10^{13}$	2.1255	$1.0353 \cdot 10^{3}$	$1.2103 \cdot 10^{3}$

and magnitude of the Dirac point changed with most GFETs as shown in Figure 4.12. The Dirac point was found to fix at a certain value after several sweeps.

Graphene is easily contaminated because it is a surface, but there are ways to clean graphene. First, annealing at ultrahigh vacuum or Ar/H_2 environment is proven to clean graphene. The downside of this method is that the graphene samples may recontaminate when transferred from the annealing chamber. Second method is to clean the graphene samples with driving

Table 4.5: Curve-fitting results for CVD GFETs.

L/W	$R_{contact}$ [Ω]	n_0 [cm^{-2}]	μ [cm^2/ Vs]	MSE	mean MSE (k-fold)
1/50	19.3	$1.9 \cdot 10^{12}$	2177	4.8726	5.7628
1/50	19.1	$6.1 \cdot 10^{12}$	519	0.5195	0.6262
2/50	14.6	$2.9 \cdot 10^{12}$	1151	6.1477	6.7512
2/50	43	$1.2 \cdot 10^{12}$	3955	87.7654	96.2758
2/50	33.5	$1.8 \cdot 10^{12}$	2250	13.0291	13.6072
4/50	0	$3.25 \cdot 10^{12}$	1286	24.8477	28.7943
4/50	0	$3.14 \cdot 10^{12}$	1284	1.7941	2.2392

a relatively high current (milliamperes) through the sample [49]. The current-induced cleaning is easily performed when measuring electrical characteristics of GFETs. The downside of this cleaning method is that the GFET may be damaged in the process, though according graphene can withstand significant currents without damage. This method is based on electromigration and Joule heating.

The current induced cleaning was tried on a CVD GFET sample, but cleaning was not used methodically on all samples because there were only a few (8) samples and the cleaning might have damaged the samples. In future measurements it may be beneficial to use current-induced cleaning if the GFET damage thresholds are measured first.

Summary

Graphene is an interesting new material that is relatively easy to produce. It has so many interesting potential applications that it could become the 'new silicon'. The many electrical and mechanical properties of graphene make it a 2D wonderland of physics, not to mention the bountiful chemical properties that have only just began to be researched. It is no surprise then, that graphene is researched in several fields and new findings are reported almost every week.

This master's thesis begun as a part of a joint Nanoradio project, and the ambitious goal in the beginning was to create a DC and small-signal model, so that circuit simulations could be made in the near future.

A literature survey was carried out and the state-of-the-art GFETs were compared to the NMOS technology. GFET small-signal models have been modelled as MOSFETs in literature and the same approach was used in this thesis. DC measurements were made on the SiC based GFETs and CVD GFETs. The SiC GFETs were found to be very nonuniform in electrical properties due to unintentional doping, graphene quality and contact resistance. CVD GFETs showed more uniform operation and were superior to the SiC GFETs.

The measurements on CVD GFETs showed that the Dirac point would wander with repeated sweeps due to sample contamination. Future measurements should include stability and durability measurements on GFETs. The top-gate sweeps could be repeated at certain time intervals to find out if the ambient environment changes the electrical properties. At the moment, the wearing of the contact electrodes constrains the number of measurements that can be performed on a GFET to less than ten if the probe tips are lifted after each measurement. This will make it difficult to observe how the properties change with time.

The DC measurement data was plotted and a commonly used model for total device resistance was chosen to fit the data, and to extract contact resistance, conductivity mobility and residual carrier concentration. The total device resistance model was validated using k-fold cross validation. Good GFET samples were chosen for S-parameter measurements. Alas, the calibration of the network analyzer turned out to be difficult and thus only one sample was accurately measured. The small-signal model parameters and cut-off frequency were calculated from the S-parameter data. The measure GFET showed a cut-off frequency of

80MHz at maximum. The cut-off frequency coincides with the theoretical calculation that predicted approximately 140 MHz for the CVD GFETs.

GFETs are at the moment very interesting for RF applications, because the cut-off frequency can potentially be raised to the teraHertz range. However, the operation of GFETs is limited by the low current on/off ratio and high contact resistance. Also, the question of the existence of full current saturation in graphene remains. The importance of reducing contact resistance is crucial in GFETs with very short channel, because high contact resistance may otherwise limit the operation and thus lower the cut-off frequency. Furthermore, the cut-off frequency is dependent on the channel length; short channel means high cut-off frequency.

Another issue is the very low gain of GFETs. The gain is limited by the contact resistance, current on/off ratio and nonexistent current saturation. Gain is needed in order to cascade GFETs. The low gain is one of the main reasons why there hasn't been an integrated circuit with GFET technology yet, though IBM is said to be working on a graphene IC.

All in all, the first GFETs were made just some six-seven years ago, and the pace of improvement is fast. It took decades for silicon technology to replace old vacuum tubes. The main issue in graphene technology actually getting to the consumer markets is the big semiconductor companies themselves. The success and fall of a technology in the end is dictated by the fine dance of ecomics with the need for better, faster and stronger transistors.

Bibliography

[1] R. van Noorden, “The trials of new carbon,” *Nature*, vol. 469, pp. 14–16, January 2011.

[2] A. K. Geim and K. Novoselov, “The Rise of Graphene,” *Nature Materials*, vol. 6, pp. 183–191, 2007. [Online]. Available: http://dx.doi.org/10.1038/nmat1849

[3] F. Schwierz, “Graphene transistors,” *Nature Nanotechnology*, vol. 5, pp. 487–496, 2010. [Online]. Available: http://dx.doi.org/10.1038/nnano.2010.89

[4] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, “Electric Field Effect in Atomically Thin Carbon Films,” *Science*, vol. 306, no. 5696, pp. 666–669, 2004. [Online]. Available: http://www.sciencemag.org/cgi/content/abstract/306/5696/666

[5] “The era of carbon allotropes,” *Nature Materials*, vol. 9, pp. 868–871, 2010. [Online]. Available: http://dx.doi.org/10.1038/nmat2885

[6] R. Schaller, “Moore’s law: past, present and future,” *Spectrum, IEEE*, vol. 34, no. 6, pp. 52 –59, june 1997.

[7] “More-than-Moore, White paper,” 2010? [Online]. Available: http://www.itrs.net/Links/2010ITRS/Home2010.htm

[8] A. K. Geim, “Graphene: Status and Prospects,” *Science*, vol. 324, no. 5934, pp. 1530–1534, 2009. [Online]. Available: http://www.sciencemag.org/content/324/5934/1530.abstract

[9] F. Schedin, A. K. Geim, S. V. Morozov, E. W. Hill, P. Blake, M. Katsnelson, and K. Novoselov, “Detection of individual gas molecules adsorbed on graphene,” *Nature Materials*, vol. 6, pp. 652–655. [Online]. Available: http://dx.doi.org/10.1038/nmat1967

[10] Y. Xu, C. Chen, V. Deshpande, F. DiRenno, A. Gondarenko, D. Heinz, S. Liu, P. Kim, and J. Hone, “Radio frequency electrical transduction of graphene mechanical resonators,” *Applied Physics Letters*, vol. 97, no. 24, p. 243111, 2010. [Online]. Available: http://link.aip.org/link/?APL/97/243111/1

[11] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres, and A. K. Geim, "Fine Structure Constant Defines Visual Transparency of Graphene," *Science*, vol. 320, no. 5881, p. 1308, 2008. [Online]. Available: http://www.sciencemag.org/content/320/5881/1308.abstract

[12] A. H. Castro Neto, F. Guinea, N. M. R. Peres, K. S. Novoselov, and A. K. Geim, "The electronic properties of graphene," *Rev. Mod. Phys.*, vol. 81, no. 1, pp. 109–162, Jan 2009.

[13] J. Oostinga, H. Heersche, X. Liu, A. Morpurgo, and V. L.M.K., "Gate-induced insulating state in bilayer graphene devices," *Nature Materials*, vol. 7, pp. 151–157, 2008. [Online]. Available: http://dx.doi.org/10.1038/nmat2082

[14] S. K. Banerjee, L. F. Register, E. Tutuc, D. Basu, S. Kim, D. Reddy, and A. H. MacDonald, "Graphene for cmos and beyond cmos applications," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2032 –2046, December 2010.

[15] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Phys. Rev. Lett.*, vol. 100, no. 20, p. 206803, May 2008. [Online]. Available: http://prl.aps.org/abstract/PRL/v100/i20/e206803

[16] A. K. Geim, M. Katsnelson, and F. Guinea, "Energy gaps and a zero-field quantum Hall effect in graphene by strain engineering."

[17] P. Avouris, "Graphene: Electronic and photonic properties and devices," *Nano Letters*, vol. 10, no. 11, pp. 4285–4294, 2010. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl102824h

[18] J. Hass, R. Feng, T. Li, X. Li, Z. Zong, W. A. de Heer, P. N. First, E. H. Conrad, C. A. Jeffrey, and C. Berger, "Highly ordered graphene for two dimensional electronics," *Applied Physics Letters*, vol. 89, no. 14, pp. 143 106 –143 106–3, 2006.

[19] S. Garaj, W. Hubbard, and J. Golovchenko, "Graphene synthesis by ion implantation," *Applied Physics Letters*, vol. 97, no. 18, p. 183103, 2010. [Online]. Available: http://link.aip.org/link/?APL/97/183103/1

[20] D. Kosynkin, A. L. Higginbotham, A. Sinitskii, J. R. Lomeda, A. Dimiev, K. B. Price, and J. M. Tour, "Longitudinal unzipping of carbon nanotubes to form graphene nanoribbons," *Nature*, vol. 458, pp. 872–876. [Online]. Available: http://dx.doi.org/10.1038/nature07872

[21] F. Chen, J. Xia, and N. Tao, "Ionic screening of charged-impurity scattering in graphene," *Nano Letters*, vol. 9, no. 4, pp. 1621–1625, 2009, pMID: 19301857. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl803922m

[22] A. Das, S. Pisana, B. Chakraborty, S. Piscanec, S. Saha, U. Waghmare, K. Novoselov, H. Krishnamurthy, A. Geim, A. Ferrari, and A. Sood, "Monitoring dopants by Raman scattering in an electrochemically top-gated graphene transistor," *Nature Nanotechnology*, vol. 3, pp. 210–215, 2008. [Online]. Available: http://dx.doi.org/10.1038/nnano.2008.67

[23] W. Liu, M. Li, S. Xu, Q. Zhang, Y. Zhu, K. Pey, H. Hu, Z. Shen, X. Zou, J. Wang, J. Wei, H. Zhu, and H. Yu, "Understanding the Contact Characteristics in Single or Multi-Layer Graphene Devices: the Impact of Defects (Carbon Vacancies) and the Asymmetric Transportation Behaviour." International Electron Devices Meeting, 2010, 2010.

[24] Y.-M. Lin, H. Chiu, K. Jenkins, D. Farmer, P. Avouris, and A. Valdes-Garcia, "Dual-gate graphene fets with f_T of 50 ghz," *Electron Device Letters, IEEE*, vol. 31, no. 1, pp. 68 –70, jan. 2010.

[25] K. Nagashio, T. Nishimura, K. Kita, and K. Toriumi, "Contact resistivity and current flow path at metal/graphene contact," *Applied Physics Letters*, vol. 97, no. 14, p. 143514, 2010. [Online]. Available: http://link.aip.org/link/?APL/97/143514/1

[26] D. Schroder, *Semiconductor Material and Device Characterization*. Wiley, 2006.

[27] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with al[sub 2]o[sub 3] dielectric," *Applied Physics Letters*, vol. 94, no. 6, p. 062107, 2009. [Online]. Available: http://link.aip.org/link/?APL/94/062107/1

[28] F. Schwierz, "Electronics: Industry-compatible graphene transistors," *Nature*, vol. 472, pp. 41–42. [Online]. Available: http://dx.doi.org/10.1038/472041a

[29] Y. Wu, Y.-M. Lin, K. Jenkins, J. Ott, C. Dimitrakopoulos, D. Farmer, F. Xia, A. Grill, D. Antoniadis, and P. Avouris, "Rf performance of short channel graphene field-effect transistor," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, dec. 2010, pp. 9.6.1 –9.6.3.

[30] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-GHz Transistors from Wafer-Scale Epitaxial Graphene," *Science*, vol. 327, no. 5966, p. 662, 2010. [Online]. Available: http://www.sciencemag.org/content/327/5966/662.abstract

[31] Y.-M. Lin, K. Jenkins, A. Valdes-Garcia, J. Small, D. Farmer, and P. Avouris, "Operation of graphene transistors at gigahertz frequencies," *Nano Letters*, vol. 9, no. 1, pp. 422–426, 2009. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl803316h

[32] Y. Wu, Y. Lin, A. Bol, K. Jenkins, F. Xia, D. Farmer, Y. Zhu, and P. Avouris, "High-frequency, scaled graphene transistors on diamond-like carbon," *Nature*, vol. 472, pp. 74–78. [Online]. Available: http://dx.doi.org/10.1038/nature09979

[33] B. Hardwidge, “Ibm: Graphene as it is won’t replace silicon in cpus,” January 2011. [Online]. Available: http://www.bit-tech.net/news/hardware/2011/01/21/ibm-graphene-wont-replace-silicon-cpus/1

[34] X. Yang, G. Liu, A. A. Balandin, and K. Mohanram, “Triple-mode single-transistor graphene amplifier and its applications,” *ACS Nano*, vol. 4, no. 10, pp. 5532–5538, 2010. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nn1021583

[35] R. Sordan, F. Traversi, and V. Russo, “Logic gates with a single graphene transistor,” *Applied Physics Letters*, vol. 94, no. 7, p. 073305, 2009. [Online]. Available: http://link.aip.org/link/?APL/94/073305/1

[36] S. Thiele, J. Schaefer, and F. Schwierz, “Modeling of graphene metal-oxide-semiconductor field-effect transistors with gapless large-area graphene channels,” *Journal of Applied Physics*, vol. 107, no. 9, p. 094505, 2010. [Online]. Available: http://link.aip.org/link/?JAP/107/094505/1

[37] J. Xia, F. Chen, J. Li, and N. Tao, “Measurement of the quantum capacitance of graphene,” *Nature Nanotehcnology*, vol. 4, pp. 505–509, 2009. [Online]. Available: http://dx.doi.org/10.1038/nnano.2009.177

[38] S. Sonde, F. Giannazzo, V. Raineri, and E. Rimini, “Dielectric thickness dependence of capacitive behavior in graphene deposited on silicon dioxide,” vol. 27, no. 2. AVS, 2009, pp. 868–873. [Online]. Available: http://link.aip.org/link/?JVB/27/868/1

[39] P. Drude, “Zur elektronentheorie der metalle,” *Annalen der Physik*, vol. 306, no. 3, pp. 566–613, 1900. [Online]. Available: http://dx.doi.org/10.1002/andp.19003060312

[40] I. Meric, M. Y. Han, B. Ozyilmaz, P. Kim, and K. L. Shepard, “Current saturation in zero-bandgap, top-gated graphene field-effect transistors,” *Nature Nanotechnology*, vol. 3, pp. 654–659, 2008. [Online]. Available: http://dx.doi.org/10.1038/nnano.2008.268

[41] M. Lemme, T. Echtermeyer, M. Baus, and H. Kurz, “A graphene field-effect device,” *Electron Device Letters, IEEE*, vol. 28, no. 4, pp. 282 –284, april 2007.

[42] C. Dimitrakopoulos, Y.-M. Lin, A. Grill, D. Farmer, M. Freitag, S. Y., S.-H. Han, Z. Chen, K. Jenkins, Y. Zhu, Z. Liu, T. McArdle, J. Ott, R. Wisnieff, and P. Avouris, “Wafer-scale epitaxial graphene growth on the si-face of hexagonal sic (0001) for high frequency transistors,” *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 28, no. 5, pp. 985–992, 2010. [Online]. Available: http://link.aip.org/link/?JVB/28/985/1

[43] I. Meric, C. Dean, A. Young, J. Hone, P. Kim, and K. Shepard, “Graphene field-effect transistors based on boron nitride gate dielectrics,” in *Electron Devices Meeting (IEDM), 2010 IEEE International*, dec. 2010, pp. 23.2.1 –23.2.4.

[44] J. L. Xia, F. Chen, P. Wiktor, D. K. Ferry, and N. J. Tao, "Effect of top dielectric medium on gate capacitance of graphene field effect transistors: Implications in mobility measurements and sensor applications," *Nano Letters*, vol. 10, no. 12, pp. 5060–5064, 2010. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/nl103306a

[45] M.-H. Bae, Z.-Y. Ong, D. Estrada, and E. Pop, "Infrared microscopy of joule heating in graphene field effect transistors," in *Nanotechnology, 2009. IEEE-NANO 2009. 9th IEEE Conference on*, july 2009, pp. 818 –821.

[46] A. Barreiro, M. Lazzeri, J. Moser, F. Mauri, and A. Bachtold, "Transport properties of graphene in the high-current limit," *Phys. Rev. Lett.*, vol. 103, no. 7, p. 076601, Aug 2009. [Online]. Available: http://link.aps.org/doi/10.1103/PhysRevLett.103.076601

[47] E. Alpaydin, *Introduction to Machine Learning*. The MIT Press, 2004.

[48] S. Xu and Q. Zhang, "Causes of asymmetry in graphene transfer characteristics," in *Junction Technology (IWJT), 2010 International Workshop on*, may 2010, pp. 1 –3.

[49] J. Moser, A. Barreiro, and A. Bachtold, "Current-induced cleaning of graphene," *Applied Physics Letters*, vol. 91, no. 16, p. 163513, 2007. [Online]. Available: http://link.aip.org/link/?APL/91/163513/1

Appendix A

The curve-fitting MATLAB-script

The main program is shown below.

```
%% Groundwork
clear all;
close all;

% destroy backups
delete('*.ui*~');

tdstot= dir('*.ui*');
%load data, filename here
filut=cell(size(tdstot));
[filut{:}]=tdstot.name;
% filut is a cell array with file names as elements

folds = 10;
repeats = 3;
%constants
d= 25e-9; %oxide thickness
% L * W = 2 micron * 50 micron
Nsq1 =1/50; % L/W SIC102
Nsq2=2/50; % SIC505
Nsq3=4/50; % SIC105

Cox=3.2e-7; %F/cm2 ; %e_r =9 assumed

meanParams=nan(length(filut),3);
```

```
STDParams=nan(length(filut),3);
minParams=nan(length(filut),3);
maxParams=nan(length(filut),3);
finalParams=nan(length(filut),3);

meanMSE=nan(length(filut),1);
stdMSE=nan(length(filut),1);
minMSE=nan(length(filut),1);
maxMSE=nan(length(filut),1);
finalMSE=nan(length(filut),1);

tTotal = tic;

for i=1:length(filut);
    nimi=filut{i};
    DATA=load(nimi);
    Id=DATA(:,2);
    Vg=DATA(:,1);
    Vd=DATA(:,3); % drain-source voltage
    %the total resistance is the current divided by
    %source-drain voltage
    R = Vd./Id;

    %insert here the correct dirac point value
    [Idp minIdInd]=min(Id);
    Vdp=Vg(minIdInd);

    %Vdispl is a vector
    Vdispl = abs(Vg-Vdp);

    switch nimi(1:4)
    case 'cvd7'
        Nsq=Nsq1;
    case 'cvd5'
        Nsq=Nsq2;
    case 'cvd2'
        Nsq=Nsq3;
    end
```

```
    OptFun = @(Vdispltrain, Rtrain, Vdispltest, Rtest) optimVal(Nsq,
Vdispltrain, Rtrain, Vdispltest, Rtest);


    fprintf('Starting crossval for file #%d: %s\n',i, nimi);
    tFile = tic;
    %k-fold cross validation, k=10 by default

    paroptions = statset('UseParallel','always');
    vals = crossval(OptFun, Vdispl, R, 'kfold',folds, 'mcreps', ...
    repeats,'Options', paroptions);
    toc(tFile)
    fprintf('Crossval at end\n');
    meanParams(i,:)=mean(vals(:,1:3));
    STDParams(i,:)=std(vals(:,1:3));
    minParams(i,:)=min(vals(:,1:3));
    maxParams(i,:)=max(vals(:,1:3));
    meanMSE(i,:)=mean(vals(:,4));
    stdMSE(i,:)=std(vals(:,4));
    minMSE(i,:)=min(vals(:,4));
    maxMSE(i,:)=max(vals(:,4));

    finalvals = optimVal(Nsq, Vdispl, R);
    assert(size(finalvals,1) == 1);
    finalParams(i,:) = finalvals(1:3);
    finalMSE(i,:)=max(finalvals(4));

    savefile=['matfiles/' nimi '.mat'];
    save(savefile, 'vals', 'finalvals', 'folds', 'repeats');

    fprintf('File #%d, %d vals\n', i, length(vals));
end
toc(tTotal)
```

The function that performs the optimization and cross-validation is shown below.

```
function [vals]=optimVal(Nsq, Vdispltrain, Rtrain,...
Vdispltest, Rtest)


%constants
```

```
d= 40e-9; %oxide thickness
Cox=1.9921e-07; %e_r =9 assumed

%% Lsq curvefit
%let's create an anon. function R
Rtot=@(Rc,n0,u, Vdispl) Rtotal(d,Nsq,Cox, ... % vakiot
       Rc,n0,u, ... % parametrit
       Vdispl);

R_curvefit=@(params,data)  Rtot(params(1), params(2),
... params(3), data);

%% Algorithm
%guess x0
r_=[5500:100:7000];
n_=[1e11:1e12:5e13];
u_=[100:100:2000];
x0vals=struc(r_,n_,u_);
x0min = [0 0 0];
x0max = [];

trainParams=nan(size(x0vals));
trainMSEs=nan(size(x0vals,1),1);

for i=1:length(x0vals)
    [x,resnorm,residual,exitflag,output,lambda,jacobian]=...
        lsqcurvefit(R_curvefit, x0vals(i,:), Vdispltrain, Rtrain, ...
        x0min, x0max,...
        optimset('Display', 'none'));
    trainParams(i,:)=x;
    trainMSEs(i)=mean(residual.^2);
   %fprintf('%d/%d\n', i, length(x0vals));
   %fprintf('lsqcurvefit: Rc=%.3f\nn0=%.3f\nu=%.3f\n',...
    x(1),x(2),x(3));
end

[minMSE ind]=min(trainMSEs);
bestParams=trainParams(ind, :);

if exist('Rtest', 'var')
```

```
    RtestEstimated = R_curvefit(bestParams, Vdispltest);
    MSEtest = mean((Rtest - RtestEstimated).^2);
    vals=[bestParams MSEtest];
else
    vals=[bestParams minMSE];
end
```

The function below defines calculates the total device resistance.

```
 function [Rtotal] = Rtotal(...
d,Nsq,Cox, ... % constants
Rc,n0,u,...
Vdispl) % "x"

hbar =  1.05457148e-34;
q = 1.6021e-19; %elementary charge
e0= 8.854e-12; %vacuum permittivity
er= 9; %Al2O3 dielectric const. value ranges from 6-9.
v_F= 1.1e6;



a=q/Cox;
b=-hbar*v_F*sqrt(pi)/q;
n= ((-b+sqrt(b.^2 +(4.*a.*Vdispl)))./(2.*a)).^2;

Rtotal=Rc + Nsq./(sqrt(n0^2 + n.^2).*q.*u);
```

Appendix B

Statistical analysis of the k-fold cross validation

Table B.1: The CVD GFET curve fit parameter interquartile ranges and k-fold cross validation mean parameter values.

Mean R_c [Ω]	R_c IQR	Mean n_0 [cm^{-2}]	n_0 IQR	Mean μ [cm^2/ Vs]	μ IQR
0.0	0.0	31.3546 $\cdot 10^{11}$	0.2$\cdot 10^{11}$	1284.04	6.9
0.0	0.0	32.5855 $\cdot 10^{11}$	0.8$\cdot 10^{11}$	1285.14	29.1
33.5	0.5	17.8381 $\cdot 10^{11}$	0.4$\cdot 10^{11}$	2249.44	62.9
42.9	2.4	11.9527 $\cdot 10^{11}$	1.5$\cdot 10^{11}$	3967.67	542.9
14.5	1.4	29.3035 $\cdot 10^{11}$	1.0$\cdot 10^{11}$	1149.84	64.3
37.0	0.4	26.7222 $\cdot 10^{11}$	0.7$\cdot 10^{11}$	3172.09	127.9
19.1	0.4	61.0147 $\cdot 10^{11}$	1.0$\cdot 10^{11}$	519.345	9.0
19.2	1.1	19.3884 $\cdot 10^{11}$	1.3$\cdot 10^{11}$	2180.39	218.5

Table B.2: The SiC GFET with 2/5 L/W ratio curve fit parameter interquartile ranges and k-fold cross validation mean parameter values.

Mean R_c [Ω]	R_c IQR	Mean n_0 [cm^{-2}]	n_0 IQR	Mean μ [cm^2/ Vs]	μ IQR
5846.8	22.0	0.837927 $\cdot 10^{13}$	0.0144772 $\cdot 10^{13}$	373.0	16.9
12386.0	224.5	0.776696 $\cdot 10^{13}$	0.100005 $\cdot 10^{13}$	307.2	108.8
4582.3	140.1	1.02052 $\cdot 10^{13}$	0.0791586 $\cdot 10^{13}$	233.0	49.0
2215.7	5562.5	2.5067 $\cdot 10^{13}$	1.92592 $\cdot 10^{13}$	254.2	141.5
4138.1	74.5	1.67246 $\cdot 10^{13}$	0.123082 $\cdot 10^{13}$	255.9	52.1
4223.3	76.0	1.73813 $\cdot 10^{13}$	0.0897204 $\cdot 10^{13}$	176.0	25.4
2444.8	219.6	3.43666 $\cdot 10^{13}$	0.100004 $\cdot 10^{13}$	22.8	2.2
4247.2	132.4	1.57432 $\cdot 10^{13}$	0.0653446 $\cdot 10^{13}$	89.9	10.5

Table B.3: The SiC GFET with 4/10 L/W ratio curve fit parameter interquartile ranges and k-fold cross validation mean parameter values.

Mean R_c [Ω]	R_c IQR	Mean n_0 [cm^{-2}]	n_0 IQR	Mean μ [cm^2/ Vs]	μ IQR
401.8	16.3	2.31841 $\cdot 10^{13}$	0.00257797 $\cdot 10^{13}$	10.5	0.0
262.0	429.7	3.13322 $\cdot 10^{13}$	0.0837919 $\cdot 10^{13}$	5.3	0.3
0.0	0.0	2.1229 $\cdot 10^{13}$	0.00244678 $\cdot 10^{13}$	10.1	0.0
73.2	4.7	2.53507 $\cdot 10^{13}$	0.00511781 $\cdot 10^{13}$	10.2	0.0
7790.0	8.7	1.31993 $\cdot 10^{13}$	9.828e-05 $\cdot 10^{13}$	59.6	0.2
20388.8	2737.6	1.60338 $\cdot 10^{13}$	0.200011 $\cdot 10^{13}$	12.7	3.9
1186.2	249.5	2.32301 $\cdot 10^{13}$	0.0428806 $\cdot 10^{13}$	10.1	0.4
400.3	69.3	1.82989 $\cdot 10^{13}$	0.00964586 $\cdot 10^{13}$	19.0	0.2
4623.0	183.9	2.20253 $\cdot 10^{13}$	0.0499378 $\cdot 10^{13}$	23.2	1.4
3253.3	111.4	2.63491 $\cdot 10^{13}$	0.0456125 $\cdot 10^{13}$	19.5	0.8
4560.1	66.5	1.26525 $\cdot 10^{13}$	0.0601356 $\cdot 10^{13}$	227.8	27.0
2210.4	151.5	3.38997 $\cdot 10^{13}$	0.10001 $\cdot 10^{13}$	29.9	2.8
7454.5	113.7	1.24 $\cdot 10^{13}$	0.100113 $\cdot 10^{13}$	269.9	52.4
5707.2	108.1	0.891739 $\cdot 10^{13}$	0.102554 $\cdot 10^{13}$	457.3	132.5
4503.2	130.1	1.3207 $\cdot 10^{13}$	0.0592211 $\cdot 10^{13}$	99.3	11.1

Table B.4: The SiC GFET with 1/1 L/W ratio curve fit parameter interquartile ranges and k-fold cross validation mean parameter values.

Mean R_c [Ω]	R_c IQR	Mean n_0 [cm^{-2}]	n_0 IQR	Mean μ [cm^2/ Vs]	μ IQR
9901.1	4870.1	2.1187 $\cdot 10^{13}$	0.800118 $\cdot 10^{13}$	49.1	44.3
16867.2	34.9	1.87238 $\cdot 10^{13}$	0.0146409 $\cdot 10^{13}$	38.2	0.4
10217.2	5.9	1.41001 $\cdot 10^{13}$	9.06126e-08 $\cdot 10^{13}$	110.3	0.2
29809.0	417.8	0.446591 $\cdot 10^{13}$	0.100054 $\cdot 10^{13}$	1095.3	516.4
17407.0	781.1	0.970019 $\cdot 10^{13}$	0.0999291 $\cdot 10^{13}$	154.8	45.8
1.7	1.0	2.68295 $\cdot 10^{13}$	0.00257214 $\cdot 10^{13}$	13.8	0.0
16066.7	219.9	0.572413 $\cdot 10^{13}$	0.101081 $\cdot 10^{13}$	1109.2	414.8
18809.1	26.4	1.10563 $\cdot 10^{13}$	0.00362022 $\cdot 10^{13}$	122.2	1.0
16002.1	439.8	1.35666 $\cdot 10^{13}$	0.100092 $\cdot 10^{13}$	141.4	23.4
522.8	657.5	3.68662 $\cdot 10^{13}$	0.0704274 $\cdot 10^{13}$	9.3	0.5
0.1	0.0	3.77962 $\cdot 10^{13}$	0.0232267 $\cdot 10^{13}$	8.8	0.1
26970.9	378.5	0.835148 $\cdot 10^{13}$	0.259299 $\cdot 10^{13}$	1518.1	1147.2

Table B.5: The SiC GFET with 0.5/1 L/W ratio curve fit parameter interquartile ranges and k-fold cross validation mean parameter values.

Mean R_c [Ω]	R_c IQR	Mean n_0 [cm^{-2}]	n_0 IQR	Mean μ [cm^2/ Vs]	μ IQR
0.4	0.2	3.40565 $\cdot 10^{13}$	0.00234053 $\cdot 10^{13}$	4.7	0.0
17169.8	4.8	0.414936 $\cdot 10^{13}$	3.91816e-07 $\cdot 10^{13}$	690.9	4.0
5993.1	128.5	2.38005 $\cdot 10^{13}$	0.0388278 $\cdot 10^{13}$	25.8	1.1
265.8	347.0	4.35643 $\cdot 10^{13}$	0.096441 $\cdot 10^{13}$	5.5	0.3
3525.2	15.7	4.91295 $\cdot 10^{13}$	0.00456337 $\cdot 10^{13}$	11.9	0.0
3510.8	11.9	4.91029 $\cdot 10^{13}$	0.000343693 $\cdot 10^{13}$	16.6	0.1
4391.8	172.7	2.90613 $\cdot 10^{13}$	0.08864 $\cdot 10^{13}$	31.5	2.5
5509.5	12.7	2.87999 $\cdot 10^{13}$	0.0384198 $\cdot 10^{13}$	150.5	4.5
1763.2	36.0	4.91048 $\cdot 10^{13}$	0.000312422 $\cdot 10^{13}$	9.7	0.1
77.2	32.5	3.89257 $\cdot 10^{13}$	0.0171416 $\cdot 10^{13}$	2.1	0.0