Helsinki University of Technology
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Electron Physics Laboratory

Fabrication and modelling of SOI and GaAs MSM photodetectors and a GaAs-based integrated photoreceiver

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Abstract

In this work metal semiconductor metal photodetectors (MSM PDs), pseudomorphic high electron mobility transistors (pHEMTs), and a monolithically integrated photoreceiver are studied. The motivation for this work is to develop a solution for high-speed data transfer in telecommunication systems. The goals are to develop the fabrication technology using electron beam (e-beam) lithography, and to achieve higher bandwidths for the detector, the transistor, as well as the photoreceiver, with submicron devices.

First, MSM detectors on different materials, i.e. silicon-on-insulator (SOI) and semi-insulating gallium arsenide (S.I. GaAs) are fabricated using both optical and e-beam lithography. The detectors are characterized with current-voltage (I-V), capacitance-voltage (C-V), scattering-parameter (S-parameter) and transient time measurements. At a bias voltage of 3 V the dark current is measured to be 135 pA for a submicron S.I. GaAs detector, which corresponds to a dark current density of 31 μA/cm^2. For micrometer feature size SOI detectors with SiN-passivation the dark current is reduced significantly, being in the pA range up to 30 V. The capacitance of the interdigitated electrode structure is shown to be very low: e.g. a GaAs-based detector with submicron finger dimensions and comprising an area of 10 x 35 μm^2 obtains a capacitance of 32 fF. The instrumentation limited rise time and full width at half maximum ($FWHM$) for a submicron MSM on S.I. GaAs (finger spacing 0.3 μm, finger width 0.2 μm) are 18 and 27 ps, respectively. The transient characteristics measured for SOI detectors indicate that with decreasing thickness of the photoactive layer the bandwidth increases. The instrumentation limited rise time and $FWHM$ for a SOI PD (different measurement setup than for GaAs detectors) with 0.5 μm top Si layer (finger spacing 3 μm, finger width 3 μm) are 64 and 100 ps, respectively. In contrast a SOI PD with 1 μm top Si layer exhibits a rise time and $FWHM$ of 77 and 142 ps, respectively. The responsivity for the GaAs detectors is reasonable and according to theoretical values around 0.25 A/W at a wavelength of 780 nm. The SOI MSM PDs, however, perform responsivities in the mA/W- range, attributed to the relatively thin photoactive top Si layer: e.g. a device with top Si thickness of 4 μm demonstrates a responsivity of 93 mA/W (quantum efficiency 14.5 %), measured at a bias voltage of 6 V and a wavelength of 800 nm. It can be concluded, that a thicker layer leads to enhanced photoresponse.

Second, GaAs based pHEMTs with various gate lengths (ranging from 1 μm down to 0.2 μm) are fabricated. The e-beam lithography technique is developed for both triangular and mushroom shaped gates. DC and RF measurements are carried out, as well as simulations based on models available in the microwave design system (MDS). The extrinsic cut-off frequency f_t and maximum frequency of oscillation f_{max} for a standard transistor (l_g = 1.1 μm, W = 200 μm) exhibit 29 GHz and 52 GHz, respectively, whereas for a submicron triangular shaped transistor (l_g = 0.35 μm, W = 160 μm) they are 61 GHz and 80 GHz, respectively. For a mushroom shaped pHEMT (top 0.6 μm, footprint 0.2 μm, W = 200 μm) f_t and f_{max} are 73 GHz and 116 GHz, respectively. The transconductance is observed to increase with decreasing gate length. A transistor with a gate length of 0.34 μm and a width of 40 μm obtains a peak extrinsic transconductance of 539 mS/mm at V_{ds} = 2 V and V_{gs} = -0.25 V (I_{dsat} = 217 mA/mm).

Finally, a GaAs-based photoreceiver is investigated, consisting of an MSM PD and a transimpedance amplifier. Two different kind of circuits are realized, either applying only optical (standard) lithography, or a combination of optical and e-beam lithography. For the standard receivers the transistors have a gate length of 1 μm and the MSMs finger spacings and widths of 1 μm, whereas the e-beam circuits have submicron transistors for the amplification stage, and a submicron MSM. The electrical, as well as opto-electronic response, is measured for the different receivers. The submicron receiver shows the largest electrical 3 dB bandwidth, as expected, 9.5 GHz (Z_T = 1.2 kΩ) compared to 8.4 GHz (Z_T = 1.3 kΩ) that of a standard receiver. According to simulations the 3 dB bandwidth of a receiver solely consisting of submicron transistor yields 16.9 GHz, indicating that reduced gate length is a major factor in achieving higher bandwidths.

Preface

This thesis was done in cooperation with the Helsinki University of Technology (HUT, Finland) and the Technical University of Eindhoven (TUE, the Netherlands).

I express my sincere gratitude to Prof. Pekka Kuivalainen, the supervisor of the thesis, for the opportunity to work in the Electron Physics Laboratory at HUT, and his support during the years. I thank Prof. Leon Kaufmann for the fruitful cooperation with the Opto Electronic Devices-group at TUE, providing me excellent working conditions and his guidance.

Special thanks belong to Barry Smallbrugge. His expertize in clean room related processing methods and equipment, and skillful practical assistance were invaluable. Dr. Ralf Bertenburg introduced me into the basics of e-beam lithography, which was essential for the successful completion of the submicron devices. I am especially grateful to Erik Jan Geluk for the many SEM-pictures, various metal depositions, and his essential technical help with the e-beam exposures. Most of all, I am deeply indebted to Thieu Kwaspen. His many S-parameter and electrical/optical measurements, and numerous discussions and advises throughout the time made this thesis possible.

I wish to express my appreciation to Dr. Kari Maula for his exceptional thoroughness in going over my thesis and the constructive comments which were a great help in bringing the thesis to its present form.

Finally, I want to thank all my colleagues at HUT and TUE for pleasant collaboration and working environment.

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Lausanne, September 2001
Katri Honkanen

Author's Contribution

The author has had an active role in all stages of the work reported in this thesis. She has been involved in the planning, performing of the experiments as well as in the interpretation of the results.

The processing of all components (MSMs, pHEMTs, transimpedance amplifiers) were performed by the author. The basic recipes, concerning the optical lithography, were gathered from experience of previous works performed by the Electron Physics Laboratory (HUT) and the OED-group (Opto Electronic Devices) at TUE. Slight modifications were made by the author.

The optimal e-beam lithography protocols were developed by the author. The total procedure consists of choosing the suitable PMMA resists, PMMA resist baking, exposure, developing and subsequent gate recess etching.

The author carried out the following measurements: I-V (dark and photo current for MSMs), C-V (both MSMs and pHEMTs), transient response (MSMs), $I_{ds}(V_{ds})$, $I_{ds}(V_{gs})$ and ohmic contact resistance (using linear TLM). The Ti:Sapphire laser system used for the transient time measurements was set up by the Physics Department at TUE and the Optoelectronics Laboratory at HUT. The S-parameter measurements for the pHEMTs, and electrical and optical characterization for the circuits were performed by J. Kwaspen at TUE. The Hall measurements were done by P. Nouwens. M. Krämer did some of the ohmic contact resistance measurements (using circular TLM). Scanning electron microscope (SEM) pictures were taken by E.J. Geluk at TUE.

Simulations and fittings were performed by the author applying physical models taken partly from literature, and using microwave design system (MDS) software provided by HP. The IC-CAP parameter extractions were done by J. Kwaspen.

List of Symbols

α	Absorption coefficient
A	Cross section area
$A_{o,v}$	DC/AC open loop voltage gain
A^* / A^{**}	Effective/Modified Richardson constant
ANA	Analyzer
APD	Avalanche photodiode
ARC	Antireflection coating
C_f	Feedback capacitance
C_g	Gate capacitance
C_{msm}	Detector capacitance
CPW	Coplanar waveguide
d	Thickness of the active semiconductor-layer
d_{ARC}	Thickness of the antireflection coating
DBR	Distributed Bragg reflector
$D_{n,p}$	Diffusion coefficient for electrons/holes
δ	Skin depth
E	Electric field
E_c	Critical electric field
$E_{C,V}$	Conduction/valence band energy level
E_F	Fermi energy
E_g	Bandgap energy
E_m	Maximum electric field
ϵ_0	Permittivity in vacuum
ϵ_s	Semiconductor permittivity
$\epsilon_{1,2}$	Permittivity of the potential well/donor-layer
ϵ_r	Dielectric constant
e-beam	Electron beam
η	Quantum efficiency
η_i	Internal quantum efficiency
FG	Finate ground
f_t	Cut-off frequency
f_{max}	Maximum frequency of oscillation
f_{3dB}	3 dB bandwidth
$FWHM$	Full width at half maximum
ν	Frequency of light
ϕ_{Be}	Effective Schottky barrier height
$\phi_{Bn,Bp}$	Schottky-barrier height for electrons/holes
$\Delta\phi_{Bn,Bp}$	Schottky barrier lowering for electrons/holes
ϕ_m	Metal work function
Φ_0	Photon flux per unit area
γ	Penetration depth
$g_{o,d}$	DC/RF output conductance
g_m	Transconductance
G	Generation rate
G_i	Internal gain
GSG	Ground source ground
h	Planck constant
h_{trap}	Number of holes trapped
HF	High frequency
HBT	Heterojunction bipolar transistor
I_{dark}	Dark current
IGT	Intermediate growth temperature
I_{ds}	Drain to source current

I_{gs}	Gate leakage current
I_{ph}	Photocurrent
ITO	Indium tin oxide
J_{dark}	Dark current density
$J_{n,p}$	Electron/hole current density
J_{sat}	Saturation current density
J_{tun}	Tunneling current density
JFET	Junction field effect transistor
k_B	Boltzmann constant
λ	Wavelength
l	Length of metal finger
l_g	Gate length
L_s	Series inductance
LT	Low temperature
m_e^* / m_l^*	Electron effective mass/Longitudinal effective mass
MAG	Maximum available gain
MDS	Microwave design system
MESFET	Metal semiconductor field effect transistor
MMIC	Monolithic microwave integrated circuit
MOSFET	Metal oxide semiconductor field effect transistor
MS	Microstrip
MSG	Maximum stable gain
MSM PD	Metal semiconductor metal photodetector
μ_o	Permeability in vacuum
$\mu_{e,h}$	Electron/hole mobility
μ_0	Low field mobility
NEP	Noise equivalent power
n	Ideality factor
n_r	Refractive index
n_s	2DEG sheet density
$N_{a,d}$	Acceptor/Donor impurity concentration
$N_{c,v}$	Effective density of states in the conduction/valence band
OE	Opto electrical
OEIC	Optoelectronic integrated circuit
pHEMT	Pseudomorphic high electron mobility transistor
P_{opt}	Optical power
PECVD	Plasma enhanced chemical vapor deposition
PIN PD	p-i-n photodiode
PMMA	Polymethylmethacrylate
q	Elementary charge
Q_s	Semiconductor charge
Q_g	Gate charge
r	Reflection coefficient
R	Responsivity
R_c	Contact resistance of the Schottky interface
R_{dark}	MSM dark resistance
R_f	Feedback resistance
R_L	Load resistance
R_0	Resistance per finger
R_s	Series resistance of the MSM electrodes
ρ	Resistivity
RF	Radio frequency
RIE	Reactive ion etching
RTA	Rapid thermal annealing
σ	Conductivity

s	Spacing between metal fingers
SEM	Scanning electron microscope
S.I.	Semi-insulating
SL	Superlattice
SOI	Silicon-on-insulator
SOS	Silicon-on-sapphire
SPL	Single pixel line
t_r	Rise time
t_f	Fall time
T	Temperature
TL	Transmission line
TLM	Transmission line method or Transfer length model
τ, τ_{tr}	Transit time constant
τ_{RC}	RC time constant
v_d	Drift velocity
$v_{e,h}$	Electron/hole velocity
v_s	Saturation velocity
v_{th}	Thermal velocity
V	Bias voltage
V_{ds}	Drain to source voltage
V_{gs}	Gate to source voltage
V_{BD}	Breakdown voltage
V_{FB}	Flatband voltage
V_{RT}	Reach-through voltage
V_{th}	Threshold voltage
V_{pp}	Peak-to-peak voltage
w	Width of metal fingers
W	Gate width
$W_{1,2}$	Depletion layer width at the cathode/anode
χ	Electron affinity of semiconductor
Z_T	Transimpedance

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Chapter 1

Introduction

1.1 Status of Research

In the last few years the demand for optical communication systems with higher bandwidths and multi-gigabit per second transmission has increased enormously, setting emphasis to the development of high-performance optical receivers. The front-end of the receiver, composed of a photodetector integrated with field effect transistor (FET) amplification stages, through which the HF and noise characteristics are determined, is of vital importance in achieving optimum and reliable performance. In this respect special attention is to be drawn to optimizing the characteristics of the discrete detector and the transistor. The type of the detector (PIN, APD, MSM) as well as the transistor (MOSFET, MESFET, HBT, HEMT) has to be determined according to the system requirements.

Depending on the application and the desired performance parameters (sensitivity, transmission rate or dynamic range) choice of the semiconductor material is crucial. For long distance communications, exceeding 1 km, InP is suitable whereas for short distance links GaAs is to be used. Considering the integration method monolithical integration as opposed to hybrid circuits is preferred as it has the advantage of reducing the effect of parasitics and thus improving the overall RF behaviour. In addition, the the cost-effectiveness of photoreceivers, in particular with respect to low packaging costs compared to hybrid solutions is enhanced.

Deciding for the photodiode different aspect have to be taken into account: speed, responsivity and dark current being the most important factors. In addition, for the development of monolithically integrated photoreceivers a high-speed photodetector compatible in processing with electronic devices is very important. PIN- and avalanche photodiodes (APDs) are generally used in commercial applications. MSM PDs have, however, shown superior characteristics in comparison with these conventional photodetectors, due to reduced capacitance per area, higher speed and lateral geometry which leads to compatible monolithical integration with OEICs (optoelectronic integrated circuits). The external quantum efficiency of the MSM photodiode is somewhat inferior to that of PINs and APDs, but can be enhanced with appropriate optimization of the device thickness and the used wavelength.

High frequency FETs operating up to the mm-wavelength regime have been focus of interest both from applications and fundamental research point of views. Commercial applications include analog and digital circuits, which benefit from the superior noise and gain properties of these devices [1]. As frequency, noise, power capacity, linearity and efficiency requirements increase, different kind of field effect transistors (e.g. the GaAs metal semiconductor FET (MESFET), junction FET (JFET), Si metal oxide semiconductor FET (MOSFET)) are being pushed to their limits in both design and performance. These requirements imply a very small transistor with submicron channel length and increased channel doping under the gate, leading to the desired large saturation current and large transconductance. However, increased doping leads to ionized impurity scattering within the doped channel region, and further to degradation of mobility and peak velocity.

Three types of FET are commonly used for millimeter-wave applications. These are the GaAs MESFET, the GaAs-based AlGaAs/InGaAs/GaAs pseudomorphic HEMT (pHEMT), and the InP-based AlInAs/InGaAs/InP HEMT. Devices grown on InP allow the use of channel layers with a higher In content than GaAs pHEMTs, providing improved channel properties and increased gain. InP

HEMTs have emerged as the device of choice for millimeter-wave low noise applications. InP HEMTs have demonstrated the highest cut-off frequency f_t of 350 GHz (for a 30 nm gate length HEMT lattice-matched to InP), and the highest maximum frequency of oscillation f_{max} of more than 600 GHz of any transistor technology [2]. However, GaAs-based pHEMTs and MESFETs are still used in many commercial applications where cost rather than ultimate noise performance is the driving factor. HEMTs are suitable in applications such as high-speed logic circuits, small-signal, high-frequency amplifiers, oscillators and switches (in e.g. dual-band/multi-mode handsets). pHEMTs offer distinct advantages for RF power switching applications.

The development of millimeter-wave MMICs includes military applications such as radar and satellite-based communication systems. Recent applications include also local multipoint distribution service (LMDS) and related systems, wireless local area networks, and automotive radar. In addition, high performance HEMTs have been used to develop digital circuits such as 75 GHz dynamic divider and an 80 Gbit/s multiplexer.

For very high power applications gallium nitride holds great promise due to the wide bandgap. One problem is, however, the high defect density in the material, due to the lattice mismatch between GaN and the sapphire or SiC substrate. GaN HEMTs have obtained f_t and f_{max} values of 50 GHz and 110 GHz respectively, for a device with a gate length of 0.15 μm, a channel length of 2.5 μm and a periphery of 2 x 100 μm^2 [3].

Recently, HEMTs with lattice-mismatched $In_xGa_{1-x}As$ / GaAs structure have received much attention for microwave and optical applications because of its excellent transport properties, wide-bandgap tuning range, and possible integration with GaAs-based circuits.

In addition, the incorporation of Si planar doping in a pHEMT has led to a new generation of low noise and medium power devices.

1.2 Goal of the Thesis

The goal of this work is to study the metal semiconductor metal photodetector (MSM PD), the high electron mobility transistor (HEMT), and a monolithically integrated GaAs-based photoreceiver consisting of these devices. The project covers technological optimization of the various processing steps, several different measurements (DC and RF), and modelling and simulations of the experimental results. The work comprises the whole path from design to characterization up to analysis of the results. The main emphasis, however, is set to developing the fabrication technology using electron beam (e-beam) lithography, in order to achieve submicron linewidths.

The thesis was done in collaboration with the Helsinki University of Technology (HUT, Finland) and the Technical University of Eindhoven (TUE, the Netherlands).

The MSM photodetectors were studied both at HUT and TUE. The SOI MSM detectors fabricated using optical lithography were investigated at HUT, whereas GaAs-based MSM detectors fabricated applying electron beam lithography were studied at TUE. The research on the pHEMT transistors and the transimpedance amplifier circuits was carried out at TUE.

The goals can be described briefly as follows:

- Fabrication of MSM PDs on silicon- and GaAs- substrates: Si-based detectors on bulk-Si- and silicon-on-insulator- (SOI)-wafers, whereas GaAs-based detectors on semi-insulating (S.I.) GaAs-substrates, using both conventional optical lithography as well as electron beam (e-beam) lithography. GaAs MSM PDs are applied to the final pHEMT photoreceiver circuit, but in order to get a good comparison between Si and GaAs as materials and their effect mainly on speed- and responsivity characteristics both semiconductor-types are considered.
- The main challenge in the development of the MSM PD structures is to obtain a short pulse response. In order to achieve high speed the dimension of the metal fingers is reduced to the submicron region. In addition to high speed desired features are low dark current and good responsivity.
- Development of submicron gate GaAs-based transistor technology based on e-beam lithography, both triangular and mushroom shaped gates. Special attention is drawn to the optimization of the

linewidth control.

• pHEMT (AlGaAs/InGaAs/GaAs) characterization using DC and S-parameter measurements. Modelling and simulations with the obtained experimental data in order to get reliable physical parameters for describing the submicron transistor behaviour.

• Transimpedance amplifier circuit fabrication on different layer structures. Two different kind of receivers: standard receivers exposed optically (1 μm gatelength), and 'submicron receivers' having a combination of 1 μm and submicron gates. Electrical as well as opto-electrical experiments, and finally simulations.

1.3 Outline

The thesis can be divided into three major parts: detector fabrication and characterization, submicron transistor technology and experiments, photoreceiver realization and measurements.

In Chapter 2 the MSM PDs are investigated. The diodes have been fabricated on both SOI- and GaAs-substrates. Characterization of detectors includes measurements such as: dark I-V, photocurrent, C-V, dynamical response and S-parameters. Physical models for dark- and photocurrent and the capacitance are developed in Section 2.3. In addition a small-signal equivalent circuit for extraction of the parasitics is presented. Finally, fitting of the experimental results to the model is carried out.

Chapter 3 covers the theoretical analysis for HEMTs, a detailed fabrication description of the e-beam lithography, and characterization including DC and RF measurements. Furthermore, modelling and fittings using the commercial software microwave design system (MDS).

Chapter 4 consists of the photoreceiver design (mask layout), the electrical and opto-electrical experiments, and simulations.

Finally, Chapter 5 gives a summary of the most significant results obtained in this work.

Chapter 2

Metal Semiconductor Metal Photodetector

2.1 Operation Principle

The MSM PD is a planar Schottky barrier device consisting of interdigitated metal electrodes deposited on a semiconductor substrate, Fig. 2.1.

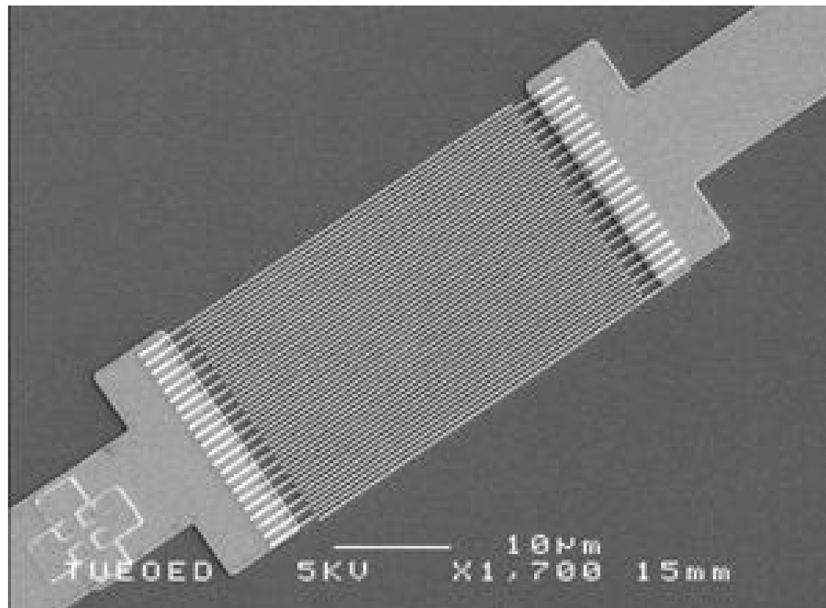

Figure 2.1: SEM picture of a GaAs-based submicron MSM PD (w = 0.2 μm, s = 0.3 μm, A = 22 x 40 μm^2, Ti/Au = 50/250 nm).

The device detects the presence of light, by converting a photon flux into an electrical signal. Figure 2.2 displays the cross section of the MSM PD, indicating the dimensions, carrier motion, the electric field orientation and the incident illumination. s and w refer to the electrode spacing and width, respectively, d to the thickness of the photoactive region and $\vec{E}$ to the electric field. The common bias points $\pm V$ and the photocurrent generation I_{ph} are indicated.

The PD is illuminated from the top with photons whose energy is larger than the bandgap energy of the semiconductor. The amount of photocarriers depends upon the photon flux. Light absorption in the semiconductor leads to electron-hole pair generation. By applying an external bias voltage to the metal contacts electrons in the conduction band and the holes in the valence band are swept in

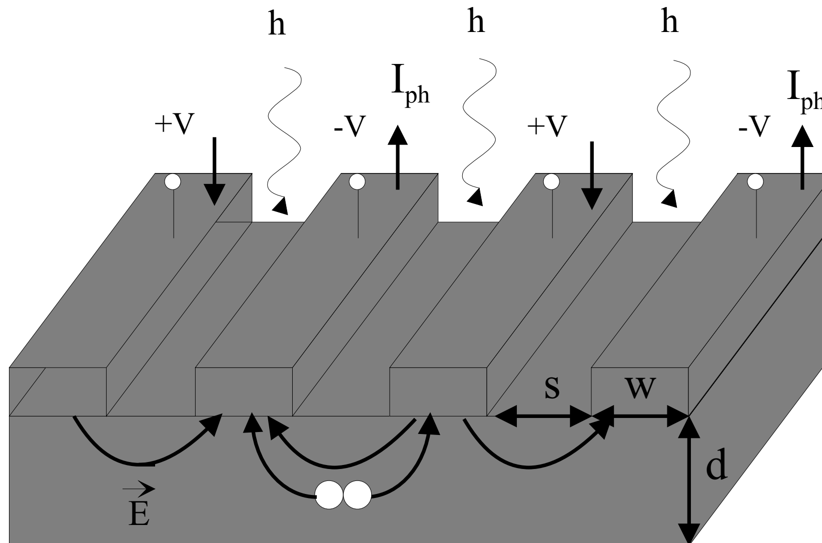

Figure 2.2: Cross section of an MSM PD.

opposite directions. Carriers are then collected at the metal pads, and a current is detected in the external circuit.

When biased, the metal fingers form two Schottky-diodes connected in series; one forward biased, the other reversed biased. The semiconductor is fully depleted in the region between the fingers if the applied bias exceeds the flatband voltage. The dopant density of the semiconductor material should be kept low to achieve full depletion of majority carriers, even at low bias.

Due to the geometry of the interdigitated electrodes the capacitance of the detector between the fingers is in the order of fFs, even for relatively large active areas. This is an especially important feature for optical-fiber coupling applications. The series resistance of the fingers can also be kept small, i.e. by optimizing the length of the fingers and the metal cross section area. The resultant RC time constant is therefore low and does not usually limit the *external* speed.

By keeping the electrode distance small the carrier transit time from one electrode to the other is reduced and thus the *intrinsic* response time improved. However, due to the 2D-nature of the device, the speed also depends on the thickness of the absorbing material. Restricting the photoactive area to a thin top layer the response time can be decreased.

On the other hand, high speed may be achieved but at the expense of the responsivity. If the used wavelength is such that light penetrates deep into the substrate responsivity suffers, and there is a severe trade-off between speed and responsivity. To overcome this trade-off the wavelength has to be chosen properly, or devices with backreflectors, rough surfaces or trench structures should be used.

The dark current is mainly attributed to the leakage of carriers over/through the reversed-biased Schottky barrier. In order to minimize the dark current, a high Schottky barrier is desirable. This can be achieved by proper selection of the metal, and a careful cleaning process of the semiconductor surface just prior to metal deposition. The photogeneration and thus photocurrent depends exponentially on the characteristic, wavelength dependent absorption coefficient and the distance from the surface. Figure 2.3 presents the energy band diagram of the MSM PD when the detector is under bias and illumination, and shows the different dark- and photocurrent components.

2.2 Parameters Describing the Performance of the Detector

2.2.1 Dark Current

The basic transport processes for a Schottky diode with n-type semiconductor under reverse bias without illumination are (1) transport of electrons, that have sufficient energy to overcome the potential

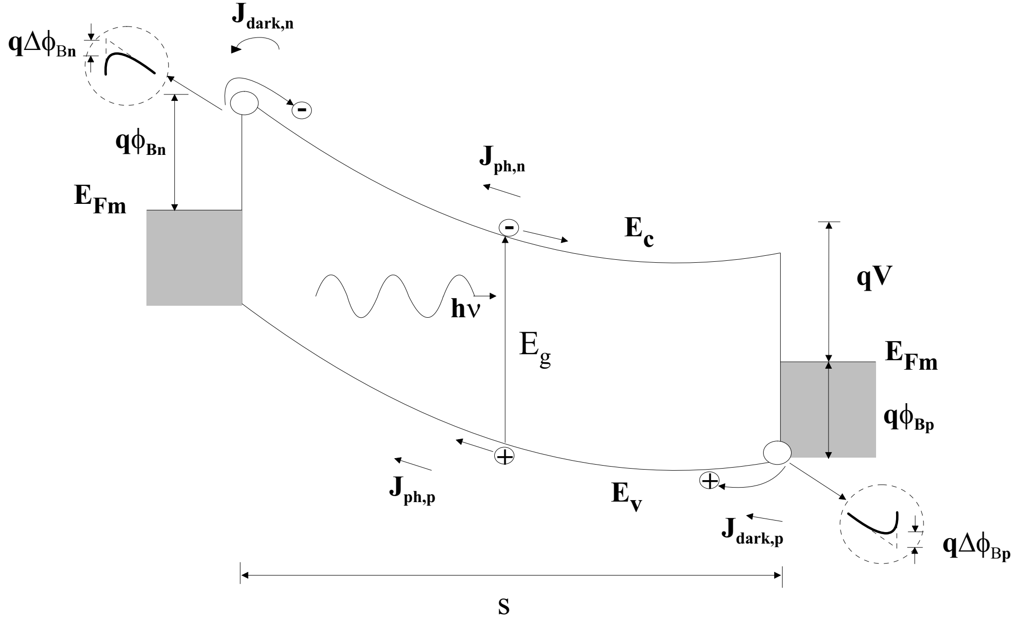

Figure 2.3: Energy band diagram of an MSM PD under bias and illumination, showing the dark- and photocurrent components.

barrier, from the metal into the semiconductor, (2) quantum-mechanical tunneling of electrons through the barrier from the metal into the semiconductor (field and/or thermionic-field emission), (3) generation in the space-charge region, (4) generation in the neutral region (equivalent to hole injection from the semiconductor to the metal), (5) carrier generation supported by states within the forbidden bandgap [4]. The inverse processes occur under forward bias. In case the defect assisted generation current (5) is noticeable, one has to take into account: (6) hopping of carriers between localized, defect related states, (7) tunneling to and from trap states within the bandgap [5].

In an ideal Schottky-junction there is no interfacial layer between the metal and the semiconductor. However, a thin layer of native oxide usually is formed between the metal and the semiconductor, causing trap states and the current components (5) and (7). For ultrathin oxide layer or under very high electric field, tunneling will occur.

An insulator layer may also cause Frenkel-Poole emission, which dominates at high temperatures, at high fields and exists as a bulk property of the insulator.

Quantum mechanical tunneling (2), is important for heavily doped semiconductors, for operation at low temperatures or at high bias-voltages.

Furthermore, the air-semiconductor interface affects the dark current. An MSM with no passivation is more susceptible to surface oxidation and contamination through time. The leakage current increases when the surface is eroded and has many surface states [6].

Finally, the dark current is enhanced through parasitic leakage paths from the metal contacts, and high electric field regions near the tips of the electrodes [7]. The contact pads and finger tips should therefore be placed on top of an insulating layer of nitride/oxide, to reduce the tunneling and thermionic emission current in the high field regions near the extremities of the electrodes.

The MSM structure has two Schottky barriers connected back to back, so that various current transport processes may deviate considerably from that of a single Schottky diode. The applied voltage has a significant role in determining the current transport; in the following different voltage-regions are investigated for an n-type MSM PD [8].

- **Thermal equilibrium**
  The charge distribution at thermal equilibrium for an MSM PD with n-type semiconductor with ionized impurity concentration N_d is shown in Fig. 2.4(b). The corresponding electric field and

potential distribution are obtained from the integration of the Poisson's equation, Figs. 2.4(c),(d). ϕ_{Bn1}, ϕ_{Bn2} are the electron barrier heights, ϕ_{Bp1} and ϕ_{Bp2} are the hole barrier heights and V_{bi1}, V_{bi2} are the built-in potentials at contacts 1 and 2, respectively. The depletion-layer widths are:

$$W_{1,2} = \sqrt{\frac{2\epsilon_s}{qN_d} V_{bi1,bi2}} \, , \tag{2.1}$$

where N_d is the donor concentration and $\epsilon_s = \epsilon_r \epsilon_0$ is the semiconductor permittivity. For a symmetrical MSM structure (same contact metals) $\phi_{Bn1} = \phi_{Bn2} = \phi_{Bn}$, and $q\phi_{Bn1} + q\phi_{Bp2} = E_g$. Further the built-in voltage $V_{bi1} = V_{bi2} = V_{bi}$:

$$V_{bi} = \phi_{Bn} - \left(\frac{E_C - E_{Fn}}{q} \right) = \phi_{Bn} - \frac{k_B T}{q} \ln \frac{N_c}{N_d} \, , \tag{2.2}$$

where E_C is the conduction band energy level, E_{Fn} is the Fermi-level in the semiconductor, k_B is the Boltzmann constant, T is the temperature, q is the elementary charge and N_c is the effective density of states in the conduction band:

$$N_c = 2 \left(\frac{2\, \pi\, m_e^*\, k_B\, T}{h^2} \right)^{\frac{3}{2}} \, , \tag{2.3}$$

where m_e^* is the electron effective mass. At zero bias no current will flow.

- **Small voltage range $\mathbf{V < V_{RT}}$**
The small voltage range applies to voltages below the reach-through voltage V_{RT} (exact definition given in Eq. (2.13)). The charge distribution, electric field and energy band profile under low bias are shown in Fig. 2.5. The contact 1 with a negative voltage with respect to contact 2 is reverse-biased (cathode) whereas contact 2 is forward-biased (anode). qV_1 is the difference between the Fermi level of metal contact 1 to that in the semiconductor; qV_2 is the difference between the Fermi level of metal contact 2 to that in the semiconductor. $V = V_1 + V_2$ is the applied voltage shared between the two contacts.

The electron current is due to the thermionic emission of electrons from the cathode:

$$J_{n1} = A_n^* T^2 e^{-\frac{q}{k_B T}(\phi_{Bn1} - \Delta\phi_{Bn1})} \left(1 - e^{\frac{-qV_1}{k_B T}} \right) \, , \tag{2.4}$$

where A_n^* is the effective Richardson constant for electrons with the corresponding electron effective mass m_e^*:

$$A_n^* = \frac{4\pi q m_e^* k_B^2}{h^3} \, , \tag{2.5}$$

h is the Planck constant, and $\Delta\phi_{Bn1}$ is the Schottky barrier lowering or image force lowering due to the applied electric field given by:

$$\Delta\phi_{Bn1} = \sqrt{\frac{qE_{m1}}{4\pi\epsilon_s}} \, . \tag{2.6}$$

The maximum electric field E_{m1} at the cathode is:

$$E_{m1} = \sqrt{\frac{2qN_d}{\epsilon_s}(V_1 + V_{bi1} - \frac{k_B T}{q})} \, . \tag{2.7}$$

The origin of the hole current is the thermionic emission of holes from the anode:

$$J_{p2} = A_p^* T^2 e^{-\frac{q}{k_B T}(\phi_{Bp2} + V_{bi2} - V_2)} \, , \tag{2.8}$$

where A_p^* is the effective Richardson constant for holes with the corresponding hole effective mass and $\phi_{Bp2} + V_{bi2} - V_2$ is the effective barrier height. Those injected holes which diffuse from x_2 to x_1 constitute the total hole current. Generally, the hole current is much smaller than

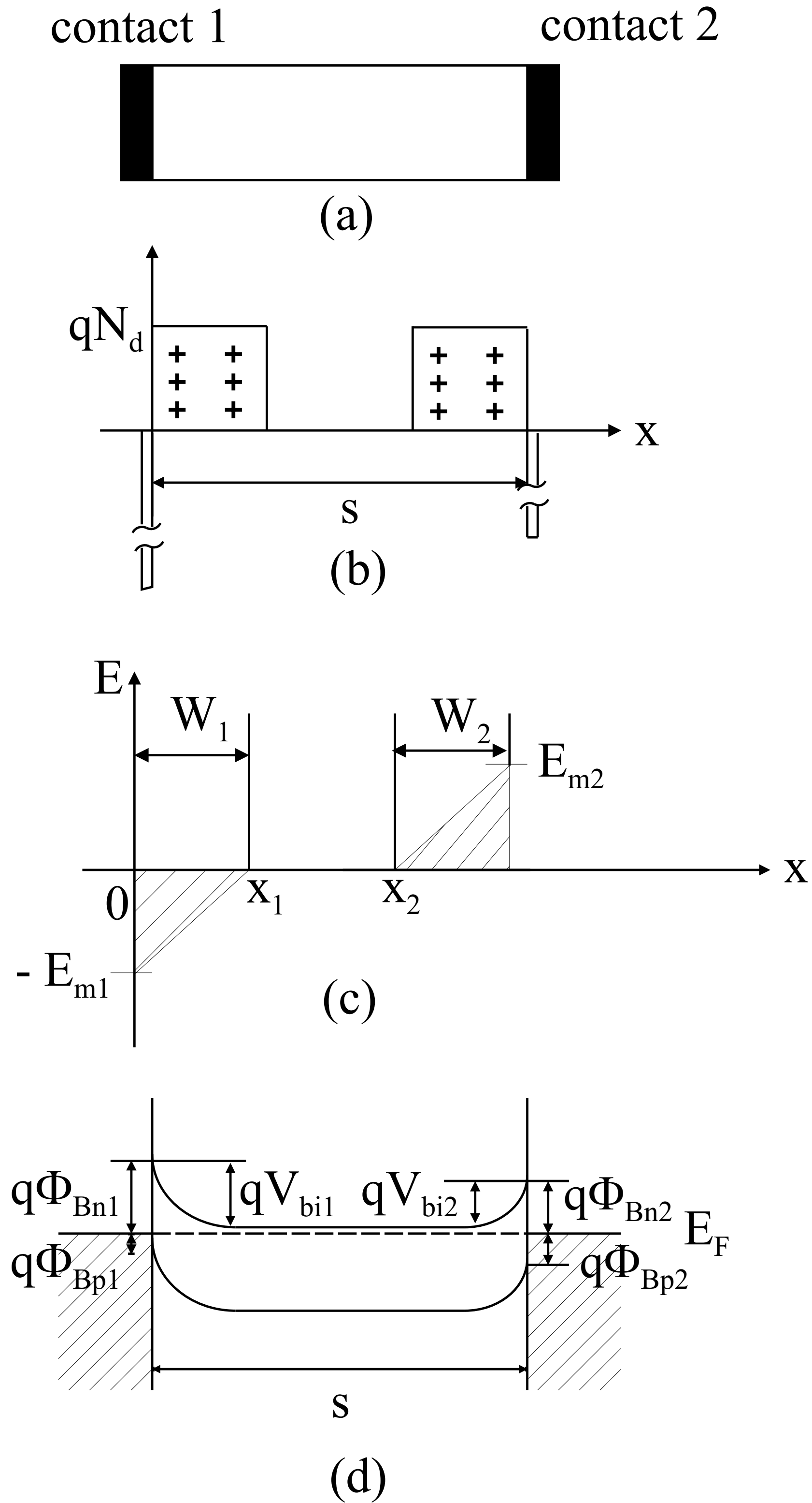

Figure 2.4: (a) Schematic diagram of an MSM structure, (b) charge distribution, (c) electric field, (d) energy band diagram at thermal equilibrium.

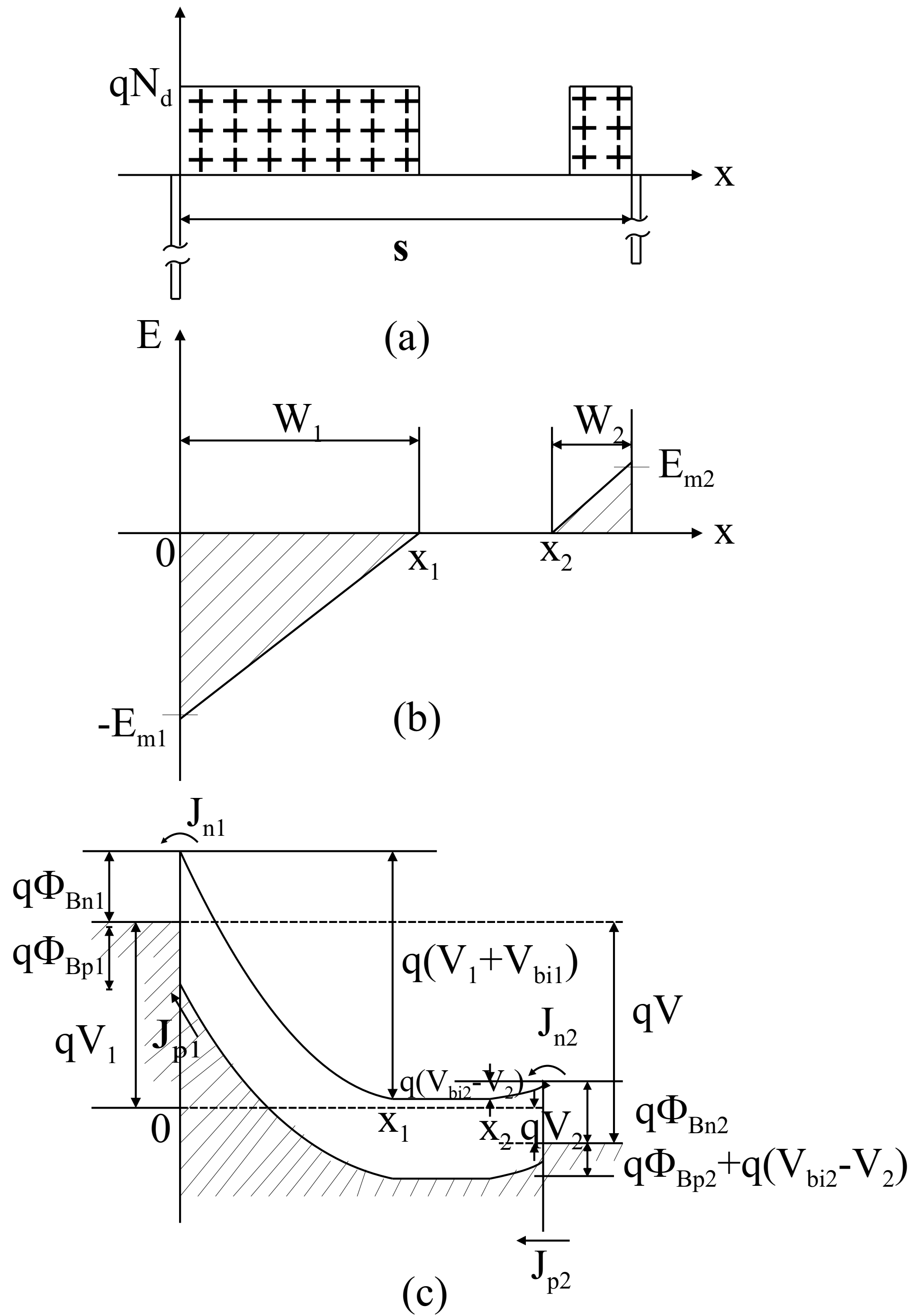

Figure 2.5: (a) Charge distribution, (b) electric field, (c) energy band diagram under bias (with negative bias on contact 1).

the electron current. Solving the current continuity equation for holes using the particle and displacement current densities, the hole current density J_{p1} at the cathode becomes:

$$J_{p1} = qD_p \frac{dp}{dx} |_{x_1}$$

$$= \frac{qD_p p_{n0} \tanh[(x_2 - x_1)/L_p]}{L_p} \left(1 - e^{-\frac{qV_1}{k_B T}}\right) + \frac{A_p^* T^2 e^{\frac{-q}{k_B T}(\phi_{Bp2} + V_{bi2})}}{\cosh[(x_2 - x_1)]/L_p} \left(e^{\frac{qV_2}{k_B T}} - 1\right) . \quad (2.9)$$

The total current is the sum of the electron- and hole-currents, Eqs. (2.4) and (2.9):

$$J_{dark} = J_{n1} + J_{p1} . \quad (2.10)$$

Under low bias the barrier for holes ($\phi_{Bp2} + V_{bi2} - V_2$) is higher than that for electrons (ϕ_{Bn1}). Therefore, the dominant current component is the reverse electron saturation current.

- **Voltages larger than the reach-through voltage $\mathbf{V > V_{RT}}$**
  By increasing the voltage, the depleted area at the cathode grows while at the anode it reduces. A small current is injected through the barriers: hole current at the forward-biased contact and electron current at the reverse-biased contact. The barrier for the holes is rapidly reduced with increasing voltage, but it is still higher than the barrier for electrons at the cathode. Therefore the total current is mainly due to electron flow. The two depletion regions touch each other at the reach-through voltage. Now the whole structure is entirely depleted. The sum of the depletion regions equals the distance between the contacts $W_1 + W_2 = s$, Fig. 2.6.

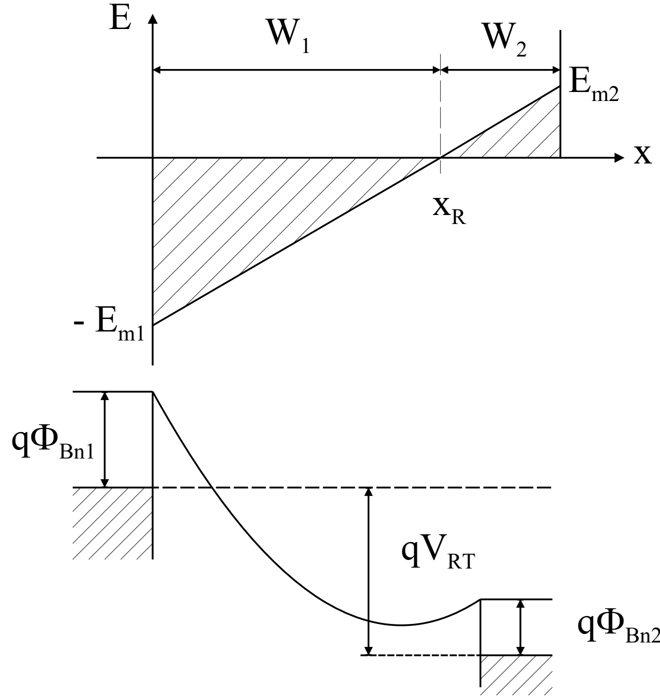

Figure 2.6: Reach-through condition (a) electric field, (b) energy band diagram.

For a symmetrical structure $V_{bi1} = V_{bi2} = V_{bi}$, so that the depletion widths are:

$$W_1 = \sqrt{\frac{2\epsilon_s}{qN_d}(V_1 + V_{bi})} , \quad (2.11)$$

$$W_2 = \sqrt{\frac{2\epsilon_s}{qN_d}(V_{bi} - V_2)} . \quad (2.12)$$

Most of the applied voltage drops across the cathode. Letting $V_1 = V = V_{RT}$ and $V_2 = 0$ in $W_1 + W_2 = s$, gives for the reach-through voltage the expression:

$$V_{RT} = \frac{qN_d s^2}{2\epsilon_s} - s\sqrt{\frac{2qN_d}{\epsilon_s}V_{bi}}\,. \tag{2.13}$$

Full depletion of the active region can occur even at zero bias, if the electrode spacing s is small enough. By setting $V_{RT} = 0$ or $W_1 + W_2 = s$ using Eq. (2.1), the spacing is defined as $s_{depleted} = \sqrt{\frac{8\epsilon_s V_{bi}}{qN_d}}$. After reach-through, the electric field is continuous and varies linearly from $x = 0$ to $x = s$, Fig. 2.7.

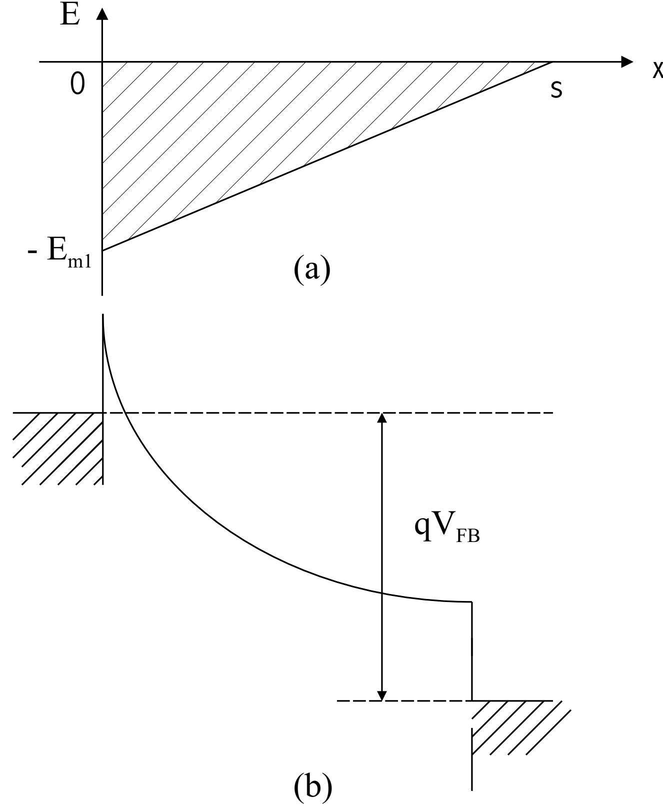

Figure 2.7: Flatband condition (a) electric field, (b) energy band diagram.

The maximum fields at the cathode and anode, respectively, are:

$$E_{m1} = \frac{V + V_{FB}}{s}\,, \tag{2.14}$$

$$E_{m2} = \frac{V - V_{FB}}{s}\,, \tag{2.15}$$

where the voltage V_{FB} is the flatband voltage which makes the depletion width at the anode $W_2 = 0$. The relation between the applied voltage and the reverse-biased/forward-biased barrier height becomes therefore:

$$V_1 + V_{bi} = \frac{E_{m1} x_R}{2} = \frac{(V + V_{FB})^2}{4V_{FB}}\,, \tag{2.16}$$

$$V_{bi} - V_2 = \frac{E_{m2}(s - x_R)}{2} = \frac{(V_{FB} - V)^2}{4V_{FB}}\,, \tag{2.17}$$

where x_R is the reach-through point (the position at which the electric field is zero): $x_R = \epsilon_s E_{m1}/qN_d = \frac{s(V+V_{FB})}{2V_{FB}}$. When the applied voltage exceeds V_{RT}, the neutral region $(x_2 - x_1)$ becomes zero and Eq. (2.9) using Eq. (2.17) reduces to:

$$J_{p1} = A_p^* T^2 e^{-\frac{q(\phi_{Bp2}+V_{bi})}{k_B T}} \left(e^{\frac{qV_2}{k_B T}} - 1 \right)$$

$$= A_p^* T^2 e^{-\frac{q\phi_{Bp2}}{k_B T}} \left(e^{-\frac{q(V_{FB}-V)^2}{k_B T 4 V_{FB}}} - e^{-\frac{qV_{bi}}{k_B T}} \right) . \tag{2.18}$$

The total current is the sum of Eqs. (2.4) and (2.18) (note that in Eq. (2.4) the second exponential term drops out, because applying a voltage V_1 it approaches zero):

$$J_{dark} = A_n^* T^2 e^{-\frac{q}{k_B T}(\phi_{Bn1} - \Delta\phi_{Bn1})} + A_p^* T^2 e^{-\frac{q\phi_{Bp2}}{k_B T}} \left(e^{-\frac{q(V_{FB}-V)^2}{k_B T 4 V_{FB}}} - e^{-\frac{qV_{bi}}{k_B T}} \right) . \tag{2.19}$$

From Eq. (2.19) it can be seen that the current increases exponentially with applied bias.

- **Voltages larger than the flatband voltage $\mathbf{V > V_{FB}}$**
As the voltage is further increased, the energy band at $x = s$ becomes flat and the electric field becomes zero. This is the flatband condition with the corresponding flatband voltage, V_{FB}. By setting $x_R = s$, the maximum field at the cathode becomes $E_{m1} = \frac{sqN_d}{\epsilon_s}$. Equalizing this with Eq. (2.14) gives for the flatband voltage:

$$V_{FB} = \frac{qN_d s^2}{2\epsilon_s} . \tag{2.20}$$

By proper selection of N_d and s, the flatband voltage can be varied from a few volts to tens of volts. Increasing the voltage in excess of V_{FB}, causes the energy band to bend further downward, Fig. 2.8.

The maximum voltage, the breakdown voltage V_{BD}, which can be applied to the MSM structure is limited by the breakdown phenomena near the maximum field at the cathode. Using Eq. (2.14) and defining the maximum field E_{m1} at breakdown as E_{BD} the maximum applicable voltage becomes:

$$V_{BD} = E_{BD}\, s - V_{FB} . \tag{2.21}$$

At $V = V_{FB}$, the factor in brackets in the hole current density, Eq. (2.18), approaches unity. The hole current reaches its critical value since the hole barrier approaches the limiting magnitude ϕ_{Bp2}. For voltages in excess of V_{FB} the hole current increases slowly due to the Schottky barrier lowering effect, i.e. the applied field reduces the barrier height. The hole current is now expressed as:

$$J_{p1} = A_p^* T^2 e^{-\frac{q}{k_B T}(\phi_{Bp2} - \Delta\phi_{Bp2})} , \tag{2.22}$$

where $\Delta\phi_{Bp2}$ is the Schottky barrier lowering for holes:

$$\Delta\phi_{Bp2} = \sqrt{\frac{qE_{m2}}{4\pi\epsilon_s}} = \sqrt{\frac{q(V - V_{FB})}{4\pi\epsilon_s s}} , \tag{2.23}$$

with E_{m2} defined in Eq. (2.15). The total current, assuming that breakdown phenomena and surface state transport can be neglected, is the sum of Eqs. (2.4) and (2.22):

$$J_{dark} = A_n^* T^2 e^{-\frac{q}{k_B T}(\phi_{Bn1} - \Delta\phi_{Bn1})} + A_p^* T^2 e^{-\frac{q}{k_B T}(\phi_{Bp2} - \Delta\phi_{Bp2})} . \tag{2.24}$$

If the injected carrier density, Eq. (2.24), is comparable to the background ionized-impurity density, the electric field in the depletion region (drift region) will vary due to the mobile carriers. This space-charge effect limits the current flow, resulting in a current density defined as $J_{dark} = \frac{2\epsilon_s v_s V}{s^2} = \frac{qv_s N_d V}{V_{FB}}$.

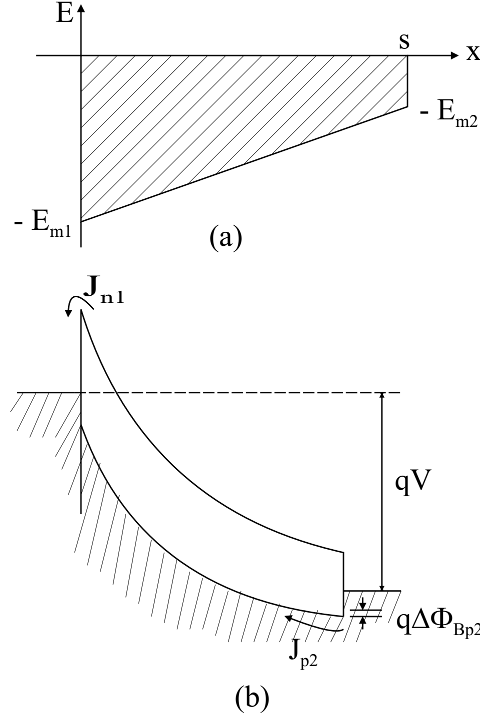

Figure 2.8: Applied voltage larger than V_{FB} (a) electric field, (b) energy band diagram.

In many MSM PDs DC-gain may occur indicating the existence of other current transport mechanisms. The DC-gain can be modelled using tunneling current, which is enhanced in the presence of excess carriers [9]:

$$J_{tun} \propto E^2 e^{\frac{-4\sqrt{2m^*}(q\phi_{Bn})^{3/2}}{3q\hbar E}} \propto V^2 e^{-\frac{B}{V}} \; , \tag{2.25}$$

where E is the electric field across the semiconductor or insulator, m^* is the effective mass, $V = Ed$ and d is the thickness of the tunneling area (semiconductor or insulator).

2.2.2 Noise

In receiver design a significant parameter is the signal-to-noise ratio, which is mainly formed by the front-end of the circuitry, i.e. the noise spectral density of the detector and the amplifier. It is important quantitatively to investigate the possible effects causing the dark current and thus noise, and to predict the limitations of MSM photodetectors. For the leakage current of an MSM PD, the biasing condition (discussed in Section 2.2.1), temperature, surface passivation, and the combination of the contact metal and the semiconductor material play a significant role.

The spectral density of the noise current source $< i_{rms}^2 >$, [A^2/Hz], can be defined as:

$$\frac{< i_{rms}^2 >}{\Delta f} = \frac{4k_BT}{R_{dark}} + 2qI_{dark} \; , \tag{2.26}$$

where R_{dark} refers to the equivalent resistance obtained from the slope of the dark current I-V curve at the bias point, I_{dark} is the dark current at the bias point, T is the equivalent resistor temperature assumed to be 290 K and Δf is the integral of the normalized transfer function of the detector. The noise equivalent power (NEP) can be calculated from the noise current: $NEP = \frac{i_{rms}}{R}$, where R is the measured responsivity. Further, NEP can be used to define the normalized detectivity: $D^* = \frac{A\Delta f}{NEP}$, where A is the area of the detector. The NEP of a 3 x 3 (finger spacing and width) GaAs and AlGaAs/GaAs MSMs with the contact pads and electrode tips on top of an isolating nitride was found

to be 26.9 nW and 8.12 nW, respectively. These values of NEP correspond to a normalized detectivity of 2.2 $\cdot 10^{10}$ and 7.32 $\cdot 10^{10}$ cm$\sqrt{\text{Hz}}$/W[7], respectively.

Investigations imply that for a GaAs MSM PD the noise at low bias (V $<$ 25 V) is caused by the photocurrent shot noise ($\simeq 2qI_{ph}$). In the voltage range of 25 - 45 V excess noise is associated with the photocurrent gain: spectral density of the mean-square noise current is expressed as $= 2qI_{po}G_i^2F(G) \simeq I_{ph}^{3.6}$, where G_i is the photocurrent gain, I_{po} is the unity gain photocurrent and $F(G)$ is the excess noise factor. When the voltage exceeds 45 V, the dark current dominates the total current so that noise is produced by the dark current shot noise [10]. In Ref. [11] a GaInAs MSM PD showed at high bias (close to breakdown) excess low-frequency noise, varying as $1/f$. This is related to traps at the Schottky interface and traps within the barrier layer. Above the cut-off frequency f_c, the detectors performance was limited by only shot noise (at frequencies above 1 MHz).

2.2.3 Responsivity

DC Responsivity

The responsivity of an MSM PD is the ratio of the photogenerated current to the incident illumination with an optical power corresponding to a photon energy $h\nu$ at the wavelength λ:

$$R = \frac{I_{ph}}{P_{opt}} = \frac{q\,\eta\,G_i}{h\nu} = \frac{\lambda\,\eta\,G_i}{1.24\cdot 10^{-6}}\ , \tag{2.27}$$

where η is the quantum efficiency of the device and G_i is the internal gain. The quantum efficiency for an MSM diode is expressed as:

$$\eta = \eta_i(1-r)(\frac{s}{s+w})(1-e^{-\alpha d})\,, \tag{2.28}$$

where η_i is the internal quantum efficiency, r is the reflection coefficient at the air-semiconductor interface depending on the material and the wavelength, α is the absorption coefficient as a function of wavelength, d is the thickness of the active region, and s and w are the spacing and width of the fingers, respectively.

For an ideal MSM PD the internal quantum efficiency, which is defined as the number of electron-hole pairs generated per incident photon and collected at the electrodes, equals unity. However, if multiplication mechanisms are present, the number of collected carriers increases, and the internal quantum efficiency exceeds 100 %, thus giving rise to G_i. In case no gain is present, the theoretical responsivity is $R \leq \frac{\lambda\,\eta}{1.24\cdot 10^{-6}}$ A/W. The limiting wavelength for photoexcitation comes from the forbidden energy gap E_g: $\lambda \leq \frac{hc}{E_g}$.

In order to optimize the responsivity of an MSM PD, different factors contributing to the quantum efficiency are investigated in the following.

(1) Optical absorption
The wavelength-dependence of the responsivity is significant since the photon wavelength determines the absorption of light into the semiconductor. The light passing through the device decreases exponentially according to $e^{-\alpha x}$, where x is the distance measured from the surface of the semiconductor. Thus, the amount of absorbed light is determined by the factor $(1-e^{-\alpha x})$.

The penetration depth of light into the semiconductor, i.e. $\gamma = 1/\alpha$, as a function of wavelength for Si and GaAs is plotted in Fig. 2.9 (calculated using α from refs. [12] and [13]). It can be seen that the absorption strongly depends on the wavelength, with a sudden increase of γ at energies below E_g = 1.12 eV ($\lambda >$ 1107 nm) for Si, and energies below E_g = 1.42 eV ($\lambda >$ 873 nm) for GaAs.

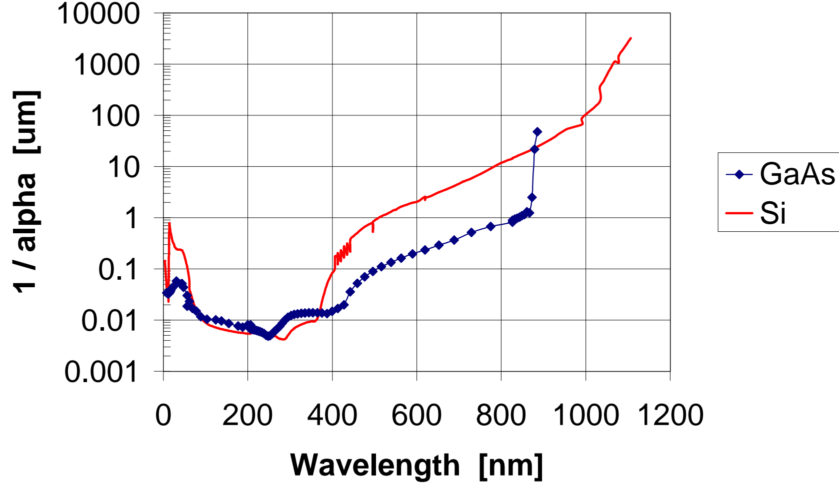

Figure 2.9: Penetration depth of light in Si and GaAs as a function of λ.

(**2**) **Reflection**
In practice only a fraction of the incident beam reaches the active area of the photodetector. The reflection coefficient at the air-semiconductor interface for an incident light coming perpendicular to the surface is:

$$r = \left[\frac{n_r(\lambda) - n_{air}}{n_r(\lambda) + n_{air}}\right]^2 , \tag{2.29}$$

where $n_{air} = 1$ for air, and n_r is the refractive index of the semiconductor [14].

In Fig. 2.10 is calculated the reflection coefficient at the semiconductor/air-interface for Si and GaAs as a function of optical wavelength (calculated using n_r from refs. [12] and [13]).

In order to minimize reflection and thus improve sensitivity an antireflection coating (ARC) can be used. An ARC also prevents surface oxidation and hence decreases the dark current. To obtain zero reflection at the air/ARC-interface, a quarter-wavelength matching can be applied, i.e. the thickness of the coating $d_{ARC} = \frac{\lambda_{ARC}}{4} = \frac{\lambda_{air}}{4\sqrt{\epsilon_{ARC}}} = \frac{\lambda_{air}}{4\, n_{ARC}}$, where $n_{ARC} = \sqrt{n_r\, n_{air}}$. Thermal oxide for Si and silicon nitride (SiN) for GaAs can for instance be used as an ARC.

Surface-reflection is avoided, if the MSM PD is integrated with a waveguide. The external responsivity of a waveguide-coupled MSM PD can be optimized by varying the detector length along the light propagation direction and by controlling the degree of coupling between the waveguiding and absorbing layer [15]. The responsivity of a waveguide-integrated MSM PD was 0.25, 0.45 and 0.5 A/W for a 75, 150 and 300 μm long detector, respectively [16].

(**3**) **Electrode shadowing**
The metal of the electrodes directly affects the responsivity. In case of opaque electrodes, the fraction of light that will reach the semiconductor surface is the ratio of the finger spacing to the pitch: $(\frac{s}{s+w})$. If transparent electrodes are used blocking of incident light by the metal fingers is reduced and more light is allowed to enter the active area. The efficiency can thus be enhanced. The high sensitivity is also due to the fact that a transparent material acts as an ARC on the substrate which reduces the ~ 35 % Fresnel reflections that can occur at the surface of an uncoated substrate [17].

Examples of sensitivity enhancing electrodes include transparent indium-tin-oxide (ITO), cadmium tin oxide (CTO) and semitransparent thin Au and Pt electrodes [18] - [22]. Light permeable ITO Schottky contacts exhibit a relevant absorption in the 1.3 - 1.55 μm wavelength region.

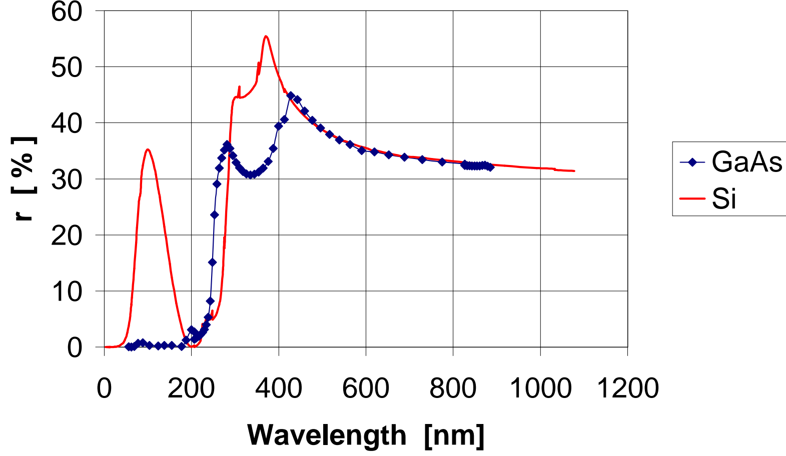

Figure 2.10: Reflection coefficient for Si and GaAs as a function of λ at the air/semiconductor interface.

In detectors based on transparent electrodes photo-generation of carriers in the region below the electrodes suffer from long transit times (slow drift velocities), since the electric field strength is lower underneath the contacts than elsewhere. The series resistance is also increased if the metal thickness is very low. For instance, Au electrodes which are transparent up to less than 10 nm, introduce a series resistance in the order of several MΩ for a usable device geometry, thus increasing the RC time constant and decreasing the overall device speed. However, both high speed and high sensitivity have been achieved with ITO InAlAs/InGaAs MSM PDs: responsivity of 0.55 - 0.6 A/W at 1.31 μm, 0.563 - 0.583 A/W at 1.55 μm, and a 3 dB bandwidth of 19 GHz (bias 5V) and 25 GHz (10 V) at 1.55 μm [18].

The responsivity, assuming zero reflection and neglecting electrode shadowing, is plotted for Si and GaAs for different device thicknesses in Fig. 2.11 (calculated using α from refs. [12] and [13]). Quantum efficiency without antireflection coating (i.e. r defined in Eq. (2.29)), and neglecting electrode shadowing is plotted for Si and GaAs for different device thicknesses in Fig. 2.12 (calculated using α and n_r from refs. [12] and [13]).

The spectral response depends mainly on three factors, like already discussed in the previous: the thickness of the photoactive layer, the electrode coverage and the surface reflection:

- **(1)** If transparent metallization is applied together with an ARC ($r = 0$), the responsivity is defined as:
  $R = \frac{q\lambda}{hc}(1 - e^{-\alpha d})\eta_i$.
- **(2)** If the metallization is opaque and an ARC is deposited the responsivity becomes:
  $R = \frac{q\lambda}{hc}(1 - e^{-\alpha d})\eta_i(\frac{s}{s+w})$.
- **(3)** In case of opaque metallization and without an ARC the expression for the responsivity is:
  $R = \frac{q\lambda}{hc}(1 - e^{-\alpha d})\eta_i(\frac{s}{s+w})(1 - r)$.

These three different situations are calculated for Si and GaAs in Fig. 2.13 for different device thicknesses (η_i is set to 1, $s/s+w$ equals 0.5, r is according to Eq. (2.29), and α and n_r are from refs. [12], [13]). It is clearly seen, that for Si the thickness of the optically active layer is more crucial, i.e. the responsivity drops significantly more for thin device thicknesses compared to GaAs. This is attributed to the smaller absorption coefficient of Si in contrast to GaAs. For GaAs device thicknesses of 0.5 μm and 1 μm are chosen, because these layer thicknesses are used in the photoreceiver circuits for the

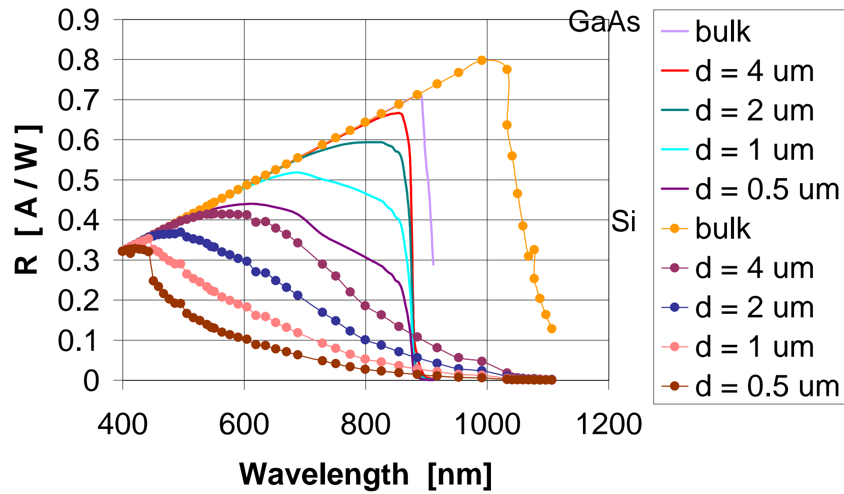

Figure 2.11: Responsivity with antireflection coating (i.e. $r = 0$) and neglecting electrode shading for Si (dotted lines) and GaAs (solid lines) as a function of λ for different device thicknesses.

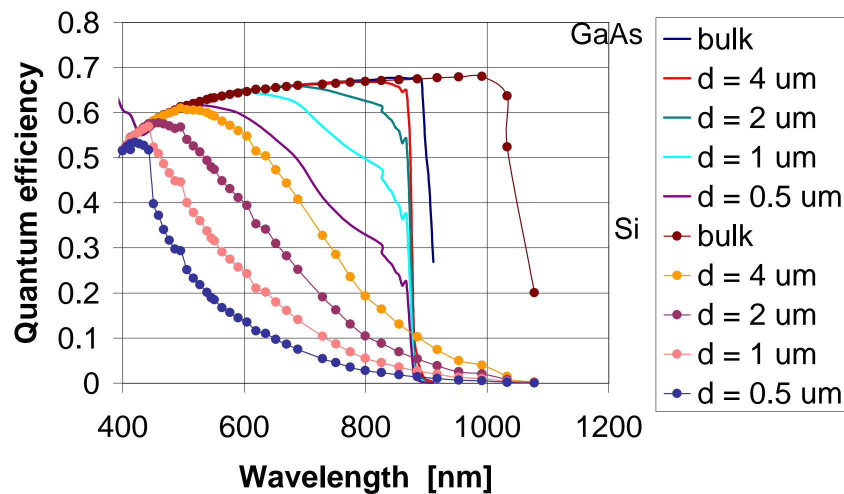

Figure 2.12: Quantum efficiency η for Si (dotted lines) and GaAs (solid lines) without antireflection coating (i.e. $r = [(n_r(\lambda) - 1)/(n_r(\lambda) + 1)]^2$) and neglecting electrode shading as a function of λ for different device thicknesses.

active layer of the MSM PDs (Chapter 4). The bulk GaAs plots give an estimation for the MSM PDs fabricated on semi-insulating GaAs (investigated in Section 2.5.3). For Si in addition to bulk Si detectors structures with thicknesses of 0.2 μm and 4 μm are presented in the figure, due to SOI MSM PDs studied with these dimensions in Section 2.5.3.

Other approaches to increase responsivity include backside illumination, using a 2DEG layer structure, manufacturing a photodetector with bottom-electrodes, or burying the electrodes in its light-absorbing layer [21], [23], [24]. Backside illumination requires substrate thinning or backside etching to avoid excess loss of signal power, or the use of a glass substrate. By using semitransparent electrodes and inserting a two dimensional electron gas (2DEG) in the layer structure leads to enhanced responsivity and to no reduction in the bandwidth. In addition, to achieve uncomplicated interfacing between optical fiber and the OEIC, light sensitive areas with circular geometry are proposed [25]. An InGaAs circular shaped MSM, with quasi-circular (double spiral) or semi-circular 0.3 - 5 μm finger electrodes, has demonstrated polarization-insensitive operation at a wavelength of 1.3 μm [26].

AC Responsivity

The AC responsivity is usually lower than that obtained at DC conditions. It can be obtained by exciting the detector with pulsed laser beam illumination. The responsivity at high frequencies is calculated by integrating the impulse response and dividing by the load resistance, giving the number of photocarriers during a single pulse. Dividing this by the pulse energy, which is the average power divided by the repetition rate of the pulse, yields the responsivity.

Low frequency responsivity can be achieved by chopping the light source with different frequencies. In [27] it was shown that at low frequencies the responsivity was considerably larger than at higher frequencies (i.e. comparing 15 Hz with 1 kHz). E.g.: at $\lambda = 500$ nm and 15 Hz the responsivity was 1.25 A/W, whereas at the same wavelength at 1 kHz it became only 0.22 A/W. The high response at 15 Hz is mainly a result of low-frequency gain. The difference between 15 Hz and 1 kHz-responsivities became smaller for lower photon energies.

2.2.4 Speed of Response

For fast operation of the detector, the carriers should move with maximum velocity. To ensure maximum velocity, an electric field exceeding the critical field E_c must be applied. The carrier velocity depends on the applied electric field E as follows [28]:

$$v = \frac{\mu_0 E + v_s \left(\frac{E}{E_c}\right)^4}{1 + \left(\frac{E}{E_c}\right)^4} , \tag{2.30}$$

where it is assumed that the maximum velocity is the saturation velocity v_s. At low fields, $E < E_c$, Eq. (2.30) reduces to: $v = \mu_0 E$; the velocity increases linearly with the field with constant mobility. At high fields, $E \geq E_c$, the velocity is independent of the field; Eq. (2.30) becomes $v = v_s$.

For Si the drift velocity reaches the saturation velocity $v_s = 10^7$ cm/s at fields above $5 \cdot 10^4$ V/cm. For GaAs, the drift velocity first reaches a peak value and then decreases toward $v_s = 6 - 8 \cdot 10^6$ cm/s [9].

The minimum voltage V_{min}, at which carriers experience a field of at least E_c from contact to contact (s = spacing) is defined as:

$$V_{min} = E_c\, s + V_{FB} . \tag{2.31}$$

The optimum bias for the MSM PD, such that breakdown is avoided, lies thus in the range $V_{min} < V < V_{BD}$, where V_{BD} is defined in Eq. (2.21).

The rise time of the transient response is primarily due to larger drift velocity of electrons, but the total bandwidth depends on the time to sweep the slower moving holes out of the absorption region. The fundamental response for a GaAs-based MSM PD is found to consist of three components: a fast initial peak due to velocity overshoot in the Γ valley electrons, a slow secondary steady state electron response, and a slow steady state hole response. The relative magnitude of the two electron responses is sensitive to the device length, the electric field and the energy of the exciting photons. The hole transit time decreases monotonically with increasing electric field [29].

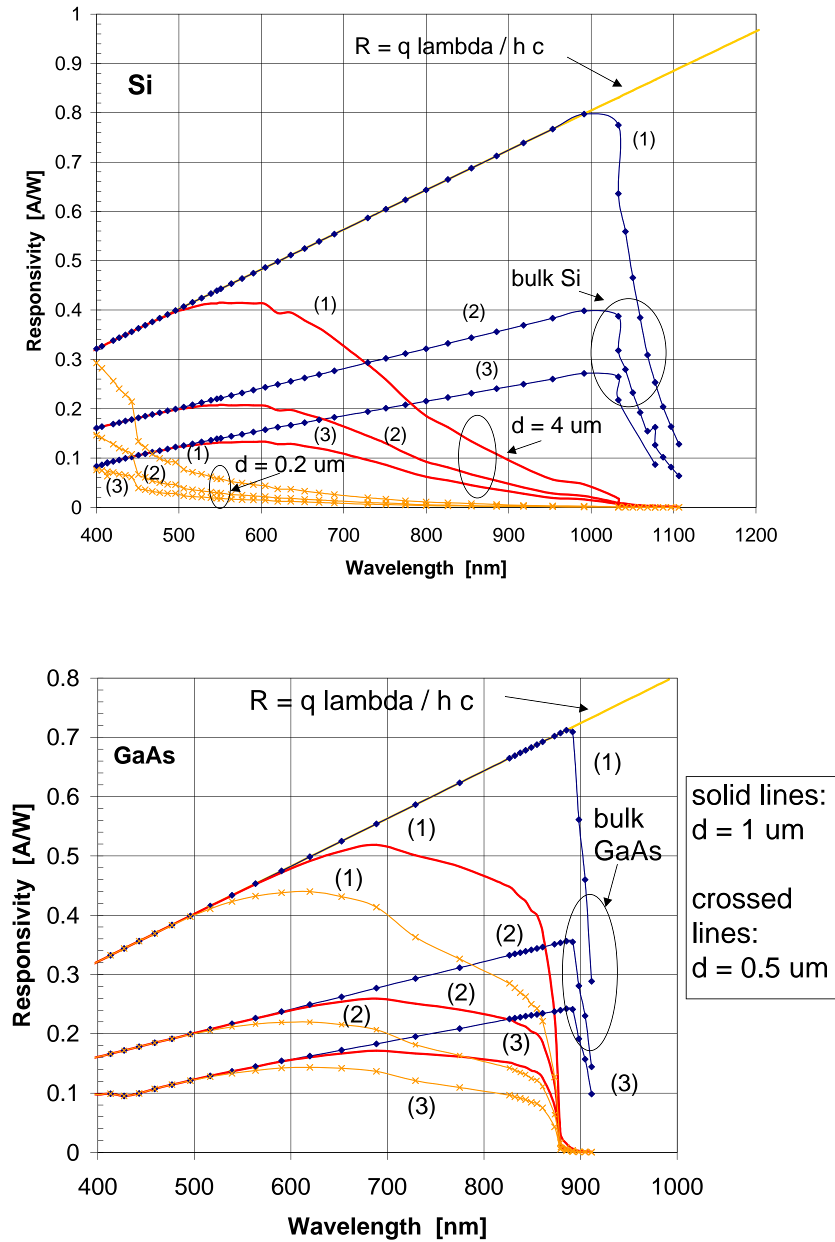

Figure 2.13: Responsivity as a function of wavelength for Si and GaAs with different device thicknesses. Also is presented the theoretical limit: $R = \eta q\lambda/hc$ with η =1. Numbers (1) -(3) are explained in the text on p. 17.

Intrinsic Response

The intrinsic dynamical behaviour of MSM PDs can be classified according to whether their speed is limited by the carrier *transit time* between the fingers or the carrier *recombination time*.
The average transit time of the generated carriers τ_{tr} ($< s >= s/2$ being the average transit distance) is estimated by:

$$\tau_{tr} = \frac{s}{2v_d} , \tag{2.32}$$

where v_d accounts for the drift velocity of electrons and holes ($v_d = 1/2(v_e + v_h)$). In practice, the applied bias is such that the obtained electrical field between the small finger spacings is high enough to move the carriers with their saturation velocities.

In *recombination time limited* detectors a high density of recombination centers is introduced into the semiconductor, leading to decreased carrier lifetime and thus enhanced speed. On the other hand responsivity is drastically decreased due to reduced carrier mobility and short carrier recombination time. *Transit time limited* detectors, fabricated on high-quality semiconductors, usually exhibit a sensitivity several orders magnitude higher, but on the contrast slower speed than recombination time limited MSM PDs. A benefit of transit time limited detectors is their compatible fabrication technology with FET-fabrication.

To improve the transient response, electron beam lithography technique allows the fabrication of nanoscale finger structures. The shorter finger spacing causes shorter intrinsic response time for the transit time limited detectors and higher responsivity for the recombination time limited devices. Nanoscale finger spacing increases the speed due to the ballistic transport (finger spacing becomes comparable to the mean free path, electrons encounter less scattering), and very high electric field between the fingers at a low bias can be achieved.

In order to enhance the transient response, many methods in addition to submicrometer technology can be utilized: low-temperature grown GaAs (LT GaAs), ion-implantation of the absorbing layer, depositing a thin amorphous layer on crystalline Si [30] or a SOI-structure [31]-[34].

• **LT/IGT GaAs**

MSMs based on low-temperature-grown GaAs (LT-GaAs) achieve high recombination time limited speed, but at the expense of low quantum efficiency. Defect density, mobility and dark current are affected by the growth temperature. Low-temperature (LT, 200 °C) GaAs exhibits an optical responsivity by a factor of two and four less than conventional-growth-temperature GaAs and Si, respectively [35]. The high speed of LT-GaAs-detectors is due to excess As in the lattice creating a large surplus of point defects. The point defects form midgap trap states, which act as short lifetime recombination centers. For LT-GaAs PDs (spacing and width 300 nm) the speed was noticed to be limited by the recombination time, yielding a full width at half maximum ($FWHM$) of only 0.87 ps with a 3 dB bandwidth of 0.51 THz [36].

Results suggest that intermediate-growth-temperature (IGT, 350 °C) GaAs gives an optimal combination of very low dark current, moderate photocurrent and bandwidth: for a 3 μm spacing device at a bias of 10 V the dark current density was measured to be 0.56 μA/cm^2, responsivity was 0.18 A/W and the $FWHM$ showed 86 ps (4 GHz bandwidth) [37]. The IGT-GaAs tailors the carrier lifetime in the material, so that the lifetime is proportional to the transit time between the electrodes. In [38], for IGT-GaAs 130 mV/pJ and a bandwidth of 6.2 GHz were measured. The photocurrent/dark current ratio of $7 \cdot 10^3$ was significantly larger than for normal growth temperature or LT-GaAs MSMs.

• **Amorphous Si**

MSM PDs based on hydrogeneted Si are attractive in many respects. In amorphous Si (a-Si) a large amount of localized band-tail states and midgap-states exist, which act as trapping and recombination centers. Due to the high density of defects and thus short carrier lifetime, an MSM PD on a-Si may achieve high speed. The possibly appearing tail in the impulse response may also be reduced due to the fast recombination time. In a-Si the lack of long-range periodicity relaxes the k-selection rule for the optical transition, the bandgap becomes direct and the optical absorption coefficient is thus large. Only a thin photoactive layer is needed to obtain better quantum efficiency compared to that of crystalline Si. In addition, the dark current is improved since i-a-Si:H (intrinsic hydrogenated amorphous Si) has a higher optical gap of 1.4 - 1.8 eV than that of 1.12 eV for c-Si [39]. The low dark current can also be attributed to the high dark resistance, i.e. the Schottky barrier height. Pt metal deposited on a-Si and c-Si demonstrated barriers of 1.1 eV and 0.8 eV, respectively [40]. In [30] an MSM with a 300 nm

thick i-a-Si:H layer grown on top of a quartz glass substrate ($s = w = 3\ \mu$m, $A = 100 \times 100\ \mu m^2$, Ni/AuGe metallization), exhibited a dark current of 1 nA at 5 V, and 28 nA at 50 V.

Detectors having a thin 70 nm i-a-SiGe:H (intrinsic amorphous hydrogenated silicon germanium) deposited on crystalline Si (resistivity 4 kΩcm) with Cr-metallization have shown high speed, good responsivity and low dark current: rise time of 21 ps, $FWHM$ of 51 ps, responsivity of 0.32 A/W at 850 nm and a dark current density of 40 $\mu A/cm^2$ [41].

- **SOI**

The Si-based detector, fabricated on a SOI-structure, is an interesting device to be studied, due to its high-speed impulse response in the infrared, i.e. 750 nm - 950 nm. Using bulk Si as the photoactive material large bandwidth is not achievable in the infrared because Si has an indirect energy bandgap and thus a low optical absorption coefficient. Since the absorption length for Si in the infrared is long (11.8, 18.5, 28.1 μm at wavelengths of 800, 850, 900 nm, respectively [12]) a large portion of carriers are generated far below the depletion region, where the electric field strength is low. The deep carriers are collected through diffusion rather than drift, resulting in a reduction of the bandwidth. In order to eliminate the deep carrier generation, MSM PDs fabricated on silicon-on-sapphire (SOS) or silicon-on-insulator (SOI)- substrates are suggested (see cross section picture of a SOI PD in Section 2.4.1, Fig. 2.26). In a SOI structure, a thin top Si layer is separated by a layer of buried oxide from the bulk Si substrate. The carriers generated in the lower Si can not diffuse across the $Si0_2$ barrier. Since the top-Si layer limits the depth of photogenerated carriers, a weak dependence on the wavelength should also be achieved.

A 200 nm SOS-structure showed a $FWHM$ of 4.5 ps and 5.7 ps at wavelengths of 400 nm and 720 nm, respectively [42]. A SOI-structure with a top-silicon layer of 100 nm (100 nm finger spacing and width) has resulted in a $FWHM$ of 3.2 ps and a bandwidth of 140 GHz at 780 nm [43].

There is, however, a severe trade-off between speed and responsivity in using nanometer-scale active layers. Since only a small part of the light is absorbed, the efficiency of a SOI-detector may be more than an order of magnitude lower than that of a bulk-based MSM PD. Roughening/texturizing the front surface or the backside of the active layer causes trapping of light inside the active layer through random scattering, thereby enhancing the efficiency [44], [45]. One possibility is also the use of a reflector underneath the active layer. A SOI MSM PD with a patterned nanometer-scale scattering reflector buried underneath a 170 nm thick Si active layer resulted in a $FWHM$ of 5.4 ps at 780 nm (corresponding to 82 GHz) and a responsivity of 0.29 A/W at 633 nm (external efficiency 57 %) [46]. The obtained responsivity for this device was 19 times larger than that for a detector without the reflector (15 mA/W). In [47] a novel SOI MSM PD with trench structure was introduced. Reactive ion etching was used to form electrodes inside the interdigitated trenches. In addition to isolating carriers generated deep inside the semiconductor substrate, this structure provides a highly uniform electric field throughout the active region of the detector. A trench-structure has also been proposed for a GaAs-based MSM PD, resulting in $FWHM$ of 31 ps and 50 % improvement in the peak amplitude of the temporal response at 5 V bias [48].

External Response

The detectors external speed is affected by the charge-up time of the diode, i.e. extrinsic parasitics. If the *RC-time constant* is longer than the transit time or the recombination time, the detector's speed is limited by this constant. R is composed of the externally applied load resistance, increased by the detectors series resistance. It is preferable to use shorter fingers and thicker metal, Eq. (2.68), in order to reduce the metal finger resistance. In practice, the resistance of the metal fingers is not significant since it is much smaller than the load resistance and the transmission line impedance. The dark capacitance of the detector discussed in Section 2.3.3, Eqs. (2.62), (2.66) and Fig. 2.19, indicate that for a given detector area and finger pitch, the smaller the finger width the smaller is the detector's total capacitance. Or alternatively the less fingers, i.e. maximizing the pitch $(s + w)$ leads to a decreased total capacitance. Bulk-GaAs nanoscale RC-time-limited PDs (spacing and width of 100 nm) have resulted in a $FWHM$ of 1.5 ps and 3 dB bandwidth of 300 GHz [35].

Electric Field Contribution to the Speed

An analytical expression for the distribution of the two-dimensional electric field inside the MSM can be determined through conformal mapping [49], [50]. The electric field reaches its maximum value at the metal-semiconductor interface, and decays when penetrating deeper into the substrate. The results indicate that the electric field penetrates much less inside the active region for an MSM with small contact separation [51], [52]. E.g. 2D simulations show that the electric field of 0.1 V/μm is at about 5 μm depth inside a 4 μm MSM PD and at only 1.4 μm depth for a 0.5 μm MSM PD at the same bias of 4 V. This has an effect on the charge velocities: electrons are collected quite quickly because they have high drift velocities both in the high and low field region whereas holes are collected much more slowly because the local electric field in the interior is almost everywhere too weak for holes to reach the saturation velocity. Therefore, in the impulse response the current peak is due to the electrons and the tail-part due to holes. Since the total impulse response is influenced by the slow current component of holes, the speed can significantly be increased by eliminating the hole current. In MSM devices, to take full advantage of small finger spacing, the generation of the carriers should be restricted to a thin surface region.

Frequency Response

The electrical time constant of a RC-circuit $\tau_{RC} = RC$, and the corresponding cut-off frequency is defined as:

$$f_{RC} = \frac{1}{2\pi RC} \ . \tag{2.33}$$

Considering an intrinsically transit-time limited detector, the time constant τ_{tr}, defined in Eq. (2.32), gives for the cut-off frequency the expression:

$$f_{tr} = \frac{1}{2\pi\tau_{tr}} \ . \tag{2.34}$$

The combined time constant $\tau = \sqrt{\tau_{RC}^2 + \tau_{tr}^2}$ gives the total bandwidth f_{3dB} in the form:

$$f_{3dB} \simeq \frac{1}{2\pi\sqrt{(RC)^2 + \tau_{tr}^2}} \ . \tag{2.35}$$

For optimal response speed the detector is neither RC nor transit time limited: $\tau_{tr} = \tau_{RC}$. In practical cases, the finger separation should be small and the applied bias high enough to reach carrier saturation velocity, hence achieving minimum transit time. In addition, the detector area should be minimized for a small capacitance value. The 3 dB bandwidth can also be calculated from the measured full width at half maximum. Illuminating the detector with an impulse with Gaussian characteristics, the bandwidth and the duration of the resulting pulse are related by [53]:

$$f_{3dB} = \frac{0.44}{FWHM} \ . \tag{2.36}$$

The bandwidth achieved from Eq. (2.36) is consistent with direct Fourier transform of the time domain response of the detector if there is no tail in the response (i.e. Gaussian characteristics). In case a tail exists, caused by the slowly moving holes, this definition is an overestimation of the bandwidth. An estimation for the 3 dB bandwidth is also achieved from the measured rise time. For an exponential rise with small overshoot (≤ 5 %), the bandwidth becomes [54]:

$$f_{3dB} = \frac{0.35}{t_r} \ . \tag{2.37}$$

For overshoots of 10 % the factor in the numerator is 0.45. Eq. (2.37) is also misleading unless the impulse response is free of any tailing effects. Reliable results of the bandwidth are therefore solely obtained with measurements in the frequency domain or through Fourier transforms.

Eqs. (2.36) and (2.37) account for the total system response, incorporating the excitation and detection time constants (e.g. laser, fiber and detector). In a practical measurement, the measured $FWHM$ or rise time has to be determined from the quadratic sum of the individual pulse durations/rise

times. The measurement setup, including bias-Ts, cables, probe heads and connectors, all contribute to the measured pulse shape and -times. These external factors need to be taken into account in order to obtain the intrinsic device $FWHM$ or rise time:

$$t_r^2(\text{measured}) = t_r^2(\text{laser}) + t_r^2(\text{probe}) + t_r^2(\text{cable}) + t_r^2(\text{bias} - \text{T}) + t_r^2(\text{msm}) \ . \quad (2.38)$$

Due to the trade-off between sensitivity and speed, a common figure of merit used is the efficiency-bandwidth product: ηf_{3dB} (η is expressed in Eq. (2.28)). Taking the gain-mechanisms of the detectors into consideration, the definition becomes: $\eta G_i f_{3dB}$.

The transit time as well as the RC- time limited cut-off frequency is presented for Si and GaAs MSM detectors in Fig. 2.14; the calculations are based on Eqs. (2.33) and (2.34). The resultant total bandwidth is also shown, Eq. (2.35). An area of A = 50 x 50 μm^2 was used with equal finger spacings and widths. The capacitance was calculated using 2D conformal mapping theory (Eq. (2.66) in Section 2.3.3), and the resistance R was set to a load resistance value of 50 Ω. To be very accurate the total resistance should in addition to the load resistance account for the series resistance of the finger structure. The finger resistance depends on the length of the fingers, the total area and pitch (i.e. number of fingers), and the metal height (Eq. (2.68) in Section 2.3.3). Using thick metal, e.g. Ti (50 nm) /Au (250 nm) like in this work for GaAs diodes, equal spacing and width and a squared area the resistance is only 0.4 Ω, and can thus be omitted. The high field drift velocity (i.e. the saturation velocity) used was: $7 \cdot 10^4$ m/s ($E = 10^5$ V/cm) and $1 \cdot 10^5$ m/s ($E > 4 \cdot 10^4$ V/cm) for GaAs and Si, respectively [9].

For Si detectors slightly higher frequencies can be obtained, due to higher velocity at high electrical fields (shorter transit time), and lower permittivity (lower capacitance).

It can be noticed that for large finger spacings/widths the resultant bandwidth is only limited by the transit time, whereas for finger spacings less than 1 μm the bandwidth becomes limited by the RC time constant. Therefore, in order to enhance the frequency in the submicron range, the capacitance should be minimized: by reducing the active area, decreasing the finger width for a fixed pitch and/or increasing the pitch (see Eqs. (2.62) and (2.66) in Section 2.3.3).

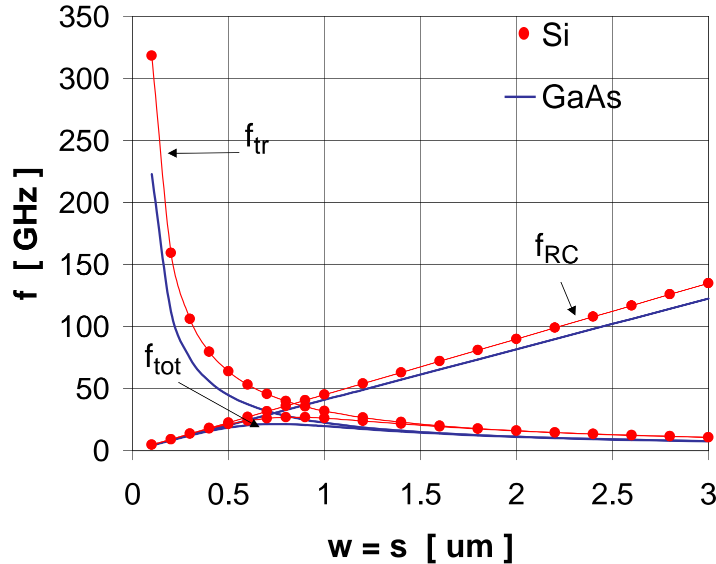

Figure 2.14: f_{RC}, f_{tr} and the total f_{3dB} for Si and GaAs MSM PDs as a function of finger spacing and width. A = 50 x 50 μm^2 (saturation velocity).

The area of the detector affects the capacitance, and thus the RC-time limited cut-off frequency. For smaller areas the capacitance is obviously less (keeping the finger width and spacing constant),

and the corresponding f_{RC} increases. This is confirmed in Fig. 2.15, which also shows the transit time limited frequency, and the total bandwidth for different detection areas for both Si and GaAs. Now the peak velocity is used for GaAs; showing that GaAs-detectors exhibit a higher bandwidth (for GaAs $2 \cdot 10^5$ m/s ($E = 3 - 4 \cdot 10^3$ V/cm) and Si $1 \cdot 10^5$ m/s ($E > 4 \cdot 10^4$ V/cm)). It is interesting to notice that for smaller areas the achieved total bandwidth not only increases, but shows a clear peak (at the point where $\tau_{tr} = \tau_{RC}$), which shifts further towards smaller dimensions with decreasing area. For instance for an area of 25 x 25 μm^2 the bandwidth peaking appears for a detector with dimensions of $s = w = 0.4/0.6$ μm for Si/GaAs-detectors, respectively. For smaller width and spacing the frequency rapidly starts to decrease, attributed to a rapid increase in the detector capacitance.

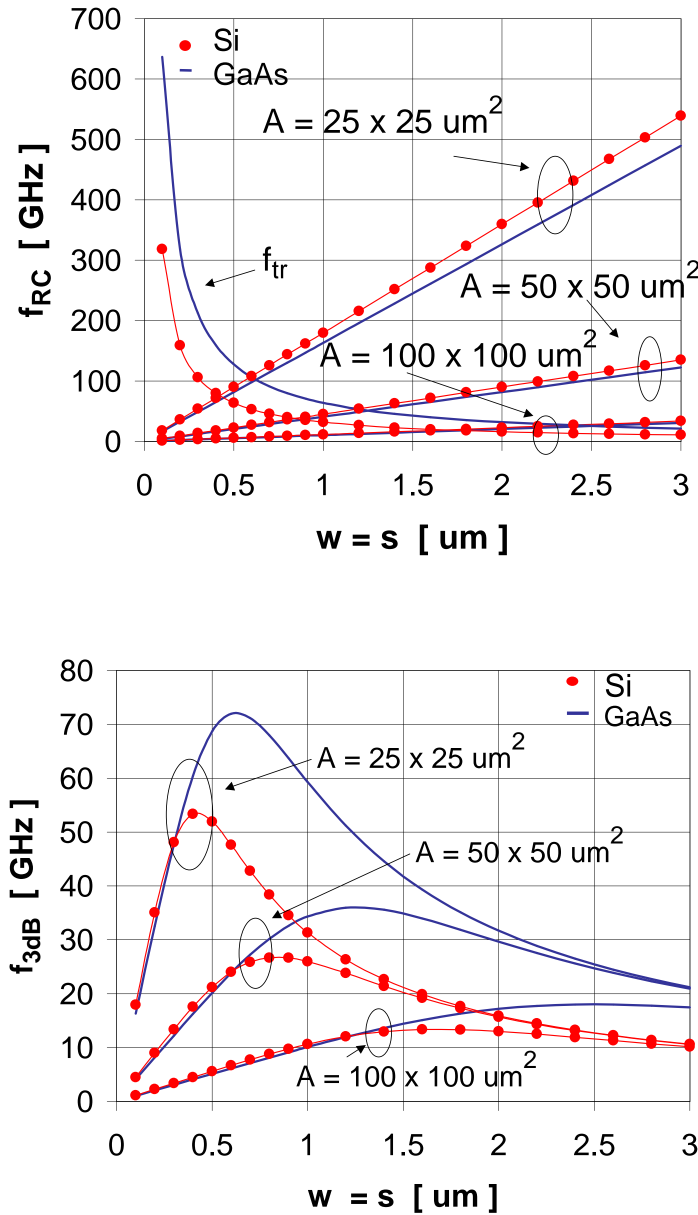

Figure 2.15: f_{RC}, f_{tr} and the total f_{3dB} for Si and GaAs MSM PDs as a function of finger spacing and width, and for different areas A (saturation and peak velocity for Si and GaAs, respectively).

In GaAs MSM PDs of submicron finger spacings, the high field velocity of $v = 6 \cdot 10^4$ m/s ($E = 2 \cdot 10^5$ V/cm) is an underestimation. The peak velocity of $v = 2 \cdot 10^5$ m/s applicable at fields in the range E = 3 - 4 $\cdot 10^3$ V/cm should be used instead. Furthermore, a unique feature of MSM PDs with nanometer finger spacings is the carrier velocity overshoot. Monte Carlo simulations demonstrate that for an MSM detector with 25 nm finger spacing and width the $FWHM$ is as short as 0.25 ps and the 3 dB bandwidth 0.4 THz due to electron velocity overshoot [55]. Figure 2.16 presents the transit time- and RC-time limited cut-off frequency, and the total bandwidth, Eq. (2.35), for a GaAs-detector with an area of A = 25 x 25 μm^2 using different velocities (capacitance is calculated from 2D conformal mapping theory Eq. (2.66) and R is set to the load resistance value of 50 Ω). The high field velocity (i.e. v_s), peak velocity and an overshoot velocity are used, showing that with higher velocity the bandwidth increases: calculated peak bandwidths are 38.8 GHz, 72 GHz and 161.2 GHz, respectively. In addition, the peak frequency shifts towards larger finger spacings/widths with increasing velocity.

Due to the 2-dimensional structure of the MSM diode, the speed is not only determined through the finger spacing and the electrode capacitance, but through the thickness of the absorbing layer. Clearly, the electric field strength within the photoactive layer scales with the applied bias. The frequency response markedly drops if the finger spacing s becomes smaller than the thickness d of the absorbing layer, associated with a significant reduction of the electric field in the depth of the photoactive layer [56]. Ref. [43] compares the carrier transit time vs. finger spacing and the diffusion time as a function of the active layer thickness, calculated from a one-dimensional Monte-Carlo model and the diffusion equation. The simulations confirmed, that when the active layer thickness is larger than 200 nm, the response is dominated by the diffusion time of the deeply generated carriers. For a detector with 100 nm finger spacing, the transit time was 3 ps. To make the diffusion time comparable to the transit time, the active layer should be restricted between 100 and 200 nm.

2.2.5 Gain

Abnormally high DC and low frequency gain has been measured for MSM photodetectors. The gain mechanism is identified as an optically-induced photoconductive effect (charge accumulation, traps or defects), as a capacitive effect or avalanche-multiplication. In all mechanisms the quality of the metal semiconductor interface is of major importance. Impurities and surface defects being present at the contact interface degrade the overall performance.

Since in MSM PDs the Schottky barrier is usually high, the injection of carriers is prevented and DC gain as it is found in photoconductors should be absent. However, charge accumulation at the metal-semiconductor interface may, in addition to the image-force lowering, lower the Schottky barrier height. Therefore, at a fixed bias the contact resistance, given later by Eq. (2.41), is effectively reduced, and tunneling and thermionic emission currents across the modified barrier increase. The result of theoretical calculation indicates that the Schottky resistance varies inversely as the square-root of the electric field [57].

In addition to DC gain, low and high- frequency gain are observed phenomena in MSM PDs. The RF impedance of the photodiode depends on the optical power illumination and the applied bias. Since photogenerated electrons and holes have different lifetimes, and in order to maintain charge neutrality, additional majority carriers are injected to neutralize the minority carriers. This results in bias dependent gain at low frequencies. At a particular bias, the gain depends primarily on the ratio of the hole lifetimes and the electron transit time.

The AC gain can be approximated by using pulsed illumination or different chopping frequencies. The photoconductive gain under pulsed illumination is defined as [58]:

$$G_{pulse} = \frac{(\mu_e + \mu_h) T_{pulse} I_{ph}}{\sigma\, w\, A} \ , \tag{2.39}$$

where A is the detection area, w is the finger width, σ is the conductivity of the semiconductor, T_{pulse} is the pulse duration, and $\mu_{e,h}$ is the electron/hole mobility.

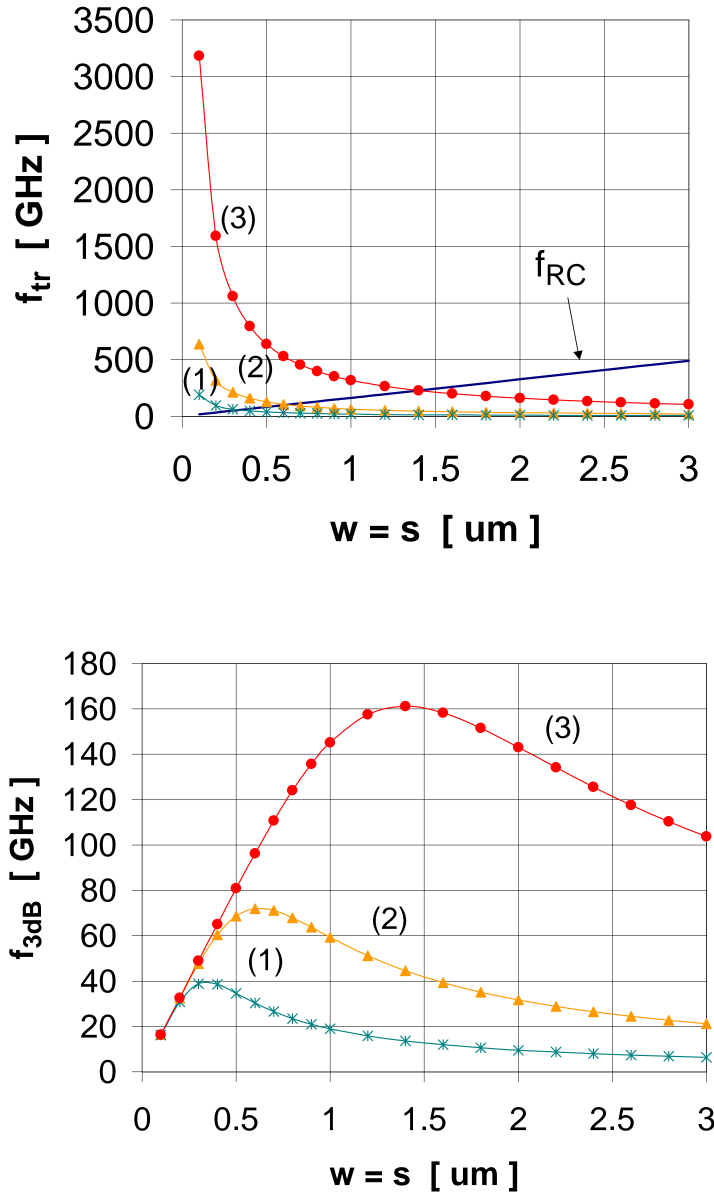

Figure 2.16: f_{RC}, f_{tr} and the total f_{3dB} for GaAs. A = 25 x 25 μm^2. (1) $v = 6 \cdot 10^4$ m/s, (2) $v = 2 \cdot 10^5$ m/s, (3) $v = 10^6$ m/s.

In the following different models/theories for the gain are presented in more detail. Models 1 and 2 are important in MSM structures with Schottky contacts, while model 3 is usually observed in structures with ohmic contacts.

1. Under bias holes are accumulated at the cathode because of the presence of a thin nonintentional insulating layer, the surface states or deep traps in the semiconductor bulk material. The residual density of holes close to the cathode momentarily sets up an electric field with image charges in the contact, and the Schottky barrier is lowered in height and reduced in width. Charge conservation must be satisfied instantaneously, thus additional thermal electrons move across the modified barrier and constitute an excess current. The gain effect is due to thermionic emission in case a temperature dependence is noticed. Otherwise, the additional charge carrier injection may happen by tunneling [59]. According to [57] the difference in transit speeds between electrons and holes also could lead to an increase in hole density in the vicinity of the cathode.

2. Thermionic emission of holes at the anode is proposed as a source of low-frequency gain [60]. Schottky barrier lowering at the anode is due to electron accumulation (charge trapping) at surface states and due to image force lowering at the edge of the metal electrode where the electric field is extremely high. Gain is also observed to increase with temperature and bias. According to [61] hole injection at the anode results from modulation of a localized barrier that is due to two-dimensional field distribution in GaAs. It is further suggested that a large applied bias produces a concave conduction band and hence electron accumulation at the anode, creating an asymmetric charge distribution. This causes hole injection from the anode and hence an increase of current [62].

3. DC and low-frequency gain is attributed to charge trapping effects in the electrodes, in the substrate, at interfaces and at the semiconductor surface [63]. Long lifetime traps in the semiconductor are filled by photoexcited carriers and cause an increase in conductivity and hence photoconductive gain by subsequent re-emission. Assuming that the gain is due to the trapping of holes, the output current is:
$$I_{ph} = \frac{q h_{trap} \mu_e V}{s^2} , \tag{2.40}$$
where h_{trap} is the number of trapped holes, s is the finger spacing and V is the applied bias. It has been shown that already a small trap density and optical flux is capable of increasing the electric field considerably near the electrodes. The trap phenomenon has little influence for long wavelengths due to the large penetration depth of light. But for high photon energies, since the light is absorbed in a thin surface layer the trap-induced gain becomes significant. A linear relationship of responsivity on bias is indicative for the photoconductive gain mechanism. This can be understood by the following expression [64]: $G_i = \frac{\mu_e+\mu_h}{\mu_e}\frac{\tau_r}{t_{tr}^e}$, $t_{tr}^e = \frac{s^2}{\mu_e V}$, where τ_r is the recombination lifetime and t_{tr}^e is the electron transit time. As voltage increases the electron transit time decreases, and the gain subsequently increases linearly.

4. An analytical model based on the behaviour of photo-generated carriers and electric fields in a GaAs MSM PD show transient excess carrier accumulation both at the cathode and anode ends causing a capacitive effect [65]. The two-dimensional numerical simulations, which apply to flatband conditions are based on the Poisson's equation, the current-continuity equations and a rate equation for charged traps. The results indicate that the electric field in the central region of the MSM PD decreases as time increases. This is due to charge separation: since photo-generated electrons and holes move in opposite directions space-charge regions are formed near both electrodes.

5. Gain is observed to be independent of the incident optical power, but directly relate to the increased bias voltage, particularly in the bias region 10 - 20 V, where the dark current is also significantly increased [66]. The gain is associated with high electric field region around the interdigitated electrode edges. At a low bias voltage, the localized field enhances the image-force lowering, according to Eq. (2.6). With increasing bias the increased field causes an avalanche effect. This explanation is further confirmed by the soft breakdown at the higher applied bias voltage in the I-V characteristics.

2.2.6 Nonlinearities

Nonlinearities in the performance of the photodiode are observed under high illumination levels and/or at high bias voltage.

By increasing the pulse power at a fixed bias, more carriers are absorbed and the peak signal amplitude increases due to a larger photocurrent. However, at a very high laser power, screening and space charge effects start to dominate. Since the applied electric field is effectively reduced by the opposite electric field due to the photoinduced carriers, the collection of the carriers at the contacts is retarded. The peak signal amplitude does not any more scale linearly with injected electron/hole density and begins to saturate [67]. The screening of the applied field also reduces the effective electron/hole transit time, thus increasing the response fall time and degrading the overall bandwidth [68].

At a low bias, the gap between the fingers is not fully depleted, and the field is too low to reach saturation velocities. As the bias is increased, the response time decreases due to higher electric field and shorter carrier transit times. The peak amplitude (photocurrent) also increases linearly. At high bias voltages nonlinearities may appear [69]. The electric field directly under the center of each interdigitated electrode is parallel to the electrode. Since the perpendicular component of electric field is small, the small number of carriers that are generated at the center (by diffraction) do not contain a significant component of drift velocity toward the adjacent electrode (holes generated under the anode drifting toward the cathode and vice versa). The few carriers which drift into low field regions of the semiconductor where their velocities can be strong functions of electric field are the reason for nonlinearities.

Best results avoiding nonlinear behaviour are obtained by using an incident pulse energy that avoids space-charge effects, and applying a bias voltage that exceeds the reach-through condition.

2.3 Modelling

The current transport of a metal-semiconductor-metal structure is based on several processes. The characterization of the current phenomena depends on the semiconductor material, the doping concentration of the semiconductor, the active layer thickness, the Schottky barrier height, the surface of the device (passivation, ARC) and the interface between the metal and the semiconductor (i.e. surface states, trap states, insulating film). Further, the measurement conditions such as the bias-voltage, the wavelength, the intensity of the light source as well as the temperature affect the current behaviour.

The basic equations governing the device operation include the Poisson's equation, the current continuity equation for both electrons and holes, and the particle current and the displacement current densities. The generation rate is due to photogeneration and impact ionization. In the following one-dimensional models for the dark- and photocurrent are presented. In fact, a simple 1D analysis is not sufficient for the MSM diode modelling, but only gives a rough estimation of the device characteristics. The reason is the lateral interdigitated geometry which gives rise to a strong spatial distribution of the electrical field inside the device. This makes the modelling more complicated in contrast to vertical optoelectronic devices.

2.3.1 Schottky Barrier Height

A measure of the contact quality between the semiconductor and the metal is the specific contact resistance, defined through Ohm's law by $R_c = \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0}$ [Ωcm^2]. Using Eq. (2.4) and neglecting the small voltage dependence of the barrier height the contact resistance becomes:

$$R_c = \frac{k_B}{qA^*T} e^{\frac{q}{k_B T}(\phi_{Bn} - \Delta\phi_{Bn})} . \tag{2.41}$$

Eq. (2.41) indicates that the Schottky barrier height should be high in order to achieve a high contact resistance, further a large voltage drop in comparison to the bulk semiconductor and small injection current over the barrier are needed.

In thermal equilibrium the Schottky barrier height ϕ_{Bn} for an n-type metal semiconductor contact simply depends on the metal work function ϕ_m and the electron affinity χ as follows:

$$q\phi_{Bn} = q(\phi_m - \chi). \tag{2.42}$$

For an ideal contact between a metal and a p-type semiconductor, the barrier height is given by: $q\phi_{Bp} = E_g - q(\phi_m - \chi)$.

Equation (2.42) is, however, only valid for an ideal Schottky junction. Generally, values of the barrier height are very sensitive to surface contamination. In practice there is also always a thin insulator layer (of atomic dimensions) on the surface of the semiconductor. The surface- and trap states within the insulator affect the Schottky barrier height. In addition, the applied bias voltage and the temperature have to be taken into account. The barrier height is generally a decreasing function of temperature, because the expansion of the lattice causes changes in the work functions and other parameters which determine ϕ_{Bn} at zero bias [4]. A reverse bias effectively reduces the barrier height compared to zero bias, while a forward bias increases the barrier height slightly. The effective change of the barrier height is called the Schottky-effect; the Schottky-barrier lowering is defined in Eq. (2.6).

The exact definition for the Schottky barrier height, including the barrier lowering effect, can be derived considering the total charge at the interface between the semiconductor and the insulator, and thus the potential drop across the insulator. The charge consists of the depletion layer charge in the semiconductor and the surface states at the interface. ϕ_{Bn} for an n-type semiconductor becomes [9]:

$$\phi_{Bn} = c(\phi_m - \chi) + (1-c)(\frac{E_g}{q} - \phi_0) - \Delta\phi_{Bn}, \tag{2.43}$$

where

$$c = \frac{\epsilon_i}{\epsilon_i + q^2 d_i D_a}. \tag{2.44}$$

Here D_a is the acceptor surface density, [1/cm^{2}eV], d_i is the thickness of the insulator layer and ϵ_i is the permittivity of the insulator. D_a is a constant from the constant energy level $q\phi_0$ to the Fermi level.

It can be seen that the equation for the barrier height is fairly complicated, depending on several different factors. The theoretical approximation of the barrier is thus usually quite difficult, and an experimental approach is preferred. Reliable results are achieved for instance by means of I-V versus temperature, C-V, activation energy or photoelectric measurements. In this work the I-V characteristics as a function of temperature are applied for determining the Schottky barrier height.

The metallization has a crucial effect on the Schottky barrier height, and thus the dark current. If both the anode and the cathode are formed by the same metal deposition process, the assumption for the barrier heights is $q(\phi_{Bn} + \phi_{Bp}) = E_g$. Whether electron injection at the cathode or hole injection at the anode dominates, depends on the choice of the electrode material.

By independently engineering the Schottky barrier heights at the anode and the cathode the dark current due to thermionic emission can be reduced in comparison to conventional MSM PDs. The barrier heights can be engineered independently by using different materials to form the cathode and anode, resulting in $q(\phi_{Bn} + \phi_{Bp}) \geq E_g$. The use of different metals on opposing sides of the interdigitated electrode structure enables the Schottky barrier height to electrons at the cathode and holes at the anode to be increased independently. The result is a decrease in dark current through a reduction in carrier injection at the Schottky contacts.

An InAlAs/InGaAs/InP-photodetector with combination of Pt/Ti/Pt/Au and Ti/Au electrodes has exhibited a dark current of 312 pA at an applied bias of 5 V, corresponding to a dark current density of 2 μA/cm^2 [70]. This is six times lower than the reported dark current density of 12.6 μA/cm^2 for an InGaAs MSM PD with identical electrodes. Significant is that by using different contact-metals no change was observed in the responsivity or the bandwidth. A hybrid combination of transparent (CTO) and opaque (Ti/Au) electrodes on InAlAs/InGaAs-substrate demonstrated a responsivity of 0.56 A/W at 1.31 μm and a low dark current density of 2.12 μA/cm^2 [19].

2.3.2 I-V Characteristics

Dark Current

Equation (2.4) applies for an ideal diode. In practice diodes never satisfy Eq. (2.4) exactly, but a modified form with the ideality factor n, and modified Richardson constant A^{**} has to be used

instead. The dark current density for a Schottky diode becomes [4]:

$$J_{dark} = A^{**}T^2 e^{-\frac{q}{k_BT}(\phi_{Bn}-\Delta\phi_{Bn})}\, e^{\frac{qV}{nk_BT}} \left(1 - e^{\frac{-qV}{k_BT}}\right) \tag{2.45}$$

$$= J_{sat}\, e^{\frac{qV}{nk_BT}} \left(1 - e^{\frac{-qV}{k_BT}}\right) ,$$

where the ideality factor is greater than unity (may depend on temperature). It accounts for the bias dependence of the Schottky barrier: $\frac{1}{n} = 1 - \frac{\partial(\phi_{Bn}-\Delta\phi_{Bn})}{\partial V}$. A^{**} takes into account thermionic emission, drift-diffusion, probability of optical phonon scattering f_p, quantum mechanical tunneling and reflection f_Q, and is expressed as [9]: $A^{**} = \frac{f_p f_Q A^*}{1+f_p f_Q v_{th}/v_D}$. A^* is as given by Eq. (2.5), $v_{th} = A^*T^2/qN_c$ is the thermal velocity and v_D is the effective diffusion velocity of electrons from the edge of the depletion layer to the potential energy maximum. In case the ideality factor is a function of bias, it can be obtained from the experimental J_{dark}-V characteristics through the relationship: $n = \frac{q}{k_BT}\frac{\partial V}{\partial \ln\left[J_{dark}/(1-e^{-qV/k_BT})\right]}$.

The total DC-characteristics for the dark current flow can be modelled by using the DC gain caused by tunneling J_{tun}, Eq. (2.25), and the thermionic emission current density J_{dark}, Eq. (2.45) [6], [20]. The fitting is divided into two regions: voltages below flatband condition and voltages exceeding the flatband voltage, i.e. the saturation region. At low voltages, below the flatband condition, the leakage current mechanism is caused by tunneling, whereas after flatband voltage the Schottky emission current becomes dominant.

The total model for the dark current in the reverse bias condition is given by:

$$I_{dark} = Y\, e^{-\frac{B}{V}} \;, V < V_{FB} \tag{2.46}$$

$$I_{dark} = X\, e^{-\frac{B}{V}} + C\, A^{**}T^2 e^{-\frac{q}{k_BT}(\phi_{Bn}-\Delta\phi_{Bn})}\, e^{\frac{-qV}{nk_BT}} \left(e^{\frac{qV}{k_BT}} - 1\right) \;, V \geq V_{FB} \tag{2.47}$$

where Y has to ensure continuity of the two equations at the flatband. Y [A], X [A], C [m^2] and B [V] are fitting constants. The tunneling current is stronger for voltages below saturation; the constants Y and X are thus used to account for this difference. The flatband voltage is given by (2.20). The Schottky barrier lowering is defined in Eq. (2.6) with the electrical field determined in Eq. (2.7). The built-in voltage is given by Eq. (2.2), and the effective density of states in the conduction band by Eq. (2.3).

Photocurrent

In MSM PDs the photocurrent depends on the applied bias and on the light intensity. An observed property is that the photocurrent shows an initial increase followed by saturation and subsequent sharp increase before breakdown occurs. Figure 2.17 shows the potential profile of an n-type MSM device under applied bias voltage and under illumination. The cathode is reverse biased by V_1 whereas the anode is forward biased by V_2. The total photocurrent is the sum of the photocurrents at the cathode and the anode on the semiconductor side.

The photo current density from the small voltage range $V < V_{RT}$ up to voltages larger than the reach-through voltage $V > V_{RT}$ is determined by [71]:

$$J_{ph} = qG(W_1 - W_2)\,, \tag{2.48}$$

where W_1 and W_2 are the depletion region widths as defined in Eqs. (2.11) and (2.12), and G is the carrier generation rate, i.e. number of generated electron-hole pairs per time- and volume unit. At reach-through the length of the undepleted region $x_2 - x_1 = 0$.

The light induced generation rate of electron-hole pairs as a function of distance x from the surface is $g(x) = \Phi_0\, \alpha\, e^{-\alpha x}$, where $\Phi_0 = \frac{P_{opt}}{h\nu A}$ is the incident photon flux per unit surface area and α is the absorption coefficient of the semiconductor material. Integrating the generation rate over the thickness of the active semiconductor region d and taking into account the internal quantum efficiency η_i (number of electron-hole pairs generated per incident photon), gives:

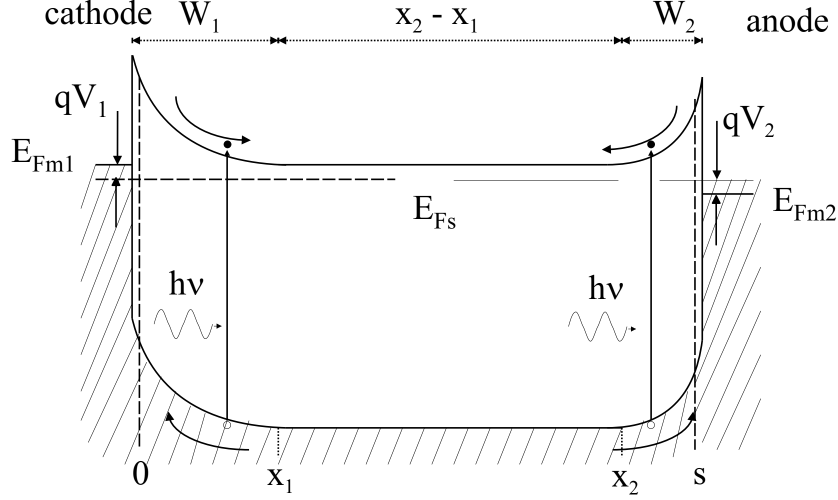

Figure 2.17: Energy band diagram of an MSM structure under low applied bias and under illumination.

$$G = \frac{1}{d}\int_0^d \frac{P_{opt}\,\eta_i}{h\nu A}\alpha\, e^{-\alpha x}dx = (1-e^{-\alpha d})\frac{P_{opt}\,\eta_i}{h\nu A d}\;. \tag{2.49}$$

At flatband the depletion region of the cathode reaches the anode, making the electric field at the anode zero. For voltages exceeding the flatband voltage $V > V_{FB}$, the photocurrent density per cross section area is characterized by:

$$J_{ph} = qGs\,. \tag{2.50}$$

At very high bias-voltages breakdown occurs at the cathode. Dark current rises screening the light response (i.e. the effect of optically generated carriers) leading to the space-charge effect. Since for the avalanche breakdown the breakdown voltage is very high, a more likely cause of breakdown is usually tunneling.

In DC steady state under constant illumination the photocurrent for an MSM structure, taking into account the surface reflectivity r, the shadowing due to the metal fingers, and using Eqs. (2.49) and (2.50), becomes:

$$I_{ph} = (\frac{s}{s+w})(1-r)\left(1-e^{-\alpha d}\right)\frac{qP_{opt}\,\eta_i}{h\nu}\;. \tag{2.51}$$

Here opaque electrodes are considered since the term $(\frac{s}{s+w})$ defines the fraction of the free semiconductor surface. Eq. (2.51) is valid when the voltage is above flatband voltage, i.e. the current has saturated.

The total DC-characteristics can be modelled by combining the contributions of the photocurrent I_{ph}, Eq. (2.51), the thermionic emission current density J_{dark}, Eq. (2.45), and the DC current gain due to light enhancement tunneling J_{tun}, Eq. (2.25) [6]:

$$I_{dc} = I_{ph}\,Y\,e^{-\frac{B}{V}}\;, V < V_{FB} \tag{2.52}$$

$$I_{dc} = I_{ph}\left[1 + X\,e^{-\frac{B}{V}} + C\,A^{**}T^2 e^{-\frac{q}{k_BT}(\phi_{Bn}-\triangle\phi_{Bn})}\,e^{\frac{-qV}{nk_BT}}\left(e^{\frac{qV}{k_BT}}-1\right)\right]\;, V \geq V_{FB} \tag{2.53}$$

where Y has to ensure continuity of the two equations at the flatband. B [V], Y [ ], X [ ] and C [m^2/A] are fitting constants. The flatband voltage is expressed in (2.20). The Schottky barrier lowering is given by Eq. (2.6) with the electrical field determined in Eq. (2.7). The built-in voltage is defined in Eq. (2.2), and the effective density of states in the conduction band by Eq. (2.3).

2.3.3 Small-Signal Equivalent Circuit Model

Capacitance

The dark capacitance of the MSM PD can be approximated by two commonly used physical models based on a one-dimensional (1D) depletion region approximation [8] or a two-dimensional (2D) conformal mapping technique [72]. In the 1D approximation the variation of the dark capacitance is caused by the modulation of the depletion regions at both electrodes and can be considered in terms of two voltage ranges; voltages less or greater than the reach-through voltage V_{RT}.
At $V < V_{RT}$, the capacitance per unit area is due to two back-to-back Schottky contacts in series:

$$\frac{1}{C_{dark,1D}} = \frac{1}{C_1} + \frac{1}{C_2}\,, \tag{2.54}$$

where $C_1 = \frac{\partial Q_{s1}}{\partial V_1} = \frac{\epsilon_s}{W_1}$ and $C_2 = \frac{\partial Q_{s2}}{\partial V_2} = \frac{\epsilon_s}{W_2}$ are the capacitances of the reverse- and forward-biased electrodes, respectively. The charges per unit area in the semiconductor Q_{s1} and Q_{s2} are associated with the doping concentration: $Q_{s1,s2} = qN_dW_{1,2}$. The widths of the depletion regions W_1 and W_2 for a symmetrical structure are defined in Eqs. (2.11) and (2.12). Equation (2.54) yields thus:

$$C_{dark,1D} = \frac{\epsilon_s}{W_1 + W_2} = \sqrt{\frac{\epsilon_s q N_d}{2}}\left[\frac{1}{\sqrt{V_{bi} - V_2} + \sqrt{V_{bi} + V_1}}\right]. \tag{2.55}$$

The built-in voltage is given in Eq. (2.2) and N_c in Eq. (2.3). As the voltage is increased, most of it will drop across the reverse-biased contact (i.e. $V_1 = V$, $V_2 \simeq 0$) leading to:

$$C_{dark,1D} = \sqrt{\frac{\epsilon_s q N_d}{2}}\left[\frac{1}{\sqrt{V_{bi}} + \sqrt{V_{bi} + V}}\right]. \tag{2.56}$$

Equations (2.55) and (2.56) indicate that the capacitance increases from its zero-bias value to a maximum and then decreases monotonically. At zero-bias, the capacitance is exactly one-half of that for a single Schottky-junction.
At $V > V_{RT}$, which is the normal operation mode for MSMs, the device is completely depleted ($W_1 + W_2 = s$) and the capacitance becomes independent of the applied bias. The capacitance defined in Eq. (2.55) equals then the parallel plate capacitor:

$$C_{dark,1D,sat1} = \frac{\epsilon_s}{s}\,. \tag{2.57}$$

Equations (2.56) and (2.57) describe the 1D capacitance as a function of the applied bias. In reality, even though reach-through condition has already been reached at the surface, the field region will extend from the surface deep into the substrate as bias is increased. The substrate (or the barrier layer) underneath the photoactive layer induces a capacitance, which is in parallel to the surface capacitance, see Fig. 2.18 which shows the model for a SOI structure [73]:

$$C_{dark,1D,sat2} = \frac{\epsilon_s}{s_2\left[\frac{\epsilon_s}{\epsilon_{barrier}}\right] + 2\,d}\,, \tag{2.58}$$

where s_2 is the effective distance between the electrodes in the substrate (or the barrier layer). The total saturation capacitance per cross section area is the sum of Eqs. (2.57) and (2.58):

$$C_{dark,1D,sat} = \frac{\epsilon_s}{s} + \frac{\epsilon_s}{s_2\left[\frac{\epsilon_s}{\epsilon_{barrier}}\right] + 2\,d}\,. \tag{2.59}$$

The model used in simulations is now a combination of Eqs. (2.56) and (2.59), multiplied by the number of fingers and the cross section area $A = l_{finger}\,d$, where d is the active top semiconductor layer thickness (for SOI-structures) or the bias dependent depletion depth.:

$$C = X\sqrt{\frac{\epsilon_s q N_d}{2}}\left[\frac{1}{\sqrt{V_{bi}} + \sqrt{V_{bi} + V}}\right](N_f - 1)\,\mathrm{A},\quad V < V_{FB}. \tag{2.60}$$

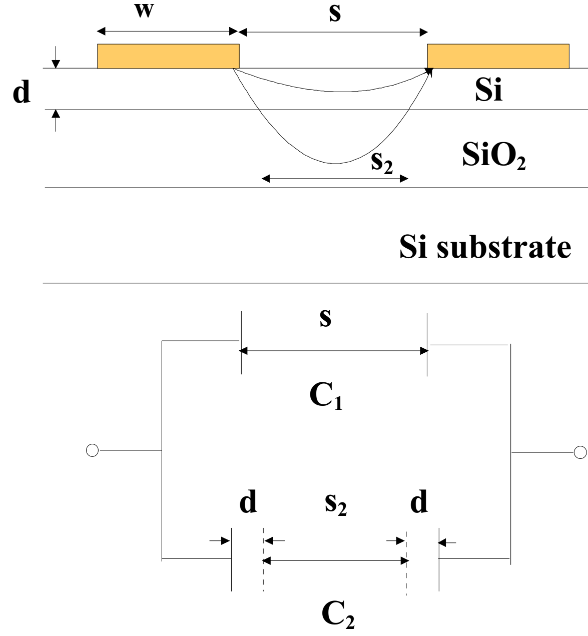

Figure 2.18: Model for the electrode capacitance of a SOI MSM.

$$C = Y \left[\frac{\epsilon_s}{s} + \frac{\epsilon_s}{s_2 \left[\frac{\epsilon_s}{\epsilon_{barrier}} \right] + 2\, d} \right] (N_f - 1)\, \mathrm{A}, \quad V \geq V_{FB}. \tag{2.61}$$

X [ ] and Y [ ] are fitting constants. X has to ensure continuity at the flatband voltage.

A more accurate model for estimating the depletion capacitance is given by a 2D conformal mapping theory. Conformal mapping for a coplanar alternating electrode pattern gives for the gap capacitance of the electrodes per finger length and pitch:

$$C_{dark,2D} = \frac{(\epsilon_0 + \epsilon_s)}{(w+s)} \frac{K(k)}{K(k')} \,, \tag{2.62}$$

where $\epsilon_s = \epsilon_0\, \epsilon_r$, K(k) and K(k') are Legendre's complete elliptic integrals of the first kind:

$$K(k) = \int_0^{\frac{\pi}{2}} \frac{d\phi}{\sqrt{1 - k^2 \sin^2 \phi}} \,, \tag{2.63}$$

$$k = \tan^2 \frac{\pi w}{4(w+s)} \,, \tag{2.64}$$

$$k' = \sqrt{1 - k^2} \,. \tag{2.65}$$

It has been assumed that the metal thickness approaches zero. This is an accurate enough approximation, since the metal thickness in practical MSM PDs varies between 0.1 - 1 μm.
The total dark capacitance of the detector, taking into account the active detection area $A = l\ (s+w)$ $(N_f - 1)$, where l is the finger length and N_f the number of fingers, is:

$$c_{dark,2D} = C_{dark,2D} \cdot A = l\,(N_f - 1)(\epsilon_0 + \epsilon_s) \frac{K(k)}{K(k')} \,. \tag{2.66}$$

The theoretical capacitance, according to Eq. (2.66), is plotted for a squared-area GaAs MSM as a function of finger length in Fig. 2.19. Minimizing the MSM capacitance a smaller area and/or increased s/w-ratio should be applied.

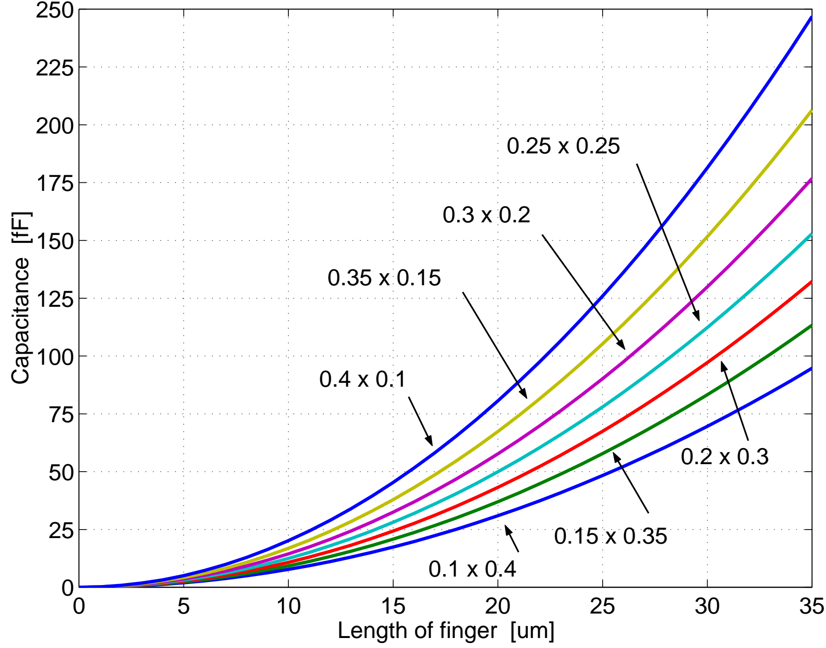

Figure 2.19: Capacitance of the interdigitated finger structure based on conformal mapping: with different widths and spacings (w x s in μm x μm) for GaAs (ϵ_r =13.1). The area is a square, and the pitch is kept constant at $p = w + s = 0.5$ μm.

Noticeable is that in the conformal mapping-approximation the width and length of the electrodes contribute differently to the capacitance, compared to the 1D approximation. Equation (2.62) defines the gap capacitance of electrodes per unit length and pitch, and the contribution of the metal finger width is already included. But on the other hand an assumption of the absence of electrical charge in the system has been made for this approach. Thus, Eq. (2.66) can only be used as a good estimation of the detector capacitance when the active area is fully depleted, i.e. saturation has been reached.

The capacitance depends, in addition to the bias voltage, on the light intensity. Equation (2.56) takes into account the depletion capacitance caused by charges associated with doping N_d. When the active area is illuminated, the polarization of the photocarriers contribute to the capacitance unless the electric field is strong enough to move all the photocarriers at their saturation velocity. The photogenerated carriers are trapped near the surface and in the bulk. These trapped carriers act like stored charges against the applied potentials (photovoltaic effect) and are measured as the excess capacitance [74]. Depending on the intensity of the incident light and the substrate doping concentration, the photocarrier-induced capacitance may be much larger than the depletion capacitance. With increased light intensity the depletion width decreases causing the capacitance to increase. Hence, under strong laser light the measured capacitance is most probably greater than the predicted theoretical value and reaches saturation under a higher applied bias.

Resistance

The series resistance R_s is due to the metal fingers on the semiconductor substrate. It can be estimated by using a DC model, in which the resistance per finger is calculated from the resistivity of the metal and the finger geometry:

$$R_0 = \rho\, l/A, \tag{2.67}$$

where ρ is the resistivity of the metal, $A = hw$ is the cross section area, h is the thickness of the metal, w is the width of the finger and l is the length of the finger. On each contact pad there are $N_{elec.} = \frac{L}{2\,(s+w)}$ number of fingers parallel-connected to each other (L is the width of the detection area). Taking both electrodes into account, the total resistance of the detector is the sum of two resistors connected in

series. The factor two drops out of the sum in that the average traversal distance is one half the full finger length, so that

$$R_s = \frac{R_0}{N_{elec.}} \ . \tag{2.68}$$

In order to minimize the resistance, short fingers with a large cross sectional area should be used.

At DC, charge carriers are evenly distributed through the entire cross section of the electrode. As the frequency increases, the reactance near the center of the finger increases, resulting in higher impedance to the current density in the region. Therefore, the charges move away from the center of the electrode towards the edge. As a result, the current density decreases in the center of the finger and increases near the edge of the finger (called the skin effect). The depth into the conductor at which the current density falls to 1/e, or 37 % of its value along the surface, is known as the skin depth. It is a function of the frequency, the permeability and the conductivity of the medium. The skin depth is given by $\delta = \frac{1}{\sqrt{\pi f \mu_o \sigma}}$. The electrode resistance increases with frequency, and the resistance due to skin depth is called the AC resistance [75]. In MSM PDs the metal thickness is usually less than δ; thus skin depth effects and radiation losses appearing at high frequencies can be neglected. For instance at f = 40 GHz the light penetration depth for Ti is 1.63 μm and for Au 386 nm, which both exceed the metal thickness of Ti/Au = 50/250 nm used in this work.

Total Device Model

The small-signal equivalent circuit under illumination is presented in Fig. 2.20 [76] (used for fitting of the experimental results in Sections 2.5.4 and 4.6.2).

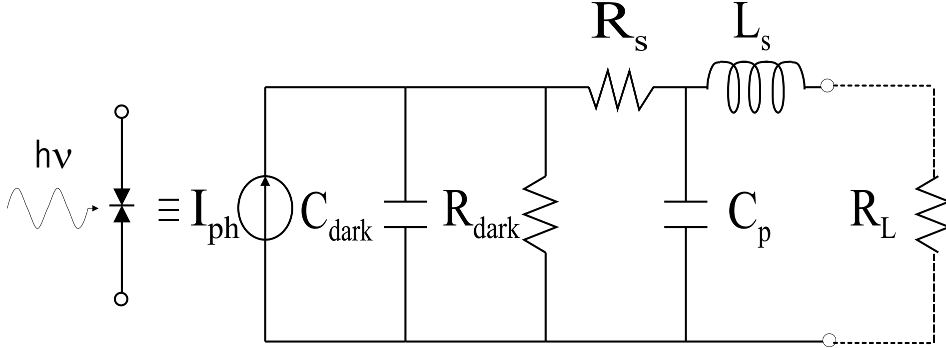

Figure 2.20: Small-signal equivalent circuit of an MSM PD.

Assuming that the bias is high enough to fully deplete the semiconductor between the contacts, the components of the model are:

$I_{ph} = \frac{P_{opt} R}{1+j\omega\tau_{tr}}$ = detector's intrinsic photoresponse, where P_{opt} is the incident optical power, $R = \frac{I_{ph}}{P_{opt}}$ is the responsivity and τ_{tr} is the carrier transit time.

C_{dark} = saturation dark capacitance due to the metal finger geometry, Eq. (2.66).

$R_{dark} = \frac{V}{I_{dark}}$ is the dark DC resistance, where I_{dark} is Eq. (2.24) multiplied by the cross section area of the current flow.

R_s = total ohmic series resistance due to the metal fingers, Eq. (2.68).

L_s = series inductance due to the bonding wires and/or due to connecting metal transmission lines.

C_p = capacitance due to the contact areas.

Generally, R_s is much smaller than R_{dark} and the load resistance R_L. Therefore, in total resistance-approximations the series resistance can be neglected.

2.3.4 Series MSM

The mask layout for a series MSM PD (the detector connected in series with two coplanar lines) is shown in Fig. 2.21. Different area MSMs were designed, ranging from 10 x 10 μm^2 to 35 x 35 μm^2 by varying the length of the metal pads, i.e. by changing the distance in between the metal pads while keeping the distance to the metal frame at the outer ends constant. A two port measurement can be carried out by placing the measurement probes on the contact pads. The corresponding circuit diagram for S-parameter modelling purposes is presented in Fig. 2.22, with the S-parameter ports S1 and S2 placed at the reference planes (denoted as small squares in the mask layout). The metal connections are modelled in MDS (microwave design system) using microstrip and coplanar transmission lines. The series MSM is especially designed for parameter extraction purposes.

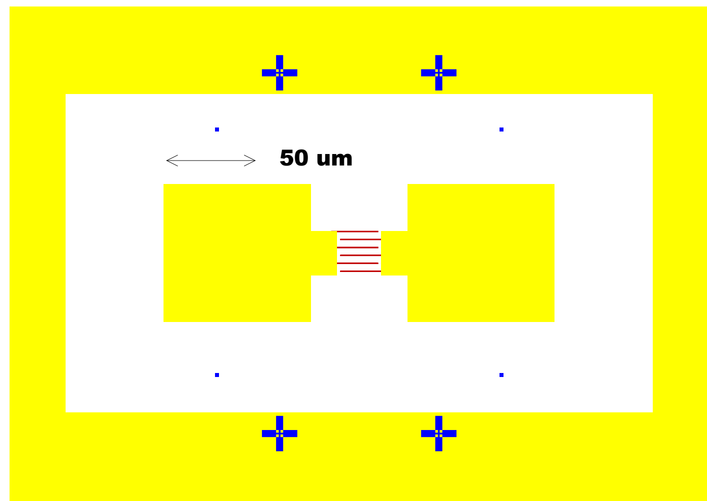

Figure 2.21: Mask layout for a series MSM PD. The crosses are for e-beam alignment, whereas the small squares for accurate placement of the RF measurement probes.

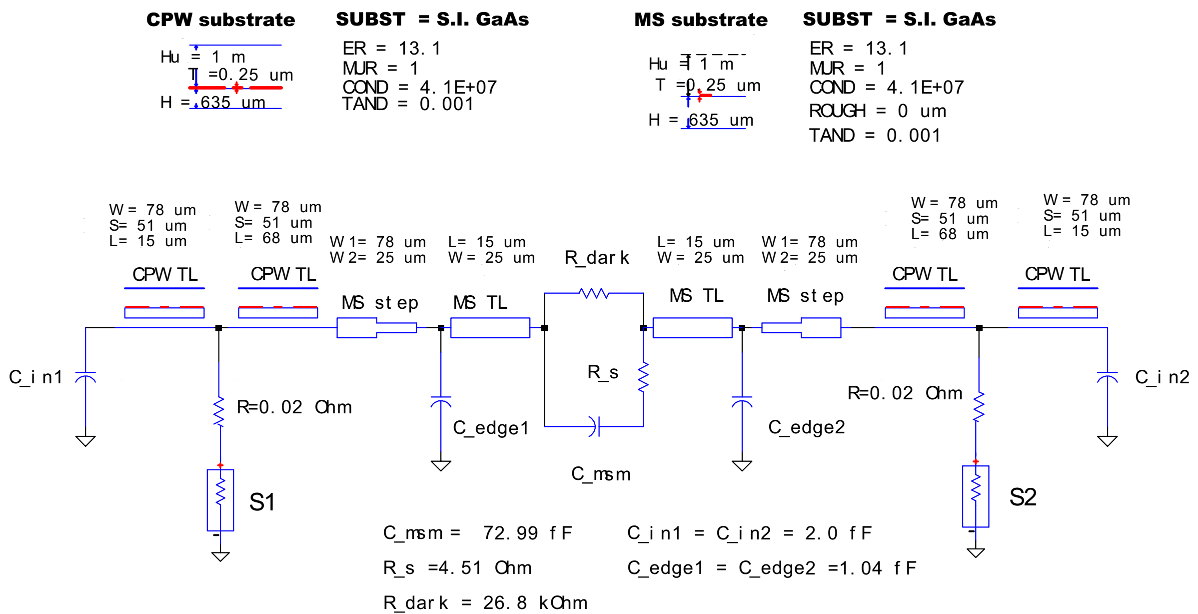

Figure 2.22: Small-signal equivalent circuit of a series MSM PD.

2.3.5 Tapered MSM

The mask layout for an MSM PD with tapered configuration (the detector terminating a tapered coplanar line) and the corresponding circuit diagram for S-parameter modelling are presented in Figs. 2.23 and 2.24, respectively. In the latter one the S-parameter port S1 is placed at the reference plane, corresponding to the small squares in the mask layout. The taper is designed to 50 Ω, and the metal connections are modelled using pieces of coplanar transmission lines with decreasing width (W) and spacing (S.) The main purpose of this design is the usefulness for optical and capacitance measurements: one measurement probe is needed, and the laser beam light can easily be focused on the MSM finger structure. Different area MSMs were designed, ranging from 10 x 35 μm^2 to 35 x 35 μm^2. This was done by shifting the terminating metal bar on the right side while keeping the tapered metal structure on a fixed position.

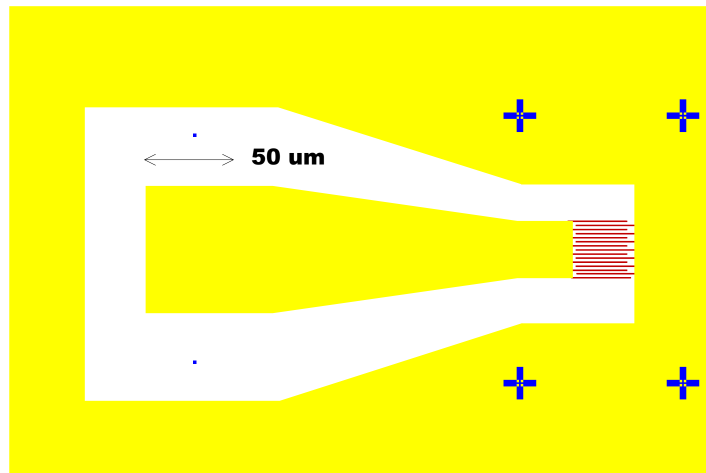

Figure 2.23: Mask layout for a tapered MSM PD. The crosses are for e-beam alignment, whereas the small squares for accurate placement of the RF measurement probe.

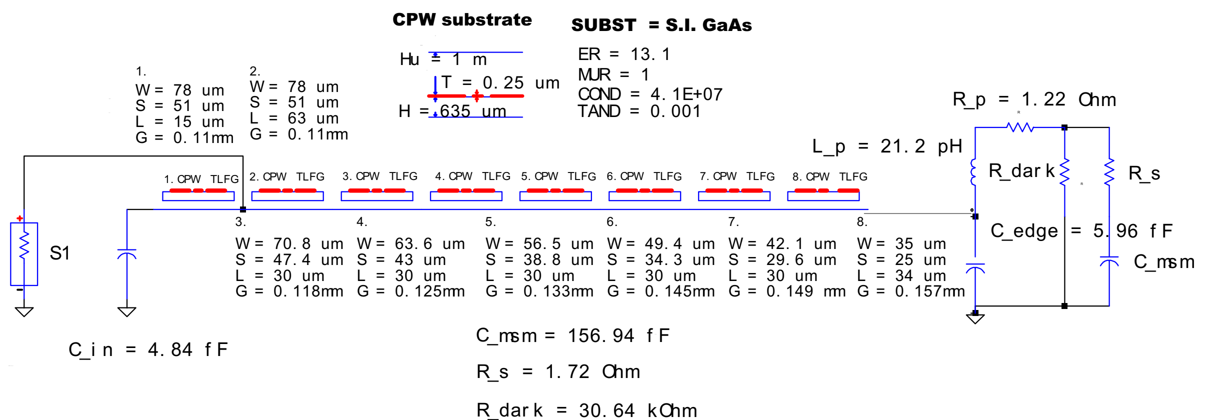

Figure 2.24: Small-signal equivalent circuit of a tapered MSM PD.

2.4 Fabrication

MSM PDs were fabricated on bulk-Si-, SOI- and S.I. GaAs-substrates. Detectors, consisting of finger structures and contact pads, were fabricated using both optical and e-beam lithography, and lift-off technique. SOI MSM PDs were processed by using optical lithography having an active area of 100 x 100 μm^2, and finger widths and spacings ranging from 1 - 3 μm. Detectors with submicron dimensions were fabricated on S.I. GaAs by combining optical- and e-beam lithography methods: fingers by e-beam exposure whereas contact pads by standard optical lithography. Area for nanoscale detectors ranged from 10 x 10 μm^2 to 35 x 35 μm^2, and finger widths and spacings between 0.15 - 0.25 μm and 0.25 - 0.35 μm, respectively. Figure 2.25 shows the side profile of submicron MSM electrodes.

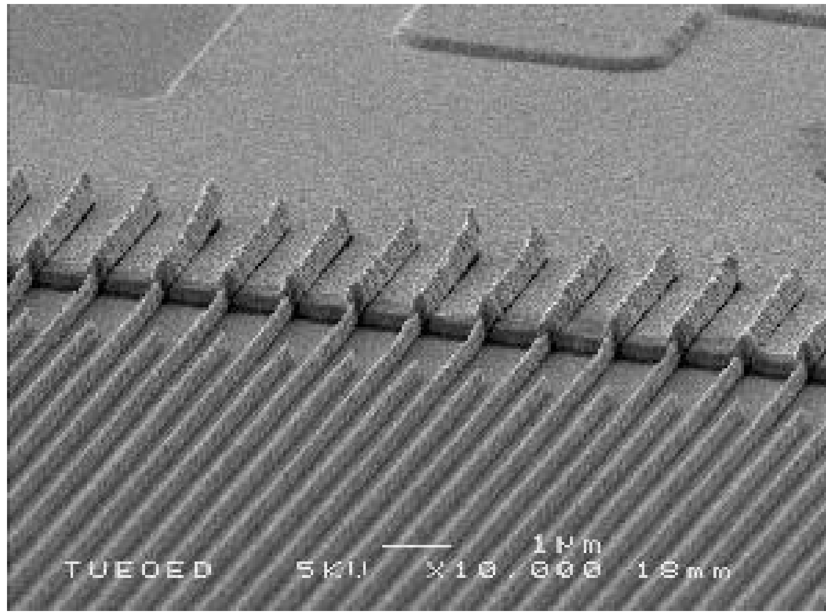

Figure 2.25: SEM photograph of submicron MSM fingers on S.I. GaAs, $w = 0.2$ μm, $s = 0.3$ μm, Ti/Au = 50/250 nm. Fabricated with a 3-layer resist stack.

2.4.1 SOI Structures

The SOI photodetectors were fabricated on SIMOX (Separation by IMplanted OXygen) wafers with (100) orientation, supplied by Ibis Tech./USA. The thickness of the buried SiO_2-layer was 390 nm whereas the top Si layer thickness was varied: 0.2, 0.5, 1, 2 and 4 μm, respectively. Three investigated detectors had p-type Si top layers (boron doping concentration 10^{15} cm^{-3}) with thicknesses of 0.2, 0.5 and 1 μm. Two investigated detectors had n-type Si top layers (phosphorus doping concentration $3 \cdot 10^{14}$ cm^{-3}) with thicknesses of 2 and 4 μm. Figure 2.26 shows the cross section of a SOI structure: Si-substrate, on which is grown a thin SiO_2 layer for isolation, and a doped Si-layer on top. The diffusion of carriers generated deep in the bulk is prevented by the SiO_2-isolation layer. The thin top Si layer acts as the photosensitive area, mainly determining the transient and responsivity characteristics of the detector.

Exposure was done by optical lithography using the Karl Suss MJB 3/UV mask aligner (intensity 10 mW/cm^2). Metallization for the n-type Si samples was done by the Edwards E306A-vacuum-evaporator (thickness of aluminium 90 nm (bulk Si) or 120 nm (SOI)). The p-type Si-samples were metallized using an electron beam gun evaporator (thickness of metal layers: Ti/Au = 50/100 or 50/120 nm).

The detailed processing techniques are explained in Table B.3. In order to reduce the parasitic leakage current from underneath the contact pads and thus to improve the device performance in

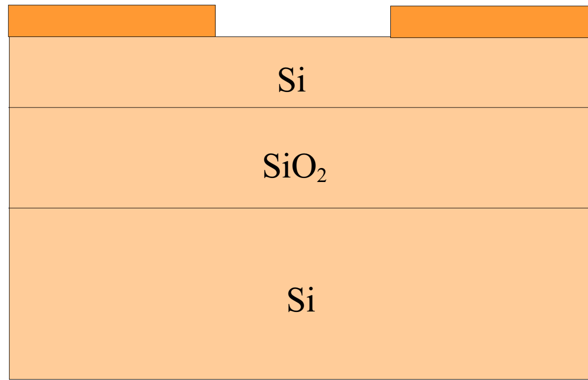

Figure 2.26: Schematics of a SOI MSM PD.

respect to low noise applications, a 100 nm thick wet oxide was grown on the semiconductor surface prior to metal deposition. Windows for the MSM active areas were then etched with buffered HF. In order to study the effect of a passivation coating, a layer of Si_3N_4 with a thickness of 100 nm was grown by PECVD method on half of the samples.

Also bulk Si MSM PDs were processed in order to compare their characteristics to those of SOI structures. Bulk wafers had n-type doping (phosphorus) and a resistivity of 4 - 6 Ωcm (corresponding to $N_d = 9 \cdot 10^{14} - 10^{15}$ cm^{-3}).

2.4.2 GaAs-based Detectors

The GaAs MSM diodes were fabricated on single-crystal, semi-insulating (011) oriented wafers with resistivity of 2 - 5 $\cdot 10^7$ Ωcm (mobility 6800 - 7400 cm^2/Vs at T = 300 K) (grown by American Xtal Tech.). The processing steps for MSM diodes on S.I. GaAs using e-beam exposure for narrow electrode definition, and standard optical lithography for contact pads are explained in detail in Tables B.4 and B.5, respectively. The finger width and spacing in the e-beam file were set to 0.15 μm and 0.35 μm, respectively. However, depending on the used exposure dose [μC/cm^2], and used PMMA resist layers and thicknesses the final linewidth ranged from 0.15 to 0.25 μm.

Two different methods were applied:
• Thin 200 nm single layer of PMMA 495K.
Metallization: Ti/Au = 30/40 nm.
• 3-layer resist stack system PMMA 495K/50K/495K = 200/180/200 nm.
Metallization: Ti/Au = 50/250 nm.

Using the thin single layer PMMA results in best linewidth accuracy (w = 0.15 μm as is set in the design). The proximity effect (backscattered electrons from the substrate) as well as forward scattering (incident electrons propagating through the resist) are less pronounced in a thin layer of PMMA than compared to those in a thick layer, thus leading to better control of the desired linewidth. With 580 nm thick 3-layer PMMA-system the linewidth became 0.2 - 0.25 μm.

2.5 Measurements and Fittings

2.5.1 Dark I-V and I-V versus Temperature

The I-V characteristics for the SOI detectors were measured using the HP 4155A semiconductor parameter analyzer, whereas for GaAs detectors the HP4141B DC Source/Monitor with automated IC-CAP software was used.

Current-voltage measurement vs. temperature (range from 25 °C up to 83 °C) were performed with a thermoelectric cooler; a solid state heat pump that utilizes the Peltier effect.

SOI detectors

The dark current measured for a SOI PD with p-type Si top layer of 0.5 μm is presented in Fig. 2.27 (also is shown a curve measured in room light), (A = 100 x 100 μm^2, $s = w = 3$ μm). The dark current increases from 45.8 nA (0.5 V) up to 74.6 nA (2 V), indicating a small leakage current.

The dark current density was calculated, using $J = I/A$, where A is the cross section area of the current flow. Calculation of J is, however, not straight forward because the junction area through which the current flows for a lateral 2D-geometry has some uncertainty. The cross section area can roughly be estimated as: A = finger length * junction depth * number of finger pairs [77]. This is an approximation, since it assumes a constant current distribution in this area, and does not take into account the variation of the electric field depending on the bias voltage nor the dimension of the finger spacing. The difficulty arises further in evaluating the junction depth. An approximation for the junction depth close to the real value is the Schottky depletion depth, i.e. the high field region which mainly causes the current flow. The depletion depth is bias dependent according to Eq. (2.11), where the built-in voltage is calculated using Eq. (2.2).

The dark current density at a bias voltage of -0.5 V is $3.4 \cdot 10^{-3}$ A/cm^2 and at 2 V $5.4 \cdot 10^{-3}$ A/cm^2. Corresponding depletion depths are 1.1 μm and 1.8 μm. Values for calculating the current density are: $N_a = 10^{15}$ cm^{-3}, $N_v = 1.04 \cdot 10^{19}$ cm^{-3} at T =300 K, $\epsilon_r = 11.8$ and $\phi_{Bp} = 0.7$ eV.

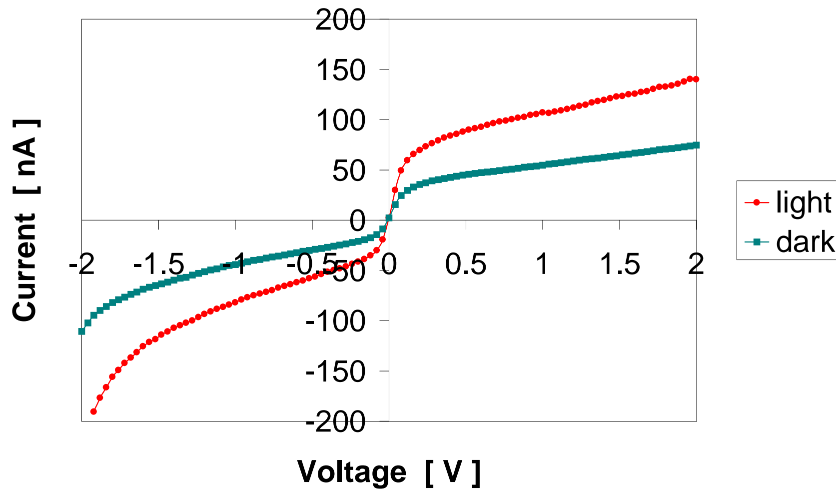

Figure 2.27: Dark current of a SOI MSM PD with top Si layer thickness of 0.5 μm ($s = w = 3$ μm, A = 100 x 100 μm^2).

The dark current as a function of applied voltage is measured for a SOI detector with n-type 4 μm top Si layer, for which an oxide layer was grown underneath the contact pads in order to reduce the parasitic leakage current, Fig. 2.28 (A = 100 x 100 μm^2, $s = w = 2$ μm). Values used for calculating the bias dependent depletion depth, and further the current density are: $N_d = 3 \cdot 10^{14}$ cm^{-3}, $N_c = 2.8 \cdot 10^{19}$ cm^{-3} at T =300 K, $\phi_{Bn} = 0.7$ eV and $\epsilon_r = 11.8$. The depletion depth is bias-dependent until 3.2 V, after this it is defined as the top Si layer thickness ($d = 4$ μm, since depletion depth exceeds 4 μm). The dark current at a voltage of 10 V is only 98.5 pA (1.8 μA/cm^2) and even at a high voltage of 40 V 199 pA (4.3 μA/cm^2). This extremely low leakage current is mainly due to the isolating oxide layer grown underneath the metal contacts.

A SiN passivation layer grown on top of the optically active MSM area was shown to reduce the dark current significantly. The dark current measured for two SOI PDs with and without SiN coating, respectively, is presented in Fig. 2.29 (A = 100 x 100 μm^2, $s = w = 2$ μm). For both detectors an

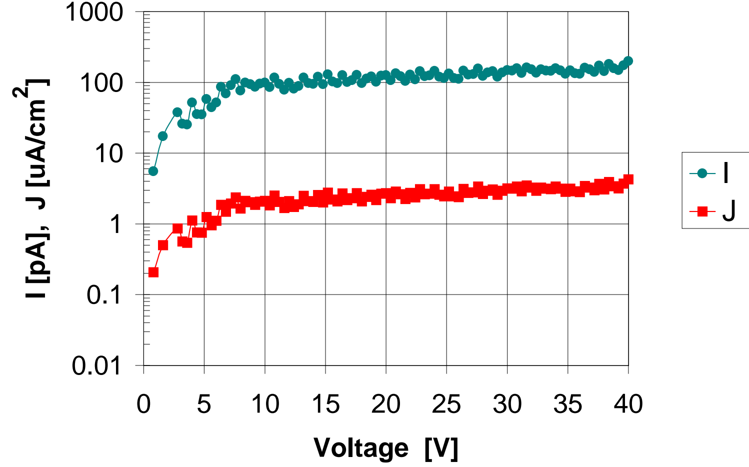

Figure 2.28: Dark current (measured) and dark current density (calculated) for a SOI MSM PD with top Si layer thickness of 4 μm ($s = w = 2$ μm, $A = 100$ x 100 μm^2).

oxide layer was also grown underneath the contact pads. The dark current at a bias voltage of 4 V is 4.5 pA and 1.2 pA for detectors with and without SiN-passivation, respectively, but increases rapidly at higher voltages for the unpassivated detector. The dark current at 6 V is 194 nA for the uncoated device compared to that of 7 pA for the SiN-coated detector.

The passivated detector exhibits at a voltage of 10 V a dark current of 10.8 pA and even at 30 V only 27.3 pA. This extremely low leakage current is mainly due to the isolating oxide layer underneath the metal contacts, and the SiN passivation layer on top. It also is an indication of a good-quality, and a high Schottky barrier at the metal-semiconductor interface. Comparable result is reported for a GaN Schottky MSM PD (epitaxial layer thickness 4 μm, finger spacing and width 2 μm), for which the dark current was only $\sim$ 800 fA at 10 V bias, and remained $<$ 10 pA at a reverse bias of 100 V [78].

S.I. GaAs detectors

The dark current is measured for a submicron S.I. GaAs detector, Fig. 2.30 (A = 15 x 15 μm^2, $s = 0.3$ μm, $w = 0.2$ μm). The figure shows also the response to microscope and room light illumination (an increase by a factor of almost 1000). The leakage current is very small, rising from 30.5 pA (1 V) up to 0.52 nA (5 V). The dark current density calculated from this data, $J = I/A$, where A is the cross section area of current flow, is also presented (area definition explained in detail in the previous section for SOI detectors). The depletion depth is calculated using Eqs. (2.2) and (2.11) with values of: $N_d = 10^{15}$ cm^{-3}, $N_c = 4.7 \cdot 10^{17}$ cm^{-3} at T =300 K, $\epsilon_r = 13.1$ and $\phi_{Bn} = 0.7$ eV. The dark current density rises from 10.4 μA/cm^2 at 1 V, 30.5 μA/cm^2 at 3 V up to 94.4 μA/cm^2 at 5 V (with depletion depths of 1.5, 2.3 and 2.8 μm, respectively). These low current densities are indicative of a high-barrier, good-quality Schottky contact. The bias dependent increase of the current is attributed to a DC gain mechanism (Section 2.2.5, model no 3).

The I-V characteristics at varying temperatures were measured for several different MSMs in order to obtain values for the Schottky barrier height, the modified Richardson constant A^{**} and the ideality factor n for these devices. A typical measurement for a submicron S.I. GaAs detector is plotted in Fig. 2.31. For convenience, in the following the effective Schottky barrier height is noted as $\phi_{Be} = \phi_{Bn} - \Delta\phi_{Bn}$. The dark current is basically the Schottky barrier emission current, Eq. (2.45). For the current density calculations here, a depletion depth of 1.5 μm was used, Eq. (2.11) with $V_{bi} = 0.54$ V, $V = 1$ V, $N_d = 10^{15}$ cm^{-3} and $\epsilon_r = 13.1$.

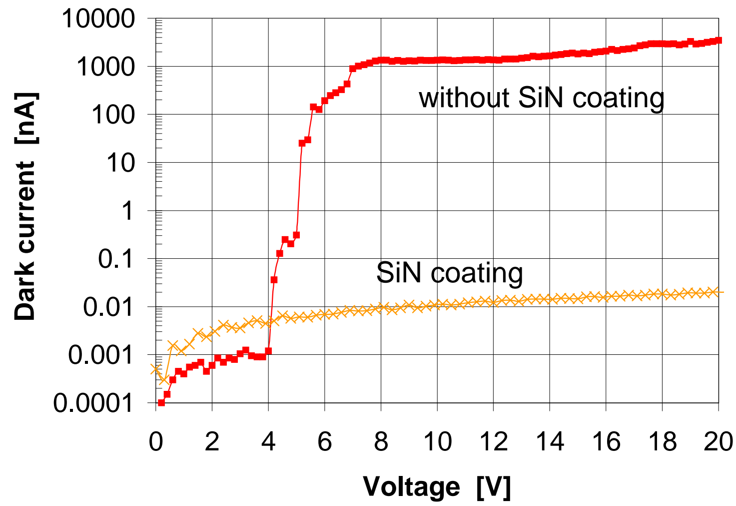

Figure 2.29: Dark current for SOI MSM PDs with SiN-coating and without ($s = w = 2\ \mu$m, $A = 100 \text{ x } 100\ \mu\text{m}^2$).

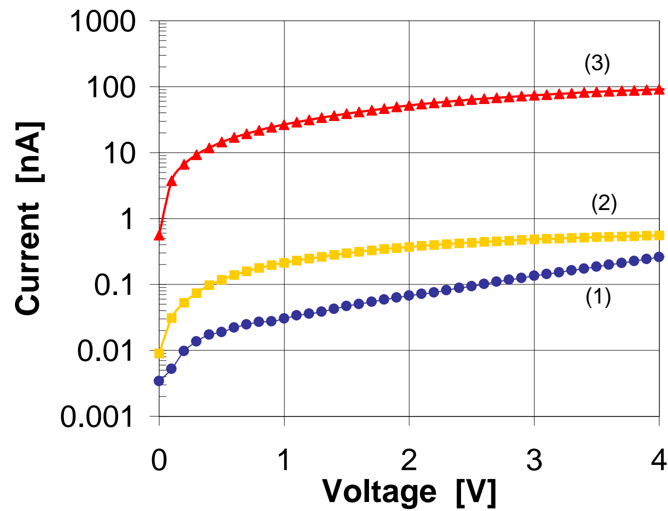

Figure 2.30: Current as a function of voltage for a S.I. GaAs MSM PD. (1) in the dark (2) in room light (3) under room and microscope light ($s = 0.3\ \mu$m, $w = 0.2\ \mu$m, $A = 15 \text{ x } 15\ \mu\text{m}^2$).

The steps in achieving ϕ_{Be}, A^{**} and n from the I-V-temperature data are as follows.

• Take the logarithm of Eq. (2.45), and plot $\ln(J)$ as a function of V. From the slope the ideality factor can be found directly, whereas the intersection with the vertical axis (extrapolation of the curve to $V = 0$ V) gives $\ln(J_{sat})$.
• J_{sat} has two unknown parameters (ϕ_{Be}, A^{**}), so that knowledge of J_{sat} as a function of temperature is needed. Because J_{sat} was found by extrapolating $\ln(J)$ to $V = 0$ V, the value for the barrier height determined in the next step actually applies for zero bias condition, i.e. $\phi_{Be} = \phi_{Be0}$ (with image-force barrier lowering also with $V = 0$ V).
• Plot $\ln(J_{sat}/T^2)$ against $1/T$, which gives a straight line with slope of $\frac{-q\phi_{Be0}}{kT}$, and intercept with the vertical axis of $\ln(A^{**})$.

The procedure described above was done for four samples. With the obtained parameters for ϕ_{Be0}, A^{**} and n a dark current fitting using the model outlined in Section 2.3.2, Eqs. (2.46) and (2.47), was performed. Table 2.1 indicates the fitting parameters, and Fig. 2.32 shows the corresponding measured and fitted current as a function of voltage. Samples no 1 and 2 were measured in the room light, whereas no 3 and 4 in the dark.

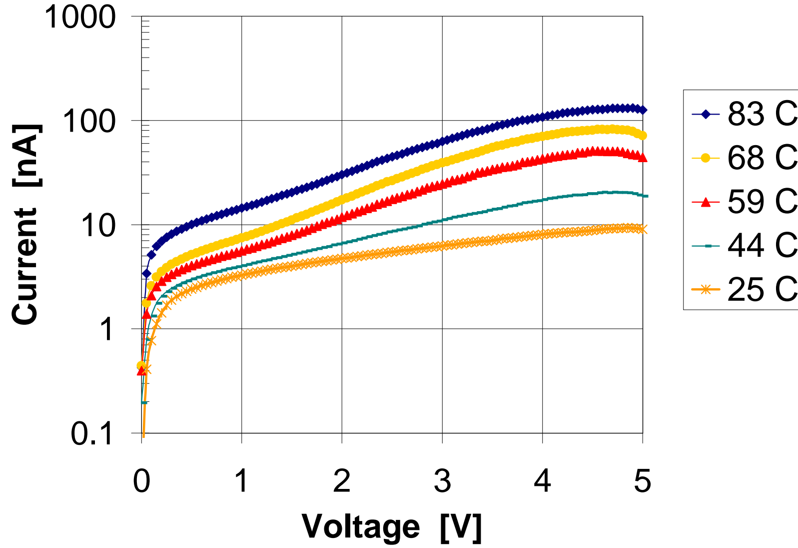

Figure 2.31: I-V characteristics for a S.I. GaAs MSM at several temperatures ($s = 0.3$ μm, $w = 0.2$ μm, $A = 35$ x 35 μm^2).

Table 2.1: Fitting parameters for I-V measurements (see Fig. 2.32).

Sample/MSM area	A^{**} [A/cm^{2}K^2]	ϕ_{Be0} [eV]	n
1 / 35 x 35 μm^2	13.98	0.602	1.0064
2 / 25 x 35 μm^2	39.72	0.617	1.0038
3 / 35 x 35 μm^2	38.5	0.720	1.016
4 / 15 x 15 μm^2	38.5	0.702	1.016

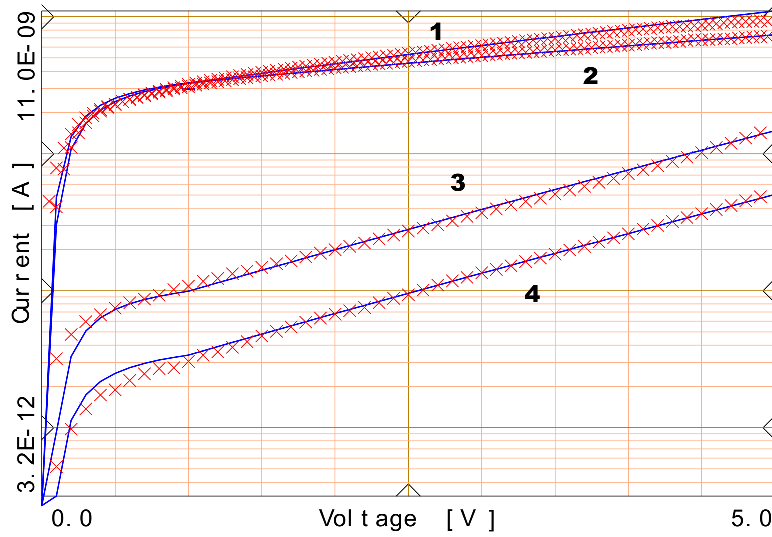

Figure 2.32: I-V characteristics for S.I. GaAs MSMs ($s = 0.3\ \mu$m, $w = 0.2\ \mu$m). Crosses (measurement), solid (fit).

2.5.2 C-V Characteristics

The capacitance as a function of applied bias was measured for SOI detectors at a frequency of 1 MHz with the HP 4192A LF impedance analyzer. For tapered GaAs detectors the capacitance measurement was performed with the HP4275A Multi-Frequency LCR meter at a frequency of 2 MHz, in dark environment, and an AC-signal amplitude either of 0.25 or 1 V. The SOI detectors were measured by placing probes on the 100 x 100 μm^2-size contact pads. For tapered GaAs diodes the measurement was done with one microwave probe placed on the metal contacts at the indicated small squares, see mask layout in Fig 2.23.

SOI detectors

The capacitance vs. applied voltage is measured for a SOI detector, Fig. 2.33, both in the dark and in the room light. At zero bias the capacitance is determined by the built-in depletion width. The capacitance measured in the light first rises with increasing reverse bias voltage and then starts to decrease due to the widening of the depletion region, according to Eqs. (2.55) and (2.56). At the flatband voltage the whole active area is depleted; thus the capacitance reaches its saturation value.

It can be noticed that the capacitance is almost a constant function of the bias voltage: decreasing from 0.68 pF at 0 V down to 0.48 pF at 2 V. Using $s = 2\ \mu$m, n-type doping concentration of $N_d = 3 \cdot 10^{14}$ cm^{-3} and $\epsilon_r = 11.8$, gives for the flatband voltage $V_{FB} = 0.92$ V, Eq. (2.20), which corresponds very well to the saturation voltage seen in the graph. The reach-through voltage, Eq. (2.13), becomes $V_{RT} = 0$ V using $\phi_{Bn} = 0.7$ eV and $N_c = 2.8 \cdot 10^{19}$ cm^{-3}.

The theoretical value based on 2D conformal mapping, Eq. (2.66), gives an intrinsic capacitance of 0.14 pF for the same geometry, which is lower than the measured one. The contribution of the large 100 x 100 μm^2 area contact pads has a significant effect on the observed high capacitance value.

Figure 2.34 shows the measured and simulated capacitance of a SOI MSM PD. The used model is presented in Section 2.3.3, Eqs. (2.60) and (2.61). Values used in the fitting are: $s = w = 2\ \mu$m, $A =$ 100 x 100 μm^2, $\epsilon_r(\text{Si}) = 11.8$, $\epsilon_r(\text{SiO}_2) = 3.9$, $d = 4\ \mu$m, $m^* = 0.66$, $T = 300$ K, $N_d = 3 \cdot 10^{14}$ cm^{-3}, $\phi_{Bn} = 0.7$ eV, $V_{FB} = 0.96$ V, $s_2 = 1.5\ \mu$m and $Y = 0.86$.

S.I. GaAs detectors

Figure 2.35 plots the capacitance as a function of voltage measured for a submicron MSM PD on S.I. GaAs (tapered configuration). The capacitance was measured also for a reference structure, i.e. a

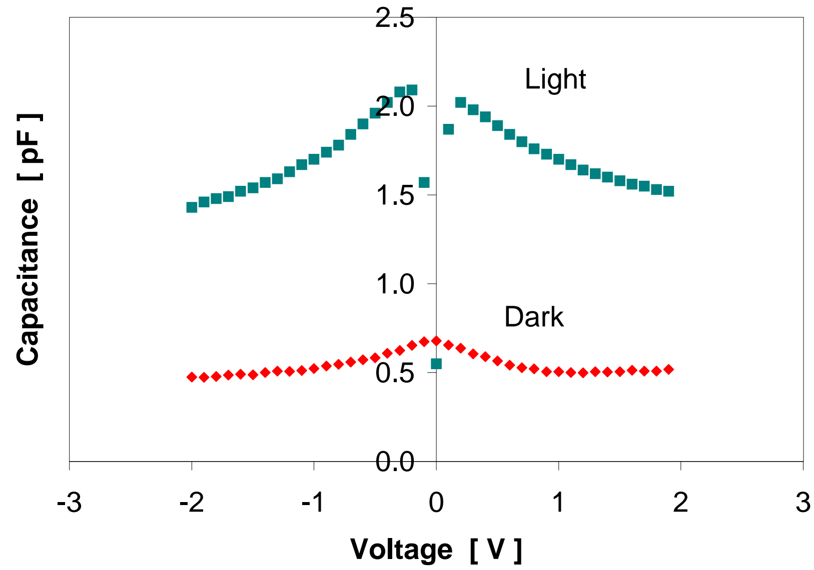

Figure 2.33: Capacitance as a function of applied bias voltage for a SOI MSM PD with top Si layer thickness of 4 μm, f_{test} = 1 MHz ($s = w = 2$ μm, A = 100 x 100 μm^2).

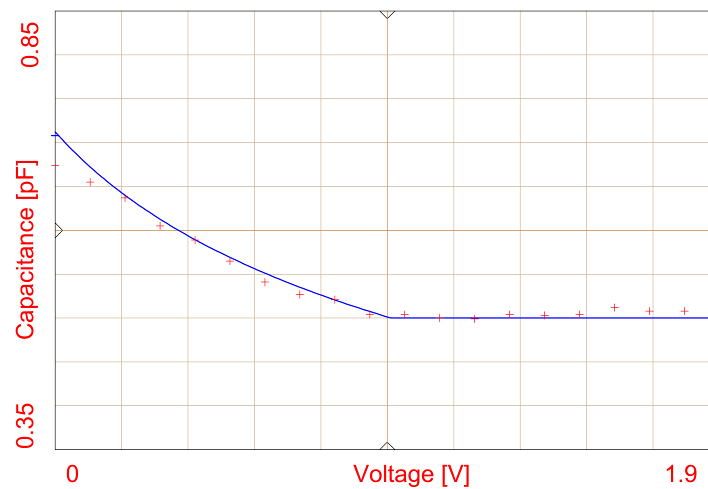

Figure 2.34: Capacitance for a SOI MSM PD with n-type top Si layer of 4 μm, $s = w = 2$ μm, f_{test} = 1 MHz. Measured (dotted line) and modelled (solid line).

tapered frame without the MSM fingers. Subtracting the reference value (76.4 fF) from the measured total capacitance, a capacitance of 85.4 fF is obtained at 1 V bias, ($C_{msm} = C_{measured} - C_{reference}$). The theoretical value based on 2D conformal mapping theory Eq. (2.66) gives 84.2 fF. It can be noticed that the capacitance is almost a constant function of the bias voltage: decreasing from 97.6 fF at 0 V down to 85.4 fF at 1 V. This means that total depletion between the fingers occurs at zero bias ($V_{RT} = 0$ V). Using $s = 0.35$ μm, a background doping concentration of $N_d = 10^{15}\,\text{cm}^{-3}$ and $\epsilon_r = 13.1$, gives for the flatband voltage $V_{FB} = 0.084$ V, Eq. (2.20).

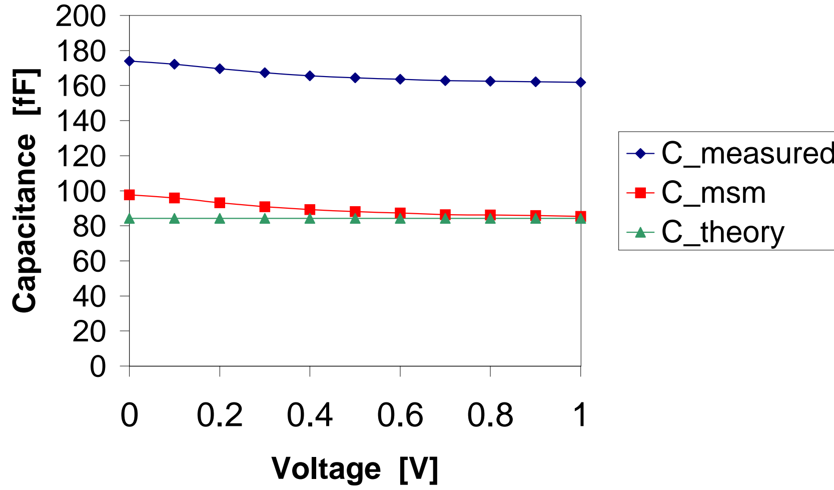

Figure 2.35: C-V characteristics for a submicron MSM PD (S.I. GaAs, $s = 0.35$ μm, $w = 0.15$ μm, $A = 25 \times 35$ μm^2, Ti/Au = 30/40 nm), $f_{\text{test}} = 2$ MHz. $C_{msm} = C_{measured} - C_{reference}$, where $C_{reference}$ = metal frame without MSM fingers.

The capacitance is also measured for different-size MSMs, Fig. 2.36. Shown in the picture is the *real* MSM capacitance, i.e. 'empty' reference value subtracted from the measured total capacitance. As expected, a larger area with more fingers leads to a larger detector capacitance.

Figure 2.37 presents the MSM capacitance ('empty' reference capacitance is subtracted from the measured total capacitance) as a function of w/s ratio for different detection areas. Three detector types with different combinations of finger width and spacing were measured: $s = 0.35$ μm, $w = 0.15$ μm; $s = 0.3$ μm, $w = 0.2$ μm and $s = 0.25$ μm, $w = 0.25$ μm. The bias voltage during the measurements was 0 V. The measured capacitance values are in good agreement with theoretical values, Eq. (2.66); see Table 2.2 for exact measured and theoretical capacitance values. As estimated from the theory, minimization of the w/s ratio and the total detection area gives the lowest capacitance.

Table 2.2: Capacitance for MSMs (see Fig. 2.37).

w/s [μm]	meas./calc. [fF] (35 x 35 μm^2)	meas./calc. [fF] (25 x 35 μm^2)	meas./calc. [fF] (15 x 35 μm^2)	meas./calc. [fF] (10 x 35 μm^2)
0.15 / 0.35	125.2/116.6	85.4/84.2	49.8/48.6	32.1/32.4
0.2 / 0.3	171.7/136.1	111.3/98.3	55.3/56.7	32.5/30.2
0.25 / 0.25		122.1/113.6	71.7/69.9	45.3/48.1

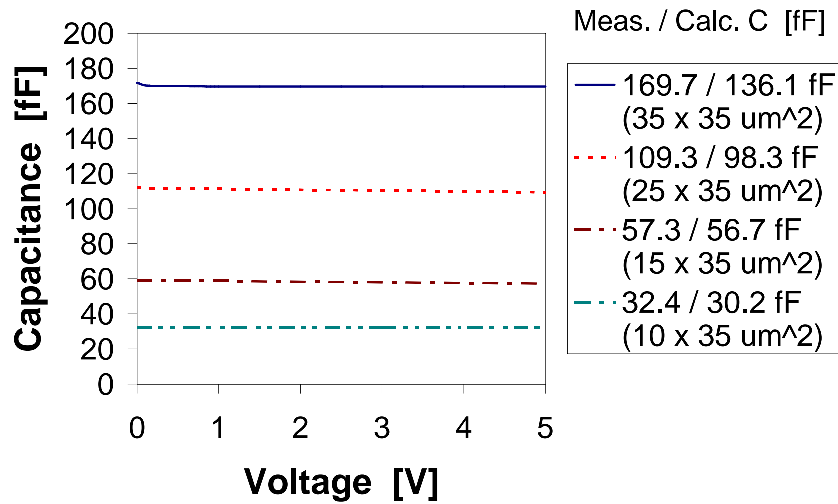

Figure 2.36: C-V characteristics for submicron MSM PDs with different detections areas (S.I. GaAs, $s = 0.3\ \mu$m, $w = 0.2\ \mu$m, Ti/Au = 50/250 nm), $f_{\text{test}} = 2$ MHz. Measured and calculated, 2D conformal mapping according to Eq. (2.66), capacitance values as indicated in the picture apply at 5 V.

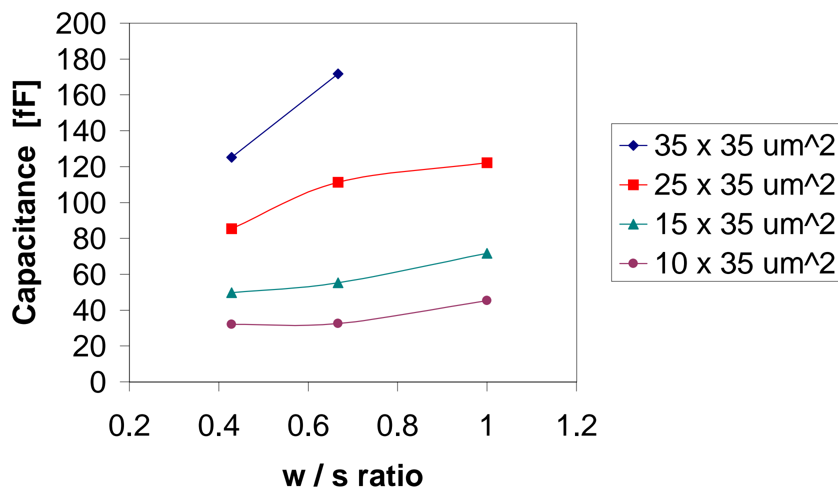

Figure 2.37: Capacitance as a function of w/s- ratio for submicron MSM PDs with different detections areas (substrate is S.I. GaAs, $V = 0$ V), $f_{\text{test}} = 2$ MHz.

The conductance was measured along with the capacitance measurements. In the simple equivalent circuit representing the finger structure, Fig. 2.20, a conductance (i.e. dark resistance) is connected in parallel with the capacitance, and is a measure of the leakage current. Figure 2.38 shows the conductance for three different-size devices. The leakage is small (in the nA range), and does not increase at higher bias voltages. E.g. at 2 V the resistances and corresponding leakage currents are 47.6 MΩ/42 nA, 30.3 MΩ/66 nA, 23.8 MΩ/84 nA for 10 x 35, 25 x 35 and 35 x 35 μm^2 size devices, respectively.

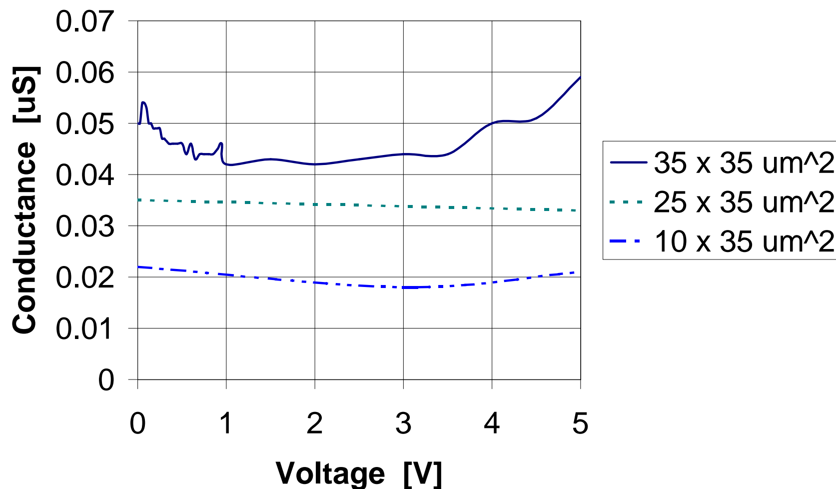

Figure 2.38: Conductance as a function of bias voltage for submicron MSM PDs with different detections areas, f_{test} = 2 MHz (S.I. GaAs, s = 0.3 μm, w = 0.2 μm, Ti/Au = 50/250 nm).

2.5.3 Photocurrent and Responsivity

The photocurrent as a function of the MSM bias voltage was measured using a Ti:Sapphire laser under CW operation (modelocked coherent MIRA 900) at different wavelengths: 800 nm, 850 nm and 900 nm for SOI-detectors; 720 nm and 780 nm for S.I. GaAs detectors. The intensity of the incident optical power was measured with a commercial power meter (the power range being between 1.2 - 252 mW for SOI, 4.3 - 35 mW for GaAs diodes). The difference in the power levels for SOI and GaAs detectors lies in the fact that the laser setup was different. Tuning and focusing of the beam (using lenses and attenuators) was done differently, thus giving rise to indicated power levels. The spot diameter of the incident light beam for both cases was larger than the MSM area, which is obviously not optimal since carrier diffusion from the surroundings may significantly affect the detected photocurrent. This is especially crucial for doped Si. (A proposal to eliminate the carrier-diffusion problem, and the estimation of the effective incident power level falling on the MSM, is the utilization of a circular shaped MSM, which size corresponds to the beam diameter; see also comments in Section 2.2.3 p. 19.)

The laser beam area was either calculated or measured, in order to be able to estimate the power density. Further, taking into account the MSM area, and assuming a beam spot without distortions from a Gaussian, the total power falling on the MSM detector could be estimated (being in the μW range). Finally, knowing the absolute power, the responsivity of the detector could be deduced.

SOI detectors

Figure 2.39 shows the photocurrent as a function of applied voltage and at different incident optical power intensities investigated at a wavelength of 800 nm for a SOI MSM PD with top Si layer thickness of 0.2 μm. When the bias voltage exceeds the flatband voltage the current saturates, which indicates a surface without recombination centers and defects, i.e. no leakage and gain phenomena. The reach-through voltage, Eq. (2.13), becomes $V_{RT} = 3.3$ V using $\phi_{Bp} = 0.7$ eV, $N_v = 1.04 \cdot 10^{19}$ cm^{-3}, $N_a = 10^{15}$ cm^{-3}, $s = 3$ μm and $\epsilon_r = 11.8$. The flatband voltage according to Eq. (2.20) gives 6.9 V.

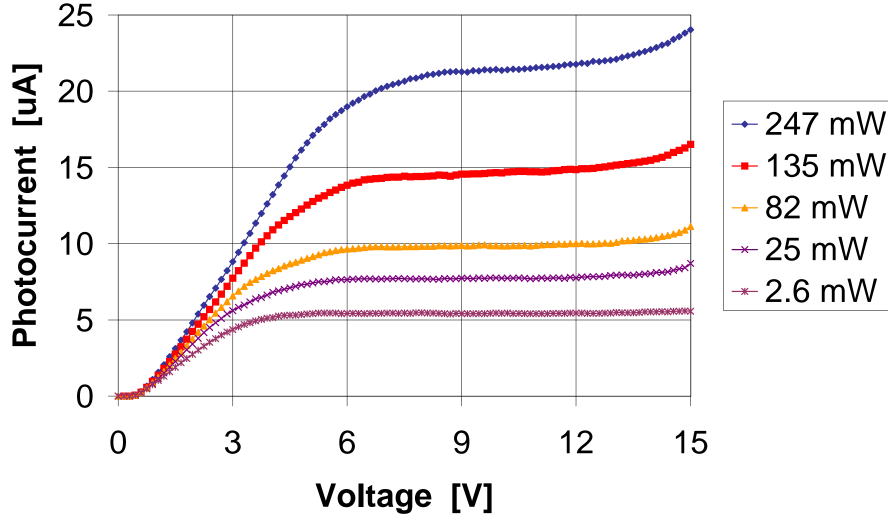

Figure 2.39: Photocurrent at different illumination levels at $\lambda = 800$ nm for a SOI MSM PD with p-type Si top layer with thickness of 0.2 μm ($s = w = 3$ μm, $A = 100$ x 100 μm^2).

A fitting to the I-V measurement is done according to the model described in Section 2.3.2, Eqs. (2.52) and (2.53); the result is shown in Fig. 2.40. The power levels indicated in the figure apply for the total laser beam spot. The fitting takes into account the diffusion of charge carriers from outside the optically active MSM area. Values used in the fitting are: $s = w = 3$ μm, $A = 100$ x 100 μm^2, $\epsilon_r = 11.8$, $d = 0.2$ μm, $\lambda = 900$ nm, $\alpha = 3.5 \cdot 10^4$ m^{-1}, $r = 30$ %, $m^* = 0.66$, $T = 300$ K, $\phi_{Bp} = 0.7$ eV, $N_a = 10^{15}$ cm^{-3}, $A_{laser} = \pi \left(\frac{1.22\,\lambda}{6 \cdot 10^{-4}}\right)^2$, $A_{diff.} = \pi\, D_n\, \tau_n$, where the diffusion constant is $D_n = 36.7$ cm^2/s and the carrier lifetime is $\tau_n = 10$ μs [79]. In addition to the fitting parameters $X = 0.18$, $B = 2.1$ V and $C = 0.38$ m^2/A, the internal quantum efficiency η_i is optimized, which if exceeding 1 is a measure of gain. Obtained values for η_i are: 7.35, 3.1, 2.27 and 1.48 for power levels of 16, 50, 76 and 150 mW, respectively. The corresponding flatband voltages are: 4.5, 5, 5.5 and 6 V. Less DC gain at higher power levels is attributed to the saturation effect: current does not rise linearly with increasing power due to the screening of the electrical field. The responsivity is therefore not a constant function of power, but in fact a decreasing function of illumination. It is noticeable though, that the photocurrent is a constant function of the bias voltage. This is explained by a good metal-semiconductor interface without defects and thus negligible leakage current (both bias-dependent tunneling and Schottky emission), even at high bias. The saturated photocurrent also explains the perfect fitting result, since in an ideal situation (detector without bias-dependent leakage current) the model is simply the definition for the constant photocurrent.

Since the MSM structure was not isolated from the surroundings (no mesa), and the laser beam spot exceeded the detector area, carrier diffusion from outside the active region may have to some extent increased the photocurrent. One possible explanation to the gain mechanism could be an avalanche multiplication effect. The high electric field between the fingers and a thin SiO_2-layer on top of the active substrate (native oxide) may lead to impact ionization along the surface (Section 2.2.5, model no 5). Also it is possible that trap induced electron injection over the reversed biased contact causes the internal quantum efficiency of greater than unity (Section 2.2.5, model no 1).

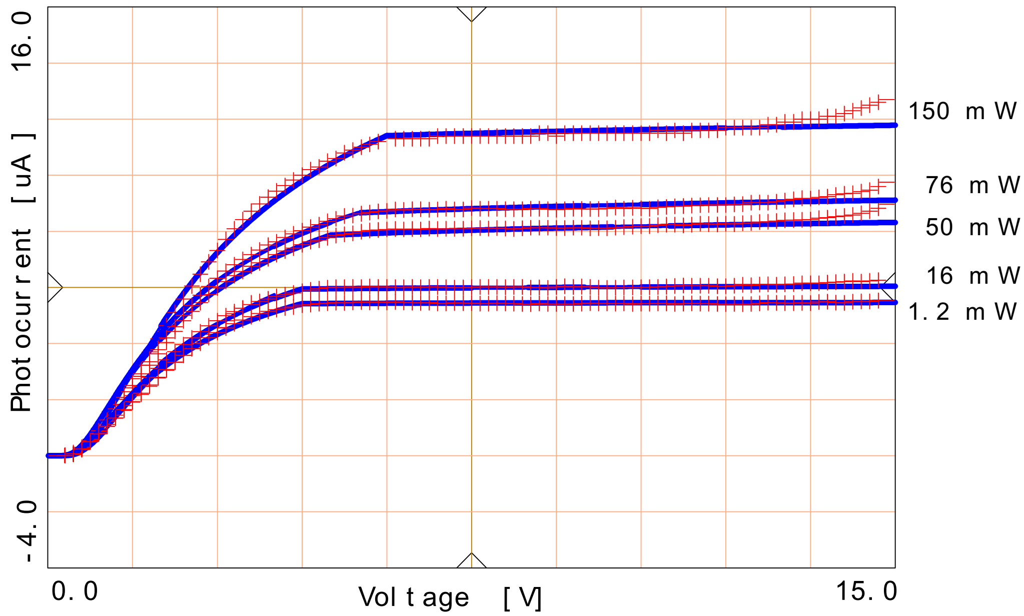

Figure 2.40: Photocurrent at different illumination levels at λ = 900 nm for a SOI MSM PD with p-type Si top layer of 0.2 μm ($s = w = 3$ μm, A = 100 x 100 μm^2). Measured (dotted line) and modelled (solid line).

The wavelength-dependence of the photoresponse is depicted in Figs. 2.41, 2.42 for SOI-detectors with 0.5 μm and 1 μm top layer thicknesses, respectively. As according to theory (see Section 2.2.3) the response is slightly higher for a lower wavelength (here at 800 nm higher response is achieved compared to that at 900 nm), attributed to a larger absorption coefficient at higher photon energies.

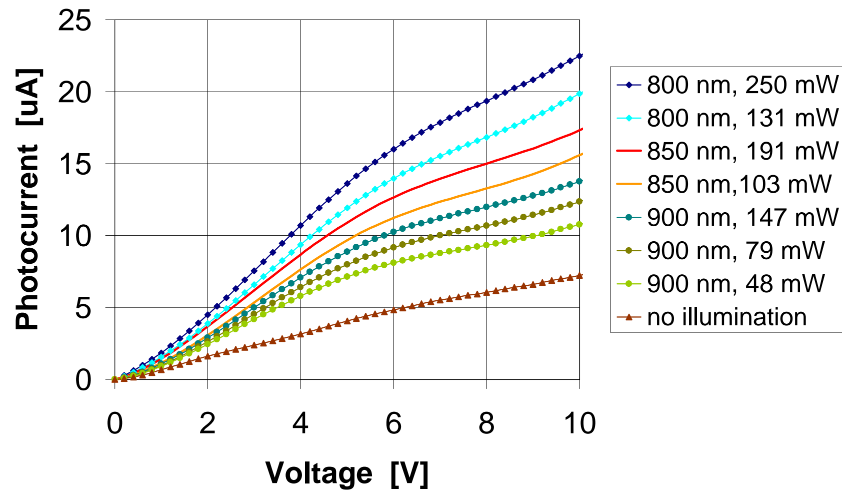

Figure 2.41: Photocurrent at different illumination levels at λ = 800 nm, 850 nm and 900 nm for a SOI MSM PD with p-type Si top layer with thickness of 0.5 μm ($s = w = 3$ μm, A = 100 x 100 μm^2, SiN coating).

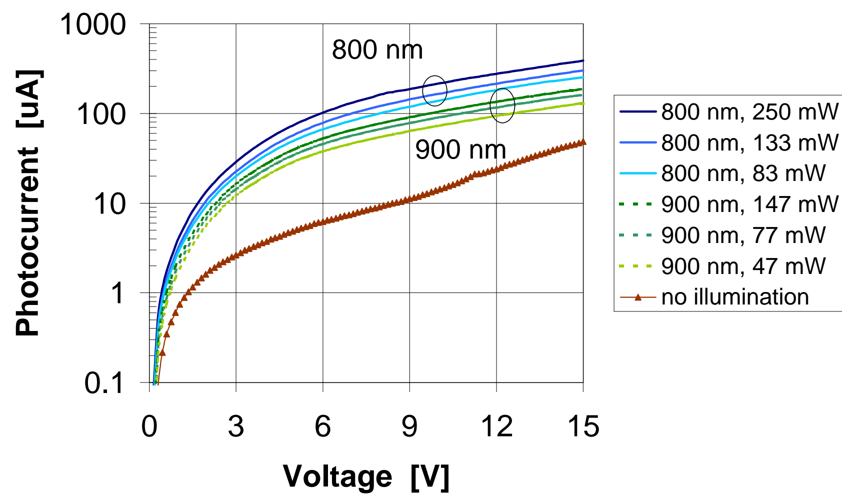

Figure 2.42: Photocurrent at different illumination levels at λ = 800 nm and 900 nm for a SOI MSM PD with p-type Si top layer with thickness of 1 μm ($s = w = 2$ μm, A = 100 x 100 μm^2).

The photocurrent measured for a 4 μm thick top layer SOI PD is depicted in Fig. 2.43, showing the increase of current with increasing illumination level. For the same device the wavelength dependence is presented in Fig. 2.44.

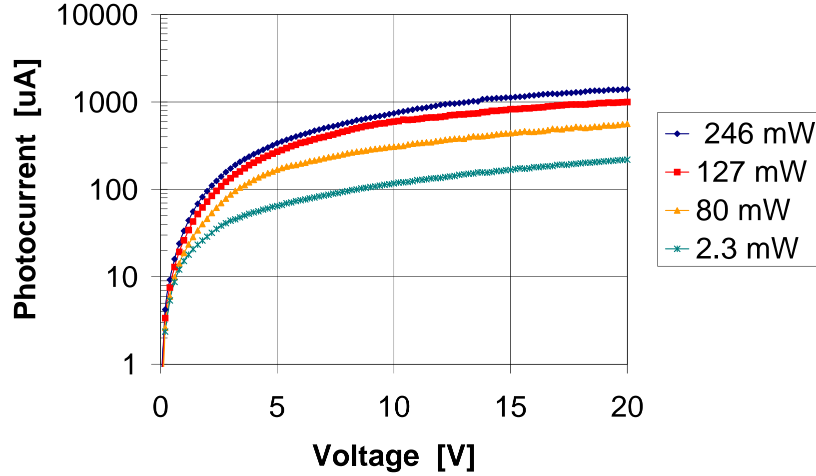

Figure 2.43: Photocurrent at different illumination levels at λ = 800 nm for a SOI MSM PD with n-type Si top layer with thickness of 4 μm ($s = w = 3$ μm, A = 100 x 100 μm^2).

The thickness of the active top Si layer directly influences the amount of photocurrent. This is presented in Figs. 2.45, 2.46, 2.47 and 2.48 for SOI PDs with various different top Si layer thicknesses, and illumination levels (measurement at wavelengths of 800, 850 and 900 nm). Also a bulk Si PD is measured to show the superior photoresponse compared to that of SOI detectors. As expected, for the thinnest top layer SOI MSM PD (0.2 μm) the photoresponse is the smallest. It is also obvious that with a higher excitation power level the photocurrent increases.

The external responsivity and the corresponding quantum efficiency is measured for different SOI detectors at 800 nm, Fig. 2.49. Hole-diffusion from the surroundings is taken into account, since the laser beam aperture exceeded the MSM area, thus giving a significant contribution to the observed photocurrent. The theoretical responsivity values are also indicated in the figure (calculated according to Eqs. (2.27) and (2.28) with $s/s+w = 0.5$, r = 33 %, $\eta_i = 1$ and $\alpha = 8.5 \cdot 10^2\,\mathrm{cm}^{-1}$): 3.6 mA/W (0.6 %), 9.0 mA/W (1.4 %), 17.5 mA/W (2.7 %), 33.6 mA/W (5.2 %), 62 mA/W (9.6 %) and 215 mA/W (33.4 %) for detectors with Si top layer thicknesses of 0.2, 0.5, 1, 2, 4 μm and the bulk-Si MSM, respectively. It is noticed that at a bias voltage around $\sim$ 5 V the measured responsivities are already higher than what the theory predicts. This is an indication of low frequency, bias-dependent gain. Table 2.3 indicates the external and internal responsivities/quantum efficiencies at two different bias points (6 V and 10 V). The internal responsivity is defined here as: $R_{in} = \frac{R_{ext}}{(1-r)(s/s+w)} = \frac{q\lambda}{hc}(1-e^{-\alpha d})\eta_i$ (the finger shadowing factor being 0.5 and the surface reflectivity 33 % at λ = 800 nm). The gain shown in the table is calculated using the theoretical values (listed above) as a reference.

It is seen from the figure that the responsivity for SOI structures depends mainly on the thickness of the top Si layer. Since the top Si layer in the studied structures is thin (d = 0.2 - 4 μm), and the optical absorption coefficient in the infrared small (e.g. $\alpha = 8.5 \cdot 10^2$ cm^{-1} at 800 nm $\Rightarrow \gamma = 11.8$ μm) the responsivity is severely limited by the factor $(1-e^{-\alpha d})$. The finger coverage of the optically active area further decreases the maximum achievable responsivity. In addition, since no *ARC* is applied, the surface reflectivity causes an even smaller external responsivity. Taking all these factors into account and assuming performance without any gain effects, the responsivity for SOI detectors with top Si layer thicknesses up to 4 μm is limited below $<$ 0.1 A/W.

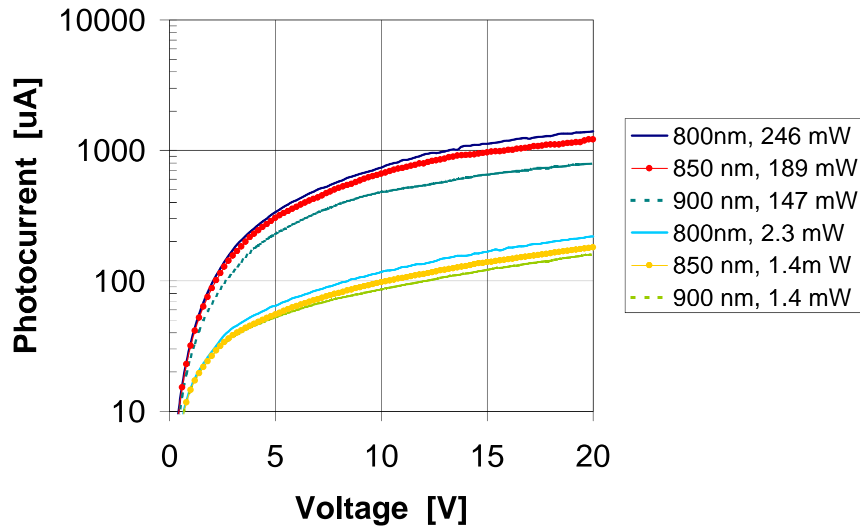

Figure 2.44: Photocurrent at different illumination levels at λ = 800 nm, 850 nm and 900 nm for a SOI MSM PD with n-type Si top layer with thickness of 4 μm ($s = w = 3$ μm, A = 100 x 100 μm^2).

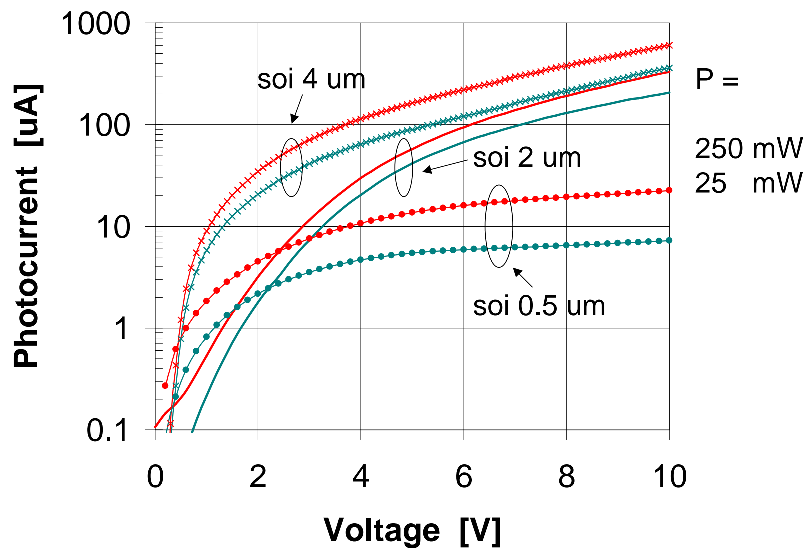

Figure 2.45: Photocurrent at different illumination levels at λ = 800 nm for SOI MSM PDs with Si top layer thicknesses of 0.5, 2 and 4 μm ($s = w$ = 3, 2 and 3 μm, respectively, A = 100 x 100 μm^2). All devices have SiN-coating.

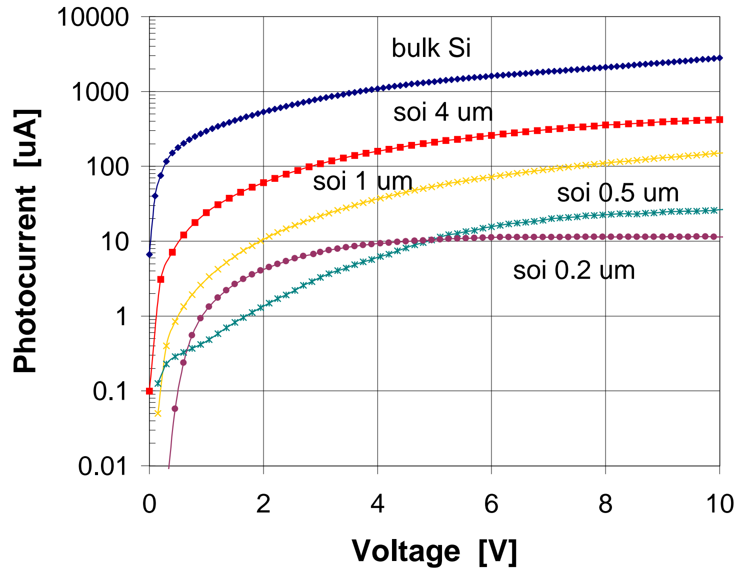

Figure 2.46: Photocurrent at a illumination level of 100 mW (107 μW on MSM) at λ = 850 nm for SOI MSM PDs with different Si top layer thicknesses and a bulk Si MSM PD (A = 100 x 100 μm^2, s and w either 2 or 3 μm).

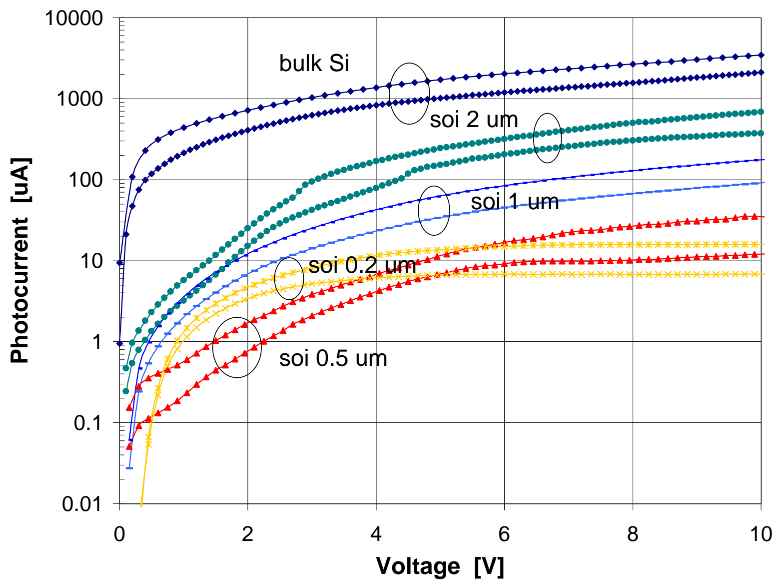

Figure 2.47: Photocurrent at illumination levels of 20 mW (21 μW on MSM) and 195 mW (208 μW on MSM) at λ = 850 nm for SOI MSM PDs with different Si top layer thicknesses and a bulk Si MSM PD (A = 100 x 100 μm^2, s and w either 2 or 3 μm).

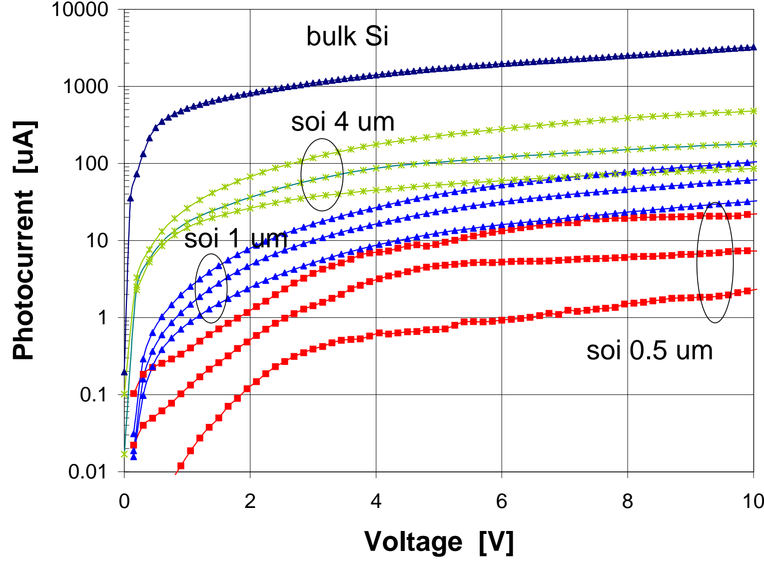

Figure 2.48: Photocurrent at illumination levels of 1.5 mW (1.4 μW on MSM), 15 mW (14 μW on MSM) and 150 mW (143 μW on MSM) at $\lambda = 900$ nm for SOI MSM PDs with different Si top layer thicknesses and a bulk Si MSM PD ($A = 100$ x $100\ \mu\text{m}^2$, s and w either 2 or 3 μm).

The responsivities achieved are comparable with other published results; previously responsivities of 7.3 mA/W (at 850 nm) and 70 mA/W (at 880 nm) were measured for SOI MSM PDs with top Si layer thicknesses of 170 nm and 4 μm, respectively [46], [44]. A SOI-structure with a top-silicon layer of 100 nm (100 nm finger spacing and width) has resulted in a responsivity of 5.8 mA/W at 780 nm [43].

The gain can be identified as surface-charge related processes: (a) Holes trapped close to the cathode in surface states and/or in a thin insulating layer between the metal and the semiconductor leading to additional carrier injection via tunneling through the reduced barrier (Section 2.2.5, model no 1), (b) avalanche multiplication along the surface (Section 2.2.5, model no 5).

Table 2.3: Responsivity of SOI-detectors at $\lambda = 800$ nm (see Fig. 2.49).

Bias voltage:	6 V	6 V	6 V	10 V	10 V	10 V
Si top layer thickness [μm]	R_{ext}/η_{ext} [mA/W, %]	R_{in}/η_{in} [mA/W, %]	gain	R_{ext}/η_{ext} [mA/W, %]	R_{in}/η_{in} [mA/W, %]	gain
0.2	3.3/0.52	10.0/1.55	0.92	3.4/0.53	10.1/1.57	0.93
0.5	7.4/1.2	22.1/3.4	0.83	13.8/2.1	41.2/6.4	1.5
1	23.7/3.7	70.7/11.0	1.4	48.0/7.5	143.3/22.3	2.7
2	43.2/6.7	129.1/20.1	1.3	100.0/15.5	298.6/46.4	3.0
4	93.3/14.5	278.6/43.3	1.5	138.8/21.6	414.3/64.4	2.2
bulk	234.8/36.5	700.9/108.9	1.1	302.5/47.0	902.9/140.3	1.4

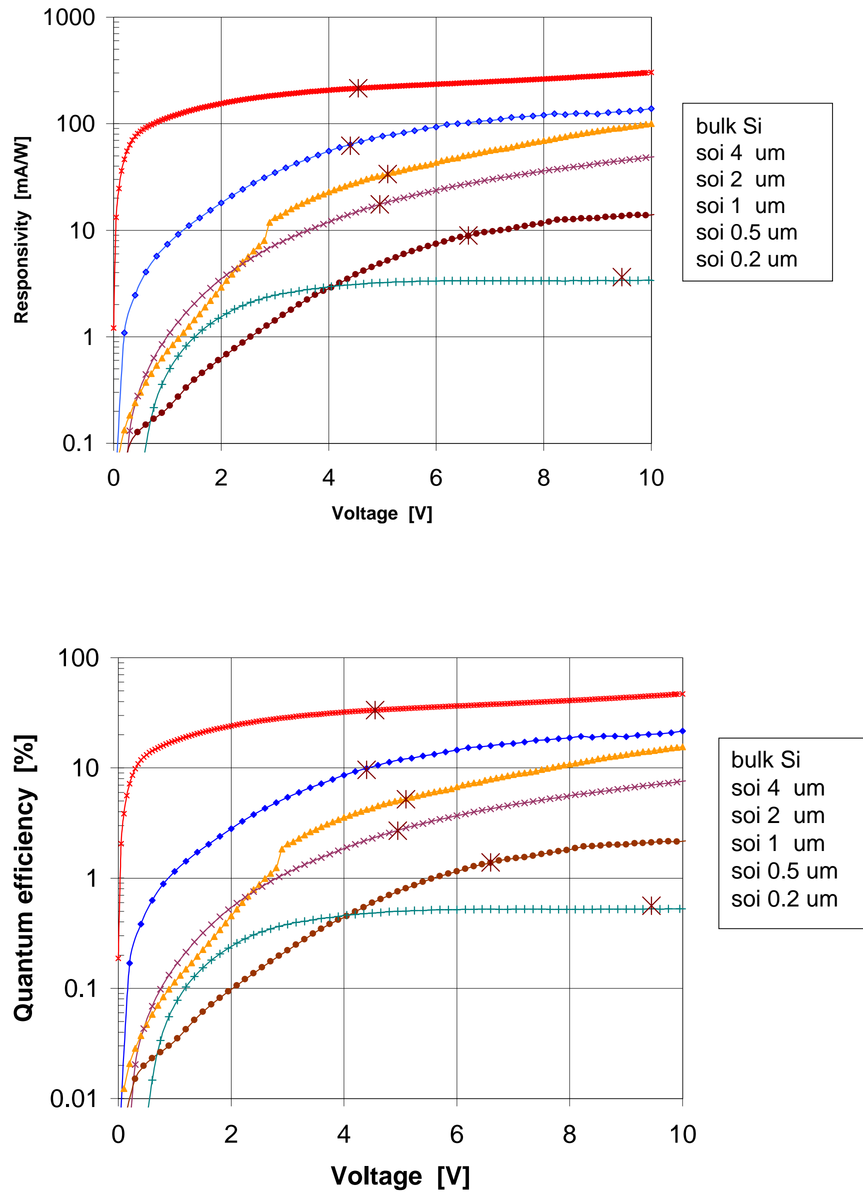

Figure 2.49: External responsivity and quantum efficiency at an illumination level of 25 mW (30 μW on MSM) at $\lambda = 800$ nm for SOI MSM PDs with different Si top layer thicknesses and a bulk Si MSM PD ($A = 100$ x $100\ \mu\text{m}^2$, s and w either 2 or 3 μm). The crosses indicate the theoretical values.

S.I. GaAs detectors

Figure 2.50 presents the photocurrent at a wavelength of 720 nm measured for submicron S.I. GaAs MSMs at two different power levels (6.2 mW corresponding to 77, 191 and 268 μW, and 29 mW corresponding to 358, 895 and 1253 μW for device sizes of 10 x 35, 25 x 35 and 35 x 35 μm^2, respectively). It is evident, that a higher level of optical power enhances the photocurrent. Also the bias voltage slightly increases the response. In addition it can be noticed, that a larger optically active area leads to a larger current.

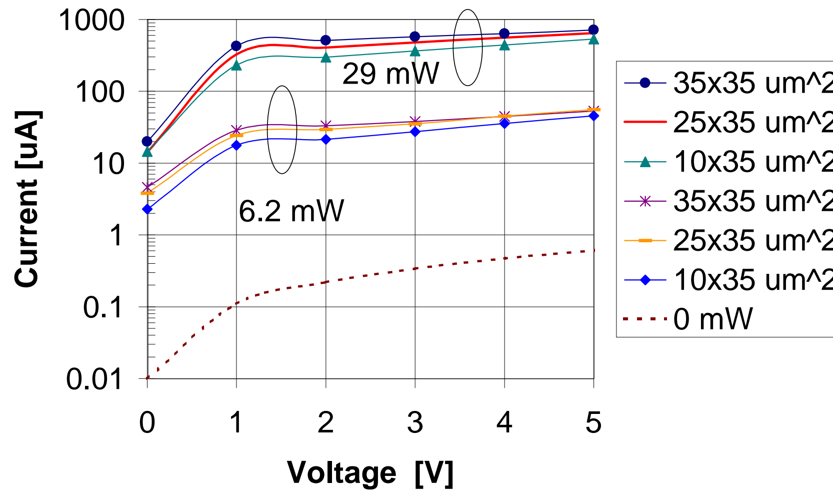

Figure 2.50: I-V characteristics for submicron S.I. GaAs MSMs at λ = 720 nm with different illumination levels (s = 0.3 μm, w = 0.2 μm). Also is indicated the measurement without illumination (room light).

Figure 2.51 shows the photocurrent at wavelengths of 720 nm and 780 nm measured for a submicron S.I. GaAs MSM with different illumination levels (4.3, 6.4, 7.9, 29 and 35 mW corresponding to 53, 79, 98, 358 and 432 μW for the MSM, respectively). At λ = 720 nm the photocurrent is somewhat higher than that at 780 nm. In addition, the power-level dependence can be seen.

The photocurrent is measured at two different wavelengths (720 nm and 780 nm) for submicron S.I. GaAs MSMs with different areas and power levels, Fig. 2.52 (6.4 mW corresponding to 119, 198 and 277 μW, and 7.9 mW corresponding to 146, 244 and 341 μW for device sizes of of 15 x 35, 25 x 35 and 35 x 35 μm^2, respectively). The area dependence can be seen in the results. In addition, a slightly higher response is achieved at λ = 720 nm. The theoretical responsivity for bulk GaAs at 720 nm and 780 nm, however, is 0.23 A/W and 0.25 A/W, respectively (the finger shadowing being 0.6, and r = 33.4 % and 33.0 % at 720 and 780 nm, respectively). (See also Fig. 2.13 in Section 2.2.3 for theoretical responsivity calculations.) On the other hand, the absorption depth of light at a wavelength of 720 nm is 0.52 μm ($\alpha = 1.93 \cdot 10^6$ 1/m), while at 780 nm it is 0.67 μm ($\alpha = 1.48 \cdot 10^6$ 1/m), which means that at a wavelength of 720 nm more photo carriers are collected before they recombine. Hence, the responsivity at 720 nm can be almost the same or even a bit more than at 780 nm.

Figure 2.53 plots the responsivity deduced from the I-V measurement (Fig. 2.52) at a wavelength of 780 nm for submicron S.I. GaAs MSMs. The optical power of the laser light beam is 7.9 mW ($P_{density} = 27.9\,W/cm^2$, scaling with MSM areas leads to 146, 244 and 341 μW for device sizes of 15 x 35, 25 x 35 and 35 x 35, μm^2, respectively). It can be seen that with decreasing size of the MSM area, the responsivity increases. This is probably due to the uncertainty in estimating the actual power falling on the MSM diode. The Gaussian shaped intensity distribution should be taken

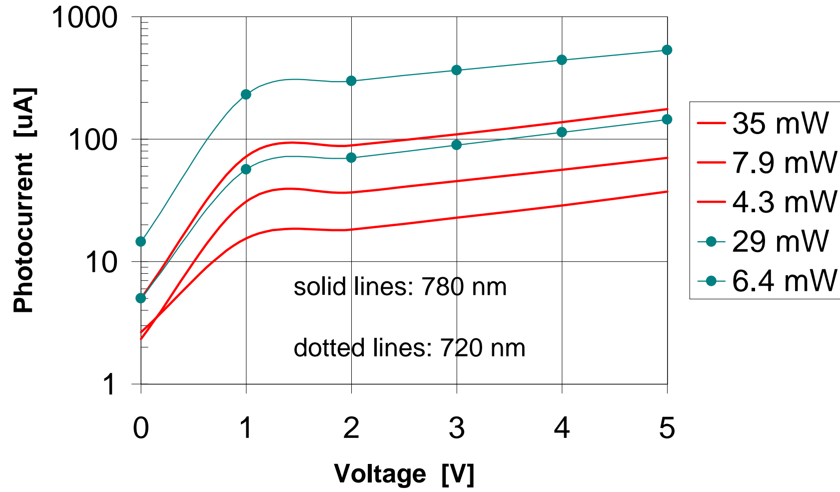

Figure 2.51: I-V characteristics for a submicron S.I. GaAs MSM at λ = 720 nm and 780 nm with different illumination levels (A = 10 x 35 μm^2, s = 0.3 μm, w = 0.2 μm).

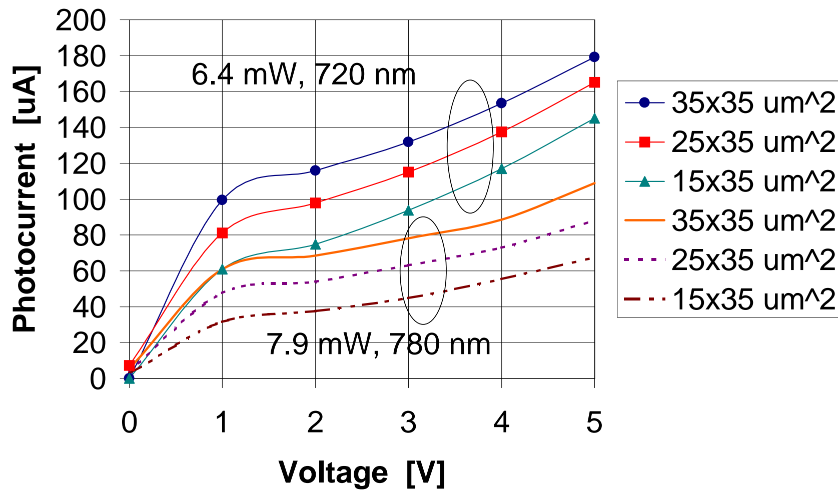

Figure 2.52: I-V characteristics for submicron S.I. GaAs MSMs at λ = 720 nm and 780 nm with varying MSM areas (s = 0.3 μm, w = 0.2 μm).

into consideration in order to get an accurate estimation for the power level. The achieved external responsivities at bias voltages around 2 - 4 V are in good agreement with the theoretical value of 0.25 A/W (η = 40.2 %)(see Eqs. (2.27) and (2.28), which take into account the surface reflection of 33 % at λ = 780 nm and the finger shadowing factor of 0.6). A slight DC gain is observed at higher voltages. With increasing voltage both the dark current, and the electric field around the finger edges increase, which most probably cause this gain effect. Furthermore, surface traps (holes) may lead to additional electron injection from the reverse biased electrode (Section 2.2.5, model no 1).

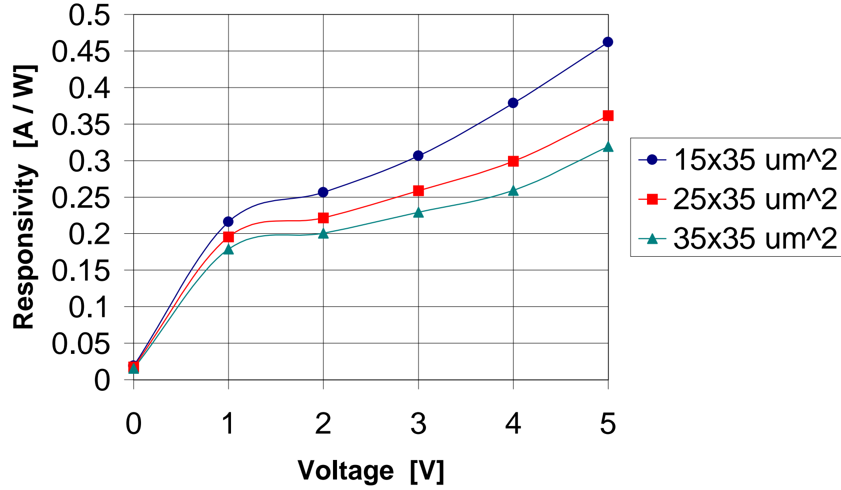

Figure 2.53: DC responsivity versus bias voltage for submicron S.I. GaAs MSMs with different areas at λ = 780 nm. P_{opt} = 7.9 mW (146, 244 and 341 μW on MSM PDs) (s = 0.3 μm, w = 0.2 μm).

The responsivity depends on the illumination level and the bias voltage, as is visible in Fig. 2.54 (corresponding I-V measurement in Fig 2.51). A high illumination level of 35 mW decreases the responsivity, indicating an optical saturation and screening effect.

Figure 2.55 depicts the responsivity at two different wavelengths (720 nm and 780 nm) (I-V characteristics in Figs. 2.50 and 2.52). The power level at 780 nm is slightly higher (7.9 mW) than at 720 nm (6.2 mW), hence a slightly greater difference in responsivities is observed than what is predicted by the theory, see Fig. 2.13. A voltage enhanced gain is visible, most probably caused by trapped photocarriers. Since the responsivity does not show a linear dependence on the voltage, a photoconductive-type gain as explained in Section 2.2.5 (model no 3) is not the origin. Instead, more probable is hole accumulation/trapping in surface states, which causes sweep-out and re-injection of electrons (either by tunneling or thermionic emission) in order to maintain charge neutrality in the space-charge region (Section 2.2.5, model no 1).

2.5.4 S-parameters

The S-parameters were measured and simulated for submicron S.I. GaAs detectors (both series and tapered configurations) with the HP85107A Network Analyzer System. The mask layout and corresponding equivalent circuit for the series and tapered MSM are seen in Sections 2.3.4 and 2.3.5, respectively. The measurement was performed with ground(G)-source(S)-ground(G) RF probes in the range from 50 MHz to 40.05 GHz (Cascade Microtech. probes). The electrical circuit parasitics of the detectors were determined from the measured S-parameter data.

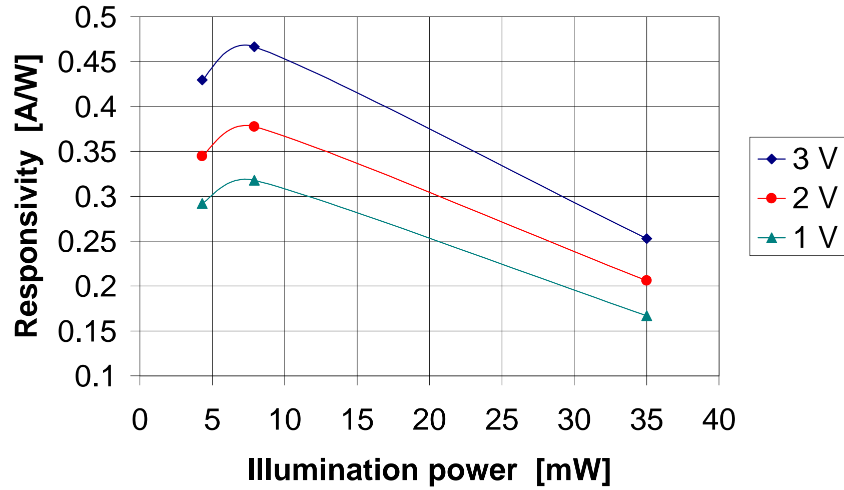

Figure 2.54: DC responsivity versus illumination power for a submicron S.I. GaAs MSM PD at different bias voltages at λ = 780 nm (A = 10 x 35 μm^2, s = 0.3 μm, w = 0.2 μm). P_{opt} = 4.3 mW (53 μW on MSM PD), P_{opt} = 7.9 mW (98 μW on MSM PD), P_{opt} = 35 mW (432 μW on MSM PD).

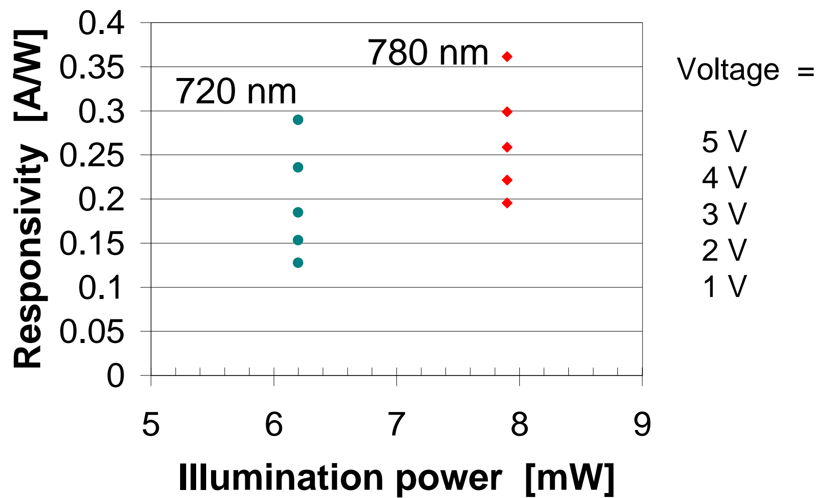

Figure 2.55: DC responsivity versus illumination power for a submicron S.I. GaAs MSM PD at wavelengths of λ = 720 nm and 780 nm. P_{opt} = 6.2 mW (191 μW on MSM PD), P_{opt} = 7.9 mW (244 μW on MSM PD)(A = 25 x 35 μm^2, s = 0.3 μm, w = 0.2 μm).

Series MSM

In Fig. 2.56 the measured and fitted S-parameters are plotted for series MSMs with varying sizes (see model in Fig. 2.22). Parameters obtained from the model-fit are indicated in Table 2.4, along with theoretical capacitance calculations based on 2D conformal mapping, Eq. (2.66).

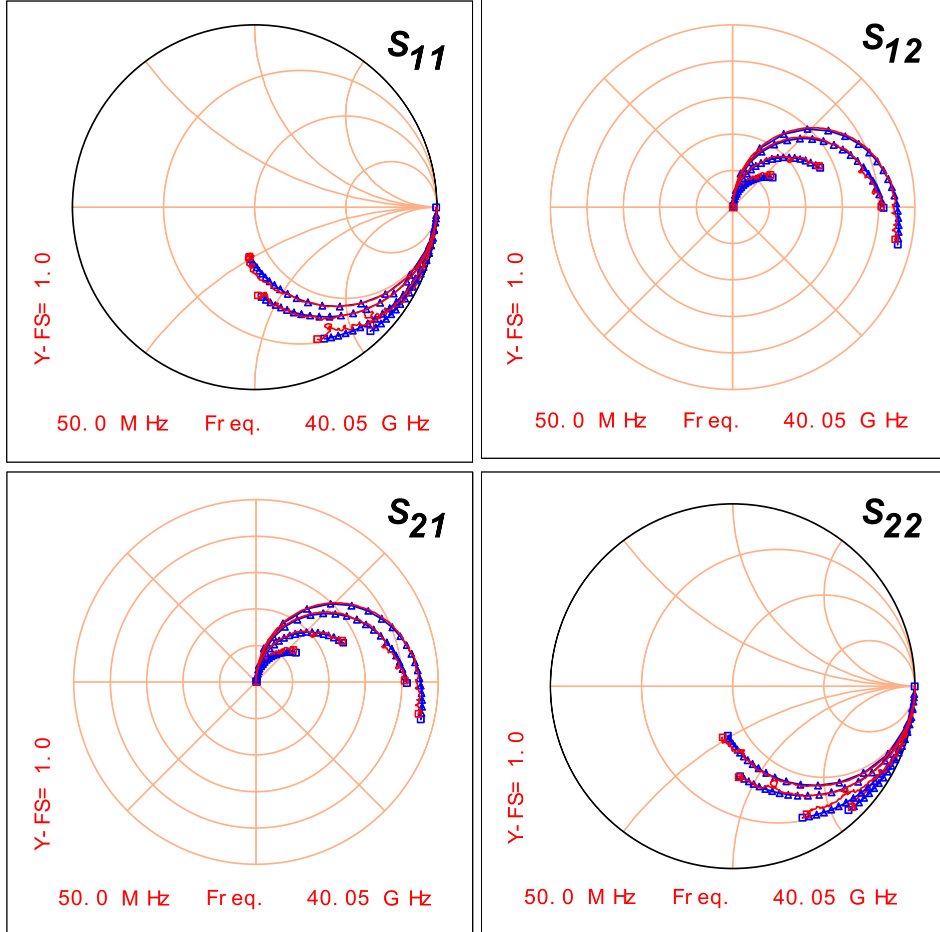

Figure 2.56: S-parameters in the frequency range from 50 MHz to 40.05 GHz. Measurement (solid) and model fit (Δ) for series MSMs on S.I. GaAs with different areas (A = 35 x 35, 25 x 25, 15 x 15 and 10 x 10 μm^2, V = 5 V, s = 0.3 μm, w = 0.2 μm).

The measurements and fittings are done in three steps:

- An *open* series structure (i.e. no fingers between the pads) in order to get values for the parasitic input capacitances C_{in1} and C_{in2}. $C_{in1} = C_{in2}$ due to symmetry. The input capacitances are the same independent of the MSM area, since the metal pad widths as well as the distances to the metal frame are kept the same (only the length of the metal bars is varied according to the MSM area).
- A *filled* shorted series structure (i.e. metal connecting the pads) in order to get values for the parasitic edge capacitances C_{edge1} and C_{edge2}. $C_{edge1} = C_{edge2}$ due to symmetry, but different for each MSM area (since the distance in between the metal pads is changed). The smaller the MSM area, the more insignificant is the contribution of the fringing capacitances of the edges.
- A *real* device for obtaining the MSM characteristic values C_{msm}, R_s and R_{dark} (keeping $C_{in1,2}$ and $C_{edge1,2}$ fixed).

The equivalent circuit in the fittings for the open and filled structure consists of a series resistance connected in parallel with a capacitance.

Table 2.4: Fitting parameters for series MSMs, also is shown the theoretical capacitance.

MSM area	C_{msm} [fF]	C_{theory} [fF]	R_s [Ω]	R_{dark} [kΩ]	$C_{in1,2}$ [fF]	$C_{edge1,2}$ [fF]
35 x 35 μm^2	149.8	136.1	3.2	70.5	2.0	1.64
25 x 25 μm^2	73.0	70.2	4.5	26.8	2.0	1.04
15 x 15 μm^2	27.0	25.9	8.5	31.7	2.0	1e-2
10 x 10 μm^2	12.1	11.9	34.3	33.7	2.0	1e-3

From Fig. 2.56 it can be concluded that the model fit is quite accurate for all S-parameters and all sizes of MSMs. The obtained fit parameters are comparable with the theory, and represent the electrical characteristics of the detector very well.

Tapered MSM

Figure 2.57 shows the measured and fitted S_{11}-parameters for tapered MSMs with varying sizes (see model in Fig. 2.24). In Table 2.5 are the obtained fitting parameters, including also the measured and theoretical capacitance values (based on 2D conformal mapping theory, Eq. (2.66)). The conditions for the capacitance measurement were: dark environment, bias voltage 5 V, f = 2 MHz, AC-signal level 0.25 V (rms). The MSM capacitance values obtained from the measurements were achieved as follows: $C_{msm} = C_{measured}$ - $C_{reference}$, where $C_{reference}$ refers to an empty structure with no MSM fingers, i.e. an open structure.

Table 2.5: Fitting parameters for tapered MSMs, also is shown the measured and theoretical capacitance.

MSM area	C_{msm} [fF]	$C_{measured}$ [fF]	C_{theory} [fF]	R_s [Ω]	R_{dark} [$k\Omega$]	L_p [pH]	R_p [Ω]
35 x 35 μm^2	156.9	169.7	136.1	1.7	30.6	21.2	1.2
25 x 35 μm^2	95.6	109.3	98.3	2.6	33.4	17.2	1.4
15 x 35 μm^2	52.3	55.8	56.7	5.8	44.4	10.3	1.1
10 x 35 μm^2	26.5	32.4	30.2	15.1	20.6	10.8	1.3

The measurements and fittings are done in three steps:

• An *open* taper structure (i.e. no fingers between the metal bars) in order to get values for the parasitic input capacitance C_{in} and the parasitic edge capacitance C_{edge}. Since the dimensions of the tapered metal bar and the distance to the metal frame is the same independent of the MSM area (only the metal bar on the right side is shifted depending on the MSM area), the fringing capacitances C_{in} and C_{edge} are constant for all MSMs. The values obtained from open structure fittings are: C_{in} = 4.84 fF and C_{edge} = 5.96 fF.
• A *filled* shorted taper structure (i.e. metal connecting the tapered metal and the metal frame) in order to get the losses due to the metal frame, i.e. the inductance L_p and the series resistance R_p. L_p and R_p are fitted for each filled structure separately (keeping C_{in} and C_{edge} fixed).
• A *real* device for obtaining the MSM characteristic values C_{msm}, R_s and R_{dark} (keeping C_{in}, C_{edge}, L_p and R_p fixed).

The equivalent circuit in the fittings for the open structure consists of a resistance connected in parallel with C_{edge}, while for the filled structure L_p is connected in series with R_p, which are in parallel with C_{edge}.

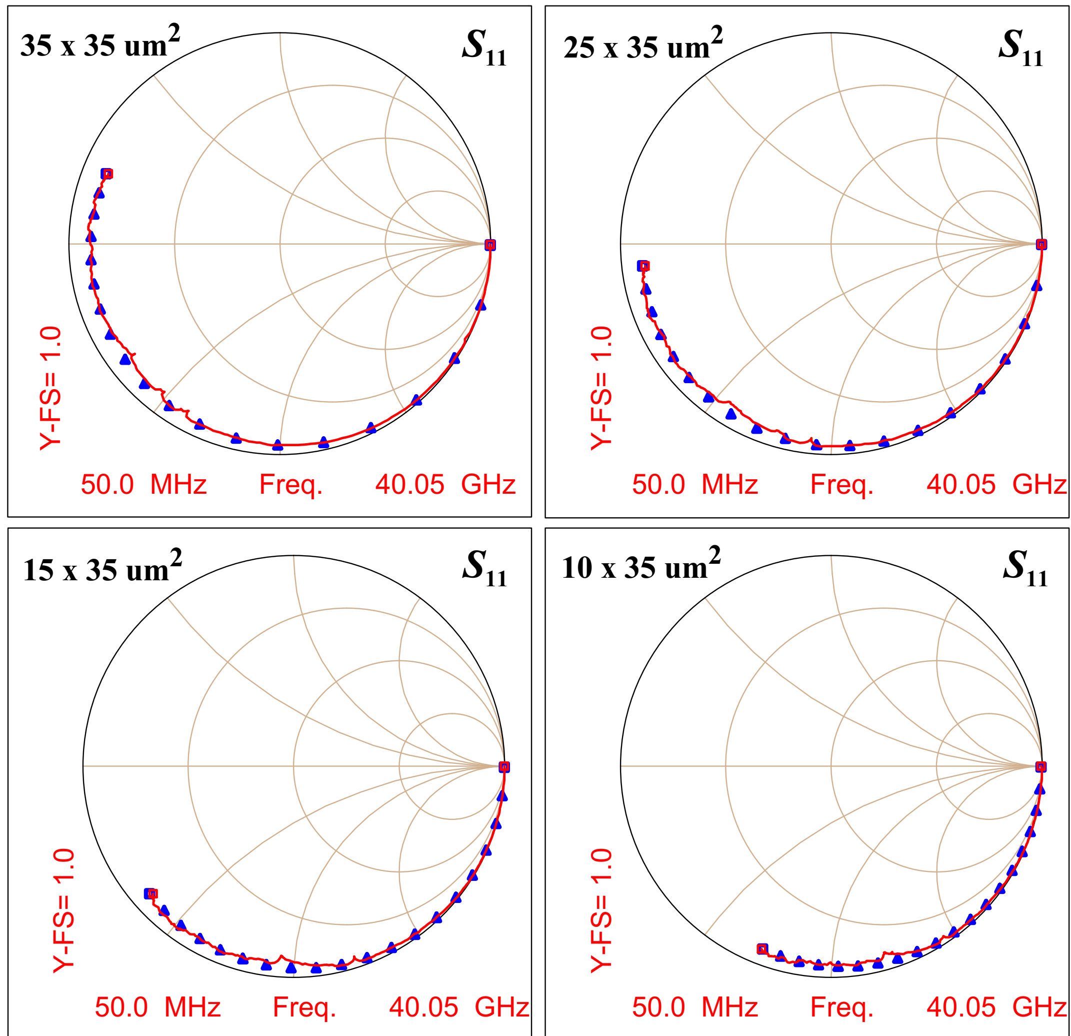

Figure 2.57: S_{11} in the frequency range from 50 MHz to 40.05 GHz. Measurement (solid) and model fit (Δ) for tapered MSMs on S.I. GaAs with different areas ($V = 5$ V, $s = 0.3$ μm, $w = 0.2$ μm).

Fig. 2.57 shows that the model fit is very accurate. Using pieces of coplanar lines for modelling the tapered metal bar, and the simple equivalent circuit for the MSM PD gives a good estimation of the electrical characteristics of the detector. Table 2.5 shows some difference between the theoretical as well as the measured MSM capacitance values. It has to be taken into account, that the 2D conformal mapping theory does not incorporate the metal thickness neither the contribution from the metal-air interface. Also it only accounts for the capacitance of one finger (with a certain length), and does not include the fringing effects at the edges of the electrodes where the electrical fields are stronger and contribute more to the real capacitance. The measured capacitances are a bit higher than the fitted values from the S-parameter measurements. This might be due to positioning of the probes always at the exact same position, darkness of the environment, temperature and charging effects. Measuring the capacitance as a function of voltage it was noticed, that there was a delay of seconds/minutes until the capacitance stabilized and saturated to a certain value. Raising the voltage increased the capacitance suddenly, but after some delay started to decrease. It is emphasized also, that the fitting with only one S-parameter (i.e. S_{11}) is less accurate than that of including all the S-parameters (as was the case for the series MSMs).

2.5.5 Pulse Response

The dynamic response was studied by exciting the detectors with a femtosecond Ti:Sapphire laser (pulse width 200 fs, repetition rate 76 MHz). For the SOI detectors the output signal was collected by a HP 54750A digitizing oscilloscope (HP 54751A 20 GHz module), while the results for GaAs detectors were monitored with a digital communications analyzer (HP 83480A) with a 40 GHz electrical sampling head (50 Ω load resistance). For the GaAs diodes the measurement was done directly on wafer; with the bias voltage fed through a bias-T. The SOI samples were bonded on a hybrid circuit consisting of a RC-circuit with load resistance of 10 Ω and capacitance of 3.3 nF. Since the measurement system for the SOI and GaAs samples is different (cables, connectors and tuning of the laser), the results presented in the following are not comparable with each other. Obviously more losses are induced for the SOI detectors through the bonding wires and the external RC circuit. In the measurements the rise and fall times are defined as 10 - 90 %, and the full width at half maximum ($FWHM$) as the pulse width at half the peak amplitude.

SOI detectors

The measured full width at half maximum was 100 ps (bias 20 V) and 142 ps (bias 15 V) for SOI PDs with 3 μm finger width and spacing and top Si layer thicknesses of 0.5 μm and 1 μm, respectively, Fig. 2.58. Using the approximation $f_{3dB} = 0.44/FWHM$, Eq. (2.36), the 3 dB bandwidth yields 4.4 GHz and 3.1 GHz for these detectors. Estimating the bandwidth from the rise time $f_{3dB} = 0.35/t_r$, Eq. (2.37), gives 5.5 GHz (64 ps) and 4.5 GHz (77 ps) for the 0.5 μm and 1 μm devices, respectively. Significant is that due to the buried SiO_2 layer an extended tail in the pulse response has been eliminated. Figure 2.59 presents the impulse measurement result for a SOI PD with finger width and spacing of 2 μm and top Si layer thickness of 4 μm. The $FWHM$ exhibits 302 ps (bias 8 V), which corresponds to 1.5 GHz, or deriving the bandwidth from the rise time gives a bandwidth of 1.8 GHz (198 ps).

For all measured diodes the $FWHM$ decreased by increasing the bias voltage, which leads to the conclusion that the speed is intrinsically limited by the transit time of the charge carriers. For comparison the transient response is shown in Fig. 2.59 for a bulk-Si MSM (finger width and spacing 2 μm). The bulk-detector has a larger $FWHM$ (446 ps at 15 V) and also a considerably long tail, extending to beyond 2.3 ns.

Calculating the theoretical bandwidth according to Eq. (2.35) for an MSM with A = 100 x 100 μm^2, $s = w = 3$ μm, and Ti/Au = 50/100 nm, the f_{3dB} becomes 10.1 GHz (using C_{msm} = 94 fF (2D conformal mapping), series resistance due to the metal fingers R_s = 1 Ω, Eq. (2.68), a 50 Ω environment and $v_s = 10^5$ m/s at an electric field of $E = 4 \cdot 10^4$ V/cm).

The transit time is 15 ps, which is larger than the RC time constant of 4.8 ps, thus being the main limitation to the total bandwidth. This was also shown in Fig. 2.15, Section 2.2.4: i.e. for an area of

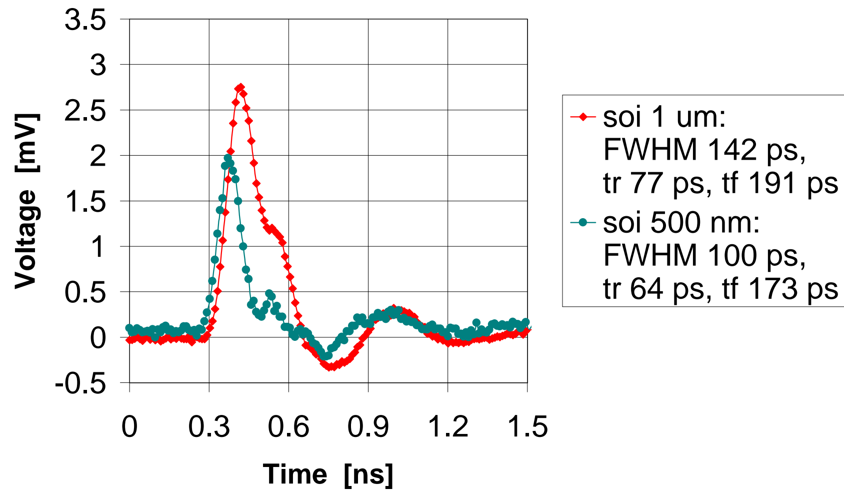

Figure 2.58: Transient response for SOI MSM PDs at λ = 800 nm. Top Si layer thicknesses are 0.5 μm and 1 μm, with bias voltages of 20 V and 15 V, respectively, P_{opt} = 3 mW, $s = w$ = 3 μm, A = 100 x 100 μm^2.

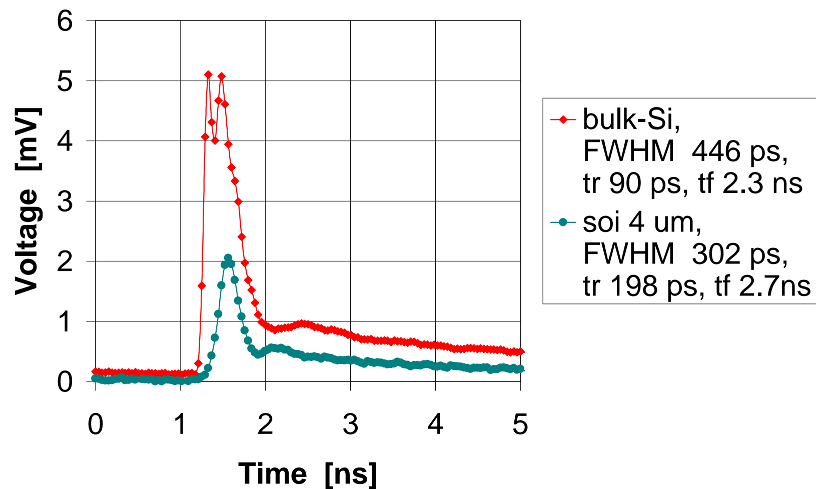

Figure 2.59: Transient response for a SOI MSM PD at λ = 800 nm. Top Si layer thickness is 4 μm, P_{opt} = 83 mW, V = 8 V. For comparison the impulse response is shown for a bulk-Si MSM PD (P_{opt} = 29 mW, V = 15 V). For both detectors $s = w$ = 2 μm and A = 100 x 100 μm^2.

100 x 100 μm^2 with finger spacings and widths exceeding 1.6 μm the speed is mainly limited by the transit time of the charge carriers rather than the external RC charging time. Estimating the speed for a detector with $s = w = 2$ μm, ($C_{msm} = 142$ fF using 2D conformal mapping), the f_{3dB} becomes 12.9 GHz.

The capacitance was measured for a SOI-detector (Fig. 2.33 in Section 2.5.2), exhibiting a saturation capacitance of 0.5 pF. Using now this value in Eq. (2.35) (MSM with $A = 100$ x 100 μm^2, $s = w = 2$ μm, Ti/Au = 50/100 nm, $R_s = 1$ Ω, Eq. (2.68), $R_L = 50$ Ω, $v_s = 10^5$ m/s at an electric field of $E = 4 \cdot 10^4$ V/cm), the f_{3dB} becomes 5.8 GHz. This is quite close to the measured bandwidth of 5.5 GHz for the SOI detector with 0.5 μm top layer. RC time constant is 25.5 ps, whereas the transit time $\tau_{tr} = 10$ ps, which indicates that the main limitation of the frequency response is caused by the large capacitance value.

S.I. GaAs detectors

Figure 2.60 shows the measured impulse response for submicron MSM PDs with various detection areas ($P_{opt} = 0.85$ mW, $V = 5$ V). The rise-and fall time, $FWHM$ and peak-to-peak voltages are recorded in Table 2.6. The speed for the different detectors lies in the same range. This is an expected result since the finger width and spacing for the measured detectors was constant ($s = 0.3$ μm, $w = 0.2$ μm). However, the smaller the detection area, the longer is the fall time. Also the peak-to-peak voltage decreases for smaller detectors. A second peak on the falling edge is clearly visible. This is most probably due to the optics in the measurement setup (the BK7 glass acting as an attenuator, and a beam splitter). Delay due to the BK7 glass (the thickness of the attenuating plate $l = 3$ mm, refractive index $n_r = 1.51246$ and 1.511 at $\lambda = 706.52$ nm and 768.2 nm, respectively) can be calculated: $t = l/v_p$, where the phase velocity in the glass is $v_p = v_{air}/n_r = 3 \cdot 10^8 \cdot 2/3$ m/s. The time delay due to two reflections yields 2 *15 ps = 30 ps.

It has to be noted that the obtained rise times and pulse widths do not represent the intrinsic speed of the detector. The rise time is severely limited by the measurement setup; i.e. the losses due to the probe head, the bias-T and the cable. In fact, a detector with 1 μm finger spacing and width was measured also, giving approximately the same rise times and pulse widths than obtained here for the submicron devices. Therefore, the observed results are the resolution limit of the measurement equipment. In order to evaluate the attenuation due to these external components, the S-parameters of the transmission path of head tips to the oscilloscope were measured at the tips for three different situations: a shorted, open and matched load (50 Ω). The equations for calculating the frequency dependent power loss, and a figure representing the loss is shown in Appendix C, Fig. C.1. The result is remarkable: the attenuation rises with increasing frequency reaching a value as high as 10 dB at 40.05 GHz, which corresponds to a correction factor of 10. The procedure for correcting for the power loss, and thus achieving the real slope for the rise time is explained in detail in Appendix C.

An approximation for the detector speed from the measurement results, using Eq. (2.37) with $t_r = 18$ ps yields a 3 dB bandwidth of 19.4 GHz. Using the definition in Eq. (2.36) with $FWHM$ of 27 ps gives a bandwidth of 16.3 GHz.

Calculating the theoretical bandwidth according to Eq. (2.35) for an MSM with $A = 25$ x 35 μm^2, $s = 0.3$ μm, $w = 0.2$ μm, Ti/Au = 50/250 nm, the f_{3dB} becomes 32.9 GHz (using $C_{msm} = 95$ fF (2D conformal mapping), series resistance due to the metal fingers $R_s = 0.34$ Ω, Eq. (2.68), a 50 Ω environment and $v_s = 2 \cdot 10^5$ m/s at a low electric field of $E = 3 - 4 \cdot 10^3$ V/cm).

It is seen that for the submicron detector the bandwidth is limited by the RC-time constant (4.8 ps) rather than the transit time (0.75 ps). This is also clearly confirmed in Section 2.2.4, in Figs. 2.15 and 2.16.

The detector intrinsic rise time and further bandwidth can be estimated taking into account the time delays in the measurement system.

Using
- f_{3dB}(probe) = 40 GHz $\Rightarrow$ t_r(probe) = 8.8 ps.
- f_{3dB}(cable) = 35 GHz $\Rightarrow$ t_r(cable) = 10 ps.
- f_{3dB}(bias-T) = 26.5 GHz $\Rightarrow$ t_r(bias-T) = 13.2 ps.
- t_r(measured) = 19 ps.

and solving the detector rise time from Eq. (2.38) (in which the total measured rise time is composed of the individual rise times, which add in square law) gives t_r(msm) = 3.1 ps, which corresponds to f_{3dB} = 113 GHz.

It has to be remarked, that the frequency calculated above is an overestimation of the actual detector speed. Like obvious from transient measurements, the impulse response which is the sum of electron and hole currents, is greatly influenced by the slow current component of the holes visible at the falling edge of the pulse.

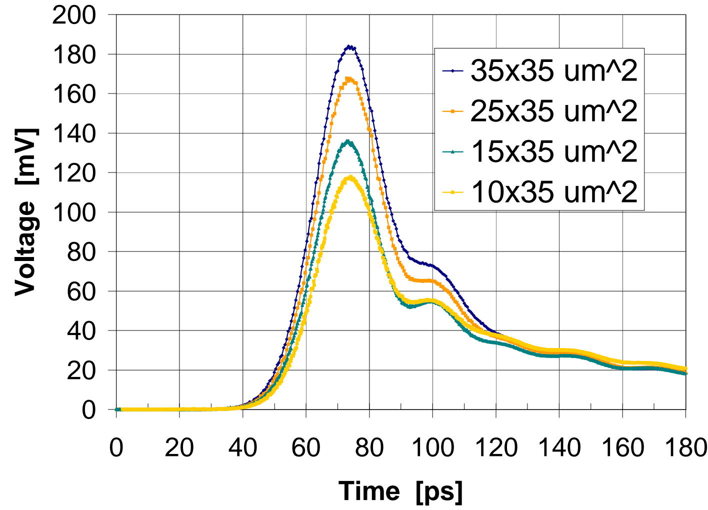

Figure 2.60: Pulse response of S.I. GaAs MSMs with varying detector areas measured at λ = 780 nm (P_{opt} = 0.85 mW, V = 5 V, s = 0.3 μm, w = 0.2 μm).

Table 2.6: Pulse response for e-beam MSMs (see Fig. 2.60).

MSM area [μm]	Rise time [ps]	Fall time [ps]	$FWHM$ [ps]	V_{pp} [mV]
35 x 35	19.1	103.0	27.6	183.5
25 x 35	18.4	116.0	26.4	167.4
15 x 35	18.2	151.1	25.6	136.3
10 x 35	18.5	180.6	27.6	117.2

In Figure 2.61 is plotted the pulse response of an MSM PD as a function of bias voltage (submicron fingers, S.I. GaAs-substrate). Since the finger distance is in the submicron range, full depletion between the fingers happens already at zero bias. This leads to fast collection of electrons (visible in the rising edge of the pulse response). The rise time and $FWHM$ are therefore almost constant independent of the voltage. However, increasing the bias voltage has an effect on the collection of the slow holes and thus the falling edge of the pulse response. A larger voltage, i.e. higher electrical field, causes the fall time to decrease, suggesting that the absorbing layer is fully depleted and that carriers are mainly generated in the high field strength regions. Furthermore, a larger bias voltage creates more charge carriers, and leads to an increased V_{pp}. The rise and fall time, $FWHM$ and peak-to-peak voltages are recorded in Table 2.7. The indicated fall times are obtained from the oscilloscope readings, which are a slight underestimation of the real full recovery pulse times. The entire recovery of the pulse extends for many detectors beyond 200 ps. For GaAs detectors the diffusion tail is more pronounced than e.g. for SOI detectors, studied earlier in this section.

Although with increasing bias the rise time appears to be constant, the fall times increase strongly at lower biases. This can be explained by the fact that the electric field at the surface is just high enough (V_{min} = 1 V) to ensure velocity saturation. At low bias this is not the case deeper in the substrate. Because of long lifetimes (tens of picoseconds) in the semi-insulating substrate, these carriers are collected at much lower speeds and cause the long tail in the response.

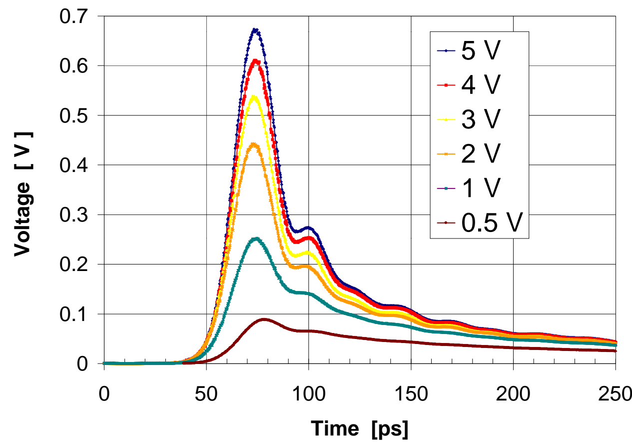

Figure 2.61: Pulse response of a S.I. GaAs MSM at λ = 780 nm with different bias voltages (P_{opt} = 5 mW, A = 15 x 35 μm^2, s = 0.3 μm, w = 0.2 μm).

Table 2.7: Pulse response for e-beam MSMs (see Fig. 2.61).

V [V]	Rise time [ps]	Fall time [ps]	$FWHM$ [ps]	V_{pp} [mV]
0.5	15.5			89.2
1	18.9			250.9
2	17.9	166.1	27.0	443.3
3	17.5	136.1	25.9	537.6
4	17.0	120.1	26.5	610.9
5	17.0	113.3	26.2	675.3

Figure 2.62 presents the pulse response of an MSM PD as a function of the incident optical power (submicron fingers, S.I. GaAs-substrate). The rise-and fall time, $FWHM$ and peak-to-peak voltages are indicated in Table 2.8. It is important to determine the optimum power level in order to obtain the desired fast rise- and fall times. A power level which is too low causes a long tail, whereas a power level which is too high leads to optical saturation, which further means screening of the initial electrical field and reduced collection speed for the charge carriers. Figure 2.62 shows clearly that with increasing illumination power the detectors become faster, and the V_{pp} increases.

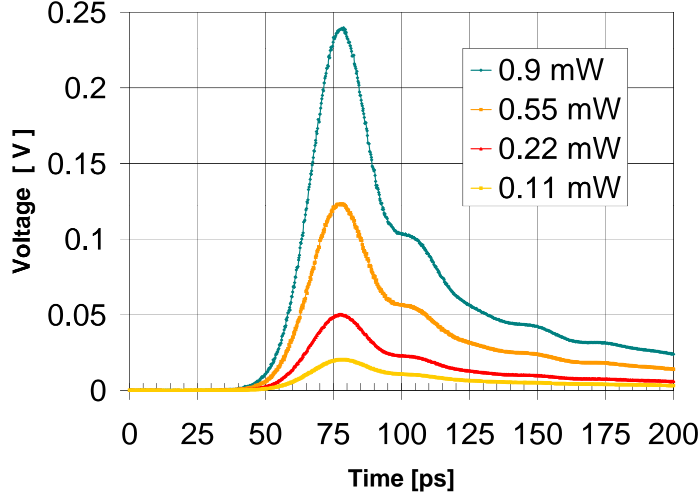

Figure 2.62: Pulse response of a S.I. GaAs MSM at λ = 780 nm with varying optical power levels (V = 5 V, A = 35 x 35 μm^2, s = 0.3 μm, w = 0.2 μm).

Table 2.8: Pulse response for e-beam MSMs (see Fig. 2.62).

P_{opt} [mW]	Rise time [ps]	Fall time [ps]	$FWHM$ [ps]	V_{pp} [mV]
0.11	19.3	180.9	40.1	20.7
0.22	18.7	146.7	29.5	50.4
0.55	18.8	141.4	29.6	123.6
0.9	18.9	117.9	28.3	239.8

Figure 2.63 shows the peak-to-peak voltage, and the AC responsivity as a function of illumination power for different size MSM PDs. Note that the x-axis is not linear, but shows the specific measurement points (i.e. power levels of 0.11, 0.22, 0.55, 0.9 and 4.6 mW).

The optical power of the beam spot was measured with a power meter. The measured power is, however, an average value, and the peak power during the short 200 fs pulse is considerably higher. In order to estimate the AC responsivity the laser light energy per pulse E_{opt} [J], defined by $E_{opt} = P_{avg}/76\,\text{MHz}$ needs to be calculated, 76 MHz being the repetition rate. The AC responsivity can be deduced by integrating the impulse response and dividing by the 50 Ω load resistance, which gives the number of photogenerated carriers during a single pulse. Dividing this by the pulse energy yields the responsivity.

The achieved AC responsivity is considerably lower than that obtained at DC conditions, even by a factor of ~ 10 (compare DC responsivity in Fig. 2.53). One reason is not accurately enough integrating the whole impulse response, i.e. not taking into account the long tail of the response. Also the pulse energy was distributed for a larger area than the detector itself. Therefore the energy on the detector was probably much less than the total energy of the beam spot, leading to a larger MSM-responsivity.

The dependence of the peak voltage, and hence responsivity (pulse spreading in accordance to the peak-to-peak voltage) on the illumination power indicates a small gain in the low power range (from 0.1 to 0.2 mW). From 0.2 mW until 0.9 mW V_{pp} is quite linear for all device-sizes, which indicates a nearly constant responsivity as a function of illumination, without either gain or optical saturation effects. At higher power levels (> 1 mW), however, screening of the incident electrical field starts to play a role, and leads to a decreased responsivity. The optimum power level of operation is therefore restricted to below 1 mW.

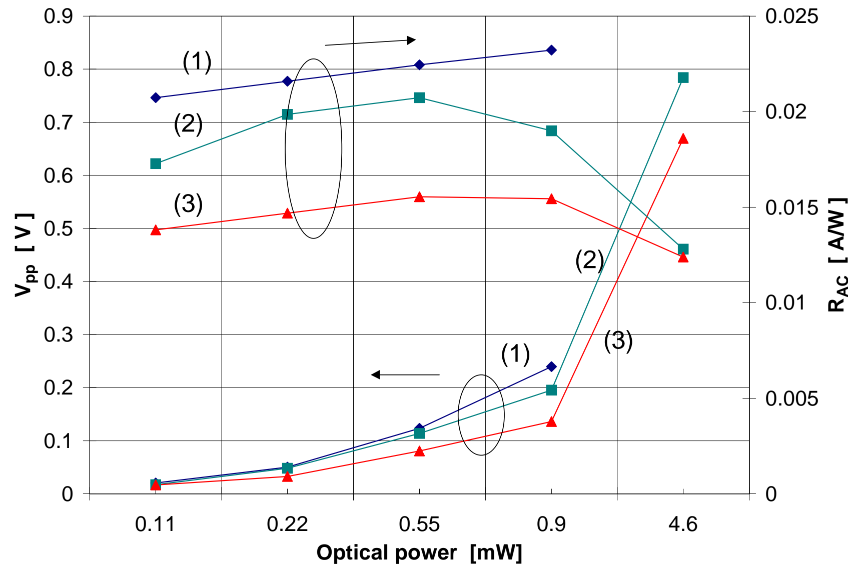

Figure 2.63: Peak-to-peak voltage and AC responsivity as a function of illumination power for different size MSMs for S.I. GaAs measured at $\lambda = 780$ nm with 0.2 ps laser beam pulse ($V = 5$ V, $s = 0.3$ μm, $w = 0.2$ μm). (1) $A = 35 \text{ x } 35$ μm^2, (2) $A = 25 \text{ x } 35$ μm^2 and (3) $A = 15 \text{ x } 35$ μm^2.

2.5.6 Opto-Electronic Response

Opto-Electronic (OE) measurements were done for submicron GaAs MSM PDs by illuminating the detector by a modulated DHS semiconductor laser beam at $\lambda = 855$ nm (laser diode current 160 mA at 2.43 V, $T = 0$ °C), fed through a glass fiber to the detector. The RF signal from the network analyzer was superimposed by a bias-T to the laser diode. The S-parameter measurements were performed in the frequency range from 50 MHz to 10.05 GHz. The dependence of the response on the MSM bias voltage is seen in Fig. 2.64. The ripples in the plots are not due to the detector, but due to the optical setup. The laser diode could have been tuned in such a way that the response would be straight, but at the expense of increased noise level. Also the fall off of the response at ca. 8.5 GHz does not represent the bandwidth of the detector, but is the limitation of the laser diode. By adjusting the micrometers of the x,y and z tables, the lens, the laser diode temperature, the current through the diode and the angle of the fiber with respect to the MSM-surface, the upper limit of the bandwidth could only be extended to 8.5 GHz. Also, at low frequencies the slightly higher level of the response is not due to the MSM characteristics, but is attributed to the higher efficiency of the laser diode modulation. The real bandwidth of the submicron PDs is certainly higher than that predicted in the plots, like already proved through impulse measurements in Section 2.5.5.

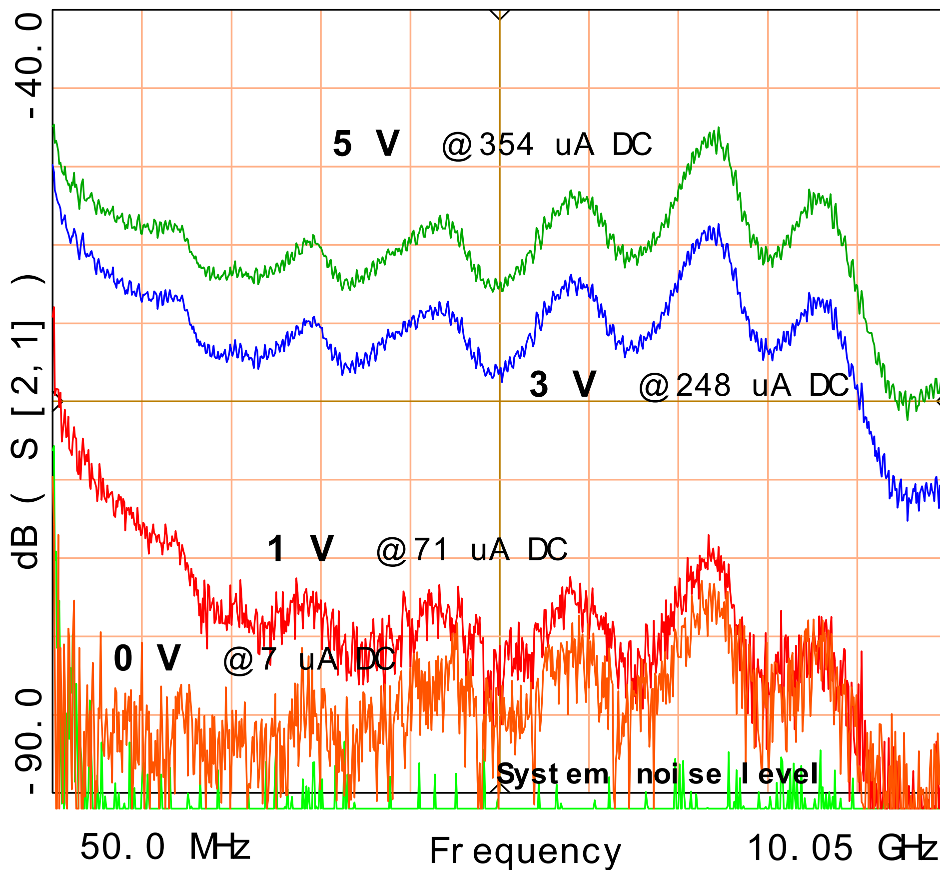

Figure 2.64: Opto-Electronic measurement for a submicron S.I. GaAs MSM PD at $\lambda = 855$ nm at different bias voltages ($A = 25$ x 35 μm^2, $s = 0.27$ μm, $w = 0.23$ μm, Ti/Au = 50/200 nm).

Figure 2.65 presents the OE response for detectors with different areas measured at a 5 V bias voltage. It is noted that the S_{21} is expressed in dBs, so that the area-dependence is not clearly visible. The exact DC current values are indicated in the figure.

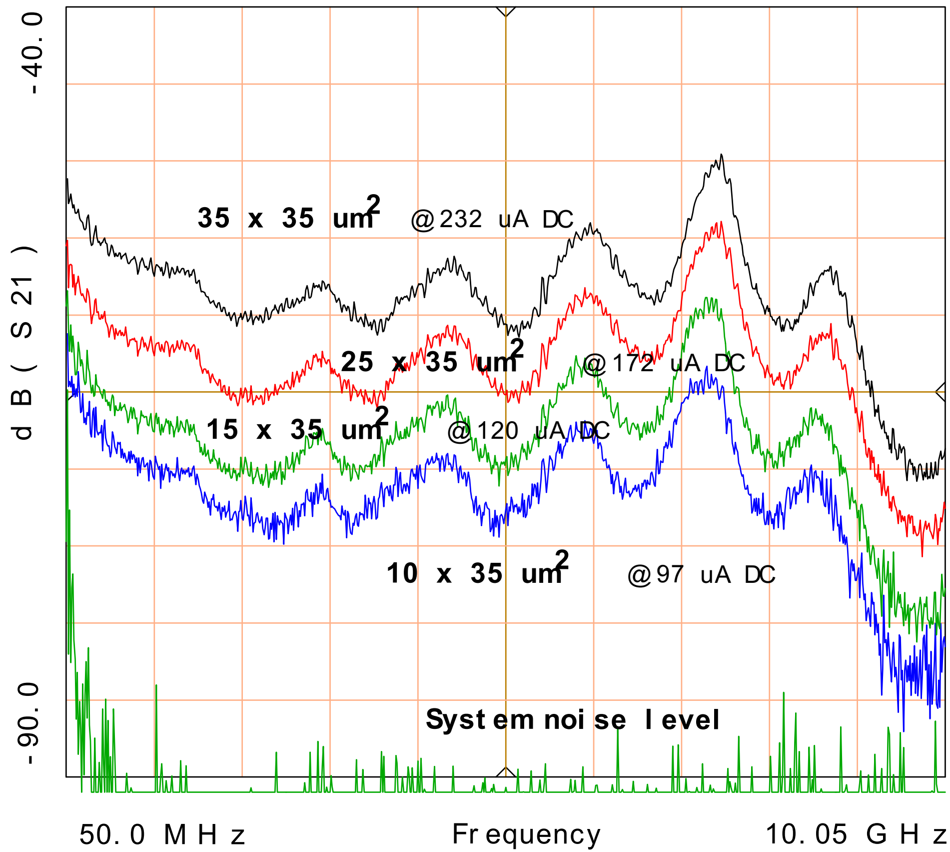

Figure 2.65: Opto-Electronic measurement at $\lambda = 855$ nm for submicron S.I. GaAs MSM PDs with varying areas ($V = 5$ V, $s = 0.3$ μm, $w = 0.2$ μm, Ti/Au = 50/250 nm).

Chapter 3

High Electron Mobility Transistor

3.1 GaAs pHEMT versus other HEMTs

In recent years an FET investigated intensively and with superior performance is the high electron mobility transistor (HEMT). The advantages derive directly from the superior transport properties obtained by using an undoped channel layer next to a doped, higher bandgap semiconductor. The carriers are accumulated at the heterojunction interface, and experience less scattering than in a doped channel with the majority carriers and doping impurities in the same region. At 300 K mobilities have been reported in the range of 8500 - 9000 cm^2/Vs, whereas GaAs MESFET doped to $N_d = 10^{17}\,cm^{-3}$ have demonstrated low-field mobilities of less than 5000 cm^2/Vs. The maximum frequency increases as the channel length decreases. Cut-off frequencies in the order of 100 GHz have been measured for channel lengths of 250 nm. For a HEMT with a single heterojunction of AlGaAs-GaAs interface electron sheet carrier densities in the order of $10^{12}\,cm^{-2}$ have been obtained. In the last few years HEMTs with an InGaAs channel have shown increasing interest, and promising results. There are three common types of InGaAs channel HEMTs:

(1) AlGaAs/InGaAs/GaAs strained, pseudomorphic HEMT (pHEMT)

(2) AlGaAs/InGaAs/GaAs metamorphic HEMT (MM-HEMT)

(3) InP-based AlInAs/InGaAs/InP HEMT (L-HEMT or strained, pseudomorphic HEMT)

• **GaAs – based pHEMT**

InGaAs cannot be grown lattice-matched to GaAs. The InGaAs channel is strained due to the mismatch between the substrate and the thin channel layer. The maximum In content of the channel is limited to 15 - 30 %, to prevent relaxation of the InGaAs layer, which would be accompanied by the formation of dislocations [3].

• **GaAs – based MM – HEMT**

MM-HEMTs offer the opportunity to combine a high In content with the processing and cost advantages of working with GaAs substrates. An MM-HEMT incorporates a thick buffer layer grown directly on the substrate to accommodate the large lattice mismatch between the InGaAs channel and the GaAs substrate. The role of this buffer layer is twofold: to lattice-match the channel layer and the substrate by formation of misfit dislocations, and to trap these dislocations and prevent their propagation into the device active layer. Using the metamorphic buffer, high quality unstrained InAlAs/InGaAs heterostructures with an arbitrarily chosen In content (from 30 to 80 %) can be grown [80]. An MM-HEMT $In_{0.4}Al_{0.6}As/In_{0.4}Ga_{0.6}As$ with T-shaped 0.1 μm gate length has demonstrated an extrinsic cut-off frequency f_t of 195 GHz and transconductance g_m of 720 mS/mm [81].

• **InP – based HEMT**

InP-based HEMT channel designs with substantially higher In content than the $In_{0.53}Ga_{0.47}As$ lattice-matched composition have increased restrictions on layer thickness due to lattice mismatch, thus limiting improvement in the channel transport properties. InP-HEMTs are possible to grow lattice matched in case the In composition is 53 % (sometimes referred to LM-HEMTs) (i.e. higher InAs mole fraction in the InGaAs channel). A higher In content 53 - 80 % results in a strained-channel, pseudomorphic

device [82]. InAlAs/InGaAs HEMTs on InP substrates have demonstrated extremely low noise figures and very high output powers. Devices with 0.3 μm T-gate InAlAs/InGaAs/InP structures have shown a cut-off frequency f_t of 116 GHz, maximum frequency of oscillation f_{max} of 229 GHz and a maximum DC transconductance of 697 mS/mm [83]. Even higher performance has been obtained for a 0.15 μm gate length device, for which f_t was found to be 160 GHz.

From a processing point of view, GaAs substrates are preferred for production of high performance monolithic micro- and millimeter-wave ICs because GaAs is less expensive and less fragile than InP, and is also available in sizes up to 6 inches in diameter. InAlAs/InGaAs MM-HEMTs on GaAs are attracting a great deal of interest for high frequency/speed applications, since they allow high In composition in the channel and thus a supplementary degree of freedom in the overall device performance optimization. As a general trend, f_t increases when the In content in the channel increases. As a consequence, MM-HEMTs show better performance than pHEMTs, and slightly lower performance than InP-based LM-HEMTs. The main difficulty, however, with the growth of the MM-structure concerns the metamorphic buffer layer. Also, the reliability of MM-HEMTs is still under investigation.

3.2 Functionality

The basic operation principle of a HEMT is very similar to other kind of FETs. The current is controlled by an electric field applied perpendicular to the direction of current. The current is in the channel region between the source and drain contacts. The major difference in a HEMT, however, is in the layer structure: use of a heterojunction and modulation doping (cross section is shown in Fig. 3.1).

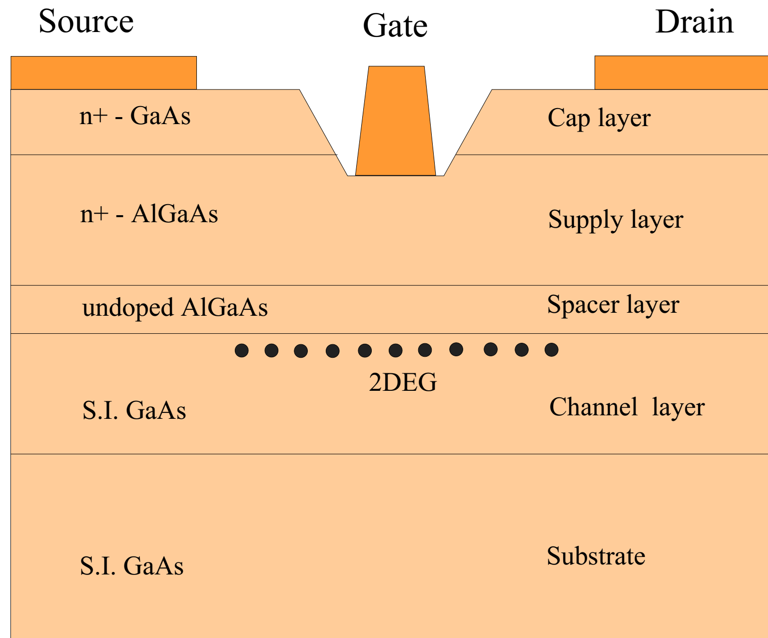

Figure 3.1: Cross section of an AlGaAs/GaAs HEMT.

The HEMT is thus sometimes referred to as a modulation doped FET: MODFET, heterojunction FET: HJET or selectively doped heterojunction FET: SDHT. In a HEMT-structure the channel region is undoped, and the electrons are supplied to it by a separate *supply* layer placed above the channel. The heterojunction has an abrupt discontinuity in the conduction and valence bands, forming a potential well in the undoped layer. Since the majority carriers and ionized impurities are separated from each other, scattering events are reduced, and increased device frequency characteristics is obtained.

The density of the carriers in the channel is controlled by a voltage applied to the Schottky gate. The carriers are confined in a potential well at the heterojunction, forming a two-dimensional electron gas (2DEG).

Figure 3.2 shows the conduction band of a GaAs-based HEMT, with the 2DEG formation at the heterojunction.

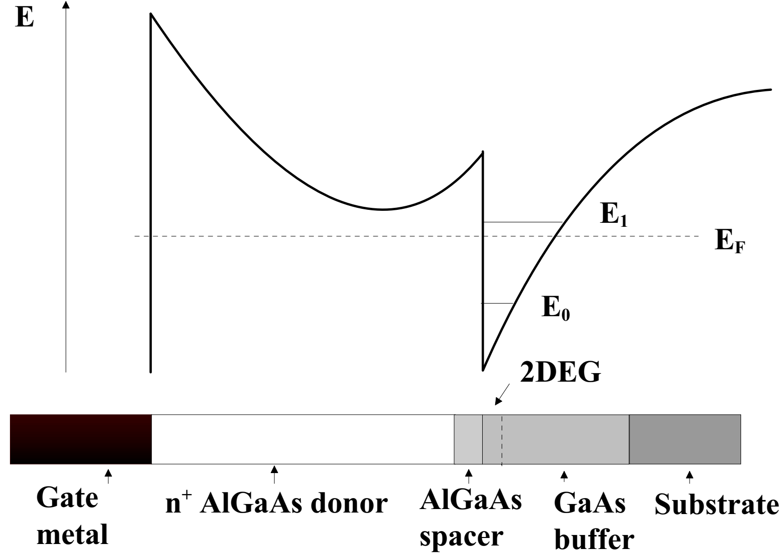

Figure 3.2: Energy band diagram of a GaAs-based HEMT.

In order to further increase the carrier mobility in the channel, an *undoped spacer* can be placed between the supply layer and the *channel layer*. The undoped spacer increases the separation of the ionized donor atoms in the supply layer from the free electrons in the 2DEG, and thus decreases the Coulomb interaction between these charges. Using the spacer layer also leads to a heterojunction interface free of any surface states. Therefore, both the impurity as well as the surface scattering are eliminated. The electron mobility in the heterojunction now only tends to be dominated by lattice or phonon scattering. An improvement in the low-field mobility and saturation velocity in the channel are ensured. Higher mobility results in large saturation currents, large transconductance values and high cut-off frequencies. In addition, $1/f$-noise due to surface states does not exist or is at least negligible, and the threshold voltage control is enhanced.

The thickness of the spacer has an important effect on the transistor performances. A thick spacer increases the electron mobility in the channel but lowers the electron transfer efficiency to the 2DEG, thus reducing the maximum 2DEG sheet concentration [84].

To improve the performance of a submicron FET, an optimum value of the supply layer thickness d_d is required. The ratio g_m/g_o (transconductance/output conductance) decreases by increasing d_d. It is shown that the magnitude of g_o is directly proportional to d_d, whereas g_m demonstrates an inverse relationship with it. Therefore in summary, to increase g_m and at the same time to reduce g_o, the supply layer should be thin ($d_d < l_g$) and heavily doped [85].

The effective minimum thickness d_m of the uniformly doped donor layer is given in [86] by:

$$d_m = \frac{n_s}{N_d} \ ,$$

in which n_s refers to the maximum channel sheet density and N_d to the doping concentration of the donor layer. The minimum thickness of the donor layer may be determined as a function of N_d for various space layer thicknesses.The minimum thickness of the donor layer, however, should be greater than d_m by a amount L_D, the Debye length:

$$L_D = \sqrt{(\epsilon_s k_B T)/(q^2 N_d)} \ ,$$

because an allowance for L_D is required from the end of the depletion region to the beginning of the neutral region. The minimum value of the donor layer thickness is thus the sum:

$$d_d \geq d_m + L_D \ .$$

An estimation of the 2DEG layer thickness is also desired; this however depends on the spacer layer thickness.

Figure 3.3 shows the energy band diagram of an enhancement mode GaAs-based HEMT under different gate voltage conditions.

- With zero bias the conduction-band edge in the GaAs is below the Fermi level, implying a large density of the 2DEG.
- When a sufficiently large negative voltage is applied to the gate, the electric field of the Schottky gate depletes the 2DEG-layer in the potential well. The conduction-band edge in the GaAs is above the Fermi level, implying that the density of the 2DEG is very small and the current in the FET would be essentially zero.
- A positive voltage applied to the gate will turn on the device, i.e. the density of the 2DEG will increase.
- Increasing the gate voltage further will increase the 2DEG density until the conduction band of the AlGaAs crosses the Fermi level of the electron gas. At this point the depletion approximation loses its validity and the donor layer starts to be neutralized by electrons. The gate loses control over the electron gas due to a parallel conduction path in the AlGaAs.

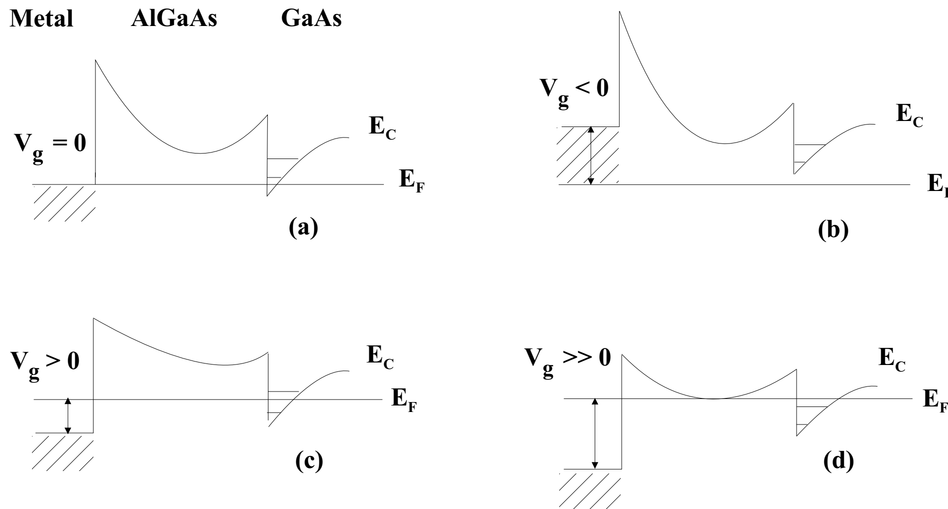

Figure 3.3: Energy band diagram of a GaAs-based HEMT: (a) with zero gate bias (b) with a negative gate bias (c) with a positive gate bias, 2DEG conduction (d) with a large positive gate bias, parallel conduction in the AlGaAs. E_F refers to the Fermi-energy level in the semiconductor.

3.3 Device Structure

In a typical GaAs-based HEMT the channel layer consists of undoped GaAs, the spacer of undoped AlGaAs, and the supply layer of doped AlGaAs or a thin delta-doped planar region within the AlGaAs layer, see Fig. 3.1. Some structures have doped layers on both sides of the channel; mainly in applications where both high cut-off frequency and increased power handling (medium and high power) capability are expected. HEMTs with even higher performance utilize an InGaAs channel layer, in order to take advantage of the superior electron transport properties of this material compared to GaAs.

For HEMTs with an $In_xGa_{1-x}As$ channel, increasing the In concentration results in higher electron mobility and peak saturated velocity in the channel, attributed to a decrease of the electron effective mass. InGaAs also has a lower bandgap compared to GaAs, thus leading to a higher conduction band discontinuity at the InGaAs-AlGaAs-interface, and enhanced carrier confinement in the 2DEG. Two contradictory effects, however, can be observed when the In value is varied. On one hand, the increase of the In mole fraction leads to better transport properties: enhanced electron mobility, saturation velocity and hence higher gain. On the other hand, the sheet carrier density in the InGaAs channel decreases when the In content increases (from 30 to 60 %) due to the decrease of the conduction band discontinuity [87].

In this work a GaAs-based pHEMT with Si atomic planar doping and an InGaAs-channel was chosen as the structure to be investigated. Tables A.1 and A.2 show the detailed layer sequences for pHEMT1, pHEMT2 and pHEMT3. The basis for the pHEMT wafer structures was previous research performed at TUE by J. Wellen [27]. Slight modifications concerning layer thicknesses and doping levels were designed by the author, in order to optimize and enhance the transistor/circuit performance. The structures were grown at Quantum Epitaxial Designs, Inc./USA. A *highly doped GaAs layer* ($2 \cdot 10^{18}\,cm^{-3}$) is grown on top for the ohmic contacts to ensure low contact resistance and thus thin barrier for carriers to tunnel through. The thickness of this top cap layer is set to 20 nm, to facilitate the gate recess etching through this thin layer (compare top layer thickness of 70 nm by J. Wellen). Under normal operating bias, the cap layer is fully depleted, and it does not give rise to the gate leakage problem. However, a too thin (e.g. 5 nm) cap layer can result in an increase in source access resistance and ohmic contact resistance [88]. An *AlAs etch-stop layer* is grown underneath the cap layer, the purpose being accurate control of the gate recess depth. A 30 nm thick *undoped AlGaAs layer* as opposed to 35 nm thick doped AlGaAs (previous work by J. Wellen) was chosen for the gate layer. The intrinsic AlGaAs increases the Schottky barrier height compared to that of doped AlGaAs and thus the gate breakdown voltage.

Under the gate layer lies a *Si-delta doped supply layer* with a doping concentration of $5 \cdot 10^{12}$ cm^{-2}. An atomic planar pulse-doping layer was chosen instead of a uniform donor supply layer with advantages of:

- An increased charge transfer into the InGaAs channel.
- Lower parasitic conduction in the AlGaAs Schottky layer.
- Reduced magnitude of the electric field near the edge of the gate electrode which greatly impacts the device output conductance and breakdown characteristics.

Finally, an *InGaAs channel layer* follows separated with a 3 nm thick *AlGaAs spacer layer* (Al composition 23 %) from the supply layer. In order to ensure high mobility and high carrier concentration the In composition in the InGaAs channel and the thickness of this layer were set to 20 % and 12 nm, respectively. A slightly higher composition and thicker channel layer (e.g. 25 % In, 15 nm thick) could lead to enhanced mobility and carrier concentration. However, these higher values are already close to the limit of relaxation, which means degraded overall device performance.

The distance from the Schottky gate to the InGaAs channel is 33 nm, slightly lower than that (38 nm) for J. Wellen's structure. The gate-to-channel distance was decreased since reducing the gate length the gate length/gate-to-channel -ratio (the so-called aspect ratio, which is explained in more detail in Section 3.4.5) has to be optimized as well for high frequency performance. For the designed gate lengths of 1, 0.6, 0.4, 0.3, 0.2 and 0.16 μm the aspect ratio becomes 30, 18, 12, 9, 6, and 5, respectively. In literature the limit for the gate-to-channel-aspect ratio for an InGaAs-channel HEMT is defined as 3 [89].

Underneath the channel layer a 50 nm *GaAs buffer layer* follows, and further an other *AlAs etch stop layer*. The second etch stop layer serves for the integrated receiver applications, and will be explained in Section 4.2.

3.4 Theoretical Analysis

3.4.1 Charge Control Model

The charge-control concept determines the 2DEG sheet charge concentration as a function of the gate potential. The potential profile from the gate electrode to the heterointerface fixes the electron distribution. A linear approximation between 2DEG sheet concentration and gate voltage V_g can be derived using depletion approximation, i.e. charge control model. For devices with gate lengths less than 0.5 μm, most of the channel is velocity saturated, and it is the saturation velocity that is of interest [90].
The wavefunctions of an electron in a linear potential consist of Airy functions. The allowed quantized energy levels in the triangular well are approximated by the formula [91]:

$$E_n[\text{eV}] = \left(\frac{\hbar^2}{2\,m_l{}^*}\right)^{1/3}\left(\frac{3}{2}\pi q E_s\right)^{2/3}\left(n+\frac{3}{4}\right)^{2/3}\;;\;n=0,1,2,... \tag{3.1}$$

where E_s is the quasiconstant electric field in the potential well (triangular well approximation), and $m_l{}^*$ is the longitudinal effective mass.
If $E_s = 10^5$ V/cm ($n_s = 7.2\cdot 10^{11}$ cm^{-2} using Eq. (3.3)) and $m^* = 0.0779$ the energy for the lowest level is $E_0 = 0.085$ eV and for the next ones: $E_1 = 0.15$ eV and $E_2 = 0.20$ eV. The thermionic energy at room temperature ($T = 300$ K) is $k_BT = 0.026$ eV. The subband-separation is $> k_BT$, which means that the quantization of the energy levels is significant.

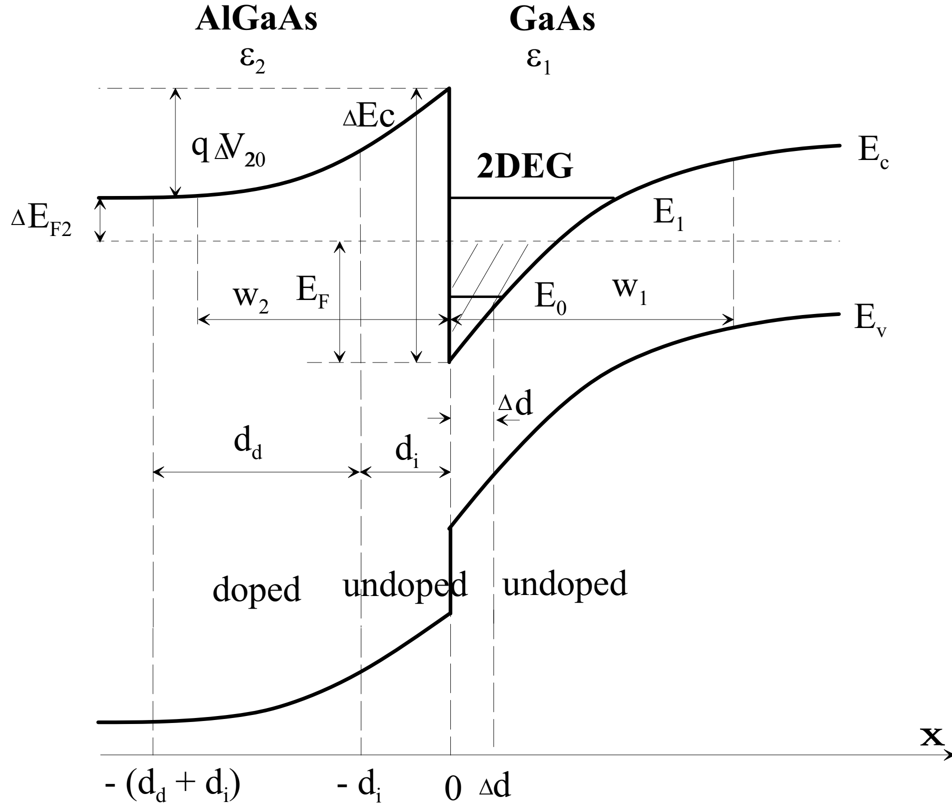

Figure 3.4: Energy-band diagram of a HEMT at equilibrium.

Figure 3.4 shows the energy band diagram of an AlGaAs/GaAs HEMT structure at equilibrium. Taking the heterojunction interface as origin and integrating Poisson's equation with boundary conditions $E(x = 0) = E_s$ (on the side of the potential well) and $E(x = w_1) = 0$ (where w_1 is the space charge region width in the well region) gives as a result:

$$E_s = \int_{\mathrm{GaAs}} \frac{\rho(x)}{\epsilon_1}\, dx = \int_0^{w_1} \frac{q}{\epsilon_1}\,(n(x) \mp N_{d,a})\, dx = \frac{q}{\epsilon_1}\, n_s \mp \frac{qN_{d,a}\, w_1}{\epsilon_1}. \tag{3.2}$$

Here ϵ_1 is the permittivity of the potential well; in this case the 2DEG consists of GaAs for which $\epsilon_1 = 13.1\,\epsilon_0$. $n(x)$ is the bulk free electron density, $N_{d,a}$ is the ionized donor/acceptor density in the depletion region within the channel-material, and the minus and plus sign refer to the donor and acceptor density, respectively. In principle, according to Gauss' law the electric field E_s is in addition to $n(x)$ and $N_{d,a}$ proportional to the interface state density $\frac{Q_i}{q\, w_1}$. In real devices, however, the contribution of the interfacial states to the total charge density is small, so that Q_i may be neglected.
Since in most applications the 2DEG-layer is unintentionally doped, i.e. $N_{d,a} \approx 0$ (to reduce impurity scattering for good mobility) the electric field is only due to the accumulated 2DEG electron density n_s. Eq. (3.2) becomes therefore simply:

$$E_s = \frac{q}{\epsilon_1}\, n_s. \tag{3.3}$$

Using now Eq. (3.3), Eq. (3.1) can be written as:

$$E_n = \left(\frac{\hbar^2}{2m^*}\right)^{\frac{1}{3}} \left(\frac{3\pi q^2}{2\epsilon_1}\right)^{\frac{2}{3}} \left(n + \frac{3}{4}\right)^{\frac{2}{3}} n_s^{\frac{2}{3}}. \tag{3.4}$$

The positions of the first two allowed energy levels in the triangular well are given by the relations:

$$E_0 = \gamma_0\; n_s^{2/3}$$

$$E_1 = \gamma_1\; n_s^{2/3}\,,$$

where γ_0 and γ_1 are adjustable parameters. Using $m^* = 0.0779$ and $\epsilon_1 = 13.1\,\epsilon_0$ for GaAs, the first two γ_n-values become:

$$\gamma_0 = 2.27 \cdot 10^{-12}\,\mathrm{eVm}^{4/3},\ \gamma_1 = 4.0 \cdot 10^{-12}\,\mathrm{eVm}^{4/3}. \tag{3.5}$$

In practice the calculated γ_0 and γ_1 are slightly different from the ones obtained from experimental results. Shubnikov de Haas and cyclotron resonance experiments give an estimation [92]:

$$\gamma_0 = 2.5 \cdot 10^{-12}\,\mathrm{eVm}^{4/3},\ \gamma_1 = 3.2 \cdot 10^{-12}\,\mathrm{eVm}^{4/3}. \tag{3.6}$$

The Fermi energy E_F can be approximated by the formula [93]:

$$E_F = E_{F0} + \frac{q^2 \Delta d}{\epsilon_2}\, n_s\ , \tag{3.7}$$

where ϵ_2 is the permittivity of the donor layer; in this case the supply layer consists of AlGas, for which $\epsilon_2 = 12.2\,\epsilon_0$. E_{F0} is under normal operating conditions a material and temperature dependent constant, which can be evaluated at the equilibrium carrier concentration n_s. For the values of n_s between $5 \cdot 10^{11}$ cm^{-2} and $1.5 \cdot 10^{12}$ cm^{-2}, $E_{F0} \cong 0$ at 300 K, and $E_{F0} \cong 0.025$ V at 77 K and below [94].

Δd is the effective distance of the 2DEG from the heterointerface, i.e. the effective width of the potential well. Δd provides an important correction factor, especially for a normally off device where Δd may be of the order of 30 nm or less. In practice only the lowest and at the most the first excited subband are occupied. If $n_s = 10^{12}$ cm^{-2} (corresponding to $E_s = 1.4 \cdot 10^5$ V/cm), the distance $\Delta d \approx 8.0$ nm, and for gate voltages V_g slightly above the threshold voltage (when $n_s \leq 10^{11}$ cm^{-2}) Δd becomes 20 nm [95].

- **2DEG sheet density**

  The electron sheet concentration in the channel is:

$$n_s = \int_0^{\infty} g(E)\, f_0(E)\, dE, \tag{3.8}$$

where the density of states-function $g(E)$ is found by summation of the separate energy levels:

$$g(E) = \sum_n g_n(E) = D \sum_n \theta(E - E_n). \quad (3.9)$$

θ is a step-function, and D is a constant for the 2D density of states $[\frac{1}{\mathrm{Jm}^2}]$, i.e. number of states per area- and energy unit:

$$D = \frac{m^*}{\pi \hbar^2}. \quad (3.10)$$

$f_0(E)$ defines the Fermi-Dirac distribution:

$$f_0(E) = \frac{1}{1 + e^{\frac{1}{k_B T}(E - E_F)}}. \quad (3.11)$$

Integrating Eq. (3.8) by applying the formula $\int \left(\frac{1}{1+e^x}\right)\, dx = -\ln[1 + e^{-x}]$, yields:

$$n_s = D\, k_B T \sum_n \ln[1 + e^{-\frac{1}{k_B T}(E_n - E_F)}],\ n = 0, 1, 2, 3... \quad (3.12)$$

Because of the negligible contributions of the higher subbands, only the two lowest subbands, $n = 0$ and $n = 1$, may be considered leading to the approximation:

$$n_s \approx D\, k_B T \ln\left[(1 + e^{-\frac{1}{k_B T}(E_0 - E_F)})(1 + e^{-\frac{1}{k_B T}(E_1 - E_F)})\right]. \quad (3.13)$$

At low temperatures Eq. (3.13) reduces to:

$$n_s = D(E_1 - E_0) + 2D(E_F - E_1) \quad (3.14)$$

or

$$n_s = D(E_F - E_0)\ , \quad (3.15)$$

when the second subband is, respectively, occupied or unoccupied.

- **2DEG density at equilibrium**

Using the depletion approximation, the voltage $V_2(x)$ in the space charge layer of the semiconductor 2 obeys the Poisson equation:

$$\frac{d^2 V_2}{dx^2} = -\frac{q}{\epsilon_2}\, N_d(x). \quad (3.16)$$

Taking the heterojunction interface as origin the following conditions must be fulfilled:
$V_2(0) = 0$, $\left(\frac{dV_2}{dx}\right)_{x=-w_2} = 0$, $\left(\frac{dV_2}{dx}\right)_{x=0} = -E_{s2}$. Integration of (3.16) over the space charge region (w_2 being the space charge layer width from the interface towards semiconductor 2, i.e. AlGaAs) results in:

$$E_{s2} = -\int_0^{-w_2} \frac{q\, N_d(x)}{\epsilon_2}\, dx. \quad (3.17)$$

Since $N_d(x) = 0$ for $-d_i < x < 0$ and $N_d(x) = N_d$ for $x < -d_i$, Eq. (3.17) yields:

$$E_{s2} = \frac{q}{\epsilon_2}\, N_d\, (w_2 - d_i). \quad (3.18)$$

Taking into account the continuity of the electric displacement vector at the heterointerface, i.e. $D_{s2}(x = 0) = \epsilon_2 E_{s2} = D_{s1}(x = 0) = \epsilon_1 E_s$, and using Eq. (3.3), the electric field vector at the interface is also expressed as:

$$E_{s2} = E(0) = \frac{\epsilon_1}{\epsilon_2}\, E_s = \frac{q\, n_s}{\epsilon_2}. \quad (3.19)$$

Here the interface states are neglected. Equations (3.18) and (3.19) result in:

$$n_s = N_d\,(w_2 - d_i). \tag{3.20}$$

It can be seen that n_s is due to the charge transferred from the upper (doped) AlGaAs-layer. The solution of Eq. (3.20) must be consistent with the 2DEG concentration in GaAs given by Eq. (3.13). Double integration of Eq. (3.16) with the conditions for the potential and for $N_d(x)$ stated above, gives:

$$\begin{aligned} V_2(-w_2) = \Delta V_{20} &= E_{s2}\,w_2 - \frac{q}{\epsilon_2}\int_0^{-w_2} dx \int_0^x N_d(x)\,dx \\ &= E_{s2}\,w_2 - \frac{qN_d(w_2-d_i)^2}{2\,\epsilon_2}. \end{aligned} \tag{3.21}$$

Solving w_2 from Eq. (3.21), using the expression for E_{s2} in Eq. (3.19) and inserting w_2 into Eq. (3.20), gives for n_s the form:

$$n_s = -N_d\,d_i + \sqrt{(N_d\,d_i)^2 + \frac{2\Delta V_{20}\epsilon_2 N_d}{q}}. \tag{3.22}$$

The electrostatic potential ΔV_{20} can be expressed as (see Fig. 3.4):

$$\Delta V_{20} = \frac{1}{q}\,(\Delta E_c - \Delta E_{F2} - E_F)\,. \tag{3.23}$$

Inserting Eqs. (3.7) and (3.23) into Eq. (3.22) yields:

$$n_s = N_d(d_i + \Delta d)\left[\sqrt{1 + \frac{2\epsilon_2(\Delta E_c - \Delta E_{F2} - E_{F0})}{q^2 N_d(d_i+\Delta d)^2}} - 1\right]. \tag{3.24}$$

- **2DEG density controlled by the Schottky gate**

  Figure 3.5 shows the energy-band diagram of the HEMT when a gate voltage V_g is applied.

  In the charge control regime the region between the Schottky contact and the heterojunction interface is totally depleted, i.e. w_2 becomes $w_2 = d_d + d_i$. The origin is likewise set to the heterointerface and $V_2(0) = 0$. The electrostatic potential obeys the Poisson's equation with: $N_d(x) = 0$ for $-d_i < x < 0$ and $N_d(x) = N_d$ for $-d_d < x < -d_i$. Double integration gives:

$$V_2(-(d_d + d_i)) = \Delta V_2 = E_{s2}\,(d_d + d_i) - \frac{qN_d\,d_d^2}{2\,\epsilon_2}. \tag{3.25}$$

Noting $V_{p2} = \frac{qN_d d_d^2}{2\,\epsilon_2}(= \frac{q\,n_{delta}\,d_d}{\epsilon_2}$ for delta doping), which is associated with the voltage across the depletion region under the gate, the electric field becomes:

$$E_{s2} = \frac{(\Delta V_2 + V_{p2})}{(d_d + d_i)}. \tag{3.26}$$

Equalizing Eqs. (3.19) with (3.26), gives for n_s:

$$n_s = \frac{\epsilon_2\,(\Delta V_2 + V_{p2})}{q\,(d_d + d_i)}. \tag{3.27}$$

Here ΔV_2 can be expressed as (see Fig. 3.5 a):

$$\Delta V_2 = -\phi_B + V_g + \frac{\Delta E_c}{q} - \frac{E_F}{q}. \tag{3.28}$$

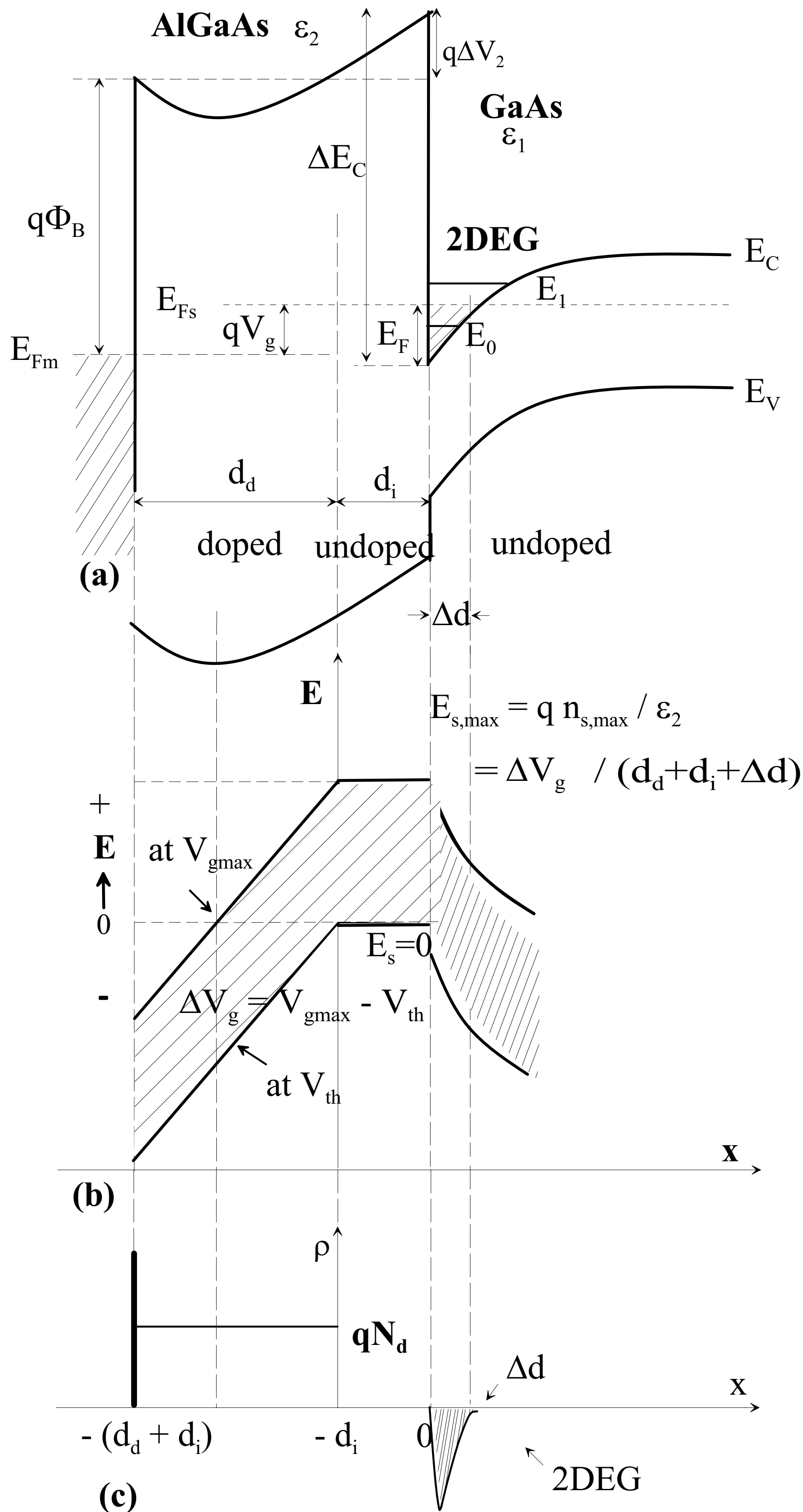

Figure 3.5: (a) Energy-band diagram of a HEMT with the Schottky gate, (b) the electrostatic field distribution at the threshold voltage ($n_s \sim 0$) and at V_{gmax} ($n_s = n_{s,max}$), (c) charge density.

Inserting Eq. (3.28) into Eq. (3.27) and using Eq. (3.7), yields:

$$n_s = \frac{\epsilon_2}{q(d_d + d_i + \Delta d)} \left[V_g - (\phi_B - V_{p2} - \frac{\Delta E_c}{q} + \frac{E_{F0}}{q}) \right]. \quad (3.29)$$

It can be noticed, that the sheet concentration depends on the gate voltage and the lateral channel potential. The threshold voltage is defined as:

$$V_{th} = \phi_B - V_{p2} - \frac{\Delta E_c}{q} + \frac{E_{F0}}{q}. \quad (3.30)$$

Equation (3.29) becomes thus:

$$n_s = \frac{\epsilon_2}{q(d_d + d_i + \Delta d)} [V_g - V_{th}]. \quad (3.31)$$

The simultaneous solution of Eqs. (3.12) and (3.24) yields the electron concentration n_s in the potential well for cases with n_s less than the equilibrium n_s, whereas the simultaneous solution of Eqs. (3.12) and (3.31) yields n_s-values for cases with n_s greater than equilibrium n_s. If the interface states cause a significant contribution to the total charge, the threshold voltage should read:

$$V_{th} = \phi_B - V_{p2} - \frac{\Delta E_c}{q} + \frac{E_{F0}}{q} - \frac{Q_i\,(d_d + d_i)}{\epsilon_2}. \quad (3.32)$$

It can be seen that the threshold voltage is determined by the Schottky barrier height, the doping concentration of the supply layer, and the conduction-band discontinuity ΔE_c between the wide bandgap Schottky contact layer and the narrow bandgap channel layer. In practice, the threshold voltage can be tuned with the factor $N_d d_d^2$.

The threshold voltage shift is an observed phenomenon, attributed to short-channel, drain bias and trapping center effects [96]. The threshold voltage shift is approximately proportional to d_d/l_g, where d_d is the doped supply layer and l_g is the gate length [97]:

$$\Delta V_{th} = V_{p2} \frac{4 d_d}{3 l_g}. \quad (3.33)$$

3.4.2 Gate Capacitance

The definition for the gate capacitance per unit area C_g $[\frac{\mathrm{F}}{\mathrm{m}^2}]$ (the area being $l_g W$) is [98]:

$$C_g = \left| \frac{d\,Q_g}{d\,V_g} \right| = \left| \frac{d\,Q_s}{d\,V_g} \right|. \quad (3.34)$$

$\Leftrightarrow$

$$\frac{1}{C_g} = \left| \frac{d\,V_g}{d\,Q_s} \right| = \left| \frac{d\,(E_{Fs}/q - E_{Fm}/q)}{d\,Q_s} \right|. \quad (3.35)$$

V_g can be solved by equalizing Eqs. (3.25) and (3.28):

$$V_g = \phi_B - \frac{\Delta E_c}{q} + \frac{E_F}{q} - \frac{q N_d d_d^2}{2\epsilon_2} + E_{s2}(d_d + d_i). \quad (3.36)$$

The charge in the potential well is a sum of the 2DEG electrons and the ionized donors (acceptors) in the depletion region within the well-material ($Q_s = q\,n_s + Q_{depl} = \epsilon_1\,E_s$). Since in most applications the 2DEG-layer is 'nonintentionally doped', i.e. $Q_{depl} = q\,N_{d,a}\,w_1 = 0$, the total charge in the channel is only due to n_s. Using E_{s2} as defined in Eq. (3.19), $E_{s2} = \frac{q\,n_s}{\epsilon_2} = \frac{Q_s}{\epsilon_2}$, the derivative of Eq. (3.36) with respect to Q_s yields:

$$\frac{1}{C_g} = \frac{d\,V_g}{d\,Q_s} = \frac{d\,(-\Delta E_c/q)}{d\,Q_s} + \frac{d\,E_F/q}{d\,Q_s} + \frac{(d_d + d_i)}{\epsilon_2}. \quad (3.37)$$

Assuming $\frac{d\,(-\Delta E_c/q)}{d\,Q_s} = 0$, C_g^{-1} simply gets the form:

$$\frac{1}{C_g} = \frac{d\,E_F/q}{d\,(q\,n_s)} + \frac{(d_d + d_i)}{\epsilon_2}. \tag{3.38}$$

It can be seen that the gate capacitance is a series connection of two capacitances:

$$\frac{1}{C_g} = \frac{1}{C_e} + \frac{1}{C_0}, \tag{3.39}$$

where C_e is due to the 2DEG electrons:

$$C_e = q^2 \left(\frac{d\,n_s}{d\,E_F}\right) \;, \tag{3.40}$$

and C_0 is due to the charge in the AlGaAs-layer:

$$C_0 = \frac{\epsilon_2}{(d_d + d_i)}. \tag{3.41}$$

Derivative of E_F with respect to n_s in Eq. (3.40) can be done by using the definition for E_F stated in Eq. (3.7.) Δd varies with E_s, and thus n_s. Considering a structure with a certain sheet density and corresponding electrical field, the effective width can be kept as a constant, and the derivation yields:

$$C_e = \frac{\epsilon_2}{\Delta d}. \tag{3.42}$$

The capacitance between the gate and the 2DEG becomes therefore:

$$C_g = \frac{1}{\frac{\Delta d}{\epsilon_2} + \frac{(d_d + d_i)}{\epsilon_2}} = \frac{\epsilon_2}{(d_d + d_i + \Delta d)}. \tag{3.43}$$

Here it can be seen that the gate capacitance is caused by the distance $(d_d + d_i)$ between the 'capacitor plates', and the effective distance of the 2DEG from the heterointerface towards GaAs.
The gate capacitance can actually be seen directly from the definition for n_s in Eq. (3.31). This equation is clearly the 'condensator law' for the dependence between n_s and V_g:

$$q\,n_s = C_g\;[V_g - V_{th}]. \tag{3.44}$$

3.4.3 I-V Characteristics

The 2DEG channel conduction current flows in response to the increasing drain voltage until the current saturates due to carrier saturation velocity. The amount of current flow is controlled by applying an appropriate voltage on the gate, i.e. an electric field perpendicular to the direction of current. In the linear region, i.e. the non-saturation region, the drain current for the ideal transistor is a function of both gate-to-source V_{gs} and drain-to-source V_{ds} voltages; whereas in the saturation region it is a function of only the gate-to-source voltage. In a conducting stage the voltage along the channel from the source to the drain changes from V_s to V_{ds}.

Various velocity versus electric field models can be used to derive the I-V characteristics. The approach taken here (charge control and velocity saturation concepts) yields satisfactory results for most situations.

Assuming a negligible gate leakage current the channel current can be expressed as the product of the channel charge and the field dependent velocity of the carriers [99]:

$$I_{ds} = W Q(x) v(x). \tag{3.45}$$

Letting the channel voltage at point x be $V_c(x)$ the electron charge density in the channel, according to the charge control model (in Section 3.4.1), is:

$$Q(x) = -q n_s = -C_g [V_g - V_{th} - V_c(x)]. \tag{3.46}$$

The carrier velocity depends on the lateral electric field, i.e. $v(x) = v(\mathbf{E}(x))$ and can be approximated as:

$$v(x) = \frac{\mu_0 \mathbf{E}(x)}{1 + \frac{\mathbf{E}(x)}{\mathbf{E}_c}}, \tag{3.47}$$

where μ_0 is the low-field mobility independent of V_s or n_s, and $\mathbf{E}_c$ is the critical field defined as:

$$\mathbf{E}_c = \frac{v_s}{\mu_0} , \tag{3.48}$$

where v_s is the electron saturation velocity. Equations (3.47) and (3.48) indicate that at the critical field $\mathbf{E}_c$ the carrier velocity attains half its saturation value.

Inserting Eqs. (3.46) and (3.47) into (3.45) and using $\mathbf{E}(x) = -\frac{dV_c(x)}{dx}$ gives:

$$I_{ds}\left[1 + \frac{\frac{dV_c(x)}{dx}}{\mathbf{E}_c}\right] = WC_g[V_g - V_{th} - V_c(x)]\mu_0 \frac{dV_c(x)}{dx}. \tag{3.49}$$

Integrating Eq. (3.49) along the channel $(0, x), (V_c(0) = V_s = 0)$ yields for the dc drain current:

$$I_{ds}\left[x + \frac{V_c(x)}{\mathbf{E}_c}\right] = WC_g\mu_0[(V_g - V_{th})V_c(x) - \frac{1}{2}V_c^2(x)]. \tag{3.50}$$

Letting $x = l_g \Rightarrow V_c(L) = V_{ds}$, the equation for the dc drain terminal current becomes:

$$I_{ds} = \frac{\frac{W}{l_g}C_g\mu_0[(V_g - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2]}{1 + \frac{V_{ds}}{V_0}}, \tag{3.51}$$

where $V_0 = l_g\mathbf{E_c}$.

The maximum drain current is identified as the saturation current I_{dsat}, obtained at the drain saturation voltage V_{dsat}. At saturation I_{dsat} becomes constant, i.e. $\frac{dI_{ds}}{dV_{ds}} = 0$. Differentiating Eq. (3.51) with respect to V_{ds}, yields:

$$V_{dsat} = -V_0 + \sqrt{{V_0}^2 + 2\,V_0(V_g - V_{th})}. \tag{3.52}$$

Inserting V_{dsat} into Eq. (3.51), gives for the saturation current:

$$I_{dsat} = \frac{\frac{W}{l_g}C_g\mu_0\,{V_0}^2}{2}\left(\sqrt{1 + \frac{2(V_g - V_{th})}{V_0}} - 1\right)^2. \tag{3.53}$$

It is good to note that for a long-channel device (long-gate-length) $V_0 >> (V_g - V_{th})$, and thus

$$I_{dsat} = \frac{W}{2\,l_g}C_g\mu_0\,(V_g - V_{th})^2, \tag{3.54}$$

which is as well-known result.

For a short-channel transistor $V_0 = l_g\mathbf{E}_c$ is small, that is $V_{dsat} = V_0 << (V_g - V_{th})$, and the saturated drain to source current Eq. (3.53) becomes:

$$I_{dsat,shortchannel} = W\mu_0\,E_cC_g(V_g - V_{th}) = Wv_sC_g(V_g - V_{th}). \tag{3.55}$$

The equation clearly indicates that the drain saturation current depends on the maximum electron velocity v_s and the maximum electron density $C_g(V_g - V_{th})$, which is appearing at the source end of the channel.

The saturated drain voltage for a short-channel transistor is expressed as, from Eq. (3.52):

$$V_{dsat,shortchannel} = -V_0 + \sqrt{2\,V_0(V_g - V_{th})}. \tag{3.56}$$

3.4.4 Transconductance and Cut-off Frequency

The intrinsic gain of a HEMT is provided by the device transconductance g_m. The transconductance is defined as the rate of change of drain current with respect to the corresponding change in gate-to-source voltage, while the output voltage V_{ds} is held constant:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \mid_{V_{ds} = \text{constant}} . \tag{3.57}$$

The maximum transconductance can be obtained under drain current saturation condition; that is differentiating I_{dsat} in Eq. (3.53) with respect to V_{gs}:

$$g_{m,max} = \frac{\partial I_{dsat}}{\partial V_{gs}} = \frac{W}{l_g} C_g \mu_0 V_0 \left(1 - \frac{1}{\sqrt{1 + \frac{2(V_g - V_{th})}{V_0}}} \right) . \tag{3.58}$$

For a long-channel transistor Eq. (3.58) becomes:

$$g_{m,max} = \frac{W}{l_g} C_g \mu_0 (V_g - V_{th}) \ , \tag{3.59}$$

whereas for a short-channel transistor Eq. (3.58) can be expressed as:

$$g_{m,max,shortchannel} = W \, C_g \, v_s . \tag{3.60}$$

It can be seen that g_m depends on the semiconductor properties and the transistor geometry. The current gain can be improved by using a layer structure with lower sheet resistance, optimized mobility against density and shorter gate length.

The conductive channel in a HEMT is a combination of multilayer conduction paths possible within the device structure. The gate voltage simultaneously changes the carrier concentrations present in several regions with different transport properties. The device g_m is a combination of all the separate conducting regions. In addition, the temperature affects the amplification: the decrease in g_m with increasing temperature is caused by a decrease in the mobility and the saturation velocity, and can be classified as a thermal effect.

The DC output conductance g_o (or the reciprocal of the conductance, the output resistance R_{ds}) is a measure of the incremental change in the output current, I_{ds}, versus output voltage, V_{ds}, while the input voltage V_{gs} is held constant:

$$g_o = \frac{\partial I_{ds}}{\partial V_{ds}} \mid_{V_{gs} = \text{constant}} . \tag{3.61}$$

For an ideal device, the slope in the saturation region should be zero, hence the transistor should have infinite R_{ds}, but for a practical device this is not the case. Increased slope in the $I_{ds}(V_{ds})$-characteristics may refer to parallel conduction in the supply layer, or kink effects caused by short-channel effects. The output conductance is also a strong function of temperature; in [100] it increased by more than five orders of magnitude when the temperature was raised from 25 to 275 °C, due to increased thermal leakage currents. At very low temperatures the electron mobility of the 2DEG is so large that the donor/buffer-layers do not contribute substantially to the overall conductance.

The DC voltage amplification (ratio of the transconductance to the output conductance) is an important figure of merit, especially in view to logic applications.

$$A_o = \frac{g_m}{g_o} \ . \tag{3.62}$$

Typically a maximum value of A_o is given, referring to the peak transconductance value $g_{m,max}$ and the output conductance obtained at the peak voltage condition.

The cut-off frequency is defined as the frequency, at which the current gain $\frac{dI_{ds}}{dI_{gs}}$ is unity:

$$\frac{dI_{ds}}{dI_{gs}} = \frac{\partial I_{ds}}{\partial V_{gs}} \frac{\partial V_{gs}}{\partial I_{gs}} = \frac{\partial I_{ds}}{\partial V_{gs}} \frac{\partial V_{gs}}{\partial Q} \tau = \frac{g_m}{C_{gs}} \frac{1}{2\pi f} \mid_{f=f_t} = 1, \tag{3.63}$$

where Q is the total charge in the channel ($Q = C_g l_g W\ V_{gs}$, see Eq. (3.46)), and τ the transit time of the electrons under the gate. Eq. (3.63) becomes simply:

$$f_t = \frac{g_m}{2\pi C_{gs}}. \tag{3.64}$$

This simple transit model shows the linear dependence of the gain g_m, i.e. f_t, on the gate voltage V_{gs} and the mobility μ_0, see also Eq. (3.59).

g_m is inversely proportional to the gate length as l_g^{-1}, and f_t as l_g^{-2}. These dependencies can, however, only be observed at low temperatures and for gate lengths 5 - 10 μm [89].

For HEMTs with submicron gate lengths the mobility can not be assumed to be constant. The drift velocity of electrons (e.g. in InGaAs and GaAs) depends strongly on the electrical field. The linear relationship $v = \mu_0 E$ is valid for fields up to $\sim 3 \cdot 10^3$ V/cm, after which the drift velocity reaches a maximum value, and starts to decrease again for higher fields [9]. The reason is electron transfer/scattering into the side maxima with less band bending, a larger effective electron mass, and hence a smaller mobility (Gunn-effect). The smaller is the energetic distance to the side maxima (Γ - L separation), the more probable is the scattering mechanism and the smaller the saturation velocity in the channel. Electrons in a lattice-matched InGaAs have a very small effective mass, furthermore is the Γ - L separation of 0.55 eV large. Increasing the In content in the channel (In mole fraction) both these factors can be further enhanced.

Assuming, that all the electrons in the channel have reached the saturation velocity, the transit time of the electrons under the gate is $\tau = \frac{l_g}{v_s} = \frac{1}{2\pi f_t}$. Thus the cut-off frequency obtains the expression:

$$f_t = \frac{v_s}{2\pi l_g}. \tag{3.65}$$

It is seen that f_t characterizes the intrinsic properties of the transistor.

In summary, in order to achieve the maximum gain and transit frequency, the gate length should be minimized as well as the channel-to-gate distance, i.e. high aspect ratio (the aspect ratio will be discussed in more detail in Section 3.4.5). Furthermore, the 2DEG sheet density n_s and mobility μ_0 should be as large as possible. High saturation velocities can be obtained through increasing the In mole fraction in the channel. In practice, not all of the electrons move with the saturation velocity and/or are confined only to the channel. Moreover, electrons exist in the doped supply layer (parasitic MESFET) or in the substrate with a considerably smaller mobility. Furthermore, more electrons are collected at the source end of the channel than at the drain end, leading to a smaller velocity for these electrons due to the continuity principle. Tunneling of electrons through the heterojunctions is important to describe the electron transport from the drain-side end of the channel into the supply layer above. For high gate voltages the I-V_{gs} curve drops off since the electrons heat up and start to surmount the energy barrier between channel and the barrier layer above known as real-space transfer of electrons. Hence, an increasing fraction of the electron transport takes place within the upper supply layer where the electron mobility is much lower than within the channel. Several physical effects, such as real-space transfer and carrier heating, on the device characteristics can be identified. These interface models allow to deal with abrupt heterojunctions and to include the effects of thermionic-field emission, which determine the current confinement within the channel layer, and properly describe how the carriers swap out into the neighboring segments [101].

3.4.5 Short-Channel Effects

Short-channel effects degrade the transistor performance for gate lengths below approximately 0.5 μm [102]. Short-channel effects cause an increase in the output conductance g_o, shift in the threshold voltage V_{th} and increased substrate leakage currents. In addition, the transconductance g_m is deteriorated, and the frequencies f_t and f_{max} show only modest improvement with decreasing gate length [103].

In fabricating a short gate-length FET, the most important consideration is to reduce the gate-to-channel separation d_{gc} along with the gate length l_g. This can be summarized as the *high aspect ratio rule*, in which the aspect ratio is defined as the ratio of l_g to d_{gc}. This ratio influences the field effect of the transistor structure. In case the ratio is too small, the gate control is reduced, and short channel effects appear (mainly threshold voltage shift), degrading the overall transistor performance.

A high aspect ratio can alleviate the threshold voltage shift, (see aspect ratios used in this work in Section 3.3).

Furthermore, a high aspect ratio is essential to minimize the g_m reduction that can result from drain-induced barrier lowering. A high g_m is important for attaining excellent high-speed performance. When the barrier thickness is reduced to the range typically suitable for deep sub-0.1-μm FETs, the thickness of the channel d_c should also be taken into account in computing the aspect ratio. A commmon approach is to use the sum of d_{gc} and d_c as the effective gate-to-channel separation. Maintaining a high aspect ratio becomes more and more difficult as l_g is reduced into the deep submicron region. First, a lower limit for the barrier thickness is imposed by the onset of enhanced tunneling current between the gate and channel. Second, but most important, the increase of side etching (also known as lateral etching) during gate recess processing must be properly controlled in order to avoid a greatly enhanced parasitic access resistances that would degrade the FET performance. This is because the side-etched region contributes to the electrical separation between the gate and ohmic regions, especially for the deep recess etching required to attain a sufficiently small barrier thickness for high aspect ratio [104]. The reduction of the threshold voltage in short channels is also argued to arise from the sharing of the depletion charge between the gate and the drain regions [105].

The increase in output conductance, referred to *kink effect*, is conventionally explained by a trap model: high fields at the drain end of the device change the charge state of traps in the buffer or in the insulator. This leads to a shift in threshold voltage, hence a rise in drain current. Recent investigations demonstrate, however, that impact ionization is in some way associated with the kink. Impact ionization generated holes accumulate in the channel, in donor layers between gate and source and/or in the substrate close to the source contact. This hole pile-up favors the injection of electrons from the source, therefore raising the channel potential and electron concentration. As a result V_{th} is shifted and the drain current increases significantly [106], [107]. This mechanism may further lead to device breakdown and burn-out.

3.5 Modelling

3.5.1 S-parameters

The small signal behavior of a transistor can be described by the measured S-parameters at two ports.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} ,$$

where S_{ij} are vector quantities (having an amplitude and phase), and $a_{1,2}$ and $b_{1,2}$ are the normalized incoming- and outgoing waves (1 and 2 referring to port 1 and 2, respectively). S_{11} and S_{22} represent the reflection coefficients at the input and output, respectively. S_{12} and S_{21} define the transmission coefficients from port 2(1) to 1(2), respectively.

$$S_{11} = \frac{b_1}{a_1}|_{a_2=0} \quad S_{12} = \frac{b_1}{a_2}|_{a_1=0}$$

$$S_{21} = \frac{b_2}{a_1}|_{a_2=0} \quad S_{22} = \frac{b_2}{a_2}|_{a_1=0}$$

For the characterization of the HF behavior the transit frequency f_t (cut-off frequency) and the maximum frequency of oscillation f_{max} are of significance [108]. An important definition is the stability factor K, which determines whether the transistor operates stable at the considered frequency, i.e. has no tendency to oscillate. $K > 1$ means absolute stability (additional requirement also $|S_{11}S_{22} - S_{12}S_{21}| < 1$), whereas $K \leq 1$ means conditional stability (oscillations) depending on the external circuitry. The stability factor is directly calculated from the experimentally obtained S-parameters as follows:

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} . \tag{3.66}$$

The cut-off frequency is defined as the frequency at which the current gain becomes unity, i.e. the H-parameter $|h_{21}(f_t)| = 1$. h_{21} is the current gain parameter of the hybrid or mixed mode matrix H.

The H-parameter h_{21} is the ratio: $h_{21} = \frac{i_2}{i_1}$ with the output port open circuited (output voltage $v_2 = 0$), derived from:

$$i_2 = h_{21}i_1 + h_{22}v_2 \ , \tag{3.67}$$

where i_1 and i_2 are the currents in the input and output port, respectively, and h_{22} is the ratio of i_2 to v_2 (the output admittance). The H-matrix can be transformed from the measured S matrix, and the current gain using S-parameters becomes [109]:

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \ . \tag{3.68}$$

The maximum frequency of oscillation determines up to which frequency the transistor still works as an active element. The limit is set by the unity power gain, $GU(f_{max}) = 1$ where:

$$GU = \frac{|\frac{S_{21}}{S_{12}} - 1|^2}{2\left(K|\frac{S_{21}}{S_{12}}| - Re\left(\frac{S_{21}}{S_{12}}\right)\right)} \ . \tag{3.69}$$

In HEMTs the power gain usually falls at the rate of 6 dB/octave or 20 dB/decade at high frequencies implying an inverse square frequency dependence. The extrapolated frequency at which the power gain falls to unity is considered as a key figure of merit that indicates the high-frequency limitation of HEMTs.

Different definitions are given for the amplification of a transistor [110].

The maximum stable gain (MSG) defines the amplification at the stability limit ($K = 1$):

$$MSG = \left|\frac{S_{21}}{S_{12}}\right| \ . \tag{3.70}$$

The maximum available gain (MAG) defines the maximum amplification in the region of unconditional stability ($K > 1$):

$$MAG = \left|\frac{S_{21}}{S_{12}}\right| \cdot \left(K - \sqrt{K^2 - 1}\right) \ . \tag{3.71}$$

The small-signal voltage amplification of a single stage (or open loop voltage gain) is defined as:

$$A_v(w) = \frac{dv_2}{dv_1} = \frac{1}{h_{12}(w)} \ , \tag{3.72}$$

where $h_{12} = \frac{v_1}{v_2}$ is the reverse voltage gain parameter of the hybrid or mixed mode matrix H, with the input port open circuited (input current $i_1 = 0$), derived from:

$$v_1 = h_{11}i_1 + h_{12}v_2 \ , \tag{3.73}$$

where v_1 and v_2 are the voltages in the input and output, respectively, and h_{11} is the ratio of v_1 to i_1 (the input impedance). At higher frequencies, especially in the microwave region, an open circuit with active devices can give rise to problems such as oscillations, consider K-factor in Eq. (3.66). The open loop gain characterized at high frequencies should thus be expressed with some other method. An alternative to defining the voltage gain can be done directly applying S-parameters. By using S-parameters the incoming and outgoing voltages/currents are replaced by in- and out travelling waves. A_v is equal to the total voltage at the output divided by the total voltage at the input:

$$A_v(w) = \frac{a_2 + b_2}{a_1 + b1} = \frac{S_{21}\Gamma_L + S_{21}}{(1 - S_{22}\Gamma_L) + S_{11}(1 - S_{22}\Gamma_L) + S_{21}\Gamma_L S_{12}} \ , \tag{3.74}$$

where Γ_L is the complex reflection coefficient of the load. If a matched analyzer port is used $\Gamma_L = 0$, the voltage gain simply becomes:

$$A_v(w) = \frac{S_{21}}{1 + S_{11}} \ . \tag{3.75}$$

The transducer power gain is important in amplifier designs, defined as the power delivered to the load divided by the power available from the source:

$$G_T = \frac{|S_{21}|^2(1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_s)(1-S_{22}\Gamma_L)-S_{21}S_{12}\Gamma_L\Gamma_s|^2} \ . \tag{3.76}$$

If a matched analyzer is used the reflection coefficients become $\Gamma_s = \Gamma_L = 0$ (Γ_s being the reflection coefficient at the source), and the power gain reduces to: $G_T = |S_{21}|^2$.

3.5.2 Small-Signal Equivalent Circuit

Figure 3.6 shows the small-signal equivalent circuit of a field effect transistor [111].

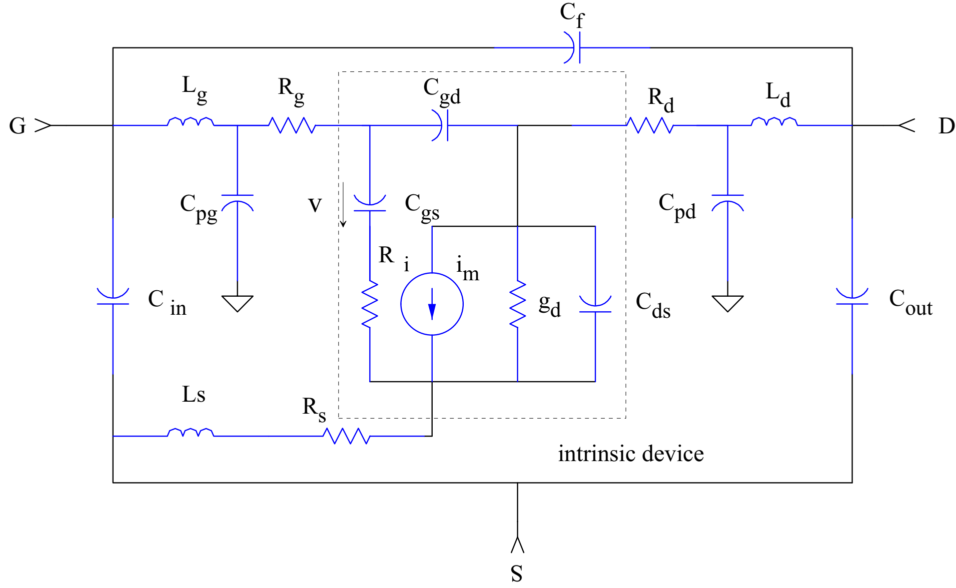

Figure 3.6: Small-signal equivalent circuit of a FET.

The equivalent circuit consists of two parts:

- intrinsic components: g_m, g_d, C_{gs}, C_{gd}, C_{ds}, R_i and τ, which are bias dependent.
- extrinsic components: L_g, L_s, L_d, R_g, R_s, R_d, C_{in}, C_{out}, C_f, C_{pg} and C_{pd}, which are independent of biasing conditions.

The amplification of the transistor g_m is presented in the equivalent circuit as a voltage controlled current source $i_m = g_m e^{-j\omega\tau} v$, i.e. an alternating voltage v over C_{gs} creates an alternating current i_m. The transit time constant τ represents the time taken by carriers to travel under the effective gate region, either side of the gate. The effective gate length is the distance between the edges of the gate depletion depth. The transconductance incorporates all the possible multilayer conduction paths in the device structure (paths via the supply layer and buffer layer under the channel). The multilayer conduction channels make the equivalent circuit problem more involved as this phenomena is bias dependent. Parallel to g_m exists the output conductance g_d, which takes into account the possible parallel conduction in the doped supply layer (parasitic MESFET) or/and in the substrate. It is observed as an increased slope in the $I_{ds}(V_{ds})$-characteristics. The capacitances C_{ij} are the capacitances between gate, source and drain, and influence at high frequencies the HF-performance of the transistor. The input gate capacitance is dependent on the depletion region under the gate and on the channel concentration, Eq. (3.31), which depends on the gate voltage and the threshold voltage. It is distributed and resistively connected to the conducting channel. The input gate-source network can be represented by a distributed series combination of capacitance C_{gs} and resistance R_i. R_i is a

measure of the channel resistance. The gate-drain capacitance C_{gd} represents a feedback path between the drain and gate due to coupling between gate and drain. It is distributed and connected to the low resistivity conducting channel. The drain-source capacitance C_{ds} is also associated with multilayer conduction paths within the device. The capacitances C_{gs}, C_{gd} are almost equal at low bias, but at higher biasing voltages $C_{gs} >> C_{gd}$. C_{gd} starts at the same value as C_{gs} for $V_{ds} = 0$. It then falls continuously with increasing V_{ds} and goes to zero when the drain side of the channel becomes pinched off. When velocity saturation is taken into account, the situation changes drastically. The gate and drain pad capacitances, C_{pg} and C_{pd} are lossless elements not contributing to the degradation of the power gain and can be absorbed in the conjugately matched input and output ports. R_s, R_d and R_g are associated with the source, drain and gate metallizations, respectively.

Parasitic elements show up at high frequencies. Especially in small devices fringing effects become more pronounced. At very high frequencies the influence of the inductance of the gate, drain and source, respectively, may increase significantly. Even though GaAs is semi-insulating, all the parasitic capacitances, resistances and inductances (especially in small circuits) of the transmission lines may have a crucial impact on the device performance.
Assuming that all the extrinsic elements are known, the intrinsic parameters can be defined from the S-parameter measurement (i.e. experimental data). The extraction of the device intrinsic Y_i matrix can be carried out by the following procedure [112]:

1. Transformation of the measured (extrinsic) S-matrix to impedance Z-matrix, and subtraction of the series parasitic inductances L_g, L_s and L_d.

$$Z_e = Z - \begin{bmatrix} j\omega(L_g + L_s) & j\omega L_s \\ j\omega L_s & j\omega(L_d + L_s) \end{bmatrix}$$

2. Transformation of Z_e to admittance Y_e-matrix, and subtraction of the parallel parasitic capacitances C_{in}, C_f, C_{out}, C_{pg} and C_{pd}.

$$Y_e' = Y_e - \begin{bmatrix} j\,\omega\,(C_{in} + C_f + C_{pg}) & -j\,\omega\,C_f \\ -j\,\omega\,C_f & j\,\omega\,(C_{out} + C_f + C_{pd}) \end{bmatrix}$$

3. Transformation of Y_e' to Z_e'-matrix, and subtraction of the terminal series resistances R_g, R_s and R_d.

$$Z_i = Z_e' - \begin{bmatrix} (R_g + R_s) & R_s \\ R_s & (R_d + R_s) \end{bmatrix}$$

4. Transformation of Z_i to Y_i-matrix.

The elements of the Y_i-matrix according to the equivalent small-signal circuit are [119]:

$$y_{11} = \frac{R_i\,C_{gs}^2\,\omega^2}{D} + j\,\omega\left[\frac{C_{gs}}{D} + C_{gd}\right]$$

$$y_{12} = -j\,\omega\,C_{gd}$$

$$y_{21} = \frac{g_m\,e^{-j\,\omega\,\tau}}{D} - j\,\omega\left[\frac{g_m\,e^{-j\,\omega\,\tau}\,R_i\,C_{gs}}{D} + C_{gd}\right]$$

$$y_{22} = g_d + j\,\omega\,(C_{ds} + C_{gd}),$$

where $D = 1 + \omega^2\,C_{gs}^2\,R_i^2$.

At low frequency ($f < 5$ GHz) and for a low-noise device the term $\omega^2\,C_{gs}^2\,R_i^2$ is less than 0.01. Therefore $D = 1$ gives a reasonable approximation. Assuming also $\omega\,\tau << 1 \Rightarrow e^{-j\omega\tau} = 1 - j\omega\tau$, lets the y-elements be expressed as:

$$y_{11} = R_i\,C_{gs}^2\,\omega^2 + j\,\omega\,(C_{gs} + C_{gd}) \tag{3.77}$$

$$y_{12} = -j\,\omega\,C_{gd} \tag{3.78}$$

$$y_{21} = g_m(1 - \omega^2 \tau R_i C_{gs}) - j\,\omega\,(g_m(R_i\,C_{gs} + \tau) + C_{gd}) \tag{3.79}$$

$$y_{22} = g_d + j\,\omega\,(C_{ds} + C_{gd})\ . \tag{3.80}$$

Inverting these matrix-elements the intrinsic transistor components become:

$$\begin{aligned} g_d &= \mathrm{Re}\,[y_{22}] \\ C_{gd} &= -\frac{1}{\omega}\,\mathrm{Im}\,[y_{12}] \\ C_{ds} &= \frac{1}{\omega}\,\mathrm{Im}\,[y_{22}] - C_{gd} \\ C_{gs} &= \frac{1}{\omega}\,\mathrm{Im}\,[y_{11}] - C_{gd} \\ R_i &= \frac{1}{C_{gs}^2\,\omega^2}\,\mathrm{Re}\,[y_{11}] \\ g_m &= \mathrm{Re}\,[y_{21}]\ {}_{\omega\to 0} \\ \tau &= \frac{1}{g_m}\left(-\frac{1}{\omega}\,\mathrm{Im}\,[y_{21}] - C_{gd}\right) - R_i\,C_{gs}. \end{aligned}$$

In practice, some of the intrinsic parameters can be obtained directly from DC and/or C-V measurements, while some of the extrinsic elements are unknown. Therefore, the procedure described above does not truly apply in all cases. Instead, the experimental S-parameters should be fitted to the model in a frequency sweep simulation by setting the known parameters fixed. The known extrinsic elements can be kept constant for all bias points, which makes the simulation faster and more convenient.

In a first approximation, the alternating input current, especially at high frequencies, is only capacitively loaded, and expressed as: $I_{gs} = j\omega(C_{gs} + C_{gd} + C_p)V_{gs}$, where C_{gs} is the intrinsic capacitance between the gate and the source, C_{gd} is the feedback capacitance between the gate and the drain, and C_p is the parasitic source-to-gate capacitance. $C_{gd} = C_p = \frac{\pi\epsilon_2 W}{2}$ and $C_{gs} = \frac{\epsilon_2 l_g W}{h(V_{gs})}$, where $h(V_{gs})$ is the width of the depletion layer under the gate bias of V_{gs} (see Eq. (3.43), in which $h(V_{gs}) = d_d + d_i + \Delta d$). The alternating output current is: $I_{ds} = g_m V_{gs}$. The cut-off frequency is defined through the condition $I_{ds} = I_{gs}$ (current gain is unity). For f_t follows [113]:

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_p)}. \tag{3.81}$$

If neglecting C_{gd} and C_p the cut-off frequency obtains the expression already derived in Eq. (3.64). In Eq. (3.81) g_m is the extrinsic transconductance. The relation between the intrinsic and extrinsic transconductance is defined as follows [114]:

$$g_{m,int} = \frac{g_m[1 + (R_s + R_d)g_d]}{(1 - R_s g_m)} \tag{3.82}$$

The maximum frequency of oscillation (frequency, at which the power gain becomes one) derived from the equivalent circuit model shown in Fig. 3.6 is expressed as follows [115]:

$$f_{max} = \frac{f_t}{\sqrt{(4g_d/g_m)[g_m R_i + (R_s + R_g)/(1/g_m + R_s)] + (4C_{gd}/5C_{gs})[1 + 2.5(C_{gd}/C_{gs})](1 + g_m R_s)}}\ . \tag{3.83}$$

The addition of T-gate structure (i.e. mushroom shaped gate) will increase f_t and f_{max} significantly. The T-gate structures have the advantage of offering submicron gate-lengths with reduced electron transit time, and gate capacitance (due to shallow footprint, $C_g = \frac{\epsilon_s l_g W}{d_{gc}}$), while maintaining a large cross-sectional top cap to minimize the gate resistance R_g. When using the traditional triangular and rectangular gates, R_g is proportional to l_g^{-2} ($R_g = \frac{\rho W}{l_g h}$, where the height of the gate h is comparable to l_g). Therefore, in state-of-the-art devices whose gate length has been shortened up to 30 nm, it is

fundamental to use T-gate technology to avoid the increase of R_g. This kind of technology can reduce the value of R_g from seven to ten times with respect to triangular or rectangular gates [116]. The device width W can also be reduced in order to minimize the gate resistance. In this case, the drawback is that the current provided by the device is also reduced (being proportional to W). Multifinger gates can be the solution for this problem since they permit to diminish R_g without reducing the total device width.

Results indicate that the alignment of the gate in respect to drain and source affect the current saturation behaviour, and ultimately the frequency behaviour. Since the parameters g_m/g_d and C_{gs}/C_{gd} are increasing functions of the increased effective gate length, (now defined as $l_g + l_{gd}$, where l_{gd} is the gate-to-drain distance), f_t is a decreasing function of the same. But on the other hand the unity power gain frequency, f_{max}, is enhanced for an optimum gate-to-drain separation. l_{gd} should be wide enough to reduce the peak electric field in the InGaAs channel near the drain, but on the other hand not too wide to reduce f_t significantly. The reduced peak channel electric field in turn increases the breakdown voltage and reduces the output conductance [117].

The measured maximum transconductance was increased from 370 to 395 mS/mm when the gate-to-source distance l_{gs} was reduced from 0.45 to 0.25 μm (GaAs-based pHEMT with $l_g = 0.25$ μm). The device with smallest l_{gs} showed also a lower output conductance and higher drain breakdown voltage without notable degradation in the other characteristics [88].

The data indicate that for a short-gate length device the f_{max} depends more critically on l_{gd} compared to that for a longer gate-length device.

f_t is more important than f_{max} in terms of digital performance. However, f_{max} is more important in analog integrated circuit applications. In addition, f_{max} is preferable to f_t for characterizing high-frequency devices due to the fact that f_{max} takes into account the losses associated with the gate resistance R_g, the output conductance g_d and the parasitic resistances and capacitances. In the design of devices that will operate with reasonable gain at a frequency around 100 GHz, g_m/g_d and C_{gs}/C_{gd} gain more influence. Hence, the relative contribution of f_t to the f_{max} of the device is less [115].

3.5.3 Microwave Design System

The simulations for the transistors were performed using HP's microwave design system (MDS)-software. The transistors were modelled with EEHEMT1-model from MDS's standard device library. Automated parameter extraction was done with IC-CAP software, which covers both DC and AC measurements/fittings. The EEHEMT1-model is based on refs. [112], [118] - [123]. The model incorporates alltogether 51 parameters, divided into 5 separate modelling sectors: (1) I_{ds}-model for DC parameters, (2) I_{db}-model for AC parameters, (3) gate model, (4) parasitics and (5) charge model (Appendix D shows the parameters for two measured transistors, Figs. D.1, D.2).

The FET model is based on the Curtice quadratic, Curtice cubic and Statz (Raytheon) theories [124]. While these models are well known for use with DC and low-frequency devices, the extraction methodology used for the EEHEMT1-model is specifically designed for high-frequency devices. The measurement and extraction software and procedures ensure accurate modelling results that are constant, rather than a function of frequency. The high-frequency FET modelling software performs a series of DC and S-parameter measurements (vs. gate/drain-bias under different drain/gate-bias and frequency conditions), based on predefined measurement configurations and on variables the user defines during the procedures. The measured values are then used to extract individual device parameters, through software conversion of the S-parameters to admittance or impedance parameters.

The EEHEMT1-model is an empirical analytic model developed for the purpose of fitting measured electrical behaviour of GaAs FETs and the HEMTs. The model includes the following features:

- An accurate isothermal drain-source current model that fits virtually all processes. The model assumes the device is symmetrical, and therefore is valid for values of $V_{ds} < 0.0$ V as well as $V_{ds} > 0.0$ V. Parameters extracted from the drain-source current measurement are: V_{to}, G_{amma}, V_{go}, V_{delt}, V_{ch}, G_{mmax}, V_{dso}, V_{sat}, K_{appa}, P_{eff}, V_{tso}.

- Self-heating correction for the drain-source current, channel-to-backside self-heating parameter: P_{eff}.

- A charge model that accurately tracks measured capacitance values. The capacitance data is obtained from measured Y-parameter data in the saturation region. The parameters are: C_{11o}, C_{11th}, V_{infl}, D_{eltgs}, D_{eltds}, L_{ambda}, C_{12sat}, C_{gdsat}, R_{is}, R_{id}, T_{au}, C_{dso}.

- A dispersion model that permits simultaneous fitting of high-frequency conductances and DC characteristics. Dispersion parameters are extracted from measured S-parameter data, to provide additional accuracy for dispersion effects at higher frequencies. The dispersion parameters are optimized to the measured transconductance data to model both DC and RF dispersion characteristics. Similarly, the dispersion parameters are optimized to the measured output conductance data. The output conductance is defined as parameter K_{appa}. Other parameters are: R_{db}, C_{bs}, G_{dbm}, K_{db}, V_{dsm}, G_{mmaxac}, V_{deltac}, V_{toac}, G_{ammaac}, K_{appaac}, P_{effac}.

- A breakdown model that describes gate-drain current as a function of both V_{gs} and V_{ds}.

- The capability to extrapolate outside the measurement range used to extract the model.

- Some FETs and almost all HEMTs exhibit tranconductance compression, in which tranconductance peaks and then decreases. Additional parameters used for g_m compression are: V_{co}, M_u, V_{ba}, V_{bc}, D_{eltgm} and A_{lpha}.

The analytical model for the drain current uses a hyperbolic tangent function [121]:

$$I_{ds} = \beta\,(V_g - V_{th})^2\,(1 + \lambda\,V_{ds})\tanh(\alpha\,V_{ds}), \tag{3.84}$$

where $\beta = \frac{W\,\epsilon_2\,\mu_0}{2\,(d+d_i+\Delta d)\,l_g}$ [A/V^2] (λ is a parameter proportional to drain conductance, and α determines the voltage at which the drain current characteristics saturate (as α increases, I_{ds} saturates at lower V_{ds}). Noticeable is that the drain current saturates at the same drain-to-source voltage irrespective of the gate-to-source voltage. This is different from conventional JFET or MOSFET models and occurs because the critical field $\mathbf{E_c}$ in the channel is reached at approximately the same voltage $V_0 = l_g\,\mathbf{E_c}$.

A simple interpolation formula for the saturated drain current near pinch-off follows a quadratic law, and for larger values of the drain current a square-root-like behavior [123]:

$$I_{dsat} \sim \beta\,(V_g - V_{th})^2 \;\; (\text{small } V_g - V_{th}), \tag{3.85}$$

$$I_{dsat} = W\,v_{sat}\,\sqrt{2\,\epsilon_2\,q\,N_d}\left[\sqrt{(-V_{th} + V_B)} - \sqrt{(-V_g + V_B)}\right], \tag{3.86}$$

$$(\text{larger } V_g - V_{th})$$

where V_B is the built-in potential of the gate junctions.

An empirical expression which smoothly connects Eqs. (3.85) and (3.86) can be written as:

$$I_{dsat} = \frac{\beta\,(V_g - V_{th})^2}{1 + b\,(V_g - V_{th})}, \tag{3.87}$$

where b for a bare transistor (without parasitic source and drain resistors) is a measure of the doping profile extending into the insulating substrate and thus depends on the fabrication process. $b = 0.3 - 0.45$ V^{-1} for a gradual doping profile. In case there is a truly abrupt interface between the active layer and the undoped buffer, $b = 2.6$ and 1.5 V^{-1} with pinch-off voltage of -0.5 V and -2.5 V, respectively. Eq. (3.87) is indeed quadratic for small values of $V_g - V_{th}$ and becomes almost linear for larger values. The hyperbolic tangent function provides a good analytical expression for current saturation in GaAs, which appears at rather low voltages (electric field of $3 \cdot 10^3$ V/cm) attributed to a large low field mobility. Thus the saturation of drain current with increasing drain-to-source voltage is caused by carrier-velocity saturation, rather than channel pinch-off (as is the case for Si).

3.6 Fabrication

3.6.1 Mask Layout

In Figure 3.7 is presented the mask layout for the realized transistors, U- and T-type. The U-configuration is used in the integrated transimpedance amplifier circuit.

The advantage of the T-type is the symmetrical gate-to-source as well as gate-to-drain distance in both transistor parts, despite of possible misalignments. For the U-type the alignment is more critical due to the asymmetry. However, the U-type does not contain a curved metal connection to the gate, thus reducing parasitic induction and further input reflections.

The gate length for optically fabricated transistors is 1 μm with $l_{DS} = 4$ μm, whereas for e-beam transistors the gate length ranges from 0.16 μm up to 0.6 μm. For submicron gate lengths the source-to-drain distance is scaled accordingly in order to minimize the series resistance $l_g = 0.16, 0.2, 0.3, 0.4, 0.6$ μm with $l_{DS} = 1.6, 2.0, 2.6, 3.0, 3.6$ μm, respectively. The above mentioned gate lengths are values defined in the masks (optical) / files (e-beam). The real obtained gate length and source-to-drain distance became usually slightly larger and smaller, respectively. For the optically exposed gates the gate length was typically 0.1 - 0.2 μm wider, whereas the e-beam written gates, depending on the exposure dose, had an offset of 50 - 150 nm. l_{DS} was reduced in the range of 0.2 - 0.6 μm attributed to the ohmic contact formation with RTA treatment. The different widths for the studied transistors are: 10, 20, 40, 80, 160 and 200 μm. The gates were positioned in the center between the drain and source. However, due to possible misalignments a shift towards either one of the contacts is possible.

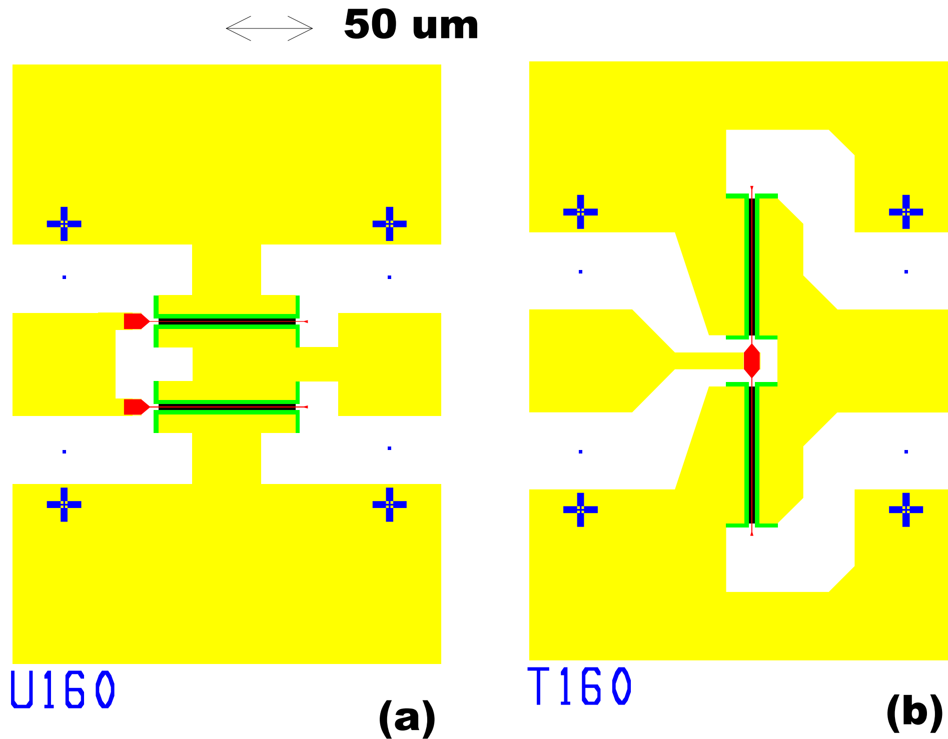

Figure 3.7: Mask layout for HEMTs. (a) U-configuration (b) T-configuration. The crosses are for e-beam alignment, and the small squares for accurate positioning of the measurement probes.

3.6.2 Processing Steps

A detailed description of all the various processing techniques can be found in Appendix B, Tables B.7 - B.12. Here only an overview is given of the four different main steps: mesa-, ohmic-, gate- and interconnection-layers. The basic recipes, concerning the optical lithography, are based on the

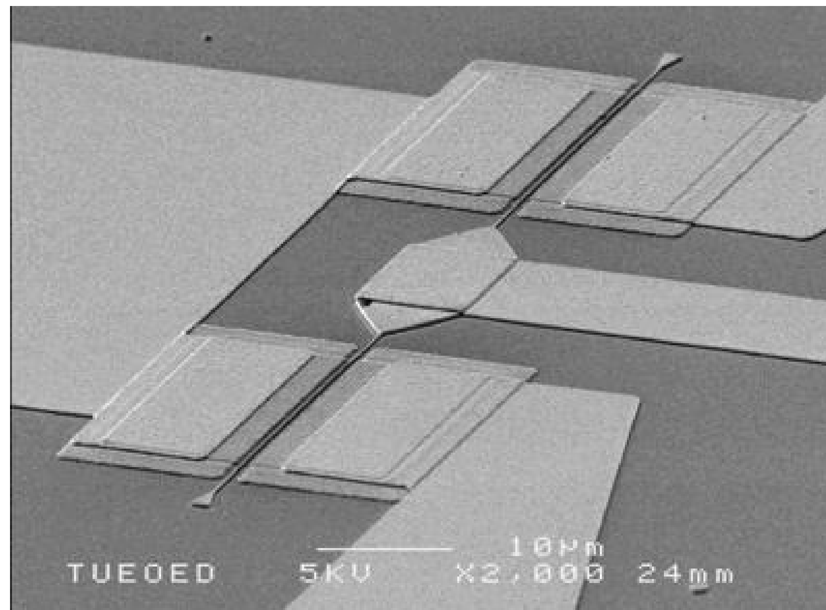

Figure 3.8: SEM photograph of a fabricated T-type HEMT, $l_g = 0.19$ μm, $l_{DS} = 1.05$ μm, $W = 40$ μm.

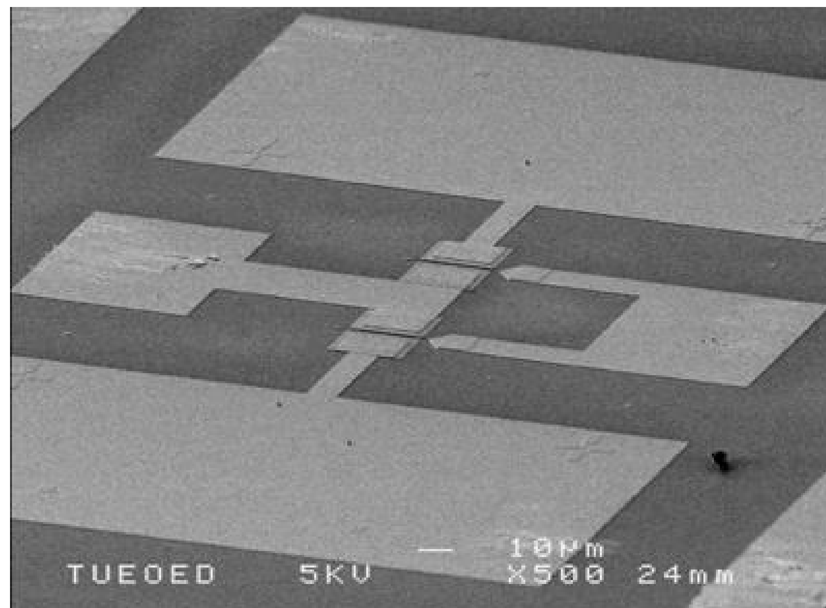

Figure 3.9: SEM photograph of a fabricated U-type HEMT, $l_g = 0.19$ μm, $l_{DS} = 1.05$ μm, $W = 40$ μm.

experience of previous work performed by the OED-group (Opto Electronic Devices) at TUE. For optical pattern definition the contact-lithography Karl Suss MJB (UV 300 nm) mask aligner was used. Depending on the process, two different photoresists were applied. The pHEMT submicron gates were defined using e-beam exposure (Raith Turnkey 150 SEM and e-beam lithography system). The total process including PMMA resist baking, exposure, developing and subsequent gate recess etching were developed by the author for the purpose of this thesis. The e-beam lithography technique is explained in detail in Section 3.6.3. Metallization was performed using the Airco Temescal or Leybold L560UV e-beam evaporator.

The yield for the optically fabricated transistors was good, out of 288 transistors on one sample (within the wafer area of $\sim$ 1 x 1 cm^2), 239 showed good performance corresponding to 83 %. The yield for the e-beam processed transistors was very much depending on the specific sample. Factors that affected the yield applying e-beam technique are the used exposure dose, resist stack and etch solution/time. For a sample etched in citric acid -solution for 45 s the yield became 91.7 % within an area of $\sim$ 0.5 x 0.5 cm^2. Using ammonia based etching for 5 s the obtained yield was 76.7 %. For mushroom-gate transistor samples the yield was less, attributed to more difficult gate definition with 2 subsequent exposures. For a mushroom-sample with 2-layer resist stack and ammonia based etching for 5 s, 58.3 % of the transistors showed high performance.

(1) Mesa etching

The purpose of the mesa patterning is to electrically isolate the different devices from each other on the wafer. The etching is done down to the S.I. buffer layer grown underneath the active top transistor layers. The mesa patterning is performed using S1805 photoresist, and the mesa etch using wet chemical etching with non-selective etchant $H_2SO_4 : H_2O_2 : H_2O$ = 1:1:60 for 1 minute at $T = 20\ °C$. The etch rate being 1.4 - 1.5 nm/s the mesa height became ca. 84 - 90 nm, and the distance to the second etch stop layer 34 - 28 nm, respectively.

(2) Ohmic contacts

The ohmic contacts for the source and drain are patterned using AZ5214 photoresist. Ge/Ni/Au = 20/15/150 nm metal layers are deposited, followed by lift-off in acetone. Alloying of the metal contact is realized by rapid thermal annealing (RTA) at 400 °C for 30 seconds. The contact resistance was measured utilizing the transmisssion line method (TLM) using a four probe measurement. The obtained contact resistance was in the range 0.17 - 0.44 Ωmm. Section 3.7.1. explains in detail the measurement method, and the results.

(3) Gate recess

A Schottky gate contact with high barrier height and large cross-sectional area is essential for high performance transistors. A good contact is achieved using unintentionally doped semiconductor for the Schottky metal (in this work i-AlGaAs), and accurate cleaning process, de-oxidation of the semiconductor surface just prior to metal deposition.

Furthermore, and of much more significance is a reproducible gate recess etch, (i.e. removal of the top GaAs cap layer in order to place the gate metal on the Schottky layer), since the device characteristics, yield and uniformity are severely dependent upon the recess depth. In the vertical direction the recess depth defines the gate-to-channel distance, whereas in the horizontal direction it influences the gate length, thus for an important part the frequency characteristics of the device.

In the following major factors are discussed.

- **Influence on the threshold voltage**

A selective wet etch is commonly used to 'recess' the gate in order to control the threshold voltage. V_{th} will be shifted, if the gate-to-channel distance is not controlled in a reproducible manner, i.e. the aspect ratio changes. Typically, a threshold voltage uniformity of less than 20 mV is required for good noise margin. This translates into an etch depth control of about 0.5 nm [125]. In this work an AlAs etch stop layer was utilized. As a consequence of the extremely accurate etch depth control afforded by the inclusion of the etch stop layer, the threshold voltage of the HEMTs should be very repeatable and uniform.

- **Selectivity of the etchant**

Since the depth to which the gate is recessed determines the transistor performance, a selective wet etch which etches the etch stop layer (AlAs) slower than the n^+-GaAs cap layer (hence high selectivity) is needed for better control of gate recessing. Commonly used etchants in GaAs/AlGaAs systems are citric acid (CA)/hydrogen peroxide and ammonia/hydrogen peroxide solutions [126]. CA/hydrogen

peroxide solution has been shown to be very selective in respect to AlAs [127]. It was shown that selective wet etching using a 4:1 citric acid/H_2O_2 in conjunction with a thin AlAs etch stop layer provides very high selectivities needed for the fabrication of HEMTs incorporating an AlGaAs donor layer with x < 0.3. Without an AlAs layer (i.e. a n^+-GaAs cap/AlGaAs system) the selectivity is a very sensitive function of the Al-mole fraction, the exact etch ratio, the temperature and the impurities in the solution. Using an AlAs stop layer and CA : H_2O_2 = 4 : 1 solution a 300 nm thick n^+-cap GaAs was removed already after 41.5 s, but it took approximately 10 min to etch through 3 nm of AlAs. This translates to a selectivity of 1450 for GaAs over AlAs [125].

- **Lateral etching**

High selectivity allows freedom in defining the recess etch time. Hardly any etching of the Schottky layer will occur. However, increased etch time will result in lateral etch of the cap layer underneath the resist [128].

Uncontrollable side etching can be problematic for a wet etch process, while a prolonged dry etch may lead to excessive surface damage.

The recess etch has a direct influence on the obtained gate length, since it affects both the etch profile within the resist and the lateral etching at the resist-substrate interface. Therefore, only a brief dip in HCl-based solutions is necessary to remove the AlAs. Overetching may result in an undercut which separates the cap layer from the donor layer. This can result in slight increases in parasitic drain and source resistances. Lateral etching is enhanced by increased etch time, thus giving rise to a larger effective gate length and increased parasitic resistance.

In this process the lateral underetch became usually 50 - 100 nm (depending on the used etchant and the time) on each side of the gate. Figure 3.10 shows a submicron gate, etched with NH_4OH : H_2O_2 solution for 5 seconds. With ammonia/hydrogen peroxide etchant the linewidth control was observed to be slightly better than using the CA-based solution. However, more experiments should be performed in order to draw exact conclusions about the best etchant and etch time.

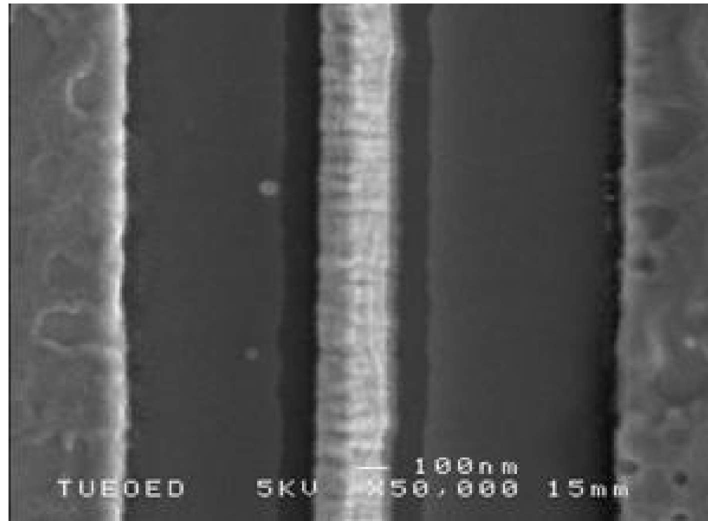

Figure 3.10: SEM photograph of a submicron gate (l_g = 0.26 μm, l_{DS} = 1.75 μm, W = 20 μm, Ti/Au = 50/250 nm). Lateral recess etching is visible, being $\sim$ 100 nm on each side of the gate line. Gate recess etching is done with an ammonia-based solution.

- **Small gate lines**

One important etching characteristic is the etch rates for small geometries. Major etch depth variations appear when the etch depths are over 0.1 μm. This is due to a conductance problem which results in reduced mass transport of etching species and the etch products in and out of the narrow etched lines. This becomes severe as the linewidths get smaller (below 0.25 μm). As a result, overetching is almost always needed to guarantee complete removal of the GaAs cap layer in deep submicrometer-gate HEMTs.

Etching experiments

For optimizing the gate recess etching several etching experiments were performed. Tests were done using a succinic acid (SA)-based, citric acid (CA)-based and NH_4OH/hydrogen peroxide solutions. The surface roughness confirmed with SEM pictures revealed, that best smoothness can be achieved with CA- and ammonia-solutions. SA : NH_4OH : H_2O_2, pH 5.5 adjusted, resulted in a very rough surface. For this reason CA : H_2O_2 and pH-adjusted NH_4OH : H_2O_2 solutions were utilized in this work. For CA : H_2O_2 etching experiments included tests with different ratios. Fig. 3.11 indicates that CA : H_2O_2-solution with a ratio of 1:1 is suitable for etching the thin 20 nm top GaAs layer due to its low etch rate. In addition to slow etch rate, better surface smoothness and less underetching were observed for the ratio of 1:1.

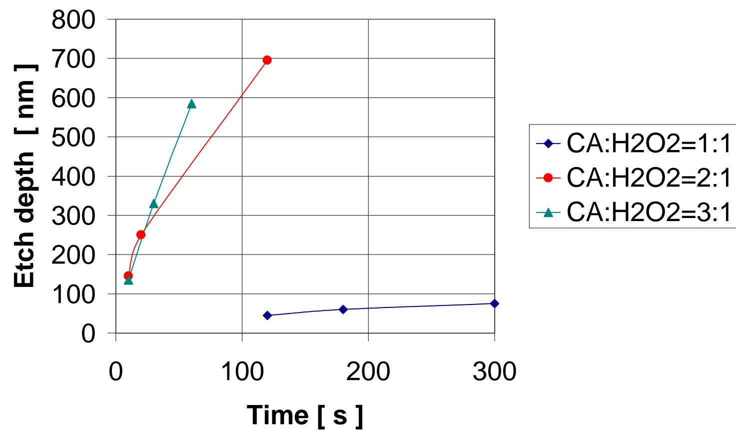

Figure 3.11: Etch depth using CA : H_2O_2 with different ratios for S.I. GaAs at T = 21 °C.

Figure 3.12 shows the surface morphology using CA : H_2O_2 = 1:1, and in Fig. 3.13 is seen the large underetching using a ratio of 3:1. Figure 3.14 presents the result of applying CA-ratio of 2:1 and a long etching time of 2 minutes, leading to very uneven surface.

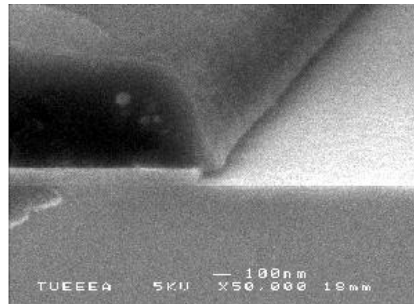

Figure 3.12: S.I. GaAs etching with CA : H_2O_2 = 1:1, 5 min, etch depth 75 nm (underetch ~ 100 nm).

It is noted, that using CA : H_2O_2-solution with a ratio of 1:1, and hence a large amount of H_2O_2 may slowly consume and damage the PMMA and the photo resist. However, for a n^+ GaAs-cap layer with a thickness of 50 nm or less this is not a problem. Also with ammonia/hydrogen peroxide etchant the resist may be attacked, but due to the thin cap layer and short etch time no damages were observed.

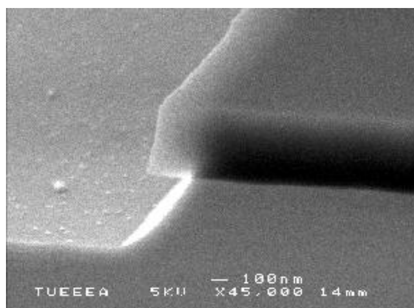

Figure 3.13: S.I. GaAs etching with CA : H_2O_2 = 3:1, 1 min, etch depth 585 nm (underetch ~ 200 nm).

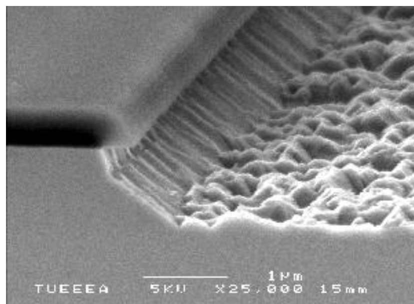

Figure 3.14: S.I. GaAs etching with CA : H_2O_2 = 2:1, 2 min, etch depth 695 nm (underetch ~ 300nm).

Figure 3.15 plots the etch depth versus time utilizing NH_4OH/H_2O_2 = 50 ml : 5 drops (pH 8), and CA : H_2O_2 = 1:1 for S.I. GaAs. The etch rates are 8 nm/s at T = 21 °C and 1.7 nm/s at T = 20 °C for ammonia- and CA-solution, respectively.

Gates were patterned using either optical or e-beam lithography (the optically defined transistors are referred to as 'standard' transistors):

Gate definition using photolithography

For the gate patterning photoresist S1805 is utilized, and metallization consists of e-beam evaporated layers of Ti/Au = 50/150 nm. Lift-off is performed in acetone. The top GaAs layer is selectively etched in a solution composed of NH_4OH : H_2O_2 (pH 8), for 6 seconds at T = 21 °C. Before etching the sample is dipped into D.I. H_2O for wetting purposes, and after etching the underlying AlAs etch stop layer is removed by a dip into HCl:H_2O = 1:10 at T = 21 °C. No agitation is performed while etching. The etch depth is confirmed with resist height measurement on diode structures.

Gate definition using e-beam exposure

For e-beam gates different PMMAs (950 K, 495K, 50K) and the copolymer PMMA/MAA(8.5) EL10 are used, with different layer stacks and thicknesses depending on the gate process, i.e. triangular shaped or mushroom gate (exact resist layer thicknesses are listed in Section 3.6.3).
- Before the gate recess etching, O_2-plasma etching at 20 W for 30 seconds is performed in order to clean the bottoms of the e-beam lines from resist traces, and thus facilitating the lift-off. The resist thinning due to O_2-plasma treatment is typically 25 - 45 nm.
- Prior to gate recess etch a wetting step consisting of 30 seconds in HCl : H_2O = 1:1 at T = 21 °C is applied.
- The gate recess etch is performed either using selective pH-adjusted NH_4OH : H_2O_2 solution or citric acid(CA):H_2O_2 = 1:1 solution. The citric acid is prepared by dissolving 1:1 weight ratio of citric acid monohydrate with deionized water. Both ammonia and CA-based solutions are freshly prepared before etching. No agitation is performed while etching.

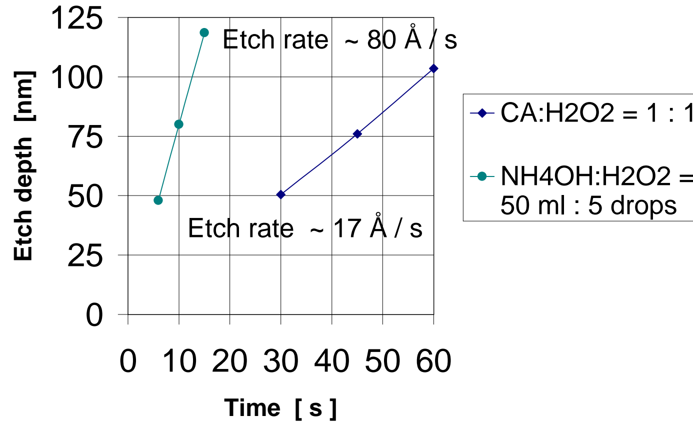

Figure 3.15: Etch depth for S.I. GaAs using CA : H_2O_2 (T = 20 °C) and NH_4OH : H_2O_2 (T = 21 °C).

- After etching the underlying AlAs etch stop layer is removed by a dip into HCl : H_2O = 1:10 at T= 21 °C. The AlAs selective etchant oxidizes the surface, so that in order to enhance the quality of the Schottky contact, the surface is cleaned using a mild selective phosphoric acid based etchant $H_3PO_4/H_2O_2/H_2O$ = 1:1:200 for 4 seconds just prior to metallization. The etch depth of the cap layer and the etch stop layer is confirmed with a resist height measurement using a monitor window of a size of 50 x 50 μm^2 exposed with e-beam on the mesa.
- Metallization is performed using e-beam evaporation (exact metal thicknesses are listed in Section 3.6.3).
- The final step, i.e. lift-off, is done in acetone, but without an ultrasonics (US) -treatment due to the narrow e-beam lines.

(4) **Interconnections**

The final metal layer defines the contacts for the probe heads and supply voltages. For patterning photoresist AZ5214 is used, followed by e-beam evaporation of Ti/Au = 20/200 nm, and subsequent lift-off in acetone.

3.6.3 E-beam Lithography

Electron beam lithography is used for defining the submicron electrodes for the MSM diodes on S.I. GaAs, and the gates for the pHEMT transistors. The used system is the Raith Turnkey 150 SEM with electron beam lithography software, consisting of LEO-32 (type 1530) SEM with a laser-interferometer stage (Raith) and the hardware module ELPHY Plus (Raith).

For high-resolution application a 300 μm x 300 μm writing field is chosen. The acceleration voltage is set to 20 kV, and the beam aperture to 10 μm giving a beam current of 32 - 45 pA and corresponding spot size of the incident beam in the range of 20 - 30 nm. The definition for the dose is [$\frac{\mu\text{C}}{\text{cm}^2}$]:

$$\text{Dose} = \frac{I_{beam}\, t_{dwell}}{\text{step size}^2} \;, \tag{3.88}$$

where I_{beam} is the beam current. t_{dwell} is called the dwell time, and it refers to the short exposure time (in the range of microseconds) after each step of the beam. The minimum step size of the beam is determined as: field size/2^{16}, corresponding to one pixel (in this process, with a field size of 300 μm the minimum step size$_{\text{min}}$ = 5 nm). In principle, highest resolution is achieved with smallest step size.

Proximity effect

Proximity effect, attributed to scattering events, results in a poor control of the shape and the linewidth of the gate metal. The primary electron beam leads to small angle scattering events (forward scattering in the resist), creation of secondary electrons with a typical energy of a few eV, and large angle scattering events (backscattering from the substrate) [129]. Figure 3.16 depicts the scattering events, and the energy distribution of the incident Gaussian beam.

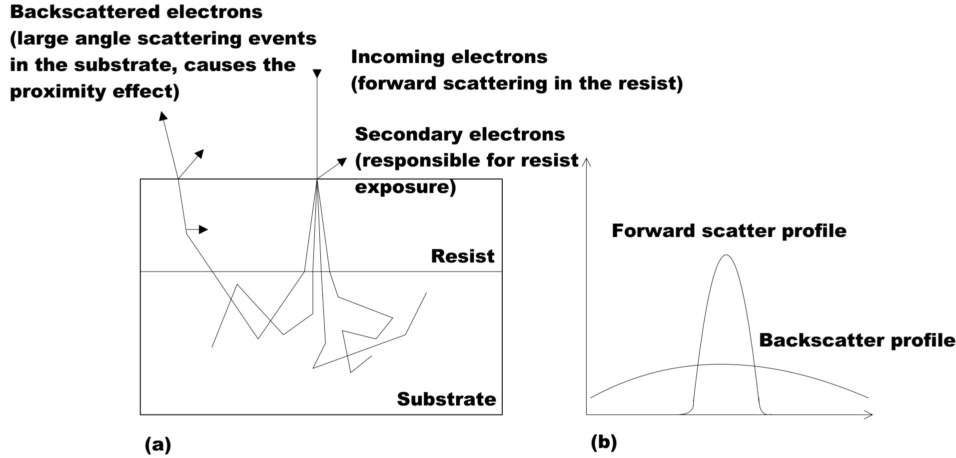

Figure 3.16: (a) Different scattering events. (b) Energy distribution of electrons in the resist.

Several different factors have an effect on the resolution of the linewidth. Principles, which lead to good resolution can be listed as: (1) Double or triple layer resist stack based on PMMA and PMMA/MAA both exhibiting high contrast. (2) Accelerating voltage as high as possible ($V_{acc} > 40$ kV) to prevent intra-proximity effect. (3) Total resist thickness as small as possible (d $<$ 800 nm) to minimize scattering effects within the resist [130].

In the following the different scattering mechanism are described in detail.

• *Forward scattering*

As the electrons penetrate the resist, they undergo many small angle scattering events, which result in a broader beam diameter at the resist-substrate interface than at the top. The increase in effective beam diameter is given by

$$d_{eff} = 0.9(R_0/V_{acc})^{1.5} \text{ [nm]}$$

where R_0 is the resist thickness in nanometers, and V_{acc} the acceleration voltage in kV [131]. From the equation is it clear that forward scattering can be minimized by utilizing the highest available beam voltage and the thinnest possible resist layer.

• *Secondary electrons*

Incident electrons, which slow down and dissipate much of their energy (2 to 50 kV) while propagating through the resist, are called secondary electrons. They cause the bulk of the actual resist to be exposed. Because their range is only a few nanometers in the resist, they contribute little to the total proximity effect. The effective widening of the beam diameter is roughly 10 nm [131]. Minority of secondary electrons may have high energies in the range of 1 keV, thus referred to as 'fast secondary electrons'. Their contribution to the proximity effect is in the order of a few tenths of a micron.

• *Backscattering*

Many of the electrons that penetrate through the resist into the substrate, experience large angle scattering events. They may return back into the resist, causing additional resist exposure, even at a significant distance from the incident beam. These backscattered electrons cause the actual proximity effect, contributing significantly to the total exposed electron dose. Since the intensity distributions of the incident beam as well as of the scattered electrons superpose the resultant spot size at the resist-substrate interface is significantly larger than the incident electron beam itself. For substrate materials with high backscattering efficiency this contribution could be up to 50 % of the total dose [132].

The amount and intensity of scattering events in the substrate is greatly determined by the semiconductor properties (type of substrate, low atomic number materials giving less backscatter) as well as the acceleration voltage (energy of the primary electrons). Energy deposited in the resist is roughly $\propto V_{acc}^{-1}$, i.e. with increasing V_{acc} the electrons penetrate deeper into the substrate, hence leading to less backscattered electrons at the resist-substrate interface. The dose is therefore proportional to the beam voltage [129]. The dose is also pattern dependent, since the total dose received in a given exposed area is affected by electrons scattered from the neighboring exposed areas. As shown in Fig. 3.16 the main contribution of the actual resist exposure is attributed to the backscattered electrons.

Clearing dose tests

Clearing dose tests were done for the used PMMAs (950K, 495K and 50K), the PMMA/MAA (i.e. the copolymer), and a 3-layer resist system (495K/50K/495K). The tests for the PMMAs and the copolymer are done on S.I. GaAs, while for the 3-layer-stack on pHEMT1. Squares of sizes of 50 x 50 μm^2 are used. The resist layer thickness is 200, 400 and 600 nm for the PMMA- the copolymer-and the 3-layer sample, respectively. The acceleration voltage is set to 20 kV. The remaining resist thickness is measured after exposure and development for each used dose value (with TENCOR Alpha Step 200 system). The contrast curves, i.e. normalized resist thickness (R/R0 = remaining resist thickness after exposure/original resist thickness) as a function of dose are shown in Fig. 3.17. The contrast of the resist is the slope of the remaining resist thickness versus the logarithm of the dosage. The figure proves, that highest sensitivity is measured for the copolymer, while lowest for the PMMA 495K. Furthermore, with increasing exposure dose the solubility increases for each resist type.

It is important to note:

• Here the tests were done for areas of 50 x 50 μm^2. The clearing dose, however, for narrow e-beam lines is considerably higher compared to that of big area squares attributed to the proximity effect which is more pronounced for larger areas. But the result for the big squares is already a good starting point and gives valuable information about the contrast of the different resists, and the sensitivity.

• Since all the exposure parameters are dependent on the physical properties of the substrate, especially regarding backscattering, the experiments done on S.I. GaAs are not directly comparable with tests that would have been done on pHEMT-structures.

• The test samples did not have any patterns (i.e. mesa, ohmic or alignment marks), so that the clearing dose will be slightly different for 'real' pre-structured samples.

Linewidth tests

Figure 3.18 presents the achieved linewidth versus dose, using 495K PMMA on S.I. GaAs. The resist thickness is 200 nm, acceleration voltage 20 kV, and metallization Ti/Au = 20/30 nm. The sample is etched prior to metallization (CA : H_2O_2=2:1, 5 s). This may have an effect on the final results, since the etchant most probably etches also resist traces and thins the resist layer on the bottom of the line. Thus, without etching, the optimum dose value for getting the desired linewidth would have been a bit higher. It can be seen that the dose increases when the linewidth gets smaller. This is due to the proximity effect, which is less pronounced in the case of narrower lines.

In Figure 3.19 is shown the achieved linewidth versus dose, using copolymer PMMA(8.5)MAA 10 % on S.I. GaAs. The resist thickness is 400 nm, acceleration voltage 20 kV, and metallization Ti/Au = 50/200 nm. For each linewidth the exposure is done with both 6 nm and 14 nm step size. It is obvious (as is already evident from the previous linewidth-test for the 495 K PMMA, Fig. 3.18), that the dose for a fixed step size has to be increased in order to achieve narrower lines.

In the following two aspects concerning the ***step size*** are addressed:

1. The 6 nm/10 nm step size in contrast to a step size of 14 nm was observed to be more suitable for exposing narrow lines (< 300 nm) (especially significant for the mushroom gates with small footprints). As long as the lines are not too narrow (< 100 nm) the step size actually has no direct influence on the accuracy of the linewidth. Instead, the step size affects the roughness of the edges. When smaller lines are exposed, the roughness of the edges is enhanced. By decreasing the step size from 14 to 6 nm/10 nm this effect can be overcome. The reason is that by using a

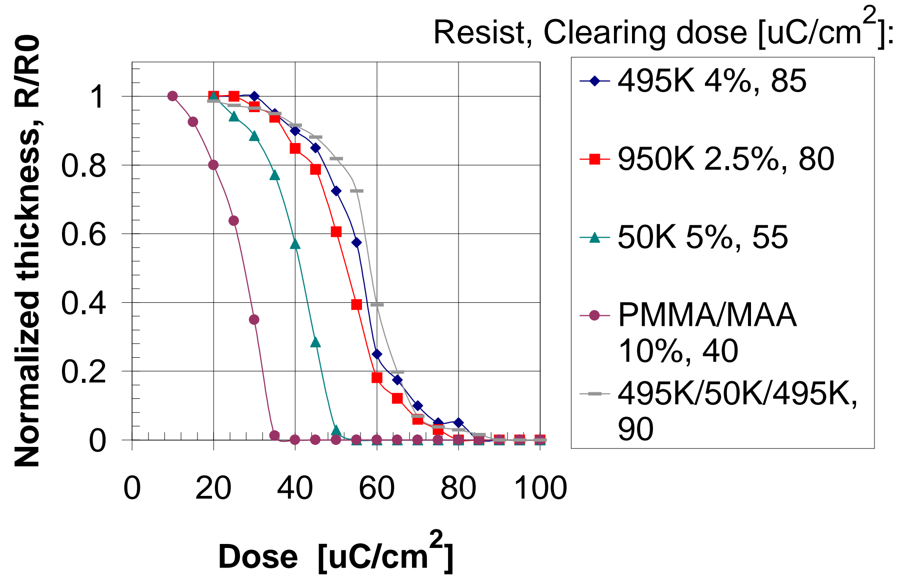

Figure 3.17: Clearing dose curves for the used PMMAs, the copolymer and a 3-layer-resist stack (squares of 50 x 50 μm^2, 20 kV).

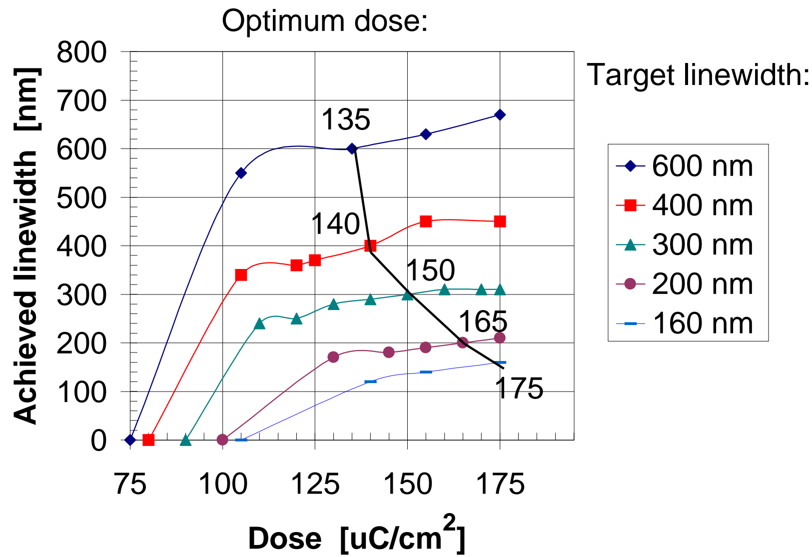

Figure 3.18: Achieved linewidth vs. used dose for different target linewidths, using 495 K PMMA 4 % on S.I. GaAs.

smaller step size there is more overlap of the separate exposures (after every step of the beam), which causes a smoothing of the edges. When writing very broad lines the roughness of the edges is not a problem, because there is an increased effect of the proximity effect, which makes the edges smoother. There are a lot more exposures in the middle of the broad line (also exposing the sides somewhat because of the proximity effect), so that the edges get even a higher dose distribution.

2. Figure 3.19 shows clearly that using the smaller step size of 6 nm, a higher dose (20 - 25 $\mu C/cm^2$) compared to the 14 nm step size is needed to obtain the desired linewidth. The reason for having a higher dose with smaller step size is more complicated to explain; only speculations can be given at this stage. After each step of the beam there is a very short exposure of some microseconds, which is the dwell time. This exposure has the shape of a circle and the size of the incident e-beam spot (30 - 100 nm at the surface of the wafer). Because of the proximity effect, which exists in each exposure, a certain area around this circle will also be slightly exposed. Part of it will get a dose high enough to be developed after the exposure. If the step size is halved, the dwell time is 4 x shorter, according to Eq. (3.88). The range of the backscattered electrons (causing the proximity effect) stays the same, but the area that gets a dose high enough to be developed becomes smaller because of the 4 x shorter dwell time. At the points where the steps of the beam overlap each other this is not noticed, but at the edges of the lines the reduced dwell time becomes relevant.

An other significant factor, which is especially crucial for multilayer resists, is the optimization of the development time. In this work a 30 second development time was used for both the one layer as well as the multilayer systems. In fact, when using multilayer resist stacks the development time should be increased. The development is always a process that is moving from the top to the bottom; starting in the center and spreading horizontally towards the sides. Ref. [133] shows how the resist profile changes during development (with 5 second intervals). The resist profile development for a T-gate (70 nm-thick PMMA 50K (top), 350 nm-thick P(MMA/MAA), 120 nm-thick PMMA 950K (bottom)) is calculated: after 20 seconds only the top layer is completely developed, whereas the outermost profile is reached only after 60 seconds [134].

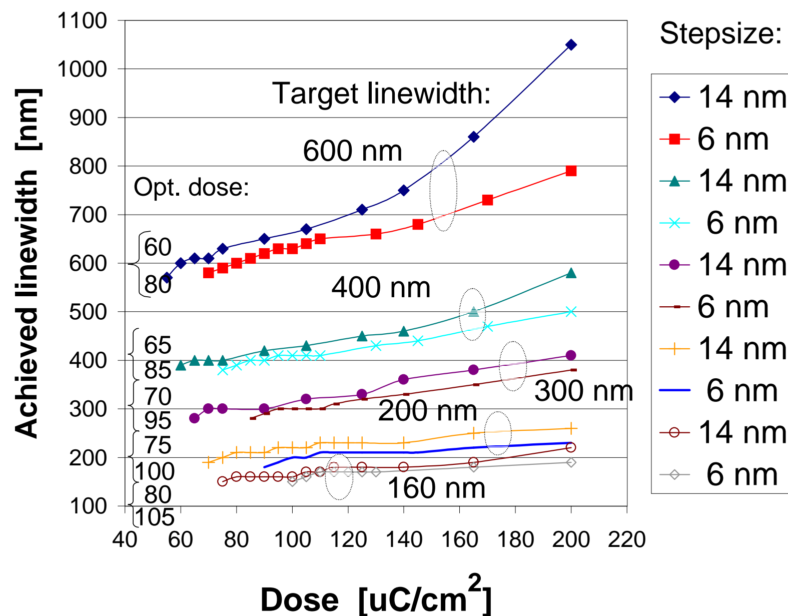

Figure 3.19: Achieved linewidth vs. used dose for different target linewidths, using copolymer PMMA/MAA 10 % on S.I. GaAs. For each linewidth a step size of 6 nm and 14 nm was used.

Triangular and mushroom shaped gates

Figure 3.20 shows the resist profiles for the 3 different used layer stacks, (a) resist system for triangular shaped gates, and the MSM electrodes, (b) and (c) layer stacks applied for mushroom shaped gates.

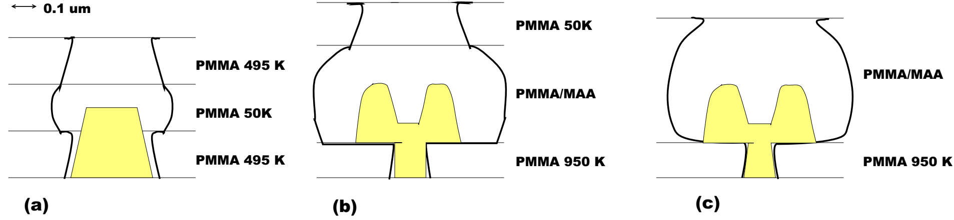

Figure 3.20: PMMA resist profiles. (a) triangular shaped gates and MSM fingers (b) 3-layer mushroom gates (c) 2-layer mushroom gates.

- PMMA layers for **triangular shaped gates**:
  495K/50K/495K = 200/180/200 nm, total thickness ~ 580 nm.
  Metallization: Ti/Au = 50/250 nm.

- PMMA/copolymer layers for **mushroom gates**:
  - 2-layer: copolymer/950K = 550/130 nm, total thickness ~ 680 nm.
  - 3-layer: 50K /copolymer/950K = 180/430/130 nm, total thickness ~ 740 nm.
  Metallization: Ti/Au = 50/350 nm.

The exact dose-values and other processing parameters can be seen Tables B.10 and B.11. Remarkable is the utilized resist thickness in contrast to the metal thickness. In principle, to guarantee a successful lift-off, the resist should be three times or at least twice as thick as the deposited metal. Here, however, for the triangular shaped gates the ratio of resist to metal is 1.9, and for the mushroom-gates it is 1.7. and 1.85 for 2-layer and 3-layer resist-systems, respectively. Despite of these low ratios no problems were encountered during lift-off.

The top layer in the resist structure is used for patterning of the T-gates. In addition, the process latitude and yield are improved. In this work the top layer in the triple-resist system was chosen to be PMMA 50K, since it has lower sensitivity compared to the underlying copolymer (see Fig. 3.17), thus guaranteeing a nice undercut lift-off profile.

The shape and the thickness of the gate determines the series resistance. A gate with a large cross-section area gives rise to a low gate resistance. Therefore, instead of a triangular or rectangular shape the cross section should be matched to a T-like (i.e. mushroom) shape, in which the upper wide layer increases the cross-section area of the gate. The benefit of T-shaped gates is further reduced gate capacitance attributed to the narrow footprint. See also remarks in Section 3.5.2 on p. 94-95.

The realization of T-shaped gates is somewhat more complicated than that of triangular-gates. For the **mushroom gates two separate exposures** have to be applied. First, a *single pixel line (SPL) exposure with high dose for the footprint definition* is necessary. A high dose is needed for the narrow beam to penetrate the total resist stack. Second, a *low dose exposure with a line of the desired linewidth for the top part definition* is used. The low dose has to be such, that the beam does not penetrate through the whole resist stack, but stops at the copolymer/ bottom-PMMA interface. Therefore, the copolymer has to be highly sensitive to electron beam, whereas the bottom PMMA layer less sensitive with a very high contrast-value. Obviously, the larger the difference between the sensitivity of the copolymer and the bottom-PMMA resist the easier it is to optimize the right exposure dose.

The step size is set to 14 nm (2 pixels) for all exposures except the mushroom gate single line exposures, in which the step size is 6 nm (1 pixel) and 10 nm (2 pixels) for 2-layer and 3-layer systems, respectively.

Figure 3.21 shows the SEM photograph of a triangular shaped e-beam written gate.

Figures 3.22 and 3.23 show fabricated mushroom gate pHEMTs.

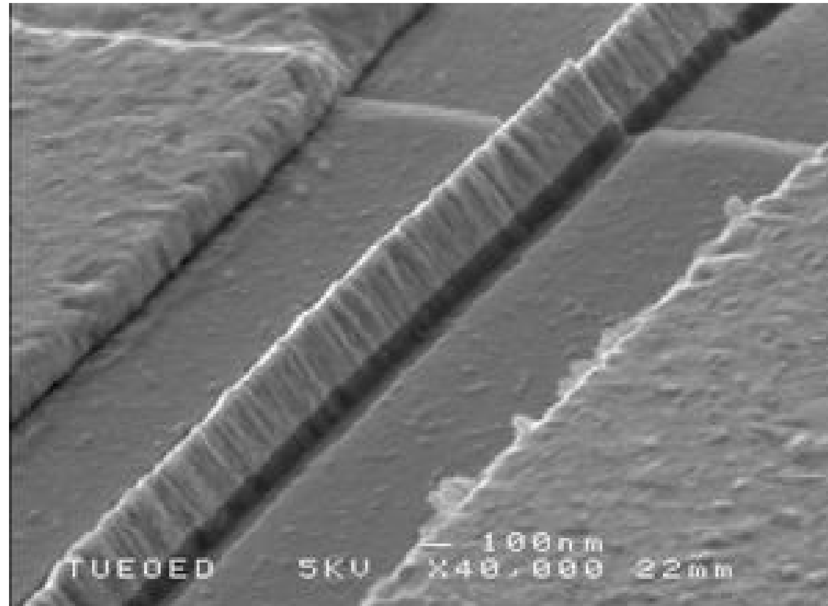

Figure 3.21: SEM photograph of a fabricated triangular shaped gate pHEMT. $l_g = 0.35\ \mu$m, $l_{DS} = 2.1\ \mu$m, $W = 10\ \mu$m, Ti/Au = 50/250 nm. Fabricated with 3-layer resist system (see Fig. 3.20 a).

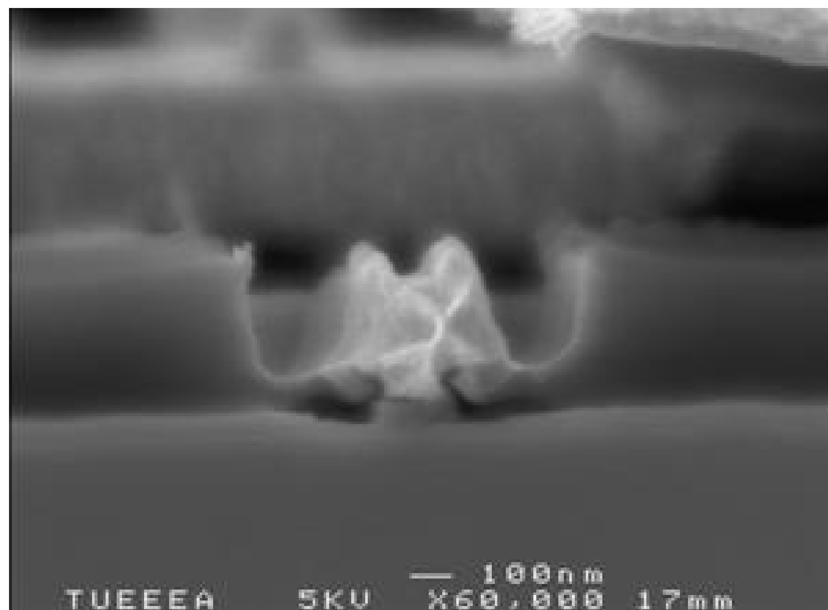

Figure 3.22: SEM photograph of a fabricated mushroom gate pHEMT (lift-off is not done yet). l_g in the middle part = 0.4 μm, footprint = 0.15 μm, Ti/Au = 50/350 nm. Fabricated with 3-layer resist system (see Fig. 3.20 b).

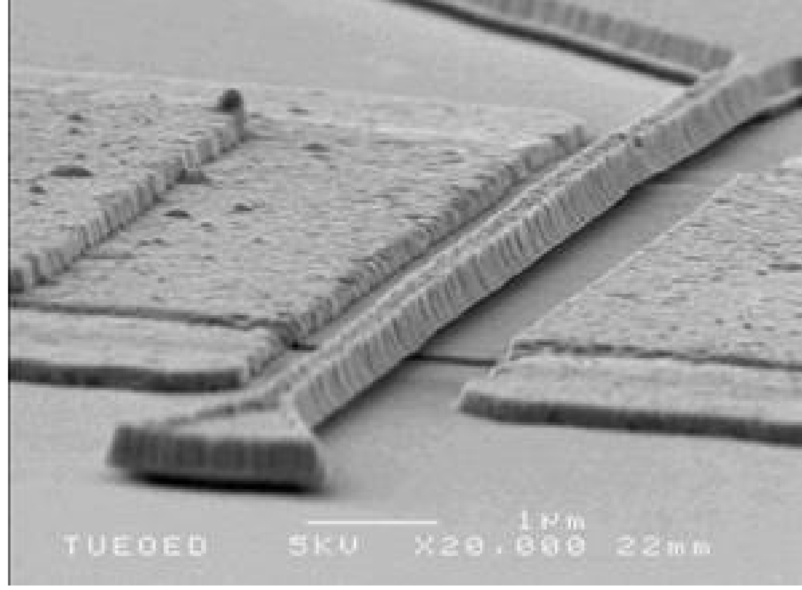

Figure 3.23: SEM photograph of a fabricated mushroom gate pHEMT. l_g in the middle part = 0.4 μm, distance between the peaks of the mushroom gate = 0.1 μm, l_{DS} = 1.4 μm, W = 20 μm, Ti/Au = 50/350 nm. Fabricated with 2-layer resist system (see Fig. 3.20 c).

3.7 Experimental Results and Simulations

3.7.1 DC Characteristics

Ohmic contact resistance and semiconductor sheet resistance

Two commonly used techniques, conventional linear TLM (LTLM) [135] as well as circular TLM (CTLM) [136] were applied for defining the ohmic contact resistance. The used measurement setup was HP4141B and a probe station with four tungsten probes. The measurement results for various pHEMT1 samples are indicated in Table 3.1. The samples were fabricated using identical processing steps (see Table B.8). However, due to small variations during processing, the contact resistance was observed to variate: measurements indicate a contact resistance in the range of 0.17 - 0.44 Ωmm.

• In the LTLM configuration the test pattern is composed of similar ohmic contact areas, differently spaced. The contacts have the width W, the length L, and are separated by a variable distance l. The whole pattern is mesa isolated to restrict current to flow only across the distance l, and to omit current spreading.

• In the CTLM configuration no mesa is needed due to the circular contact geometry, i.e. metal rings with various gap spacings. The CTLM simplifies the fabrication procedure, and achieves a more symmetrical current flow pattern by eliminating edge effects, lateral current crowding and gap effects, which always exist in the LTLM structures. The CTLM technique therefore results in more accurate results compared to those achieved utilizing the LTLM configuration.

Applying the LTLM configuration, the measured total resistance between two ohmic contacts with distance l is expressed as:

$$R = 2R_c + R_{sh}\frac{l}{W} = 2R_{shc}\frac{L_T}{W} + R_{sh}\frac{l}{W} \ , \tag{3.89}$$

where L_T is the transfer length (the lateral distance required for the current to flow into or out of the ohmic contact; $L_T << L$ = length of the ohmic contact), and R_{sh} and R_{shc} are the sheet resistance of the semiconductor layer between the contacts and under the contacts, respectively.

Plotting 3.89 as a function of the contact distance l yields the contact resistance and the sheet resistance: R_c is obtained from the intercept point with the Y-axis while R_{sh} from the slope of the curve. The contact resistance is usually expressed in [Ωmm], i.e. $r_c = R_c L$.

For alloyed contacts R_{shc} is lower than R_{sh}, while for nonalloyed contacts these element values may be considered to remain constant. In this work alloyed contacts were processed. However, considering $R_{shc} = R_{sh}$ gives a reasonable approximation and is thus used here. Knowing R_{shc} permits to determine L_T and further the specific contact resistance $r_c^* = R_c\,A_{eff} = R_c\,L_T\,W$, or alternatively $r_c^* = R_{sh}\,L_T^2$. r_c^* is the contact resistance of a unit area for current flow perpendicular to the contact. A_{eff} is hence the effective surface for conduction, i.e. not equal to the physical dimensions of the contact but the area restricted to the edges of the contact. L_T can also be obtained graphically from the $R(l)$ - curve intercept point with the x-axis: $L_T = l_0\,/\,2$. Both L_T and r_c^* are often used for characterization of the quality of the ohmic contacts.

The same procedure for obtaining the contact- and sheet resistance values applies for the CTLM technique: by plotting the measured total circular resistance as a function of gap spacing, and determining R_c, L_T and R_{sh} from the figure. It is obvious that the contact width W has to be replaced by $2\pi r$, where r is the radius of the inner disc contact. In order to yield accurate results, the nonlinear relationship between the original measured total resistance and the gap spacing is transformed into a linear relationship using correction factors calculated for the gap spacings. The gap spacings were measured due to inaccuracy induced by the fabrication process and thus different distances than specified on the mask. With the correction factors a linear CTLM data can be achieved. Further, a linear fit to this corrected data is used to obtain the final values, Fig. 3.24.

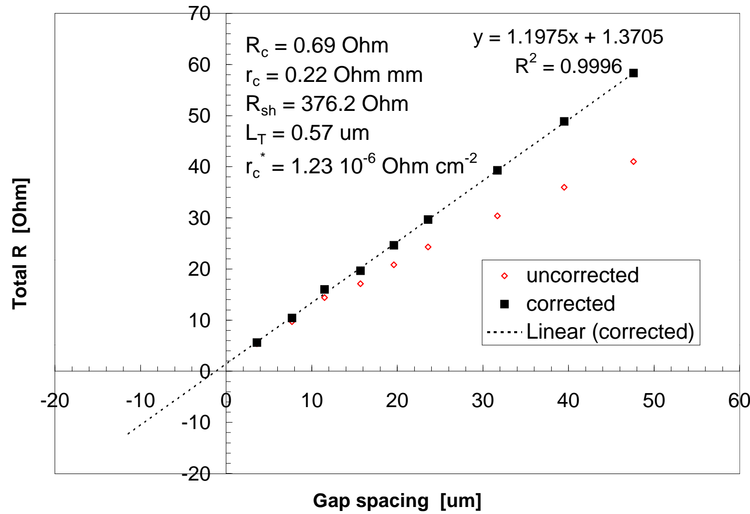

Figure 3.24: Original CTLM measurement and the linear fit approximation. R^2 is a measure for the quality of the linear curve fit (ideal situation $R^2 = 1$).

The resistivity ρ of the semiconductor is achieved by multiplying the sheet resistance by the thickness of the top semiconductor layer (mesa height): $\rho = R_{sh}d$. Since resistivity is defined as $\rho = \frac{1}{(n\mu_n + p\mu_p)q}$, the mobility may further be obtained. For the pHEMT structure the resistivity and mobility is, however, more complicated than the above description due to multiple layer conduction paths and different doping concentrations [95]. Taking the first measurement in Table 3.1, and using for the mesa $d = 85$ nm and n^+ GaAs cap layer doping of $n = 2 \cdot 10^{18}$ cm^{-3} yields $\rho = 3.16 \cdot 10^{-3}$ Ωcm and $\mu_n = 989$ cm^2/Vs. Theoretical values for resistivity and mobility for GaAs ($n = 2 \cdot 10^{18}$ cm^{-3}) are $\rho = 1.3 \cdot 10^{-3}$ Ωcm and $\mu_n = 2400$ cm^2/Vs [9].

Table 3.1: Parameters obtained from LTLM / CTLM for pHEMT1.

Method	R_c [Ω]	r_c [Ωmm]	R_{sh} [Ω]	L_T [μm]	r_c^* [Ωcm^2]
LTLM	3.10	0.31	372	0.84	$2.59 \cdot 10^{-6}$
LTLM	2.50	0.25	389	0.65	$1.63 \cdot 10^{-6}$
LTLM	2.25	0.23	393	0.55	$1.24 \cdot 10^{-6}$
LTLM	1.65	0.17	402	0.42	$6.85 \cdot 10^{-7}$
CTLM	0.95	0.30	387	0.77	$2.28 \cdot 10^{-6}$
CTLM	0.69	0.22	376	0.57	$1.23 \cdot 10^{-6}$
CTLM	1.39	0.44	376	1.16	$5.10 \cdot 10^{-6}$

2DEG sheet density and Hall mobility

The mobility and the electron sheet density of the 2DEG channel were measured for wafer pHEMT1 using the Van der Pauw method (I = 10 μA, B = 5.00 kG) at the Physics Department at TUE (TUE-NV group), Fig. 3.25. The measurement was done at different temperatures, under illumination and in the dark. The measured sheet densities of 2.113 $\cdot 10^{12}$ cm^{-2} and 2.118 $\cdot 10^{12}$ cm^{-2} at room temperature in the dark and under illumination, respectively, are close to the value given by the wafer supplier 2.7 $\cdot 10^{12}$ cm^{-2}.

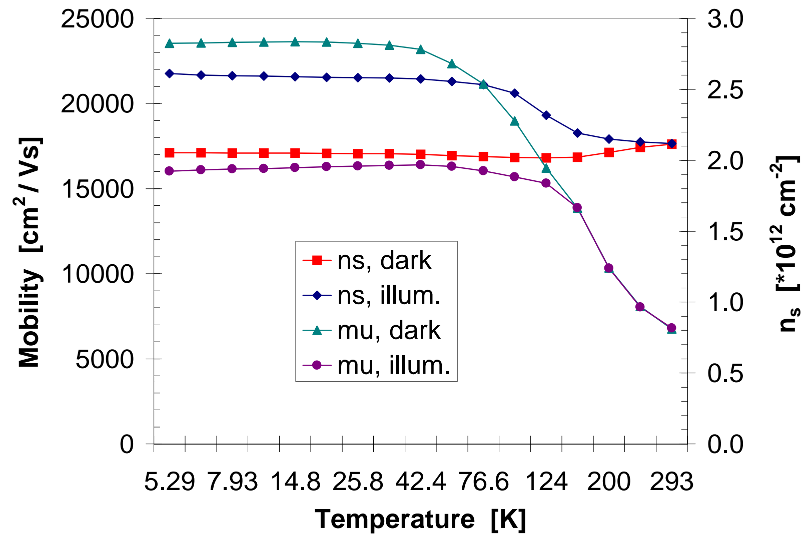

Figure 3.25: 2DEG Hall mobility and sheet density for pHEMT1 as a function of temperature, in the dark and under illumination.

Input capacitance and input resistance

The input capacitance and input conductance as a function of bias voltage were measured for submicron transistors with the HP4275A Multi-Frequency LCR meter at a frequency of 2 MHz (a CPW probe was placed on the gate and source contacts). Figure 3.26 presents the results as a function of voltage. The capacitance exhibits normal characteristics, i.e. increased capacitance as a function of voltage. The input resistance is in the MΩ range, decreasing at higher voltages, which is a sign of enhanced leakage currents.

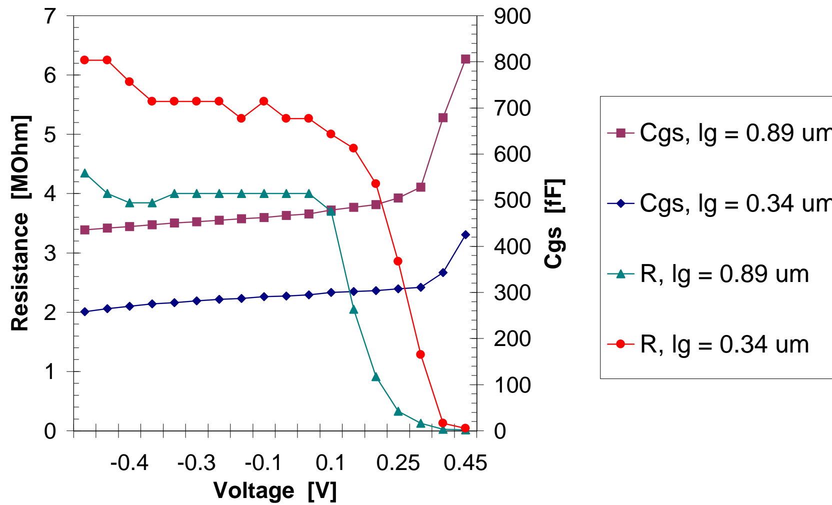

Figure 3.26: The input capacitance and input resistance measured for a U and T-type transistor with gate length of 0.89 μm and 0.34 μm, respectively. The gate width is $W = 160\,\mu$m. The measurement was done in the dark.

Circuit diagram for DC measurements and simulations

Figure 3.27 shows the circuit diagram for characterizing the DC behaviour of HEMTs, i.e. $I_{ds}(V_{ds})$ and $I_{ds}(V_{gs})$. The setup was used for both measuring and simulating the I-V characteristics. The transistor was modelled with the EEHEMT1-model (incorporating both DC- and AC-parameters) from MDS's standard device library. The detailed description of the used model can be seen in Section 3.5.3. The EEHEMT1-model parameters were obtained through IC-CAP parameter extraction method. The extraction procedure includes several different DC- and AC- measurements/simulations at various bias conditions in the frequency range from 50 MHz to 20.05 GHz. This was done for a standard as well as a submicron transistor. The results are listed in Appendix D in Figs. D.1 and D.2, respectively. The extraction simulations are rather complicated and time-consuming. Nevertheless, a fairly good fit could be obtained at most bias conditions for both type of transistors. The validity of the obtained parameters will be confirmed with DC- and AC- measurements/fittings. In the DC measurements a HP4141B DC Source/Monitor was used for measuring I_{ds} and biasing V_{ds} and V_{gs}. For measuring the gate current a HP4140B pA meter was used.

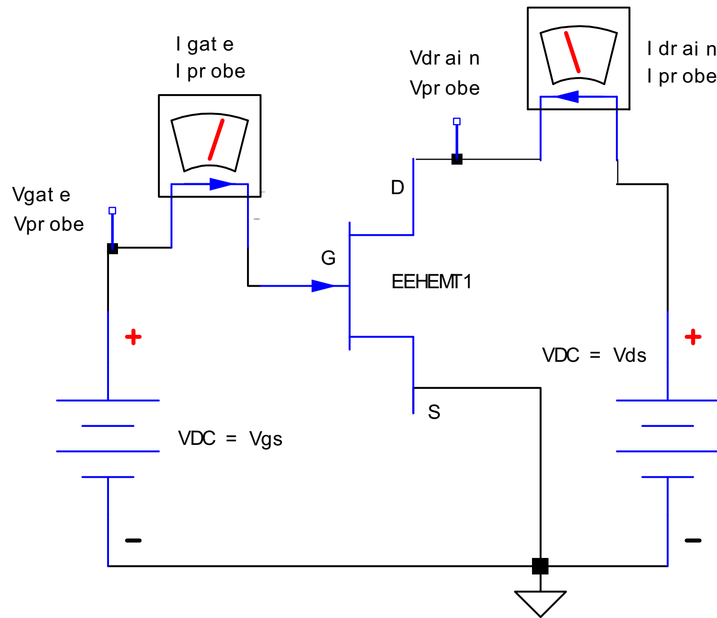

Figure 3.27: Circuit diagram for measurement and simulation of DC-characteristics of HEMTs.

Drain current $I_{ds}(V_{ds})$ and DC output conductance g_o

A drain current measurement as a function of V_{ds} at varying V_{gs} values is done for a submicron transistor (W = 200 μm), Fig. 3.28. Also is indicated the DC output conductance. The maximum voltage gain A_o at the peak transconductance condition is 55.9 (g_o = 1.4 mS and $g_{m,max}$ = 78.3 mS at V_{ds} = 2 V, V_{gs} = -0.25 V). The maximum drain current of I_{dmax} = 92 mA (460 mA/mm) is achieved at V_{ds} = 2.4 V and V_{gs} = 0.75 V. The drain current saturates, which indicates kink-free behaviour as well as no parallel conduction in layers above or/and underneath the channel (see Section 3.4.5 for short channel effects). The I_{ds} versus V_{ds} was measured for several transistors, clearly indicating the trend of lower output conductance for larger gate lengths. The results of the output conductance for a number of transistors lie between 3.4 mS/mm - 21.3 mS/mm, for which the corresponding A_o-values are in the range $\sim$ 23.1 - 91.

Fitting using the EEHEMT1-model

Figure 3.29 presents the measurement and simulation for a submicron transistor (W = 80 μm), using the EEHEMT1-model with IC-CAP extracted parameters indicated in Fig. D.2. A fairly good agreement is found between measurement and fitting. For this transistor also, neither kink effect nor parallel conduction phenomena are observed. The maximum drain current of I_{dmax} = 39 mA (487 mA/mm) is achieved at V_{ds} = 3 V and V_{gs} = 0.5 V.

Drain current $I_{ds}(V_{gs})$ and extrinsic DC transconductance g_m

- **Submicron transistors**

Varying gate widths

In Figures 3.30 and 3.31 is measured the drain current as a function of V_{gs} at V_{ds} = 2 V for submicron transistors (gate recess etching is done in citric acid solution for 30 s). Also is indicated the transconductance: in the former graph g_m is presented as an absolute value whereas in the latter as normalized to gate width (Tables 3.2 and 3.3 indicate the exact values). From the measurements it is evident that the DC transconductance increases for larger gate widths when the gate length is kept constant. For the largest measured gate width of 160 μm, however, the transconductance is noticed

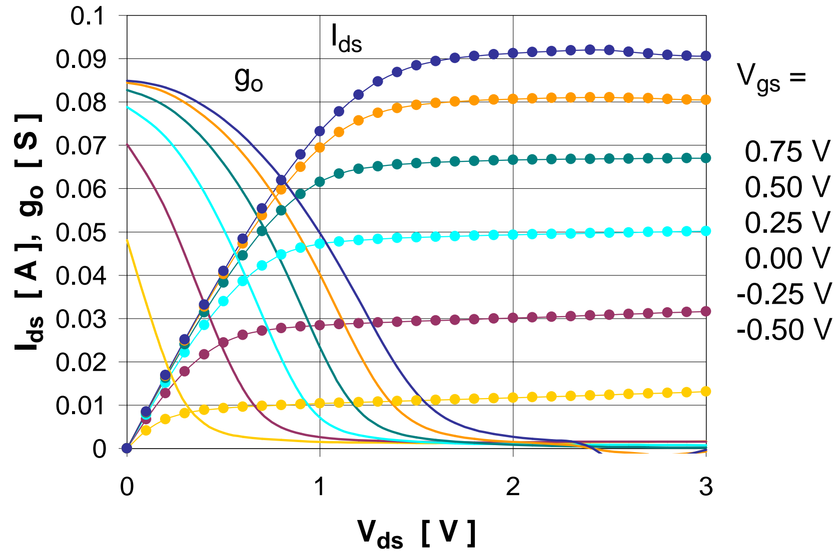

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Figure 3.28: Measured I_{ds} and g_o for a submicron transistor. l_g = 0.39 μm, W = 200 μm. g_o = 1.4 mS (7.0 mS/mm), $g_{m,max}$ = 78.3 mS (391.5 mS/mm), at V_{ds} = 2 V, V_{gs} = -0.25 V, I_{dsat} = 30.1 mA (150.5 mA/mm). A_o = 55.9. f_t = 38.8 GHz, f_{max} = 78.0 GHz, $|S_{21}|$ = 6.63 (16.4 dB) @ 0.25 GHz and V_{ds} = 2 V, V_{gs} = -0.161 V, I_{dsat} = 35.6 mA.

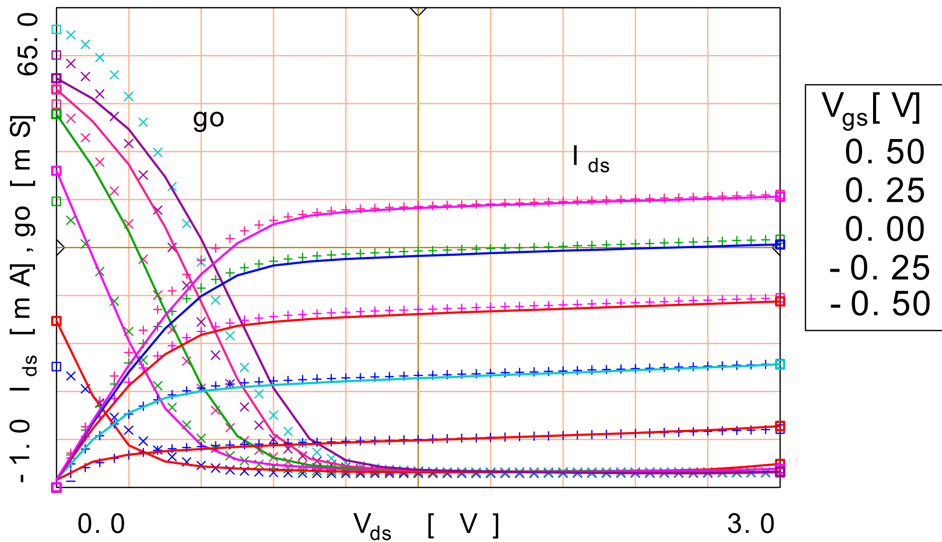

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Figure 3.29: Measured (solid line) and simulated (crosses) I_{ds} and g_o for a submicron transistor. Simulation done with parameters extracted from IC-CAP for the EEHEMT1-model (see parameters in Fig. D.2). l_g = 0.42 μm, W = 80 μm. g_o = 1.2 mS (15.4 mS/mm) $g_{m,max}$ = 36.2 mS (452.5 mS/mm) at V_{ds} = 2 V, V_{gs} = -0.25 V, I_{dsat} = 14.8 mA (73.8 mA/mm). A_o = 29.4. f_t = 45.1 GHz, f_{max} = 103 GHz, $|S_{21}|$ = 3.32 (10.4 dB) @ 0.25 GHz and V_{ds} = 2 V, V_{gs} = -0.184 V, I_{ds} = 16.73 mA.

to decrease slightly. It is emphasized that the plotted g_m values are extrinsic transconductances. This explains the fact that the normalized transconductances [mS/mm] are not constant for various gate widths; the intrinsic g_m values should be compared instead, see Eq. (3.82).

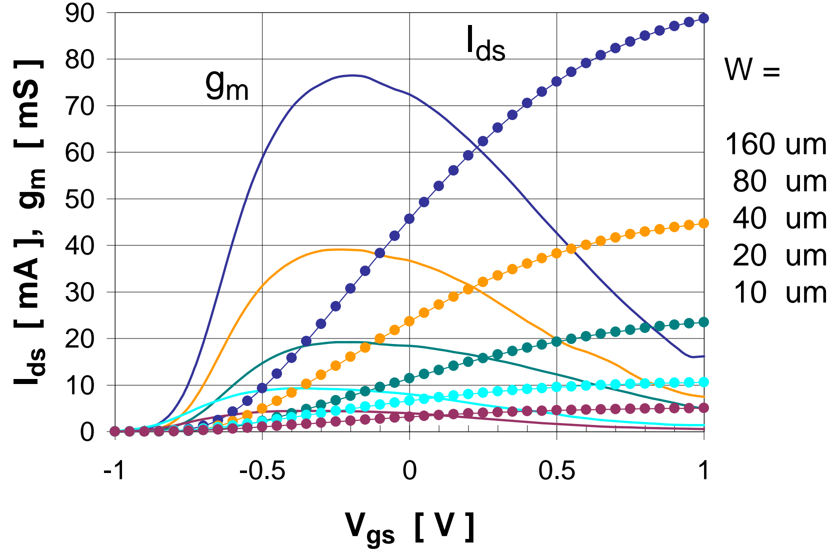

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Figure 3.30: Measured I_{ds} and extrinsic g_m for submicron transistors with varying gate widths. $l_g = 0.35$ μm, $V_{ds} = 2\,V$.

Table 3.2: Maximum DC transconductance for different gate widths. $l_g = 0.35$ μm, $V_{ds} = 2$ V. The indicated V_{gs}-voltages correspond to the maximum g_m-values. See Fig. 3.30.

W [μm]	$g_{m,max,DC}$ [mS]	$g_{m,max,DC}$ [mS/mm]	V_{gs} [V]
10	5	446	-0.35
20	9	465	-0.40
40	19	481	-0.20
80	39	489	-0.25
160	77	478	-0.20

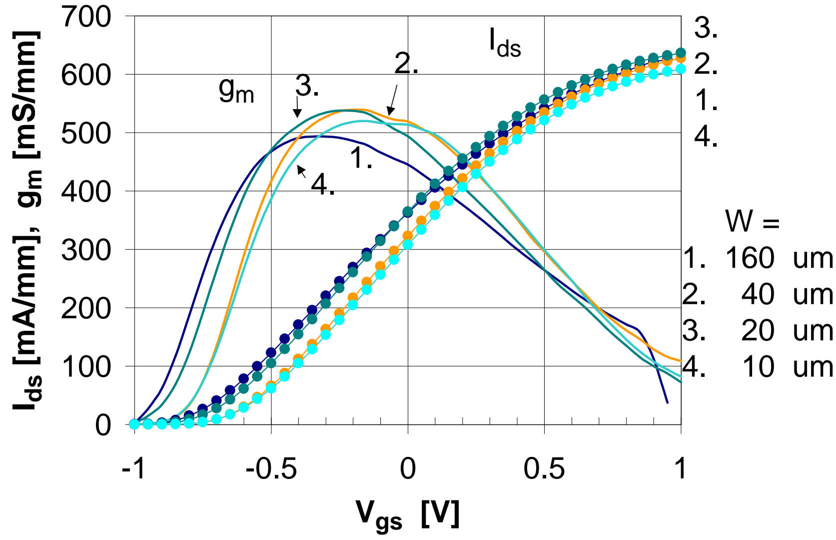

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Figure 3.31: Measured I_{ds} and extrinsic g_m per device width for submicron transistors. $l_g = 0.34$ μm, $V_{ds} = 2$ V.

Table 3.3: Maximum DC transconductance for different gate widths. $l_g = 0.34$ μm, $V_{ds} = 2$ V. The indicated V_{gs}-voltages correspond to the maximum g_m-values. See Fig. 3.31.

W [μm]	$g_{m,max,DC}$ [mS]	$g_{m,max,DC}$ [mS/mm]	V_{gs} [V]
10	5	520	-0.15
20	11	538	-0.25
40	22	539	-0.20
160	79	493	-0.35

Varying gate lengths

The transconductance depends also on the gate length: for decreasing gate length g_m increases keeping the gate width fixed, Figs. 3.32 and 3.33 (gate recess etching done in citric acid solution for 30/45 s). In the former figure g_m is normalized to the gate width of 40 μm, while in the latter graph g_m is presented as an absolute value for transistors with a gate width of 80 μm (Tables 3.4 and 3.5 indicate the exact values).

Varying gate widths and lengths

The gate length and width both affect the transconductance, as already confirmed in the previous graphs (Figs. 3.30 - 3.33). These both dependencies are plotted in Fig. 3.34 for submicron transistors, showing that with increasing gate length and width the g_m decreases and increases, respectively.

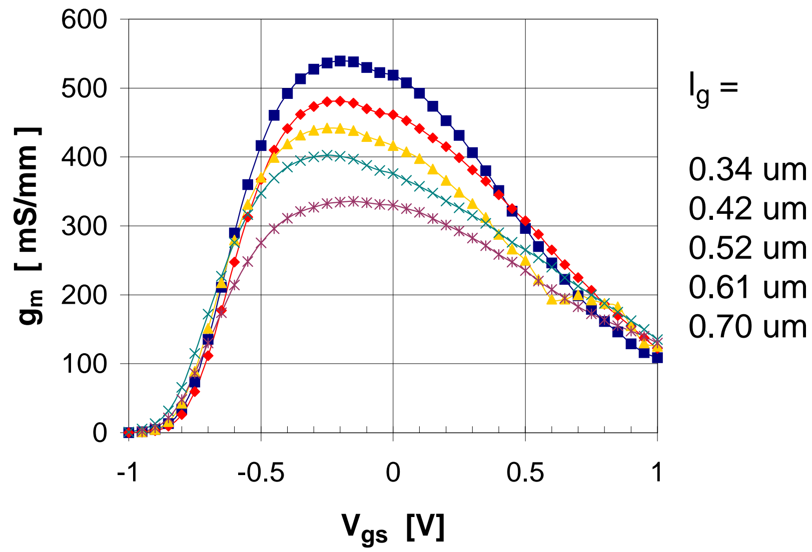

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Figure 3.32: Measured I_{ds} and extrinsic g_m for submicron transistors with varying gate lengths. $W = 40\ \mu$m, $V_{ds} = 2$ V.

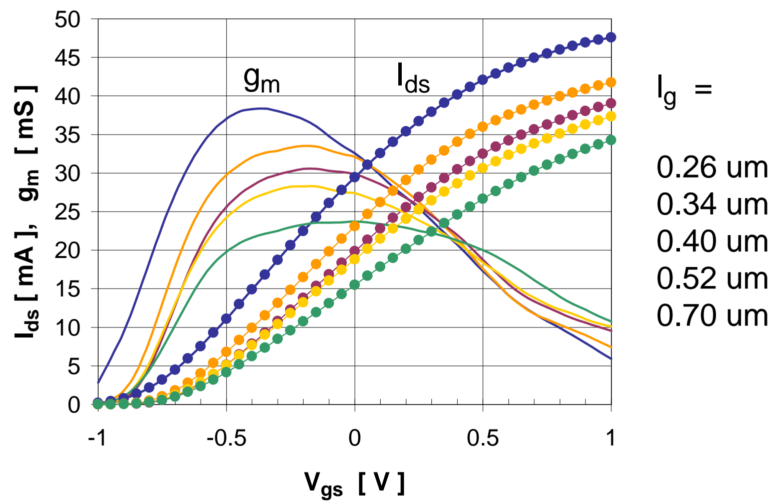

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Figure 3.33: Measured I_{ds} and extrinsic g_m for submicron transistors with varying gate lengths. $W = 80\ \mu$m, $V_{ds} = 2$ V.

Table 3.4: Maximum DC transconductance for different gate lengths. $W = 40$ μm, $V_{ds} = 2$ V. The indicated V_{gs}-voltages correspond to the maximum g_m-values. See Fig. 3.32.

l_g [μm]	$g_{m,max,DC}$ [mS]	$g_{m,max,DC}$ [mS/mm]	V_{gs} [V]
0.70	13	336	-0.15
0.61	16	403	-0.25
0.52	18	442	-0.25
0.42	19	481	-0.20
0.34	22	539	-0.20

Table 3.5: Maximum DC transconductance for different gate lengths. $W = 80$ μm, $V_{ds} = 2$ V. The indicated V_{gs}-voltages correspond to the maximum g_m-values. See Fig. 3.33.

l_g [μm]	$g_{m,max,DC}$ [mS]	$g_{m,max,DC}$ [mS/mm]	V_{gs} [V]
0.70	24	296	-0.00
0.52	28	353	-0.20
0.40	31	382	-0.20
0.34	34	418	-0.15
0.26	38	479	-0.35

Fitting using the EEHEMT1-model

Figure 3.35 shows the measurement and simulation for a submicron transistor, using the EEHEMT1-model with IC-CAP extracted parameters indicated in Fig. D.2. The result is very satisfactory.

- **Standard transistors**

$I_{ds}(V_{gs})$-measurement was done at different V_{ds}-voltages for a standard transistor, Fig. 3.36. It is evident from the graph, that increased drain-to-source voltage leads to higher peak transconductance. The maximum transconductance rises from 316.8 mS/mm (63.4 mS) at $V_{ds} = 1$ V up to 362.5 mS/mm (72.5 mS) at $V_{ds} = 4$ V.

Figures 3.37 and 3.38 show parallel conduction appearing at higher V_{gs} and V_{ds}-voltages (i.e. second peak in g_m-characteristics), observed for standard transistors with $l_g = 1.1$ μm. With increasing gate voltage, the conduction band of the AlGaAs-layer will touch the Fermi-level (see Fig. 3.3 in Section 3.2). A change in gate potential no longer modulates the field strength at the heteroinferface, hence the 2DEG is shielded from the gate and saturates towards its maximum sheet density. At this point a parallel conduction path along the AlGaAs-layer is created, leading to broadened g_m-curve, i.e. the ideal bell-shape broadens at large V_{gs} and V_{ds}-voltages. In Fig. 3.37 the maximum transconductance decreases from 312.5 mS/mm (62.5 mS) at $V_{ds} = 1$ V down to 289 mS/mm (57.8 mS) at V_{ds} 3 V, together with more pronounced deviation from the ideal bell-shape. A second peak appears at $V_{gs} = 0.55$ V and $V_{ds} = 3$ V, with g_m of 275 mS/mm (55 mS), clearly indicating the onset of parallel MESFET.

The effect of the parallel conduction is seen even more clearly in Fig. 3.38, in which the second peak at V_{ds} of 4.5 V is larger than the 'real' $g_{m,max}$: 429.4 mS/mm (34.4 mS) at $V_{gs} = 0.7$ V compared to the 'real' peak of 303.2 mS/mm (24.3 mS) at $V_{gs} =$ -0.15 V. At $V_{ds} = 3.5$ V the parallel conduction is not so pronounced yet, the second peak being less than the 'real' maximum: 288.8 mS/mm (23.1 mS) at $V_{gs} = 0.85$ V compared to the 'real' peak of 313.9 mS/mm (25.1 mS) at $V_{gs} = 0.05$ V.

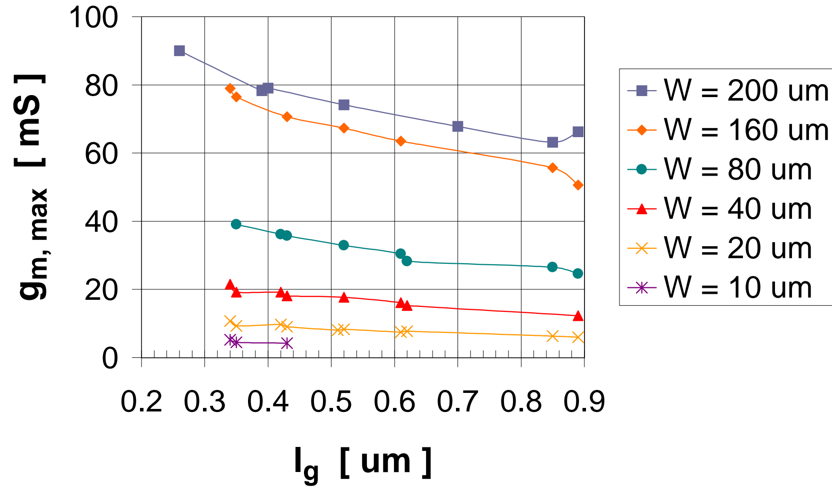

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Figure 3.34: DC $g_{m,max}$ for transistors with varying gate lengths and widths. V_{ds} = 2 V.

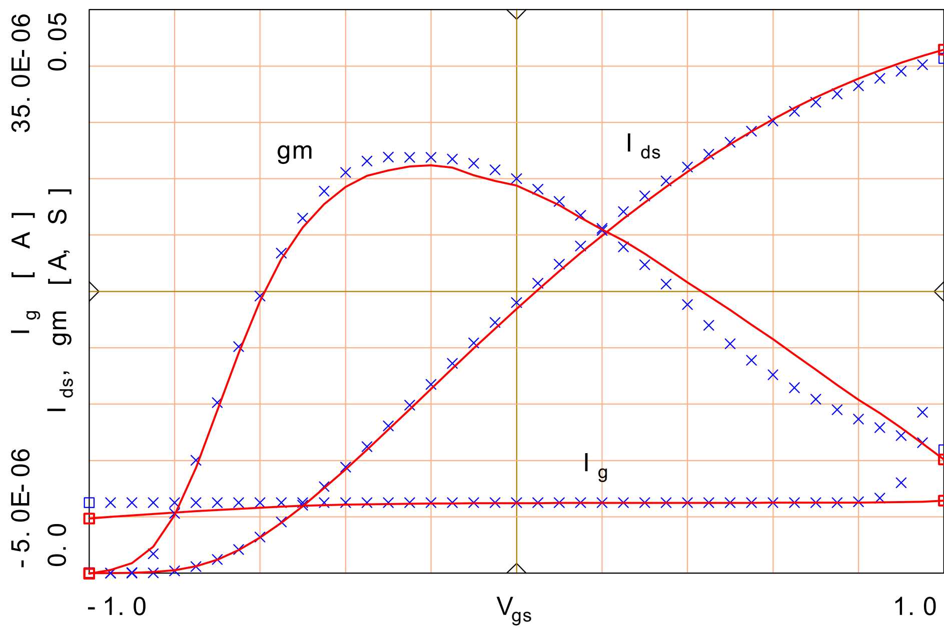

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Figure 3.35: Measured (solid line) and simulated (crosses) I_{ds}, g_m and I_g for a submicron transistor (V_{ds} = 2 V). Simulation is done with parameters extracted from IC-CAP for the EEHEMT1-model (see parameters in Fig. D.2). l_g = 0.42 μm, W = 80 μm.

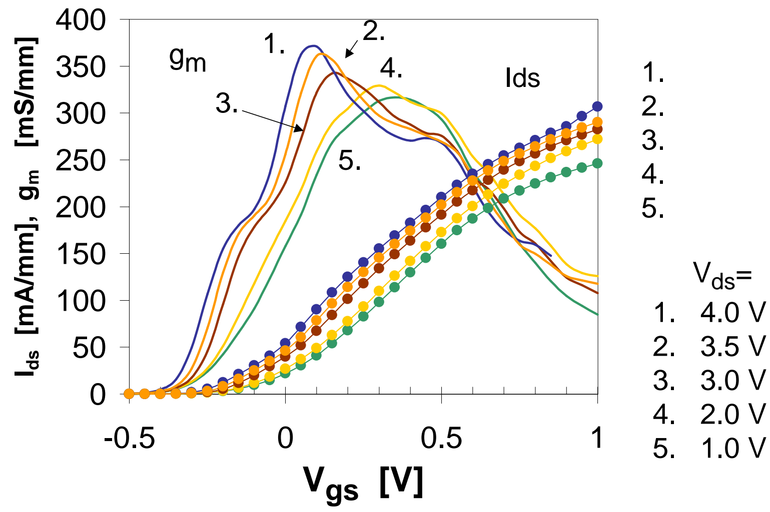

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Figure 3.36: Measured I_{ds} and g_m for a standard transistor at different V_{ds}-voltages. $l_g = 1.1\ \mu$m, $W = 200\ \mu$m, pHEMT3.

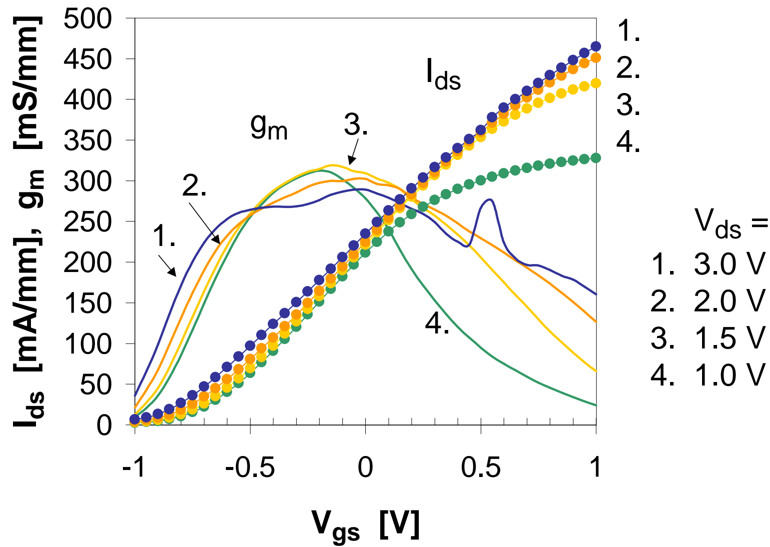

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Figure 3.37: Measured I_{ds} and g_m for a standard transistor at different V_{ds}-voltages. $l_g = 1.1\ \mu$m, $W = 200\ \mu$m, pHEMT1.

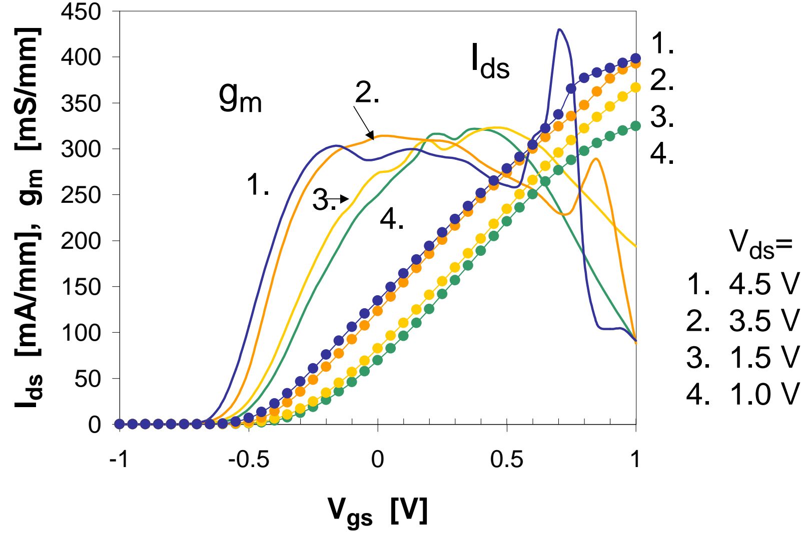

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Figure 3.38: Measured I_{ds} and g_m for a standard transistor at different V_{ds}-voltages. l_g = 1.1 μm, W = 80 μm, pHEMT3.

- **Comparison between standard and submicron transistors**

For several transistors the $I_{ds}(V_{gs})$-characteristics was measured at different V_{ds}-values, in order to see which is the optimum drain-to-source voltage for achieving maximum $g_{m,max}$. The results are presented in Fig. 3.39. The maximum tranconductance is obtained at V_{ds}-values around 1 - 2 V. Table 3.6 indicates the exact maximum g_m values. The figure also clearly shows that standard transistors with l_g of 1.1 μm obtain the lowest g_m compared to those of triangular shaped-gate or mushroom-gate transistors. In addition, it can be noticed that the standard transistors fabricated on pHEMT3-structure exhibit larger amplification compared to transistors fabricated on pHEMT1 and pHEMT2.

Table 3.6: $I_{ds}(V_{gs})$-measurement results (see Fig. 3.39). standard = optically fabricated gates. eb = e-beam written gates. triang. = triangular shape. mushr. = mushroom shape, fabricated with 2-layer resist.

Device	l_g/l_{DS} [μm]	W [μm]	V_{ds} [V]	V_{gs} [V]	$g_{m,max}$ [mS/mm]
pHEMT1, eb / triang.	0.34/1	40	1	-0.15	553
pHEMT1, eb / triang.	0.34/1	160	1.4	-0.25	500
pHEMT1, eb / mushr.	top 0.4	200	2	-0.5	415
pHEMT3, standard	1.1/3.8	200	1.5	0.35	337
pHEMT2, standard	1.1/3.8	200	1.5	-0.5	316
pHEMT1, standard	1.1/3.8	80	1.5	0.05	316

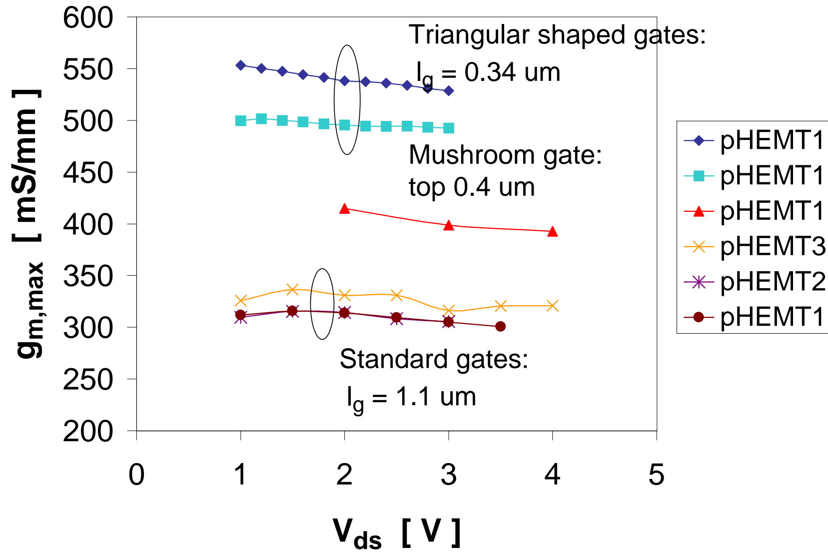

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Figure 3.39: $g_{m,max}$ as a function of V_{ds} for e-beam and standard transistors.

DC voltage amplification A_o

The maximum DC voltage amplification as a function of drain voltage ($A_o = \frac{g_{m,max}}{g_o}$, as defined in Eq. (3.62)) is depicted in Fig. 3.40.

The maximum A_o as a function of gate to source voltage for different V_{ds}- values, Eq. (3.62), is presented in Fig. 3.41.

The voltage gain is not necessarily largest for small-dimension transistors. Small-gate-length transistors (in the submicron range) have a high transconductance, but on the other hand a high level of leakage current and hence high output conductance. Therefore, the ratio g_m/g_o may be smaller for a submicron transistor compared to that of a larger gate-length device. This is seen in Fig. 3.42, where the highest A_o is achieved for a transistor with $l_g = 0.85$ μm. The voltage gain measured for a standard transistor ($l_g \sim 1$ μm) exhibited a large A_o-value of 91.1 ($g_m = 313.1$ mS/mm, $g_o = 3.4$ mS/mm).

Gate current

The gate current I_{gs} is basically the Schottky diode current between the gate and the source (thermionic emission current explained in detail in Section 2.3.2, Eq. (2.45)). Figure 3.43 shows the measurement for submicron transistors with varying gate lengths and a gate width of 40 μm. The reverse current is very low being in the nA range, and the forward current starts to increase at $V_{gs} = 1$ V. In the reverse bias region the leakage current is such a low value that the surface currents actually may dominate, attributed to unpassivated surface between the gate and the source [27].

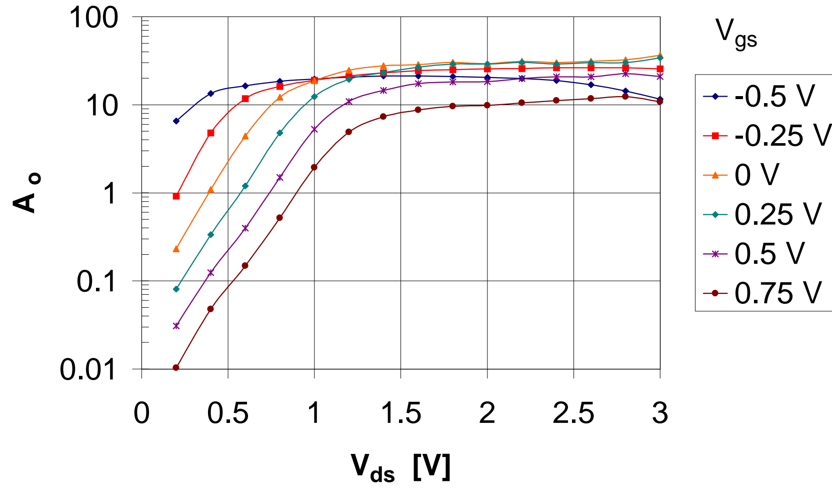

Figure 3.40: The DC open loop voltage gain A_o as a function of V_{ds} at different V_{gs} voltages for submicron pHEMT1 (l_g = 0.34 μm, W = 40 μm). At the optimum operating point of V_{gs} = -0.14 V and V_{ds} = 2 V: f_t = 44.9 GHz, f_{max} = 80.7 GHz, $|S_{21}|$ = 2.05 @ 0.25 GHz and g_m(DC) = 21.5 mS (538 mS/mm).

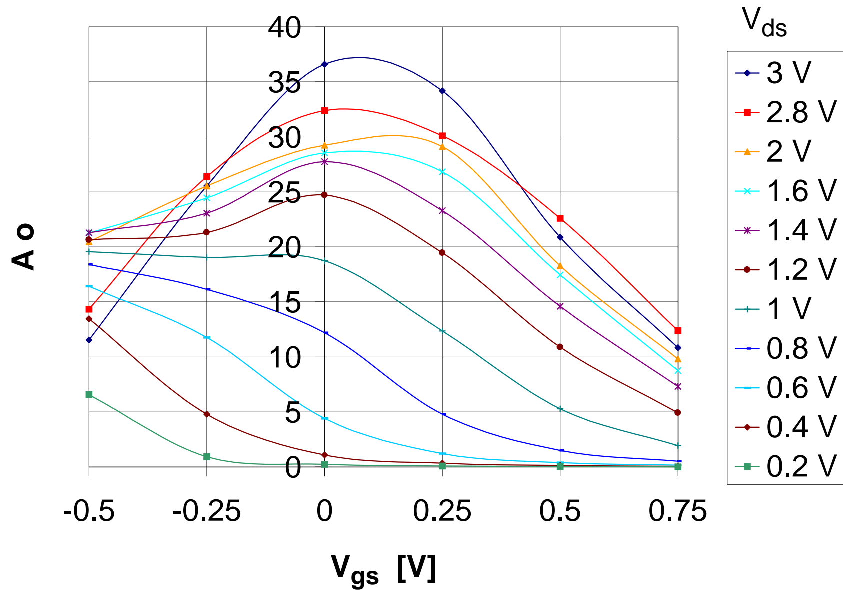

Figure 3.41: The DC open loop voltage gain A_o as a function of V_{gs} at different V_{ds} voltages for submicron pHEMT1 (l_g = 0.34 μm, W = 40 μm).

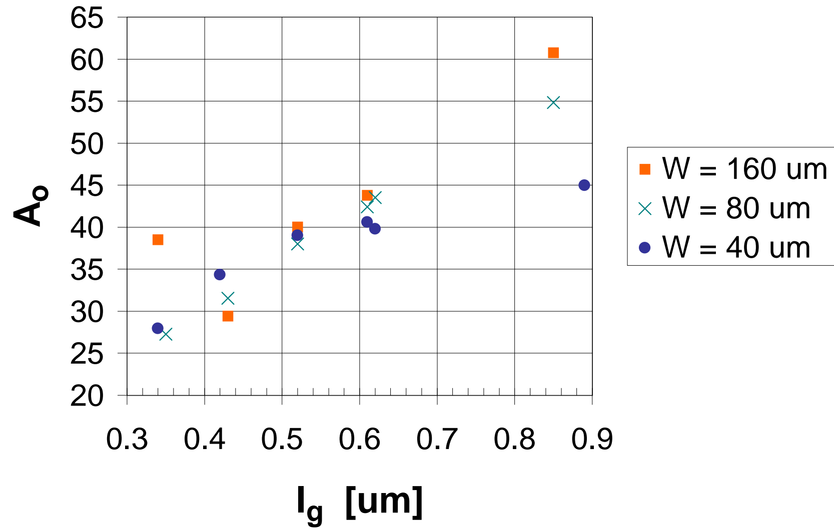

Figure 3.42: The DC open loop voltage gain A_o as a function of gate length for submicron transistors fabricated on pHEMT1 with varying gate widths (V_{ds} = 2 V, V_{gs} depending on the transistor).

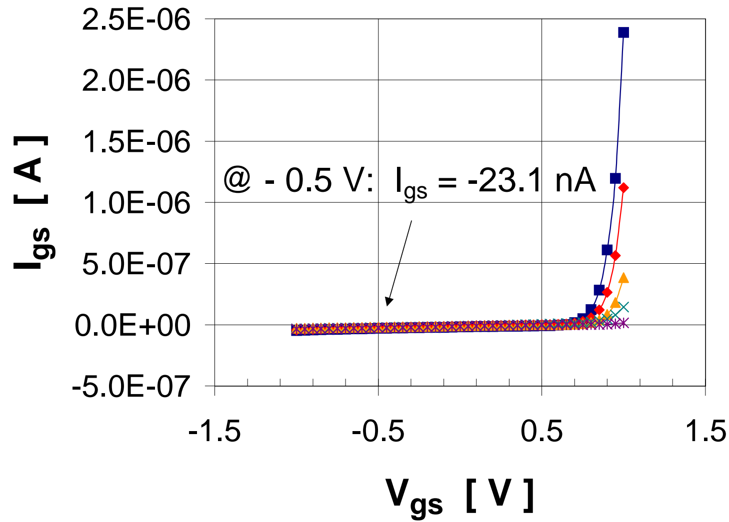

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Figure 3.43: Gate current as a function of V_{gs} for submicron transistors. W = 40 μm, l_g varying, V_{ds} = 2 V.

3.7.2 S-parameters

Circuit diagram for S-parameter measurements and simulations

Figure 3.44 shows the circuit diagram for characterizing the high frequency behaviour of HEMTs. The setup was used for both measuring and simulating the bias dependent scattering parameters at microwave frequencies ranging from 50.0 MHz to 40.05 GHz. The EEHEMT1-model (like in the DC characterization) from MDS's standard device library was used for modelling the transistor behavior.

The on-wafer S-parameters were measured with the HP85107A Network Analyzer System. Conditions while measurement were: room temperature, dark environment and output power set to 0 dBm at the analyzer (the test-signal for small-signal measurements was -10 - -13 dBm). Bias-Ts were used for supplying the DC gate and drain voltages as well as the RF signals from S-ports 1 and 2 to the transistor. It is emphasized, that in the following all presented values (e.g. g_m, f_t and f_{max}) are extrinsic measurement results.

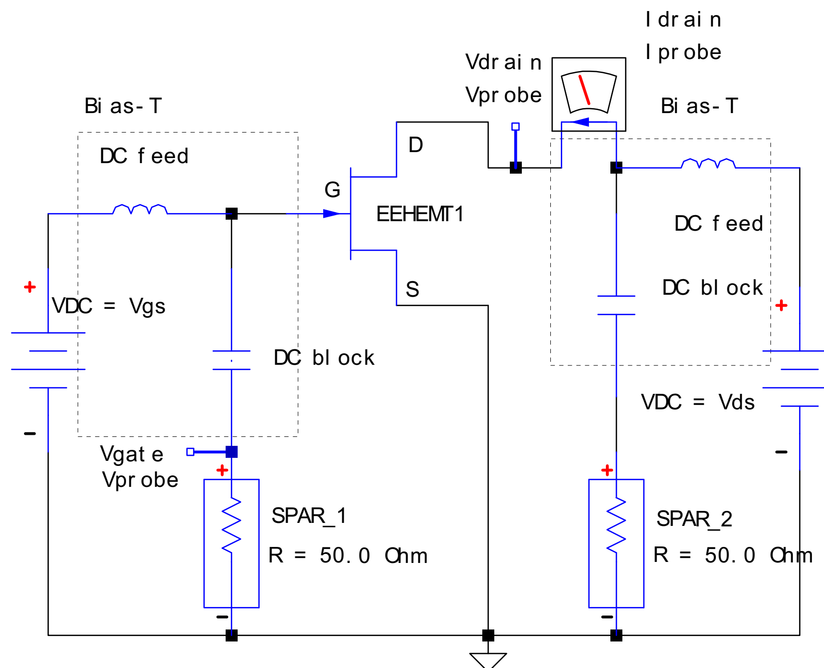


Figure 3.44: Circuit diagram for measurement and simulation of S-parameters for HEMTs.

K-factor, MSG and MAG

In Figure 3.45 is shown the extrapolation method for achieving f_t and f_{max} (- 6 dB/octave) (definitions according to Eqs. (3.68) and (3.69), respectively). Also is presented the K-factor as well as MSG and MAG for a submicron transistor, Eqs. (3.66), (3.70) and (3.71), respectively.

Measurements for triangular shaped transistors

Varying gate widths

Increasing the gate width and keeping the gate length constant leads to higher amplification and also frequency, Fig. 3.46 (a sample for which the gate recess etching is done in ammonia based solution for 5 s). For a wider gate (here with fixed gate length and gate-to-channel distance), the input capacitance becomes larger, which can be seen in S_{11}: It extends longer for increased W, thus having a lower imaginary part at the high frequency end. For wider gates S_{11} also bends more inwards, which is an indication of larger gate resistance (fixed l_g and metal thickness). $|S_{21}|$ is a measure of the

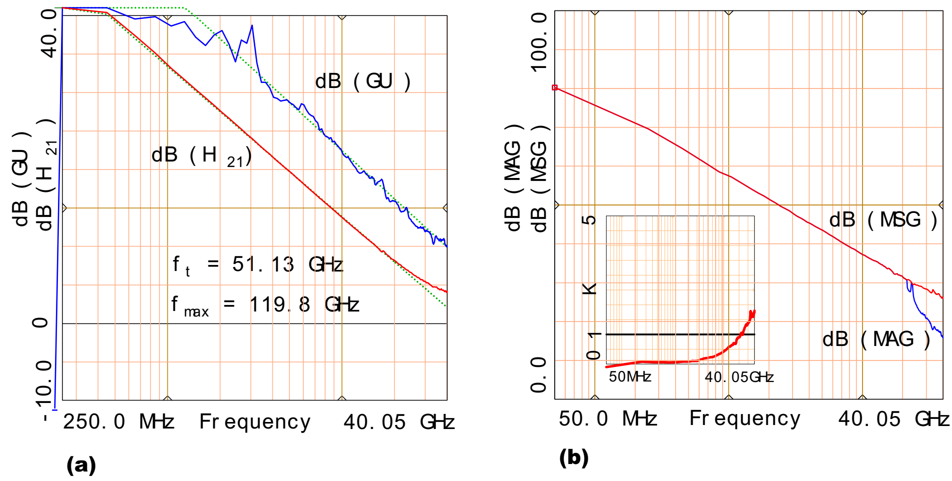


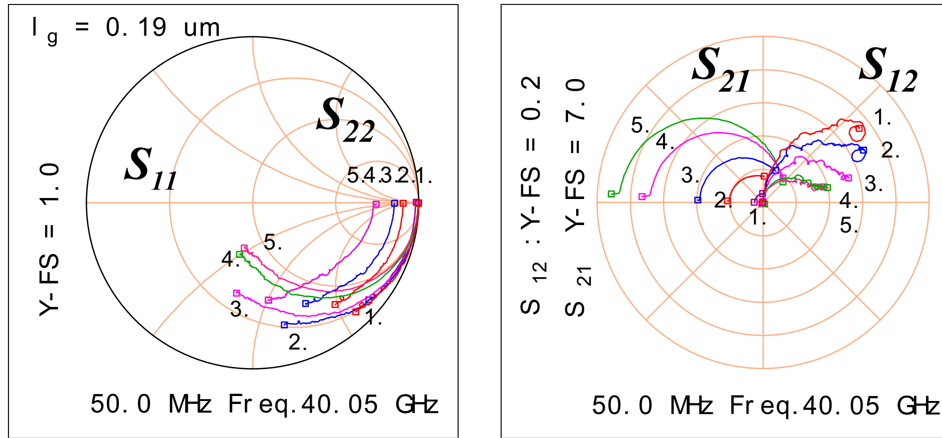
Figure 3.45: (a) f_t and f_{max} extrapolated from dB(h_{21}) and dB(GU), respectively. Extrapolation is shown with dotted lines. (b) dB(MSG) and dB(MAG) (the inset shows the K-factor). Submicron pHEMT1: l_g = 0.34 μm, W = 160 μm, V_{ds} = 2 V, V_{gs} = -0.268 V.

transistor amplification, being largest at low frequencies. S_{22} shows mainly R_{ds} (at the output from drain-to-source). At low frequency the curve starts at the AC resistance value given by the chosen bias point (differential R in $I_{ds}(V_{ds})$ plot). Since for some devices the curves start more to the left, R_{ds} is lower. The transmission from port 2 to 1, i.e S_{12}, is small (note the scale in the polar plot).

Varying gate lengths

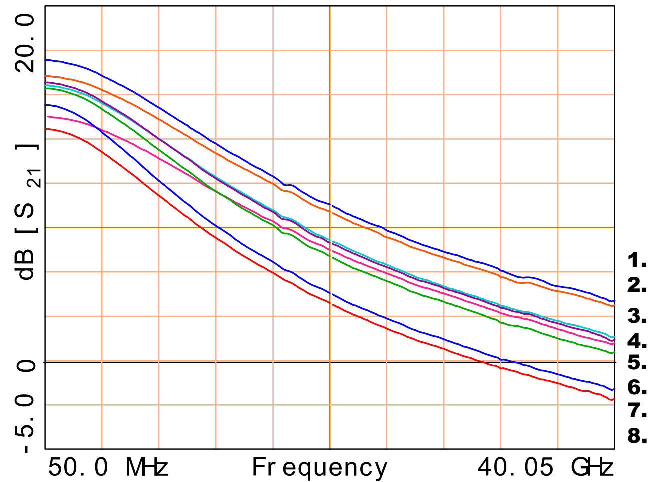
Transistors with varying gate length and fixed gate width show a clear effect on both the amplification and the cut-off frequency: smaller gate length causes a higher gain and frequency, as expected from Eqs. (3.59) and (3.65), respectively. This is seen in Figs. 3.47 (gate recess etching is done in citric acid solution for 30 s) and 3.48 (gate recess etching done in citric acid solution for 45 s), where dB $|S_{21}|$ is plotted for transistors with a fixed gate width. For the T-type transistors f_t is slightly higher than for U-types. However, for samples presented later, U-types achieve higher cut-off frequencies. This is also expected due to the U-design layout without the curved metal contact to the gate, see Fig. 3.7 (a). In the graphs $|S_{21}|$ at a low frequency of 250 MHz as well as the maximum transconductance measured at DC conditions are indicated. The maximum DC transconductance for gate lengths of 0.34, 0.35, 0.43, 0.52, 0.51, 0.61, 0.85 and 0.89 μm is 79.0, 76.5, 70.7, 67.4, 59.6, 63.5, 55.7 and 50.6 mS, respectively, Fig. 3.47 (V_{ds} = 2 V and V_{gs} at maximum g_m ranging between -0.2 - -0.5 V). The maximum DC transconductance for gate lengths of 0.26, 0.34, 0.4, 0.52 and 0.7 μm is 90.0, 61.8, 79.1, 74.2 and 67.9 mS, respectively, Fig. 3.48 (V_{ds} = 2 V and V_{gs} at maximum g_m ranging between -0.15 - -0.35 V).

In Section 3.4.4 according to Eq. (3.64) the cut-off frequency should increase proportional to l_g^{-2}. However, this is only valid for large gate lengths in the range of 5 - 10 μm and at low temperatures. Also the gain increases slightly for decreasing gate lengths. This is visible for transistors with varying gate lengths, and widths of 160 μm and 200 μm, Fig. 3.49 (transistors for which the gate recess etching is done in ammonia based solution for 5 s). For a shorter gate length (here with fixed gate width and gate-to-channel distance), the capacitance becomes smaller, which can be seen in S_{11}: It is smaller for decreasing l_g, thus having a higher imaginary part at the high frequency end. For shorter gates S_{11} also bends more inwards, which is an indication of larger gate resistance (fixed W and metal thickness). It is also interesting to notice, that the frequency does not rise very much for a wider gate. Thus, there is a slight trade-off between frequency and amplification, depending on the gate width. In addition, in the small gate length range an interesting phenomenon occurs: f_t becomes larger than f_{max}. The fact, that $f_t < f_{max}$ is attributed to parasitics: increased gate resistance, and lower g_m/g_d- and C_{gs}/C_{gd}-ratios, which lead to reduced f_{max}, see Eq. (3.83). The decreased C_{gs}/C_{gd}-ratio is in



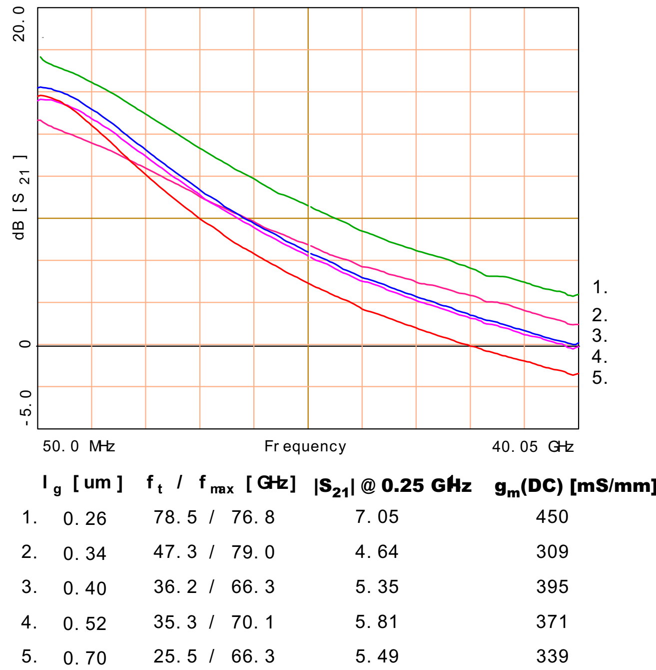
	Width	f_t / f_{max} GHz	$\lvert S_{21}\rvert$ @0.25 GHz
1.	10 um	18.0 / 49.1	0.36
2.	40 um	45.4 / 72.2	1.45
3.	80 um	58.0 / 93.8	2.69
4.	160 um	81.1 / 76.6	4.79
5.	200 um	85.9 / 66.5	6.10

Figure 3.46: S-parameters measured for e-beam transistors fabricated on pHEMT1 with varying gate widths. l_g = 0.19 μm, l_{DS} = 1.05 μm, V_{ds} = 2 V, V_{gs} = -0.52, -0.65, -0.27, -0.26, -0.18 for W = 10, 40, 80, 160, 200 μm, respectively (U-type).



	l_g [um]	f_t / f_{max} [GHz]	$\lvert S_{21}\rvert$ @ 0.25 GHz	g_m(DC) [mS/mm]
1.	0.34	51.1 / 120.0	7.04	493
2.	0.35	60.6 / 80.4	6.35	478
3.	0.43	59.0 / 61.5	5.97	442
4.	0.52	39.0 / 78.5	6.08	421
5.	0.51	41.9 / 77.5	4.88	373
6.	0.61	34.1 / 79.6	5.86	397
7.	0.85	24.4 / 68.8	5.26	348
8.	0.89	24.6 / 53.7	4.50	316

Figure 3.47: dB(S_{21}) measured for e-beam transistors fabricated on pHEMT1 with varying gate lengths, W = 160 μm, V_{ds} = 2 V. In the table below the figure is also indicated the maximum DC transconductance (both T- and U-configurations).



	l_g [um]	f_t / f_{max} [GHz]	$\|S_{21}\|$ @ 0.25 GHz	g_m(DC) [mS/mm]
1.	0.26	78.5 / 76.8	7.05	450
2.	0.34	47.3 / 79.0	4.64	309
3.	0.40	36.2 / 66.3	5.35	395
4.	0.52	35.3 / 70.1	5.81	371
5.	0.70	25.5 / 66.3	5.49	339

Figure 3.48: dB(S_{21}) measured for T-type e-beam transistors fabricated on pHEMT1 with varying gate lengths, W = 200 μm, V_{ds} = 2 V. In the table below the figure is also indicated the maximum DC transconductance.

turn an indication of gate alignment closer to the drain (see Section 3.5.2), which is possible due to manual alignment done for e-beam written gates.

The amplification S_{21} is plotted for e-beam transistors with varying gate lengths and fixed gate width of 80 μm in Fig. 3.50 (gate recess etching is done in citric acid solution for 30 s). The graph confirms that transistors with narrower gate lengths give a higher transmission from port 1 to 2 compared to those of larger gate lengths.

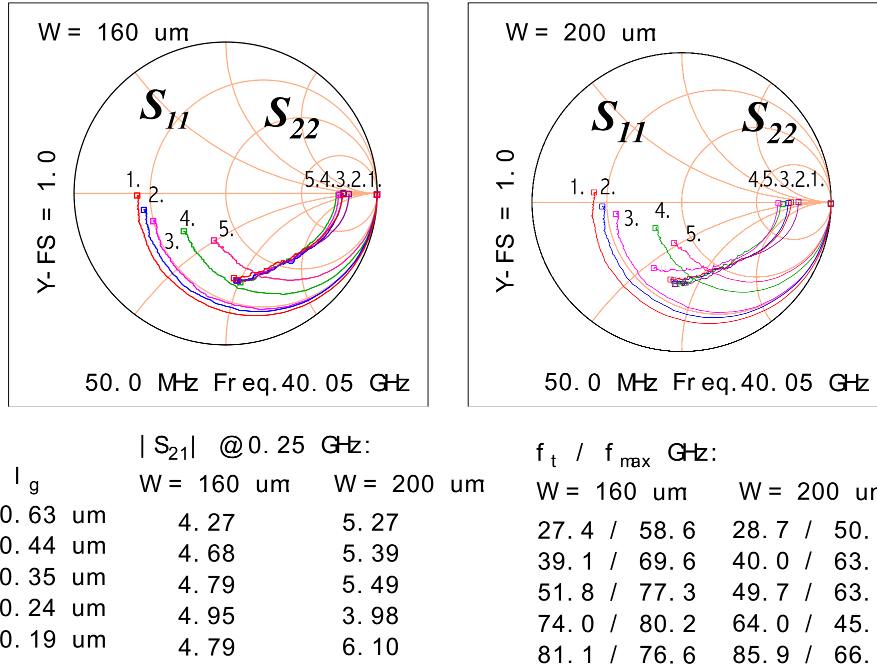
Varying gate widths and lengths

The dependence of the cut-off frequency and maximum frequency of oscillation on the gate length with varying gate widths is depicted in Fig. 3.51 (three different transistor samples). As the S-parameter plots already confirmed, smaller l_g leads to higher frequencies. Increasing the gate width also gives a better frequency performance, however, this dependence is less pronounced for gates with larger widths of 80, 160 and 200 μm. For these widths f_t is almost in the same range, or even higher for a 160 μm wide transistor compared to a transistor with a width of 200 μm. Note also that f_{max} is not necessarily highest for the widest gate. The fact that the gate-width dependence shows a tendency to saturate means that the parasitic capacitances and C_{dg} are dominant in this region.

The amplification of transistors is at its maximum when the gate width is largest (W = 200 μm). The dependence on the gate length is a bit less, but slight increase in S_{21} is achieved for smaller gate lengths, Fig. 3.52 ($|S_{21}|$ plotted at a frequency of 0.25 GHz).

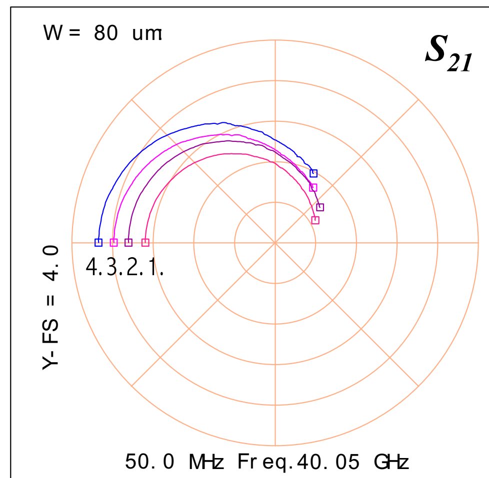
Measurements for mushroom shaped transistors

Mushroom-gate transistors are investigated in Figs. 3.53 and 3.54, fabricated with 2-layer resist system (the gate recess etching is done in ammonia based solution for 5 s). The footprint and top part dimensions vary between 100 - 300 nm, and 400 - 600 nm, respectively. Taking this into consideration conclusions about the gate-width dependence can not be drawn. The graphs, therefore, only give an overview of f_t and f_{max} for the measured T-gate shaped transistors. The high maximum frequency of



	l_g	$\|S_{21}\|$ @0.25 GHz: W = 160 um	$\|S_{21}\|$ @0.25 GHz: W = 200 um	f_t / f_{max} GHz: W = 160 um	f_t / f_{max} GHz: W = 200 um
1.	0.63 um	4.27	5.27	27.4 / 58.6	28.7 / 50.5
2.	0.44 um	4.68	5.39	39.1 / 69.6	40.0 / 63.3
3.	0.35 um	4.79	5.49	51.8 / 77.3	49.7 / 63.4
4.	0.24 um	4.95	3.98	74.0 / 80.2	64.0 / 45.0
5.	0.19 um	4.79	6.10	81.1 / 76.6	85.9 / 66.5

Figure 3.49: S-parameters measured for e-beam transistors fabricated on pHEMT1 with varying gate lengths. W = 160 μm and W = 200 μm. V_{ds} = 2 V (U-type). S_{11} and S_{22} are plotted in the graphs; below the figures are also indicated $|S_{21}|$-values at a frequency of 250 MHz.



	l_g	$\|S_{21}\|$ @0.25 GHz	f_t / f_{max} GHz
1.	0.85 um	2.56	24.0 / 74.0
2.	0.61 um	2.89	32.7 / 99.8
3.	0.43 um	3.18	49.2 / 98.2
4.	0.35 um	3.48	58.5 / 127.0

Figure 3.50: S_{21} measured for e-beam transistors fabricated on pHEMT1 with varying gate lengths. W = 80 μm, V_{ds} = 2 V, V_{gs} = -0.12, -0.11, -0.27, -0.21 for l_g = 0.85, 0.61, 0.43, 0.35 μm, respectively (U-type).

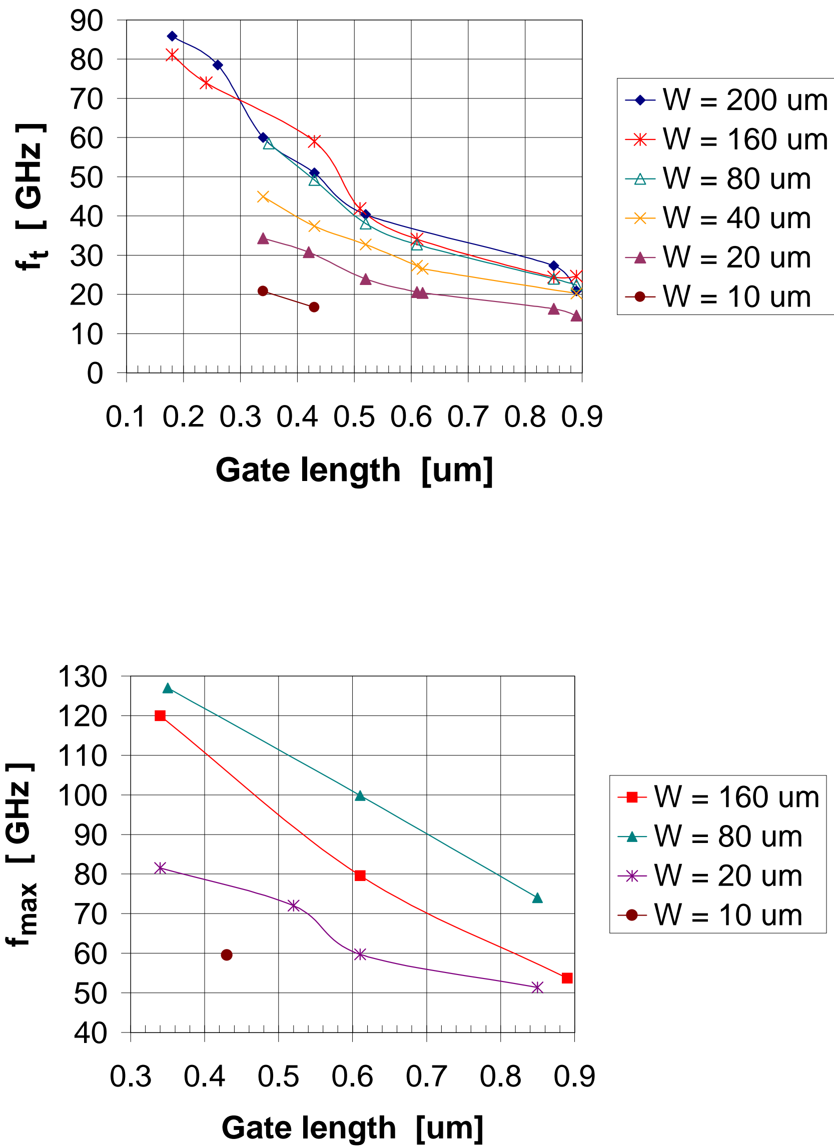


Figure 3.51: f_t and f_{max} as a function of l_g for different gate widths measured for e-beam transistors fabricated on pHEMT1. V_{ds} = 2 V, V_{gs} varying in the range -0.1 - -0.4 V.

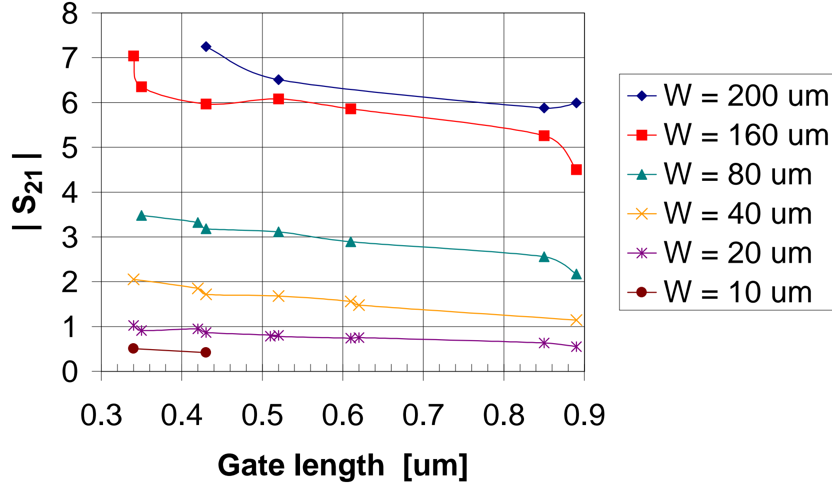


Figure 3.52: $|S_{21}|$ at 0.25 GHz as a function of l_g for different gate widths measured for e-beam transistors fabricated on pHEMT1. V_{ds} = 2 V, V_{gs} varying in the range -0.1 - -0.4 V.

oscillation (e.g. f_{max} = 187 GHz for a 200 μm wide transistor) results most probably from small gate resistance, output conductance (high g_m/g_d-ratio) and gate-drain capacitance (high C_{gs}/C_{gd}-ratio), which in turn is due to gate alignment closer to the source, see Section 3.5.2 and Eq. (3.83).

Open loop gain A_v

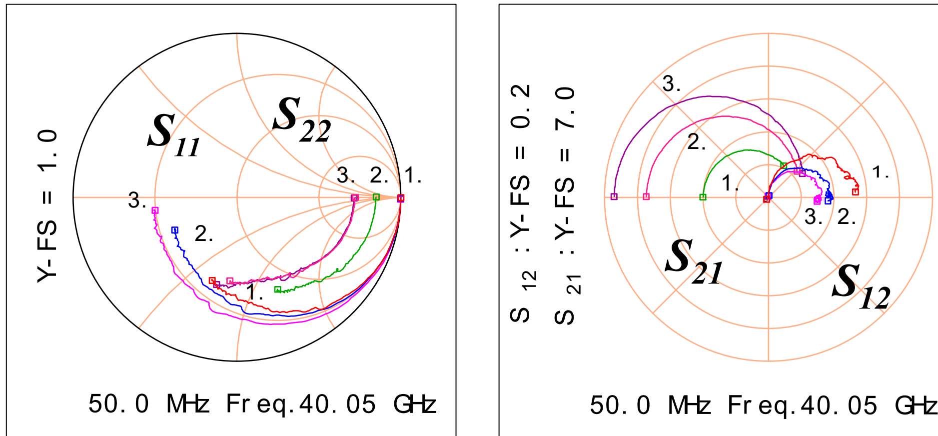
The small-signal voltage gain of a single stage $A_v(w)$, given by Eq. (3.72) ($A_v(w) = \frac{1}{|h_{12}|}$), is plotted in Figs. 3.55 and 3.56 for a submicron transistor. At higher frequencies, especially in the microwave region, an open circuit presents a problem since in practice i_1 can not be zero (i.e. there always exists a small current to the source), and thus parasitic capacitive coupling appears. Note also the remarks made in Section 3.5.1 on p. 91 about the high-frequency validity of A_v. The graphs show, that highest gain is achieved at V_{gs} = 0.5 V, and at a low frequency of 1.05 GHz. In addition, A_v exhibits a small dependence on the frequency.

Fittings using the small-signal equivalent circuit

The S-parameters were measured for an e-beam transistor with triangular shape (l_g = 0.34 μm, W = 160 μm, T-type) in the frequency range: 50 MHz - 40.05 GHz, and at several different biasing conditions. V_{ds} was kept at 2 V, and V_{gs} varied. Fitting of the small-signal parameters is performed with the FET equivalent circuit model (Fig. 3.6).

The measured and simulated S-parameters at the bias point of maximum g_m (V_{ds} = 2 V, V_{gs} = -0.268 V) are presented in Fig. 3.57. In Table 3.7 are recorded the exact results of the bias-dependent intrinsic parameters C_{gs}, g_m and g_d at different V_{gs} voltages. Table 3.7 also indicates the measured DC values for C_{gs}, $g_m = \frac{\partial I_{ds}}{\partial V_{gs}}$ and $g_o = \frac{\partial I_{ds}}{\partial V_{ds}}$. The DC measurement for C_{gs} is explained in detail below.

In order to confirm the validity of the C_{gs} values obtained from the S-parameter fittings described above, DC-measurements were performed on the same devices. The capacitance at the input was measured at a frequency of 2 MHz, by placing a CPW probe on the gate and source contacts. The bias-independent extrinsic input capacitance C_{in} was measured for an 'empty' structure, i.e. a transistor without the gate-line. Value obtained C_{in} = 15.5 fF was then subtracted from the input capacitance



	Width	f_t / f_{max} GHz	$\|S_{21}\|$ @0.25 GHz
1.	80 um	59.0 / 111	2.79
2.	160 um	72.9 / 81.2	5.21
3.	200 um	75.1 / 92.7	6.59

Figure 3.53: S-parameters measured for mushroom gate transistors fabricated on pHEMT1 with varying gate widths, l_g(top) = 400 nm, V_{ds} = 2 V, $V_{gs} = -0.53, -0.54, -0.32$ V for W = 80, 160, 200 μm, respectively (T-type).

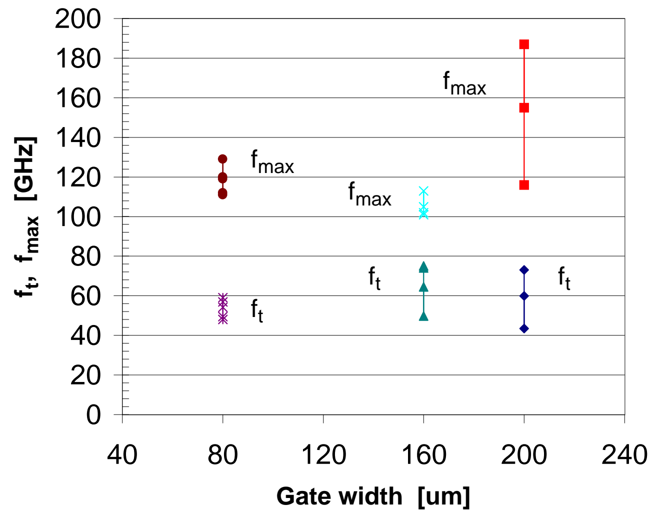


Figure 3.54: f_t and f_{max} measured for mushroom transistors fabricated on pHEMT1 with varying gate widths, V_{ds} = 2 V. The footprint varies between 100 - 300 nm and the top part range is 400 - 600 nm. (both T- and U-types)

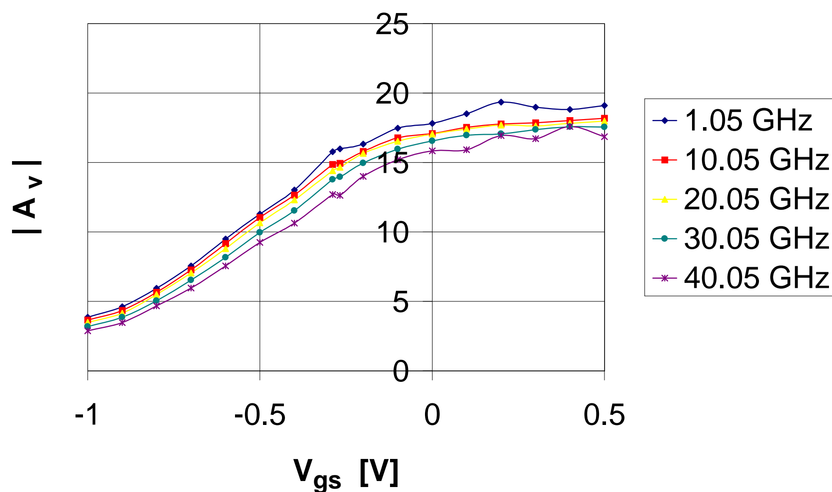


Figure 3.55: Open loop voltage gain A_v as a function of V_{gs} at different frequencies for a submicron pHEMT1 (l_g = 0.34 μm, W = 160 μm, V_{ds} = 2 V). At the optimum operating point of V_{gs} = -0.3 V and V_{ds} = 2 V: f_t = 51.1 GHz, f_{max} = 120 GHz, $|S_{21}|$ = 7.04 @ 0.25 GHz and g_m(DC) = 79.3 mS (495.6 mS/mm).

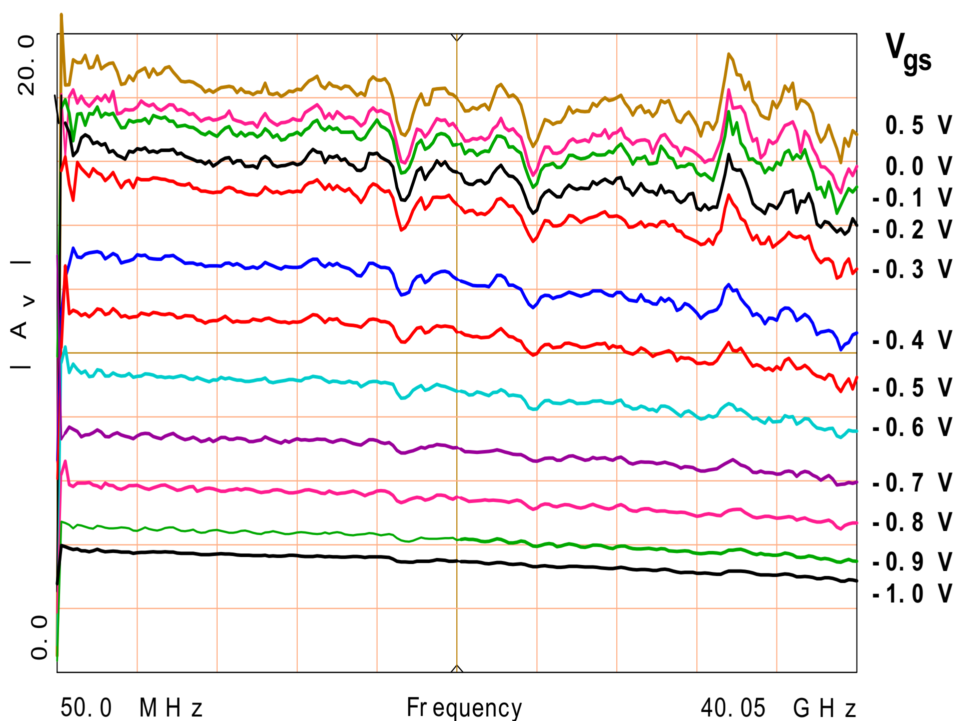


Figure 3.56: Open loop voltage gain A_v as a function of frequency at different values of V_{gs} for a submicron pHEMT1 (l_g = 0.34 μm, W = 160 μm, V_{ds} = 2 V).

measured for a complete transistor, (i.e. a structure with the same dimensions than the 'empty' one: same gate width, l_{DS}, and T-type), in order to get an estimate for C_{gs}. Other parameters such as R_i, R_g, R_s, L_g, L_s can be omitted, since their impedance is very low compared to those of C_{gs} and C_{in} at low frequencies. Figure 3.58 shows the measured and fitted capacitance and transconductance curves as a function of V_{gs}. Figure 3.59 plots the measured g_o and fitted g_d.

It can be noticed that C_{gs} rises with increasing voltage (normal capacitance characteristics), and the measured value is larger than that obtained from the simulation. Comparison of measured and fitted transconductance values gives good agreement, especially at the bias point of operation. g_m reaches its maximum 80.8 mS (fitting) / 79.3 mS (measurement) at V_{gs} = -0.3 V and V_{ds} = 2 V. The differences in simulation and measurement of g_m values is due to the measurement conditions and the setup. The DC measurement is done in a fast voltage sweep mode. In addition, and of more significance is the fact, that the fitting of the equivalent circuit parameters was done in a wide frequency range, from 50 MHz to 40.05 GHz, whereas the measured C_{gs} and g_m values were results of DC measurement.

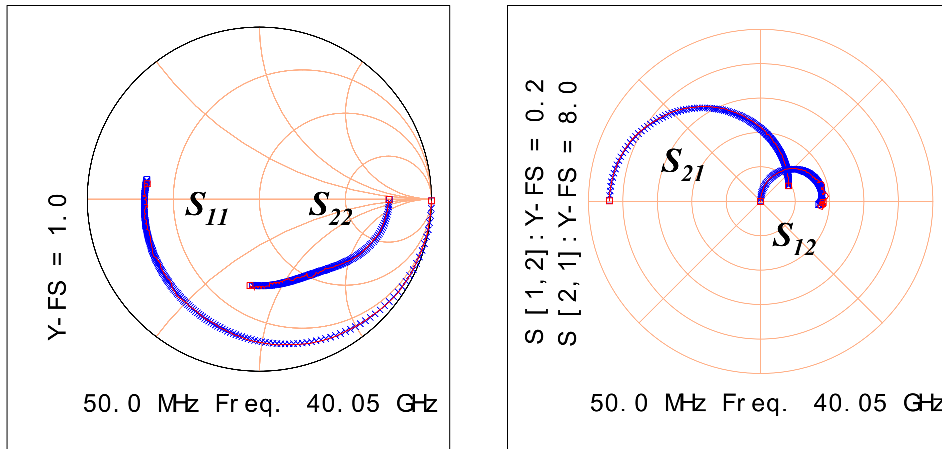


Figure 3.57: Measured (solid line) and fitted (crosses) S-parameters for a submicron pHEMT1 transistor ($l_g = 0.34$ μm, $W = 160$ μm, $V_{ds} = 2$ V, V_{gs} = -0.268 V). Fitting based on the equivalent circuit in Fig. 3.6.

Table 3.7: Fitted (RF) and measured (DC) parameters for pHEMT1, see equivalent circuit in Fig. 3.6. Figs. 3.57, 3.58 and 3.59 present the fittings.

V_{gs} [V]	C_{gs} [fF] sim.	g_m [mS]/[mS/mm] sim.	g_d [Ω] sim.	C_{gs} [fF] meas.	g_m [mS]/[mS/mm] meas.	g_o [Ω] meas.
-1	78.3	1.4 / 8.8	13712.0	142.5	0.38 / 2.4	
-0.9	108.5	10.5 / 65.6	1739.7	199.5	10.0 / 62.7	
-0.5	222.5	76.7 / 479.4	311.8	242.5	74.9 / 468.1	392.2
-0.3	242.2	80.8 / 505.0	353.3	260.1	79.3 / 495.6	487.8
0.0	219.2	75.7 / 473.1	408.7	275.2	72.4 / 452.5	425.5
0.2	249.7	71.7 / 448.1	429.9	285.7	61.3 / 383.1	451.1
0.5	257.6	64.4 / 402.5	332.7	311.5	42.6 / 266.3	408.2

The S-parameters were measured for a submicron transistor ($l_g = 0.34$ μm) at several different gate-source voltages. Figure 3.60 plots f_t and f_{max} as a function of V_{gs}. Fitting was done at certain bias voltages using the equivalent circuit in Fig. 3.6. The cut-off frequency was then calculated according to Eq. (3.64) (i.e. $f_t = g_m/2\pi C_{gs}$) using the fitted values for g_m and C_{gs}, which are indicated in Table 3.7. The cut-off frequencies obtained from the fitting agree quite well with the measured ones, confirming

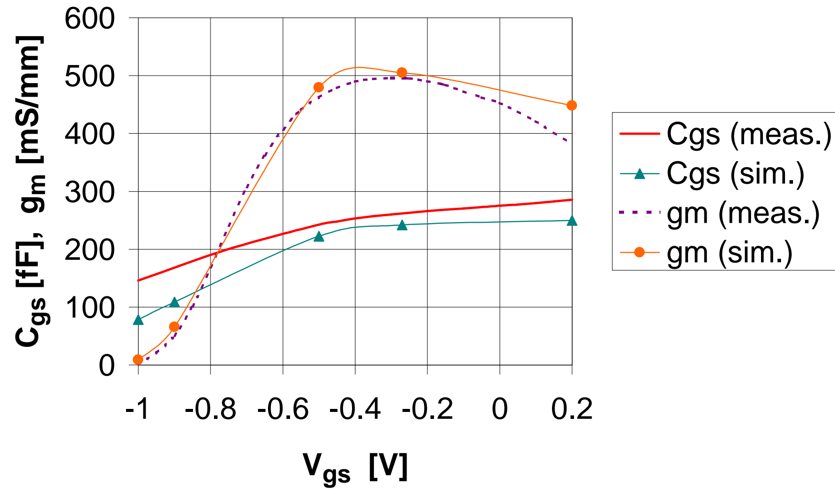


Figure 3.58: Measured (DC) and fitted (RF) C_{gs} and g_m as a function of V_{gs} for a submicron pHEMT1 (l_g = 0.34 μm, W = 160 μm, V_{ds} = 2 V).

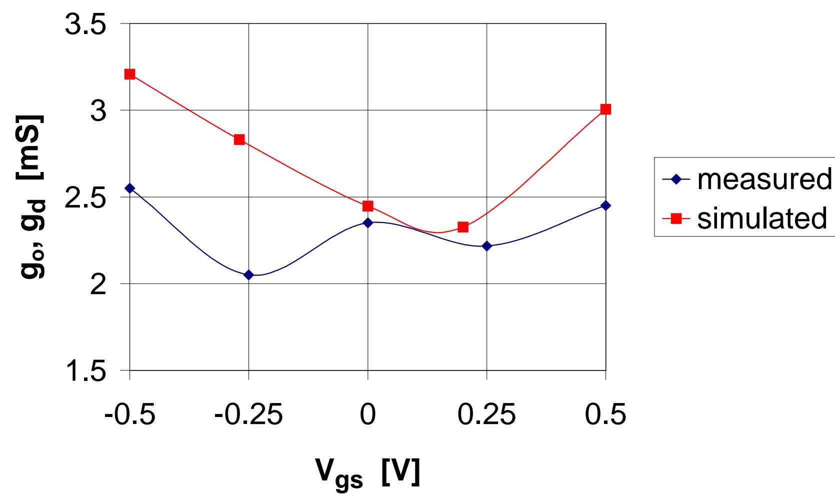


Figure 3.59: Measured (DC) g_o and fitted g_d (RF) as a function of V_{gs} for a submicron pHEMT1 (l_g = 0.34 μm, W = 160 μm, V_{ds} = 2 V).

the validity of the simple FET equivalent circuit, and the simple equation for estimating the cut-off frequency. Figure 3.61 shows $|S_{21}(V_{gs})|$ at various frequencies, both measurement and fitting (only specific points), which is done according to the equivalent circuit shown in Fig. 3.6. The fitting is very good over a wide frequency range, and at different bias conditions. In the fitting the emphasis is set to C_{gs}, g_m and g_d, which are the most important parameters of the intrinsic device.

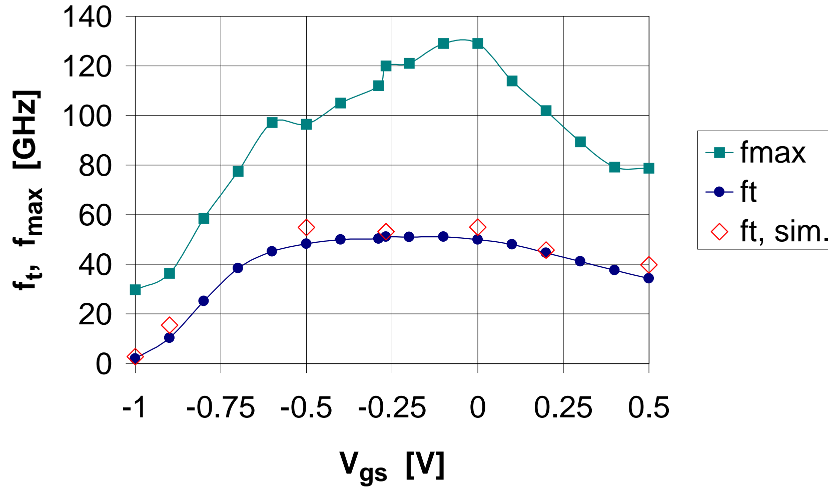


Figure 3.60: f_t and f_{max} as a function of V_{gs} for a submicron pHEMT1 (l_g = 0.34 μm, W = 160 μm, V_{ds} = 2 V). At V_{gs} = -0.1 V: f_t = 51.1 GHz and f_{max} = 129 GHz. Diamonds indicate the fitting result: $f_t = \frac{g_m}{2\pi C_{gs}}$.

Fittings using the EEHEMT1-model

The S-parameters were measured and fitted for a standard and e-beam transistor with gate width of 80 μm (Figs. 3.62 and 3.63, respectively). The fitting was done using the EEHEMT1-model with extracted parameters listed in Appendix D in Figs. D.1 and D.2 (simulation circuit is shown in Fig. 3.44). Since the IC-CAP extracted parameters only apply to the intrinsic device, parasitic inductances had to be incorporated to each terminal. For the standard transistor L_g = 40 pH, L_s = 5.5 pH, and L_d = 5 pH, whereas for the submicron transistor values of L_g = 77 pH, L_s = 5.5 pH, and L_d = 5 pH were used. The agreement between measurement and simulation is satisfactory, taking into account that the EEHEMT1-model parameters were extracted at several different bias conditions, and did not necessarily show perfect fitting at the bias voltages used in the measurements. In addition, the extracted model-parameters were achieved in the frequency range from 50 MHz to 20.05 GHz, and now the measurement/simulation was extended up to 40.05 GHz.

Summary of results

Table 3.8 indicates DC results for standard as well as e-beam-fabricated transistors. The threshold voltage V_{th} is obtained from the gate voltage intercept of a linear extrapolation of the drain current versus gate voltage curve to zero current [137]. For the mushroom-gate transistors the threshold voltage shifts towards larger negative voltages. For triangular shaped transistors the maximum transconductance was typically reached at V_{gs}-values around -0.1 - -0.3 V. Mushroom-transistors, however, needed a V_{gs} as low as -0.5 - -1.2 V for the peak g_m, which is a sign of short-channel effects (see Section 3.4.5).

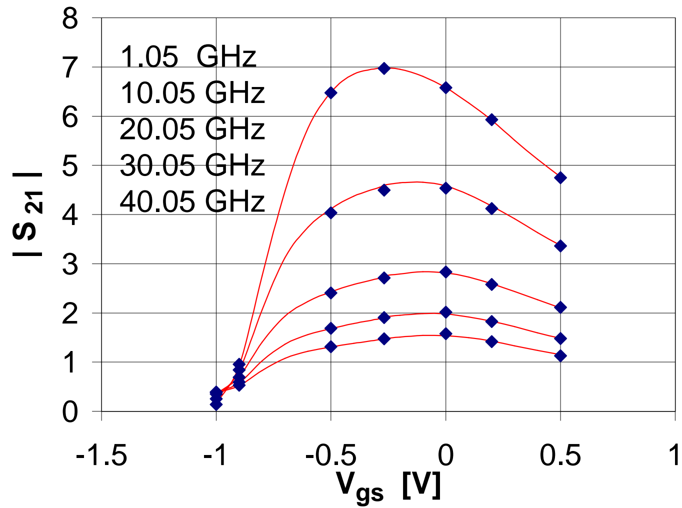


Figure 3.61: $|S_{21}|$ as a function of V_{gs} at different frequencies for a submicron pHEMT1. Measured (solid), fitting at discrete voltage points (diamonds). (l_g = 0.34 μm, W = 160 μm, V_{ds} = 2 V). At the optimum operating point of V_{gs} = -0.3 V and V_{ds} = 2 V $|S_{21}|$ = 7.04 @ 0.25 GHz.

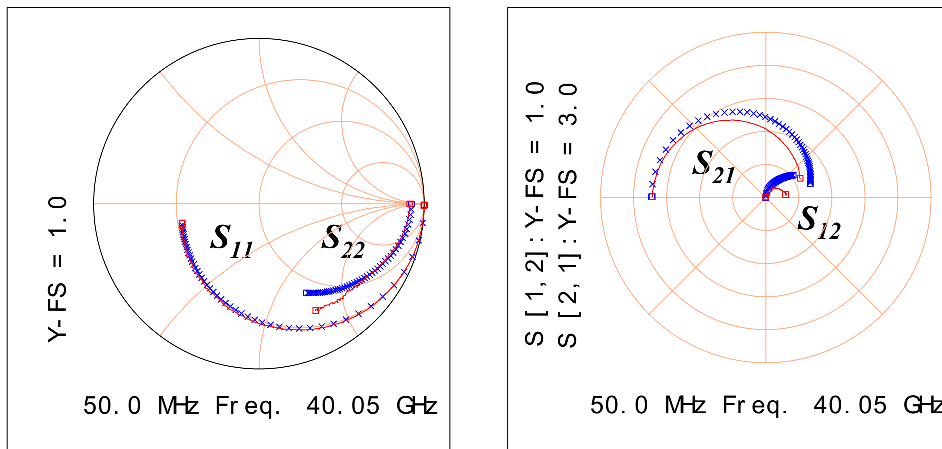


Figure 3.62: Measured (solid line) and simulated (crosses) S-parameters for a standard transistor. Simulation done with parameters extracted from IC-CAP (see EEHEMT1-model parameters in Fig. D.1). l_g = 1 μm, W = 80 μm. f_t = 18.8 GHz, f_{max} = 48 GHz at V_{ds} = 2 V, V_{gs} = -0.12 V and I_{ds} = 12.5 mA.

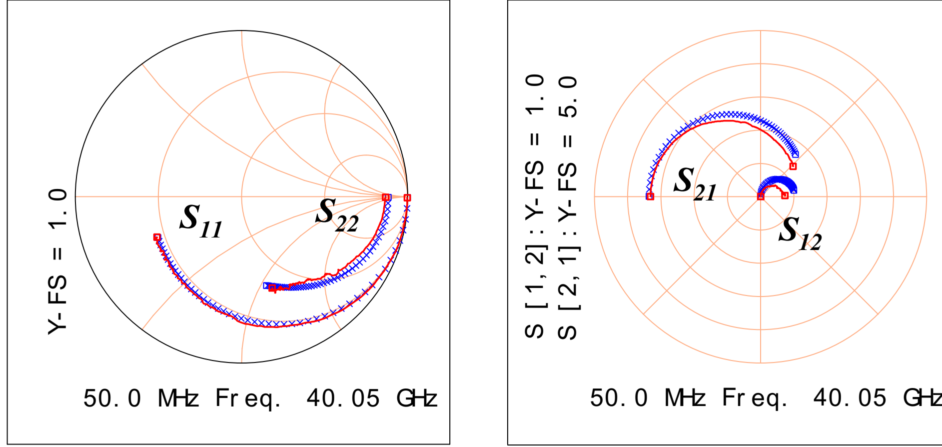


Figure 3.63: Measured (solid line) and simulated (crosses) S-parameters for a submicron transistor. Simulation done with parameters extracted from IC-CAP (see EEHEMT1-model parameters in Fig. D.2). l_g = 0.42 μm, W = 80 μm. f_t = 45.1 GHz, f_{max} = 103 GHz, $|S_{21}|$ = 3.32 (10.4 dB) at V_{ds} = 2 V, V_{gs} = -0.184 V and I_{ds} = 16.73 mA. g_m(DC) = 36.2 mS (452.5 mS/mm) at V_{ds} = 2 V, V_{gs} = -0.2 V.

Since the threshold voltage shift for the mushroom gate transistors, defined in Eq. (3.33), is less than the shift observed here, some other effects need to be involved. The AlGaAs Schottky layer is undoped, thus only a small parallel conduction is possible. Therefore, another explanation is the increased substrate current, especially for gate lengths below 0.5 μm, fatally affecting the V_{th} shift [113]. Many measured mushroom devices also showed only a small gate influence, small S_{11} angle rotation, S_{21} was much too low, and/or multiple peaks appeared. In addition, for small gate widths the power gain, defined in Eq. (3.69) started to became much noisier. Possible explanation is too a shallow gate recess etch depth, which is attributed to the used etching time. It is possible that the dose for the narrow footprint was too low, thus not opening the total resist stack. In addition, the oxygen plasma treatment for clearing the remaining resist traces (prior to etching), and/or the wetting performed prior to actual etching might have been unsuccessful. Thus, the time for the etching should have been increased, (e.g. double time compared to times used for larger footprint-devices). The etching time should not, on the other hand, be too high, in order to prevent lateral underetch at the etch-stop (AlAs)/Schottky layer interface.

Table 3.8: DC comparison of different transistors. All transistors are fabricated on pHEMT1. standard = optically fabricated gates. eb = e-beam written gates. triang. = triangular shape. mushr. = mushroom shape, fabricated with 2-layer resist system.

Device	l_g/l_{DS} [μm]	W [μm]	I_g [10^{-8} A]	I_{dsat} [mA/mm]	V_{ds} [V]	V_{gs} [V]	$g_{m,max}$ [mS/mm]	g_o [mS/mm]	A_o [ ]	V_{th} [V]
eb/triang.	0.34/1	40	-2.27	216.9	2	-0.25	539.1	19.3	27.9	-0.8
eb/triang.	0.52/2.2	200	-1.95	173.2	2	-0.25	370.8	7.0	53.0	-0.85
eb/triang.	0.85/3	160	-2.16	151.9	2	-0.25	348.1	5.7	60.8	-0.8
eb/mushr.	foot 0.15/1	200	-2.59	216.4	2	-0.50	415.0	17.8	23.4	-1.1
standard	1.1/3.8	200	-3.68	193.1	2	-0.25	293.5	7.6	38.5	-0.9
standard	1.1/3.8	200	-0.78	224.7	2	0.00	302.5	6.4	47.5	-0.9
standard	1.1/3.8	80	-0.93	172.4	2	0.0	313.1	3.4	91.1	-0.7

Table 3.9 summarizes transistor results gathered from literature.

Table 3.9: Comparison of different transistors from literature.

Device	l_g/l_{DS} [μm]	W [μm]	$g_{m,max,DC}$ [mS/mm]	f_t [GHz]	f_{max} [GHz]	ref.
GaAs pHEMT	0.25/1.35	200	395	75	190	[88]
GaAs pHEMT	0.2/		130	70	150	[138]
GaAs pHEMT	0.2/		408	23		[139]
InP pHEMT	0.5/3	100	520	70	90	[140]
GaAs pHEMT	0.2/1.0	160	496	75	102	this work

In Table 3.10 are collected all the high performance standard and e-beam fabricated transistors. The results for standard pHEMT1, pHEMT2 and pHEMT3-transistors were expected to be in the same range, since the active transistor layers are the same for these structures and the difference is only in the layers underneath the active layers (see Section 4.1 for precise description of the different transistor structures). However, for pHEMT3-transistors a V_{ds} of 4.0 V was needed instead of the usual 2 V, and the measured gain was higher for pHEMT3 compared to that of pHEMT1 and pHEMT2, but at the expense of lower frequency characteristics. The most probable explanation is parallel conduction in the buffer and/or substrate. Also, pHEMT3-transistors had a positive gate bias for maximum S_{21} instead of being negative as was the case for all other measured transistors.

Table 3.10: RF comparison of different transistors. pH2 and pH3 refer to pHEMT2 and pHEMT3, respectively. All other transistors are fabricated on pHEMT1. standard = optically fabricated gates. eb = e-beam written gates. triang. = triangular shape. mushr. = mushroom shape. 2lr/3lr = 2-layer resist/3-layer resist.

Device	l_g [μm]	l_{DS} [μm]	W [μm]	V_{ds} [V]	V_{gs} [V]	I_{ds} [mA]	f_t [GHz]	f_{max} [GHz]	$\lvert S_{21} \rvert$ @ 0.25 GHz
standard	1.1	3.8	200	2.0	-0.16	29.8	24.1	46.9	4.45
standard	1.1	3.8	200	2.0	-0.39	23.5	25.3	43.7	4.71
standard	1.1	3.8	200	2.0	-0.19	37.8	28.1	51.5	4.91
standard	1.1	3.8	200	2.0	-0.22	36.2	27.7	59.9	5.06
standard	1.1	3.8	200	2.0	-0.23	47.0	27.7	61.3	4.47
standard	1.1	3.8	200	2.0	-0.36	42.8	38.4	74.0	4.40
standard	1.1	3.8	200	2.0	-0.41	49.4	32.9	56.6	3.98
standard	1.1	3.8	200	2.0	-0.45	51.6	33.1	59.4	2.88
standard	1.1	3.8	200	2.0	-0.55	14.8	36.0	50.1	4.29
standard	1.1	3.8	200	2.0	-0.35	45.9	28.5	52.2	3.11
standard, pH2	1.1	3.8	200	2.0	-0.46	30.1	31.3	60.7	5.29
standard, pH2	1.1	3.8	200	2.0	-0.48	21.5	23.4	47.2	4.80
standard, pH3	1.1	3.8	200	4.0	+0.22	30.5	19.2	60.1	6.08
standard, pH3	1.1	3.8	160	4.0	+0.26	23.7	17.4	60.6	5.15
eb / triang.	0.19	1.0	80	2.0	-0.27	20.5	58.0	93.8	2.69
eb / triang.	0.19	1.0	160	2.0	-0.26	52.2	81.1	76.6	4.79
eb / triang.	0.19	1.0	200	2.0	-0.18	64.3	85.9	66.5	6.10
eb / triang.	0.26	1.0	200	2.0	-0.32	38.8	78.5	76.8	7.05
eb / triang.	0.28	1.9	80	2.0	-0.20	11.8	41.6	106.0	2.69
eb / triang.	0.28	1.9	200	2.0	-0.11	35.7	48.3	103.0	6.25
eb / triang.	0.34	1.0	160	2.0	-0.27	38.8	51.1	120.0	7.04
eb / triang.	0.34	1.0	200	2.0	-0.38	64.6	60.0	77.7	5.60
eb / triang.	0.34	1.4	200	2.0	-0.20	57.2	47.3	79.0	4.64
eb / triang.	0.35	1.0	80	2.0	-0.21	15.3	58.5	127.0	3.48
eb / triang.	0.35	1.0	160	2.0	-0.20	30.8	60.6	80.4	6.35
eb / triang.	0.39	2.2	80	2.0	-0.20	12.3	35.8	110.0	2.88
eb / mushr. 2lr	top 0.4	1.4	200	2.0	-0.71	75.1	73.1	116.0	3.47
eb / mushr. 2lr	top 0.4	1.0	200	2.0	-0.32	56.8	75.1	92.7	6.59
eb / mushr. 2lr	top 0.4	1.4	160	2.0	-0.70	44.4	74.1	101.0	3.74
eb / mushr. 2lr	top 0.4	1.0	160	2.0	-0.91	24.7	75.0	102.0	4.46
eb / mushr. 2lr	top 0.4	1.0	80	2.0	-0.69	17.1	56.9	120.0	2.22
eb / mushr. 2lr	top 0.4	1.0	80	2.0	-0.53	20.3	59.0	111.0	2.79
eb / mushr. 2lr	top 0.6	2.2	200	2.0	-0.05	51.2	59.9	155.0	5.83
eb / mushr. 2lr	top 0.6	2.2	200	4.0	-0.03	63.5	43.4	187.0	5.23
eb / mushr. 2lr	top 0.6	2.2	160	2.0	-0.12	35.8	64.5	105.0	4.76
eb / mushr. 2lr	top 0.6	1.9	160	2.0	-0.44	29.4	49.7	113.0	5.60
eb / mushr. 2lr	top 0.6	1.9	80	2.0	-0.34	12.8	48.0	129.0	3.04
eb / mushr. 3lr	top 0.4	1.0	160	2.0	-1.05	57.0	70.5	99.0	3.87
eb / mushr. 3lr	top 0.4	1.0	200	2.0	-0.92	57.6	68.9	105.0	5.12
eb / mushr. 3lr	top 0.6	3.0	200	2.0	-0.79	41.8	50.1	116.0	4.65
eb / mushr. 3lr	top 0.6	3.0	160	2.0	-0.83	35.5	49.1	118.0	3.87

Chapter 4

Integrated Photoreceiver

4.1 Device Structures

Three different layer structures for the integrated photoreceivers are studied. The pHEMT layers (i.e. the top layers) are the same for all of the three different receivers. However, the difference lies in the thickness of the GaAs buffer layer underneath the second AlAs etch stop layer (i.e. the photoactive MSM PD layer), and the underlying superlattice (SL)-layers grown on the S.I. GaAs substrate. Figure 4.1, and Tables A.1 and A.2 in Appendix A show the different layer structures.

Layer	Thickness
n^+ GaAs cap (2×10^{18} cm^{-3})	20 nm
AlAs etch-stop (2.5×10^{18} cm^{-3})	3 nm
i $Al_{0.23}Ga_{0.77}As$ Schottky	30 nm
Si planar doping (5×10^{12} cm^{-2})	
i $Al_{0.23}Ga_{0.77}As$ spacer	3 nm
i $In_{0.20}Ga_{0.80}As$ channel	12 nm
i GaAs buffer	50 nm
i AlAs etch-stop	3 nm
i GaAs buffer	500 or 1000 nm
S / L buffer: $Al_{0.5}Ga_{0.5}As$ / GaAs	10 x 10 nm / 10 x 10 nm
S.I. (001) GaAs substrate	625 um

(1)

Layer	Thickness
n^+ GaAs cap (2×10^{18} cm^{-3})	20 nm
AlAs etch-stop (2.5×10^{18} cm^{-3})	3 nm
i $Al_{0.23}Ga_{0.77}As$ Schottky	30 nm
Si planar doping (5×10^{12} cm^{-2})	
i $Al_{0.23}Ga_{0.77}As$ spacer	3 nm
i $In_{0.20}Ga_{0.80}As$ channel	12 nm
i GaAs buffer	50 nm
i AlAs etch-stop	3 nm
i GaAs buffer	500 nm
S / L buffer: GaAs / AlAs	6 x 57.7 nm / 6 x 70.2 nm
S.I. (001) GaAs substrate	625 um

(2)

Figure 4.1: Cross sections of 3 different types of pHEMT structures. (1) pHEMT1 and pHEMT2 with GaAs buffer layer thicknesses of 500 nm and 1000 nm, respectively and an AlGaAs/GaAs SL (2) pHEMT3 with a GaAs buffer layer thickness of 500 nm, and an AlAs/GaAs DBR SL.

The different Single Delta Doped pHEMT receivers studied in this work are:

- pHEMT1: 500 nm undoped GaAs buffer & SL buffer
- pHEMT2: 1000 nm undoped GaAs buffer & SL buffer
- pHEMT3: 500 nm undoped GaAs buffer & DBR-type SL.

The thickness of the GaAs buffer is varied: either 0.5 μm or 1 μm. The purpose of increasing the buffer layer thickness from 0.5 μm to 1 μm is to increase the MSM detector response as compared to the noise level (see Section 2.2.2), and hence to improve the overall performance of the receiver. In pHEMT3, the motivation is to achieve high responsivity for the MSM, by using a thin buffer layer

with a thickness of 0.5 μm with the combination of a distributed Bragg reflector (DBR) SL grown underneath.
The superlattices are different as follows: pHEMT1 and pHEMT2 have a 10-period AlGaAs/GaAs SL with a total thickness of 200 nm, whereas pHEMT3 has a DBR-type AlAs/GaAs SL with 80 % reflection tuned to 800 nm with a total thickness of 767.4 nm.

4.2 Fabrication

Figure 4.2 shows the monolithic integration of the pHEMT with the MSM PD. All processing steps are the same as for the individual transistors described in Section 3.6, and Tables B.7 - B.12. The role of the second AlAs etch stop layer is now of significance, since during the gate recess etching also the MSM fingers are etched. In order to prevent a possible deep etch depth in the buffer layer, the second AlAs layer is applied. Due to the 'gate recess' of the MSM fingers, a thin layer of S.I. GaAs ($\sim$ 30 nm, exact thickness depending on the mesa etch depth) is left between the fingers, and also the thin AlAs layer. However, this trenched MSM structure only probably enhances the responsivity and speed due to the strong electrical field in these regions.

Circuits were fabricated using both optical and e-beam lithography. In both cases the mesa, ohmic as well as interconnect steps were done with optical lithography. The difference lies, however, in the gate and MSM definition:

- **Standard receivers** with optically exposed gates:
  gate length 1 μm ($l_{DS} = 4$ μm), and MSM finger spacing and width 1 - 2 μm. The total area of the detectors varying from 11 x 18 up to 101 x 108 μm^2.
- **$\mathbf{E-beam}$ receivers** with a combination of standard and submicron gates:
  submicron gate lengths varying between 0.16 - 0.6 μm with scaled l_{DS} dimensions in the same manner as for the individual transistors in Section 3.6.1, and MSM PDs with spacings and widths of 0.15 μm and 0.35 μm, respectively. The total area of the detectors is: 11 x 22, 21 x 32 and 22 x 40 μm^2.

For the e-beam circuits the transistors in the amplification stage (see mask layout in Fig. 4.3) and the MSM PD were exposed by e-beam, whereas transistors in the level shift and buffer stage were fabricated applying optical lithography. A 3-layer resist-system was used for the triangular shaped submicron transistors and the MSM PD, see resist profile in Fig. 3.20 (a). The alignment marks for the e-beam exposure were fabricated in the same step as the ohmic contacts. During e-beam writing also 2 monitor windows (50 x 50 μm^2) were exposed, one on the mesa and the other next to the mesa, in order to check the gate recess depth for both the gate and the MSM fingers, respectively.

The processing of the e-beam circuits is critical considering two subsequent gate recess etching steps: first one for standard gates and the second one for e-beam exposed gates. This naturally affects the yield of high performance circuits.

4.2.1 Mask Layout

The mask layout design for the transimpedance amplifier monolithically integrated with the MSM diode is shown in Fig. 4.3, see the corresponding electrical schematic in Fig. 4.8. The input stage provides the voltage amplification of the circuit, consisting of FETs indicated with a gate width W_a. The output signal is fed back to the input through a level-shift stage, which comprises two FETs indicated by W_{ls} and two finger Schottky diodes indicated by A. The Schottky diodes provide a voltage drop, which enables the DC-coupled feedback without disturbing the optimal biasing of the input stage. The feedback consists of a fixed resistor R_f, thus being a passive feedback. Receivers with an active feedback (i.e. a feedback transistor) were also fabricated, the benefit being in the possibility to tune the transfer function of the receiver with a feedback voltage V_f. In the output stage the FETs denoted with W_b finally match the receiver output to a 50 Ω load.

In Figure 4.4 is shown the fabricated photoreceiver, consisting of submicron MSM PD and transistors. Figure 4.5 shows the part of the receiver which contains the submicron devices written by e-beam, and Fig. 4.6 presents the side-profile of a single triangular shaped (e-beam written gate) transistor.

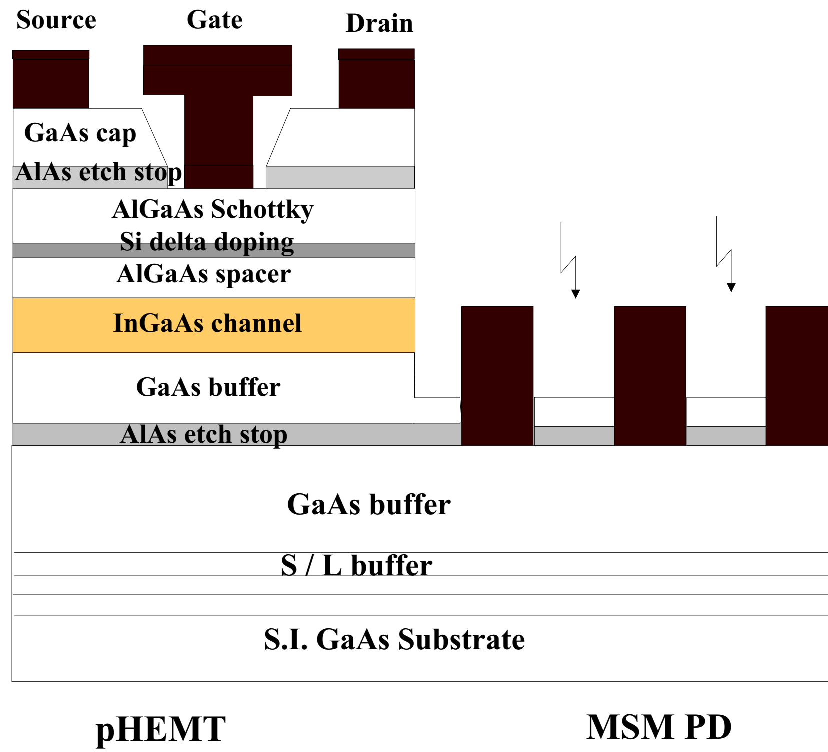


Figure 4.2: Cross section of monolithic integration of the pHEMT and the MSM PD.

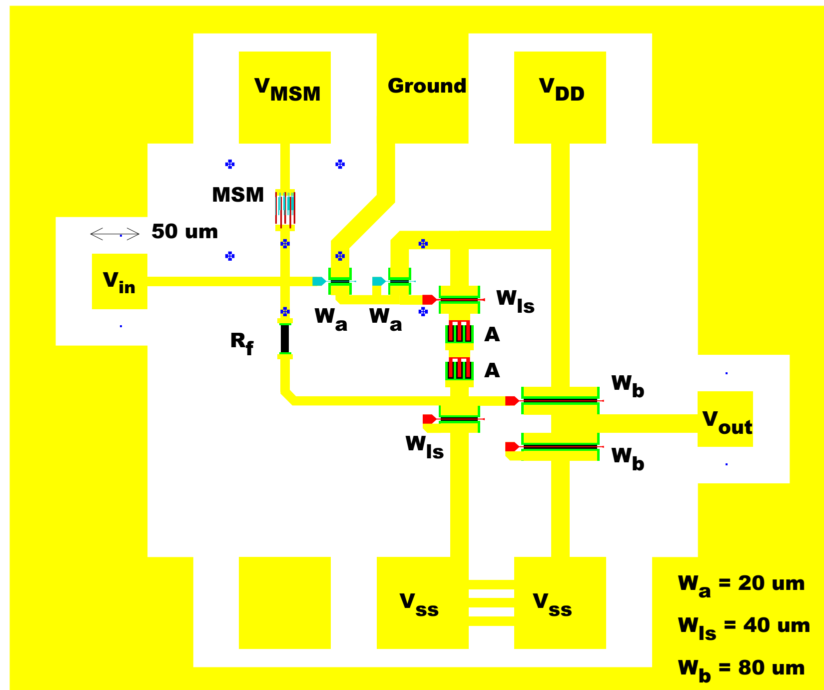


Figure 4.3: Mask layout for the integrated photoreceiver. MSM area 21 x 32 μm^2, s = 0.35 μm, w = 0.15 μm. The MSM PD and the amplifier FETs (denoted by W_a) fabricated by e-beam; the level shift FETs as well as the buffer stage FETs (denoted by W_{ls} and W_b respectively) fabricated optically. A refers to the Schottky finger diodes. The small crosses are the alignment marks for the e-beam exposure.

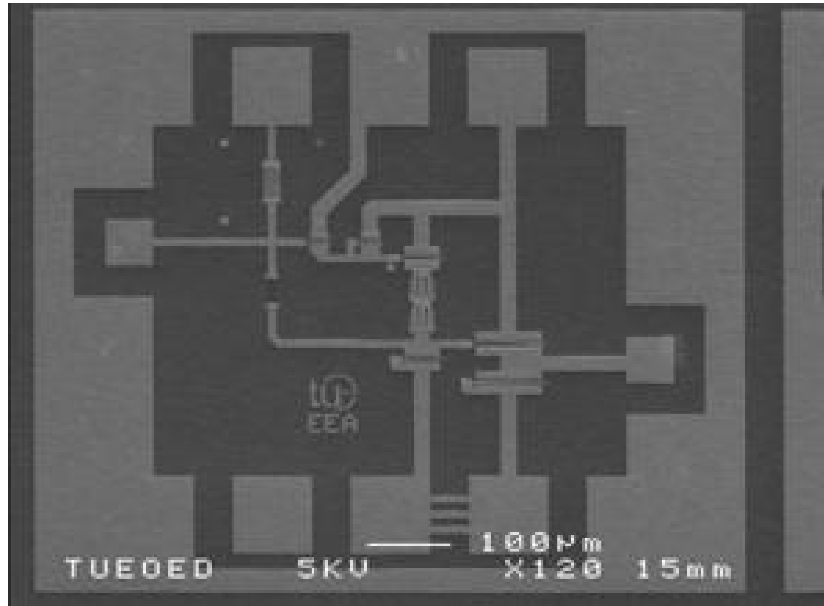


Figure 4.4: SEM photograph of the realized photoreceiver. Submicron MSM PD (w = 0.2 μm, s = 0.3 μm, A = 22 x 40 μm^2), submicron transistors for the amplification stage (l_g = 0.26 μm, l_{DS} = 1.75 μm, W = 20 μm), standard transistors for the level shift and buffer stage (l_g = 1.1 μm, l_{DS} = 3.9 μm), Ti/Au = 50/250 nm.

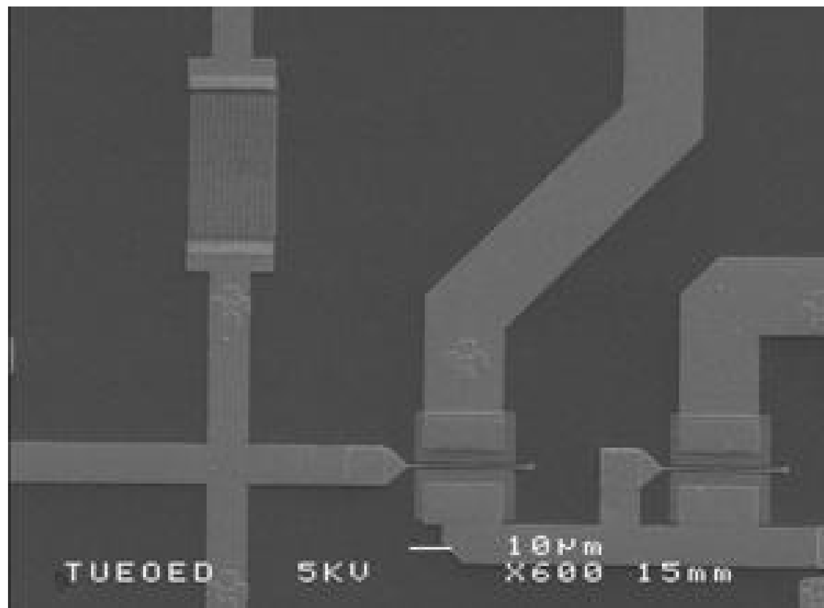


Figure 4.5: SEM photograph of the photoreceiver, showing the submicron MSM PD and amplification stage transistors fabricated by e-beam lithography. MSM PD (w = 0.2 μm, s = 0.3 μm, A = 22 x 40 μm^2), transistors (l_g = 0.26 μm, l_{DS} = 1.75 μm, W = 20 μm), Ti/Au = 50/250 nm.

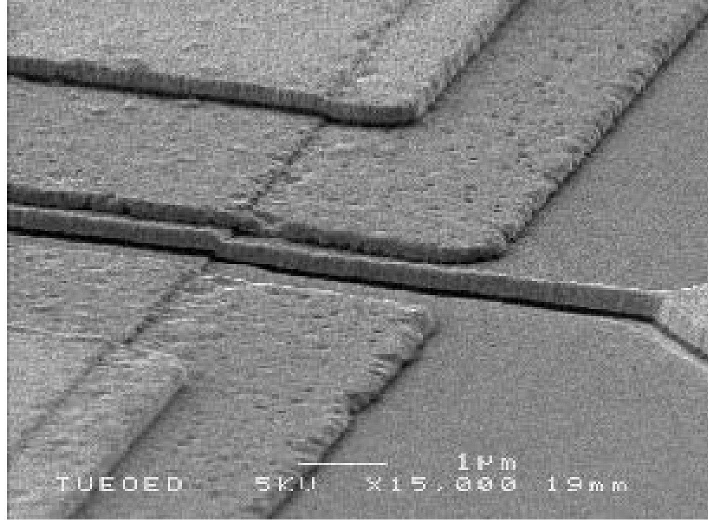


Figure 4.6: SEM photograph of an amplification stage transistor fabricated by e-beam lithography (l_g = 0.26 μm, l_{DS} = 1.75 μm, W = 20 μm, Ti/Au = 50/250 nm).

4.3 Basic Theory

The block diagram for the receiver circuit consisting of the photodetector and the transimpedance preamplifier is drawn in Fig. 4.7 [141]. The transimpedance amplifier is basically an inverting voltage amplifier with a feedback resistance R_f. The transimpedance amplifier is commonly used for its large bandwidth and low noise. Its advantage lies principally in the fact that the need for gain- and phase equalization can be avoided, while at the same time the amplifier noise may be much less than would be the case in an unequalized voltage amplifier (e.g. compared to a high impedance receiver design, in which the voltage signal is fed across a load resistance R_L to the voltage amplifier) [27].

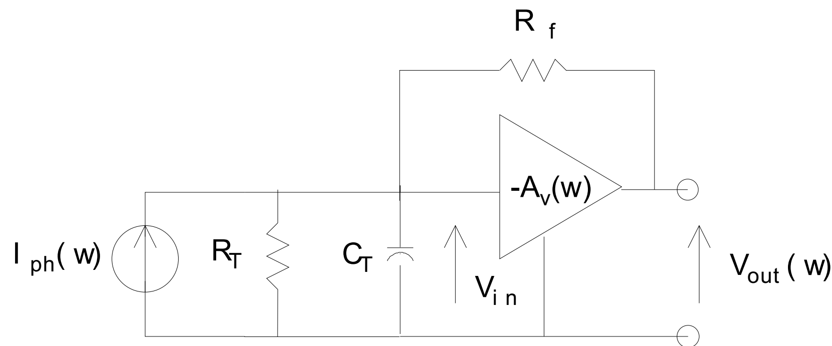


Figure 4.7: Block diagram of the photoreceiver: photodiode and transimpedance amplifier.

The open loop voltage gain A_v is defined as:

$$A_v = -\frac{V_{out}}{V_{in}} \ , \tag{4.1}$$

where $V_{in} = R_T * I_{ph}$ is the voltage signal generated from the photocurrent of the detector and fed to the transimpedance amplifier. R_T is the total input resistance of the transimpedance design: $R_T = \frac{R_f}{A_v+1}$. The total input capacitance C_T is determined as:

$$C_T = C_{msm} + C_a + (A_v + 1)C_f \ , \tag{4.2}$$

where C_{msm} is the MSM PD capacitance, C_a is the amplifier input capacitance and C_f is a parasitic feedback capacitance appearing in parallel to R_f.

The transfer function of the receiver may be derived by summing the currents at the amplifier input, and applying $V_{in} = -\frac{V_{out}}{A_v}$ [142]:

$$V_{out} = -\frac{I_{ph}R_f}{(1+\frac{1}{A_v}+\frac{R_f}{A_vR_T})\left[1+\frac{j\omega R_fC_T}{(A_v+1+\frac{R_f}{R_T})}\right]} \ . \tag{4.3}$$

- If $A_v >> (1+\frac{R_f}{R_T})$, then

$$V_{out} = \frac{-I_{ph}R_f}{(1+j\omega R_fC_T/A_v)}. \tag{4.4}$$

- Further, if $A_v >> \omega R_fC_T = 2\pi\Delta fR_fC_T$ (where Δf is the bandwidth), the output voltage simply becomes:

$$V_{out} = -I_{ph}R_f \ . \tag{4.5}$$

- In case $A_v >> \frac{R_f}{R_T}$, then

$$V_{out} = \frac{-A_vI_{ph}R_f}{A_v+1+j\omega R_fC_T}. \tag{4.6}$$

The transimpedance Z_T relates the output voltage to the photocurrent:

$$Z_T(w) = \frac{V_{out}}{I_{ph}} = \frac{-A_vR_f}{A_v+1+j\omega R_fC_T} \ . \tag{4.7}$$

- Further, if $A_v+1 >> \omega R_fC_T = 2\pi\Delta fR_fC_T$ the output voltage becomes:

$$V_{out} = -\frac{A_v}{A_v+1}I_{ph}R_f \ . \tag{4.8}$$

The transimpedance is now given by:

$$Z_T = \frac{-A_v}{A_v+1}R_f \ . \tag{4.9}$$

The 3 dB bandwidth of the receiver is:

$$f_{3dB} = \frac{A_v+1}{2\pi R_fC_T} \ . \tag{4.10}$$

Assuming that $A_v = 10$, $R_f = 1.25$ kΩ and $C_T = 200$ fF (gate to source capacitance of HEMT + stray capacitance) the bandwidth becomes $f_{3dB} \leq 7.0$ GHz.

The values of R_f and C_f together with the detector characteristics R_{dark} and C_{msm} determine the overall frequency response of the system. The gain peaking, observed at higher frequencies, is mainly attributed to the combination of the detector and the feedback capacitance. If C_f is in balance with C_{msm}, the response $Z_T(w)$ is fully compensated and has a flat amplification. The gain peaking starts to appear, whenever the response is partially compensated. If no C_f exists, the response becomes uncompensated, and the observed high-frequency gain has a very high and sharp peak. In order to control gain peaking, an extra C_f can be added to the circuit design [143]. The effect of C_f is shown in Section 4.5 with simulations with varying feedback capacitance values, Fig. 4.11(b). A figure of merit, often used to indicate the performance of the transimpedance receivers, is the transimpedance-bandwidth product: Z_T f_{3dB}.

4.4 Noise Behaviour

The objective of this work is mainly a broad bandwidth photoreceiver, with high open loop gain and low input capacitance. However, noise characteristics of the receiver are very crucial, i.e. the signal-to-noise ratio defined as $K = \frac{V_{out}}{V_N}$, where V_{out} is the voltage at the output, Eq. (4.8), and V_N the total mean square noise at the output. Since an experimental noise analysis is beyond the scope of this work, only a theoretical overview is given in the following.

The spectral density of the noise current source $< i_N^2 >$, which is an integral over the bandpass B of the detection system, [A^2/Hz], can be written as [144]:

$$\frac{< i_N^2 >}{\Delta f} = \frac{4k_BT}{R_T} + \frac{4k_BT}{R_f} + 2q(I_L) + \frac{4\,k_B\,T\,\Gamma\,\omega^2\,C_T^2}{g_m} \,, \tag{4.11}$$

in which the first and second term is the thermal noise due to the input resistance and feedback resistance, respectively (see block diagram in Fig. 4.7). The total input resistance R_T of the transimpedance design includes the detector and the amplifier input resistances. The third term is the shot noise caused by the leakage currents, comprising the detector dark current I_{dark}, the gate leakage current I_g plus average signal photocurrent. The last term is associated with the channel noise of the FET. The input capacitance C_T is as defined in Eq. (4.2), and Γ is a geometrical factor unique to the type of FET.

The primary goal in optical receiver design is to minimize $< i_N^2 >$ while maintaining the minimum bandwidth necessary to insure operation at the desired bit rate. It is obvious from the different contributions that both the detector and the gate leakage current have to be kept minimal. The value of R_f should be as large as possible to reduce the feedback contribution (small feedback transistor). In order to minimize the ratio C_T^2/g_m, which is significant at high frequencies, high level of amplification and small parasitic capacitances for the detector, amplifier input and feedback are essential. In fact, this means that a low noise photoreceiver requires a high cut-off frequency, since $f_t = g_m/2\pi C_a$, in which C_{gs} dominates C_a. The device design for maximum transconductance g_m and minimum gate capacitance C_{gs} conditions can also be controlled to some extent by proper bias choice [145]. When fabricating submicrometer gate lengths, the reduction of the gate resistance R_g, which can be obtained by utilizing a T-shaped gate with thick gate metallization, is also a key factor. Furthermore, other device improvements, such as multifinger layouts, and optimization of the transistor width should reduce the noise even more[116].

A general method for evaluating noise performance of a preamplifier is the so called noise figure, NF, which indicates what portion of the system noise is caused by the amplifier [143]: $NF = 10\log[\frac{\text{TotalNoise}}{\text{DetectorNoise}}]$. A NF of 0.1 to 3 dB is considered satisfactory. Preamplifiers with $NF > 3$ dB add significant noise to the system.

Referring to the small-signal equivalent circuit model in Fig. 3.6, a useful approximation for the noise figure of a HEMT is given by [146]:

$$NF_{min} = 1 + \frac{\sqrt{T_gT_d}}{T_o}(\frac{f}{f_t})\sqrt{4g_dR_{gs}} \,, \tag{4.12}$$

where T_g and T_d is the noise equivalent temperature at the input and output of the device, respectively. T_g is approximately room temperature for most modern microwave devices, but T_d is a material and bias dependent parameter that can vary from several hundred to several thousand degrees Kelvin. T_o is the IEEE Standard noise reference temperature (290 K), f is the frequency of interest, f_t is the unity current gain cut-off frequency, g_d is the drain-source conductance of the device and R_{gs} is the gate-source resistance. Based on Eq. (4.12), it is clear that, given a established material profile, for a low noise photoreceiver best noise performance is obtained by minimizing the source access resistance and maximizing the current cut-off frequency f_t, as already stated earlier.

Alternatively, the noise temperature, rather than the noise figure, of the device may be assessed. The noise temperature is given by $T_{min} = (NF_{min} - 1)T_o$.

The sensitivity of an optical receiver can be given by the expression:

$$\eta P_{min} = \frac{hf}{q}Q\sqrt{< i_N^2 >} \,, \tag{4.13}$$

where P_{min} is the minimum detectable mean power needed to achieve a given error rate, Q is the signal to noise ratio or quality factor needed for that error rate. For a bit error rate (BER) of 10^{-9} $\Rightarrow Q = 6$. $< i_N^2 >$ is the mean square noise current referred to the photocurrent (Eq. (4.11)), which sets the lower limit for the mean power, and $\frac{\eta q}{hf}$ is the detector responsivity. Noticeable is that the minimum detectable power is inversely proportional to the responsivity. Equation (4.13) applies for optical receivers with MSM PDs, which have no internal gain and low leakage currents, hence the noise in an optical detection system is dominated by the noise in the amplification circuits.

The noise limit of the photoreceiver sensitivity can alternatively be estimated from the integrated input-referred noise current, the responsivity of the photodiode, and the bandwidth of the photoreceiver using the relation [147]:

$$\bar{P} = \frac{SNR}{2R}\sqrt{< i_n^2 >}\left[1 - 2\ e^{-\pi f_{3dB}/B}\right]^{-1},$$

where B is the bit rate, R is the photodetector responsivity, and f_{3dB} is the bandwidth of the photoreceiver. Directly measured sensitivites of -17.7 dBm and -15.8 dBm were obtained at 10 and 12 Gb/s, respectively, for a bit error ratio of 10^{-9} for an InGaAs/InP-based PIN/HEMT photoreceiver. The directly measured sensitivities were quite close to the estimated ones, using noise and frequency response considerations, lying within 0.2 dB of the noise-limited sensitivity at 10 Gb/s and 1.3 dB at 12 Gb/s [147]. In [148] sensitivities of -24.7, -21.2 and -18.5 dBm at 10^{-9} BER were observed for 2.5, 4, and 7 Gb/s operation, respectively for a PIN/HEMT InP-based photoreceiver.

Parameters needed for a high sensitivity photoreceiver are a high loop gain required for a large feedback resistance and very low input capacitance.

4.5 Simulations

Circuit diagram for simulations

Figure 4.8 shows the circuit diagram of the integrated photoreceiver for simulations. The corresponding mask layout and fabricated receiver are depicted in Figs. 4.3 and 4.4, respectively. In the circuit schematic a feedback capacitance C_f is added in parallel to R_f in order to model the equivalent circuit of a resistor structure more precisely. The simulations were done with HP MDS. The transistors are modelled with the EEHEMT1-model from MDS's standard device library; with the parameters obtained from IC-CAP parameter extraction as described in Section 3.5.3. The interconnections and joints are simulated by microstrip components (MS transmission lines, MS tees, MS crosses).

Theoretical electrical simulations were done on different receiver types, using the circuit diagram in Fig. 4.8 with S-parameter ports 1 and 2 attached to the input and output, respectively, and replacing the symbol for the MSM photodiode with the equivalent circuit introduced in Section 2.3.3, Fig. 2.20. For the standard and submicron transistors EEHEMT1-model parameters listed in Figs. D.1 and D.2 were used. Three different receivers were simulated as follows. Receivers with:

- (1) All transistors and the MSM fabricated using optical lithography (gate length ca. 1 μm).
- (2) Submicron transistors for the amplification stage, optically defined transistors for the level shift and buffer stage and a submicron MSM.
- (3) All transistors and the MSM PD defined by e-beam exposure (gate length in the submicron region).

Receiver-types (1) and (2) were fabricated in this work, whereas receiver (3) was only simulated. The goal is not only to compare the different receivers, but also to investigate the effect of the feedback resistance R_f, the feedback capacitance C_f and the MSM capacitance C_{msm} on the bandwidth. The feedback resistance is shown to have a direct effect on the transimpedance value and thus the bandwidth, whereas the MSM and the feedback capacitance affect the peak appearing at the high frequency end. The feedback capacitance shifst the peak and defines the peak amplitude. In general, the response could be tuned with the 'correct' combination of C_{msm} and C_f-values in such a way that the transimpedance would be flat. In the following simulations are done in order to see the different factors that define the bandwidth and the transimpedance.

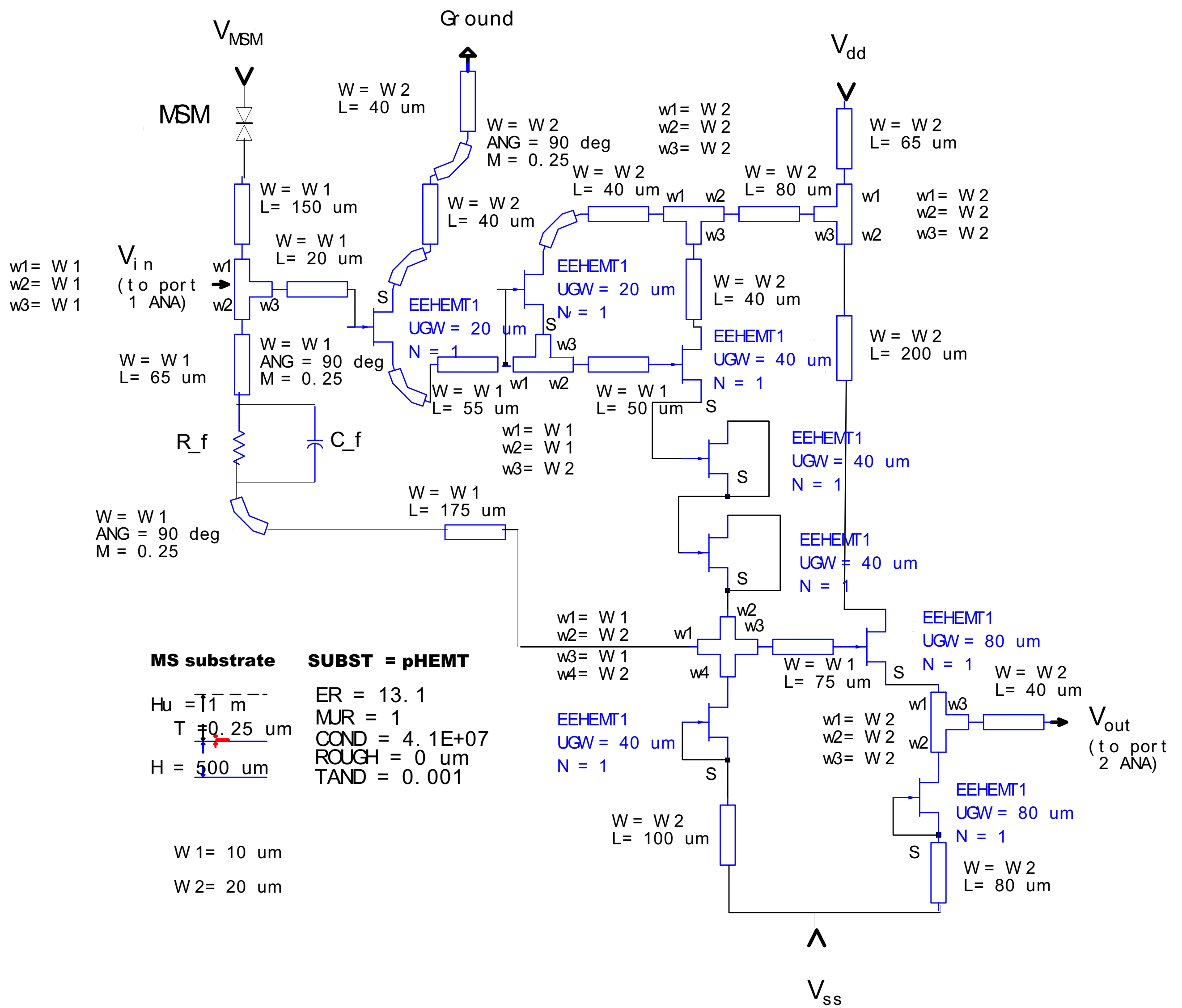


Figure 4.8: Circuit diagram for simulation of the integrated photoreceiver.

Influence of the feedback resistance R_f

Figure 4.9 (a) plots the transimpedance for the 3 various receiver types, with $R_f = 500\ \Omega$, $C_f = 10$ fF, $C_{msm} = 18$ fF ($A = 21$ x $28\ \mu\text{m}^2$, $w = s = 1\ \mu$m) and $C_{msm} = 27$ fF ($A = 11$ x $22\ \mu\text{m}^2$, $w = 0.2\ \mu$m, $s = 0.3\ \mu$m) for standard and submicron MSMs, respectively. As expected, the highest bandwidth (16.85 GHz) is obtained for the receiver consisting solely of submicron transistors. The feedback R_f is 500 Ω, and the transimpedance is 430 Ω. Figure 4.9 (b) shows the effect of the feedback resistance R_f on the 3 dB bandwidth. A receiver with a combination of submicron and standard transistors is simulated, with $C_f = 10$ fF and $C_{msm} = 27$ fF ($A = 11$ x $22\ \mu\text{m}^2$, $w = 0.2\ \mu$m, $s = 0.3\ \mu$m). With increasing R_f the transimpedance increases, but at the expense of a smaller bandwidth.

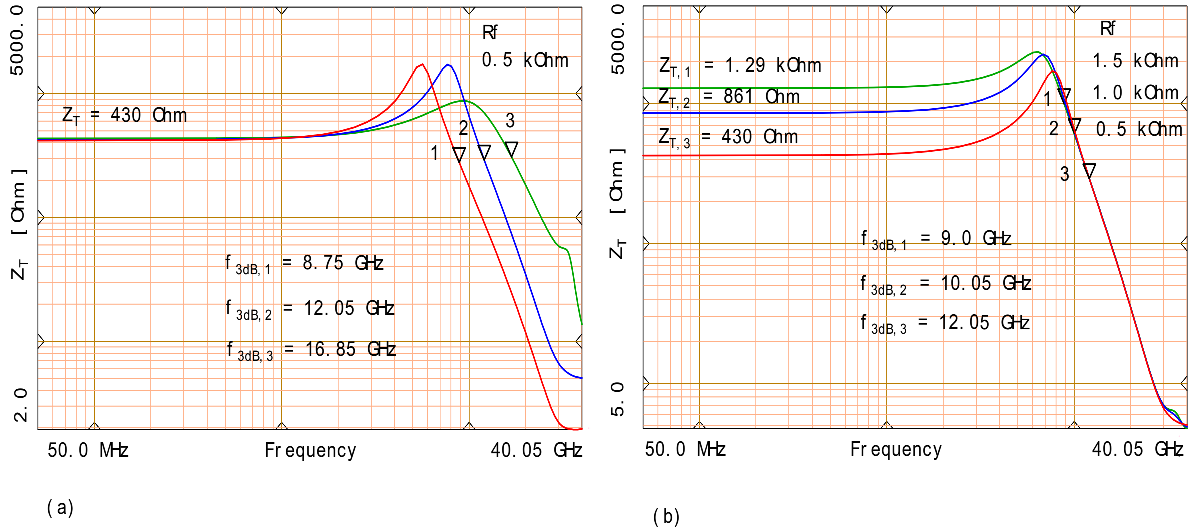


Figure 4.9: Transimpedance $|Z_{21}|$ from electrical S-parameter simulations for receivers with (a) 1. standard transistors 2. combination of submicron and standard transistors 3. submicron transistors. $R_f = 500\ \Omega$. (b) combination of standard and submicron transistors. R_f is varied from 1.5 kΩ down to 0.5 kΩ. $V_{dd} = 4$ V, $V_{ss} = -2$ V, $V_{msm} = 0$ V.

Figure 4.10 presents the simulations for the 3 different receiver types, and also the effect of the feedback resistance R_f on the 3 dB bandwidth. Values used in the simulation are: $C_f = 10$ fF, $C_{msm} = 18$ fF ($A = 21$ x $28\ \mu\text{m}^2$, $w = s = 1\ \mu$m) and $C_{msm} = 27$ fF ($A = 11$ x $22\ \mu\text{m}^2$, $w = 0.2\ \mu$m, $s = 0.3\ \mu$m) for optical and submicron MSMs, respectively. The transimpedance increases with increasing R_f, but at the expense of a reduced bandwidth. The transimpedance is 1.3 kΩ and 430 Ω for $R_f = 1500\ \Omega$ and $R_f = 500\ \Omega$, respectively.

Influence of the feedback capacitance C_f and C_{msm}

The effect of the MSM capacitance on the 3 dB bandwidth and the position of the peak is plotted in Fig. 4.11 (a) for a receiver with standard and submicron transistors. In the simulation R_f is set to 500 Ω, and C_f is 10 fF. It is evident from the simulation, that a small MSM capacitance shifts the high-frequency-peak to right and therefore gives the highest bandwidth. The position and amplitude of the peak appearing at high frequency as a function of the feedback capacitance is investigated in Fig. 4.11 (b). The plot shows the transimpedance for a receiver with standard and submicron transistors. R_f is set to 500 Ω and $C_{msm} = 27$ fF, ($A = 11$ x $22\ \mu\text{m}^2$, $w = 0.2\ \mu$m, $s = 0.3\ \mu$m). From the simulation can be concluded, that increasing the value of C_f gives a smaller peak amplitude, but it has no effect on the the bandwidth. The 3 dB bandwidth is constant for all varying C_f values: for a transimpedance of 430 Ω it gives 12.0 GHz.

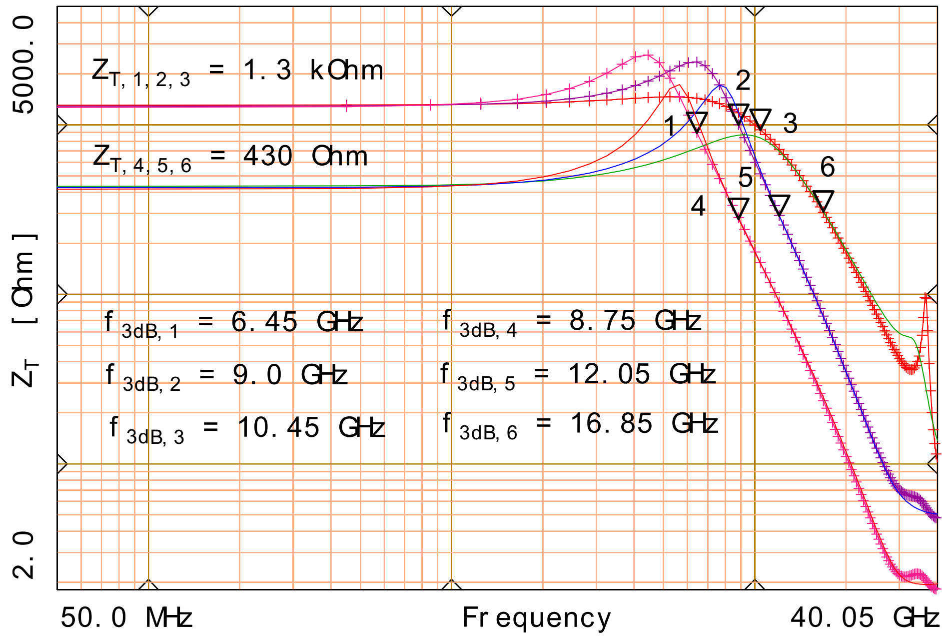


Figure 4.10: Transimpedance $|Z_{21}|$ from electrical S-parameter simulations for different receivers. (1),(4) standard transistors (2),(5) combination of submicron and standard transistors (3),(6) submicron transistors. The feedback resistance is 1.5 kΩ (3 upper curves) and 0.5 kΩ (3 lower curves). V_{dd} = 4 V, V_{ss} = -2 V, V_{msm} = 0 V.

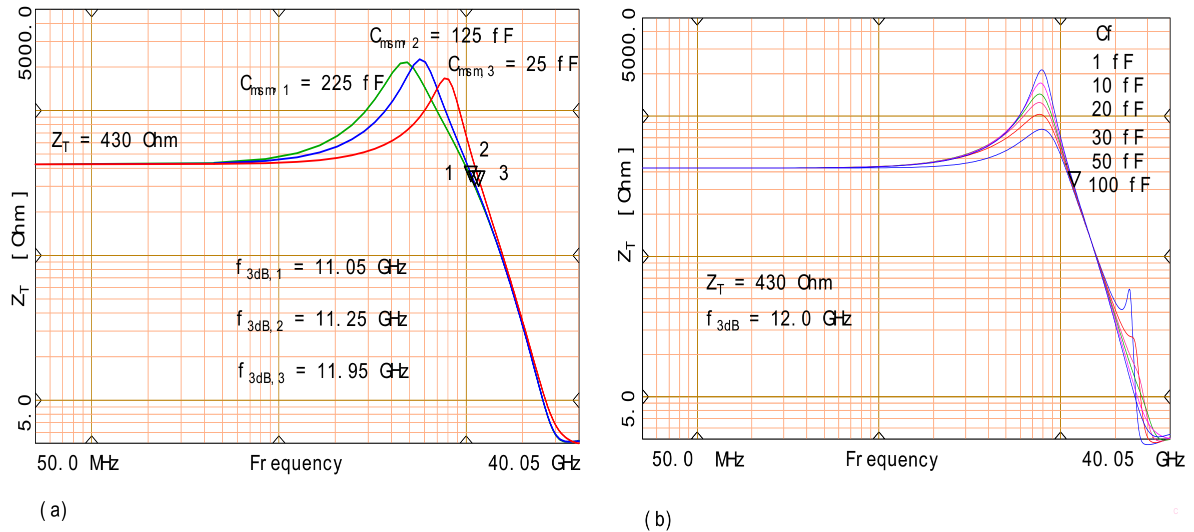


Figure 4.11: Transimpedance $|Z_{21}|$ from electrical S-parameter simulations for a receiver with standard and submicron transistors with (a) varying MSM capacitance values (b) varying feedback capacitance values. R_f = 0.5 kΩ. V_{dd} = 4 V, V_{ss} = -2 V, V_{msm} = 0 V.

4.6 Measurements

4.6.1 Electrical Characterization

Circuit diagram for electrical characterization

The electrical characterization of the circuits was done according to the schematics shown in Fig. 4.12.

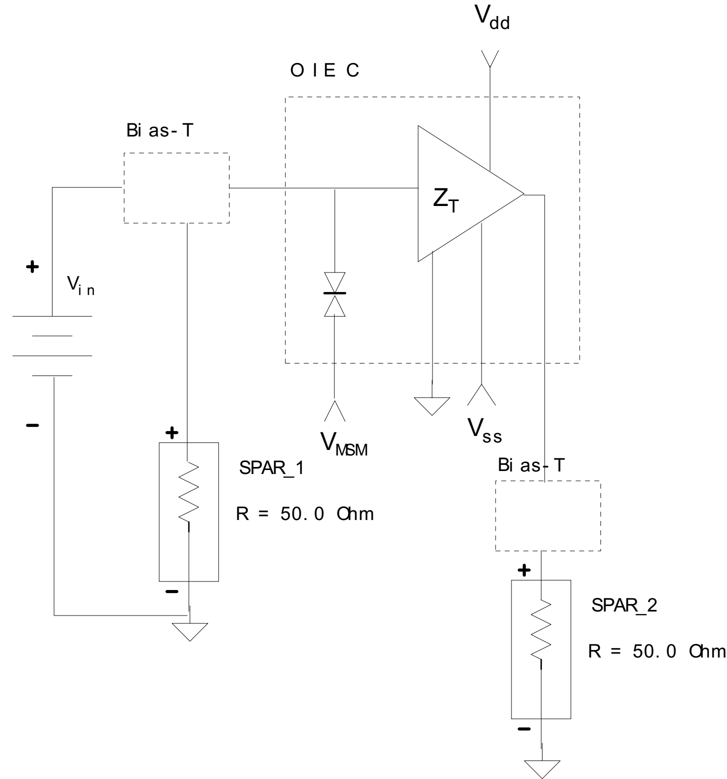


Figure 4.12: Circuit diagram for measurements of the electrical HF characteristics of the integrated photoreceiver.

Standard receivers

From the standard circuits (i.e. optically fabricated) pHEMT2 showed best performance compared to circuits fabricated on pHEMT1 and pHEMT3. The standard pHEMT2 circuits did not only obtain the largest bandwidths, but very good uniformity and yield across the whole sample. From 12 receivers in one row 9 circuits demonstrated excellent performance. Figure 4.13 plots the transimpedance of these devices.

The measurement and fitting for standard receivers on pHEMT1 is presented in Fig. 4.14. $R_f = 1200$, 1300, 1350 Ω and C_{msm} = 16 fF (A = 21 x 24 μm^2, $s = w = 1$ μm), 9.6 fF (A = 22 x 28 μm^2, $s = w = 2$ μm), C_{msm} = 16 fF from the lowest to the uppermost curve, respectively (2D conformal mapping theory). For all fittings $R_s = 5$ Ω and $R_{dark} = 50$ kΩ. The feedback capacitance C_f influences the height of the peak, as predicted in the simulations shown in Fig. 4.11(b). Values of C_f = 20 fF, 5 fF, 1 fF from the lowest to the uppermost curve were used, respectively. The inset shows several receivers measured on the same wafer; the highest bandwidth achieved is 7.88 GHz for $Z_T = 1.185$ kΩ. The fit is good considering the conditions at which the EEHEMT1-model parameters were extracted. The extractions were performed up to 20.05 GHz, and they did not show very good fitting at the high frequency end. Thus, the discrepancy at the falling edge of Z_T in Fig. 4.14 is expected.

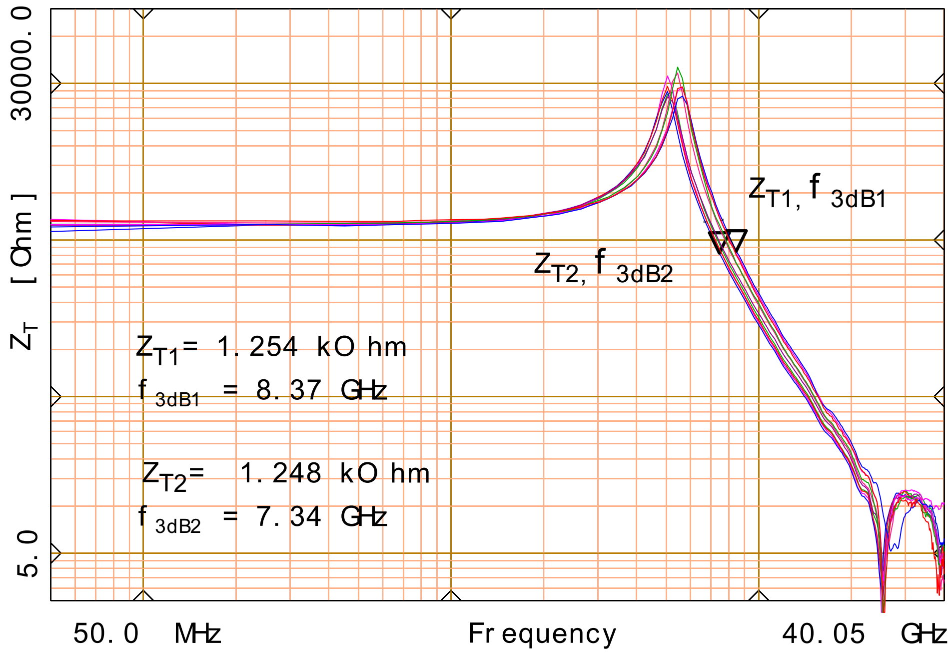


Figure 4.13: Transimpedance from electrical S-parameter measurements for standard receivers fabricated on pHEMT2. V_{dd} = 4.5 V and V_{ss} = -2.5 V, V_{msm} = 0 V.

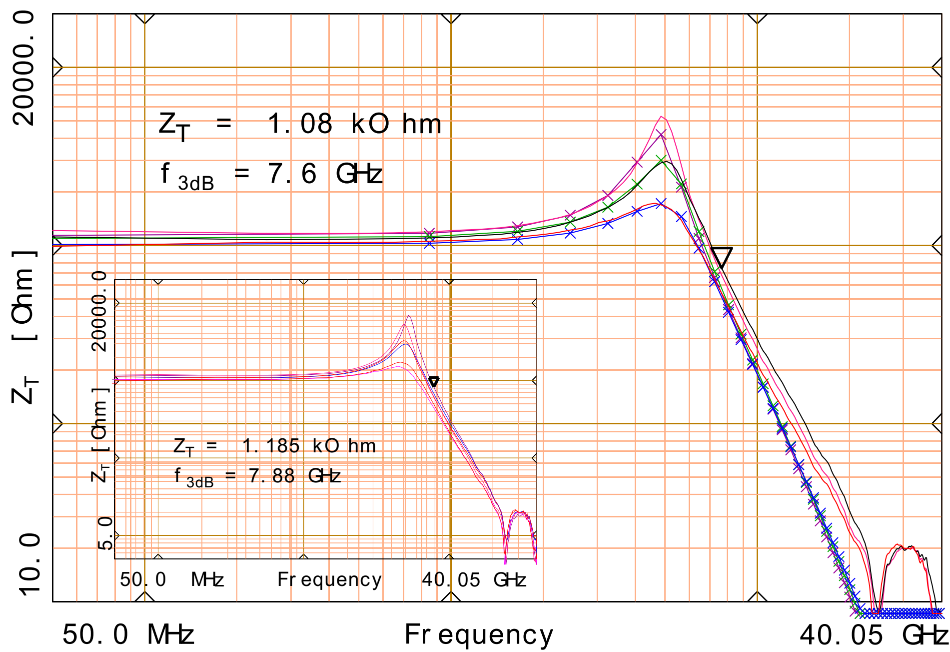


Figure 4.14: Transimpedance from electrical S-parameter measurements for standard receivers fabricated on pHEMT1. Measurement (solid line), simulation (crosses). V_{dd} = 4 V and V_{ss} = -2 V, V_{msm} = 0 V. The inset: several receivers measured on the same wafer.

E-beam receivers

Figure 4.15 shows the simulated and measured transimpedance for e-beam circuits fabricated on pHEMT2 (l_g = 0.2 μm, l_{DS} = 1 μm). In the equivalent circuit for the MSM the theoretical capacitance values based on 2D conformal mapping are used. C_{msm} = 28 fF (A = 11 x 22 μm^2, s = 0.3 μm, w = 0.3 μm), C_{msm} = 98 fF (A = 22 x 40 μm^2, s = 0.3 μm, w = 0.3 μm) for upper and lower curve, respectively. For both simulations R_f = 1.4 kΩ, C_f = 1 fF, R_s = 5 Ω and R_{dark} = 50 kΩ. In the S-parameter measurement the bias probe head was not connected to the MSM-pad (i.e. floating bias point for the MSM, and no DC current possible), which means that a high ohmic resistance ($1 \cdot 10^{12}$ Ω) in parallel to a fringing capacitance (from the pad to the metal frame = ground) had to be added to the simulated circuit model. Values for the fringing capacitance were 0.05 pF and 0.02 pF for upper and lower curve, respectively. Also for the upper curve an inductance (L_s = 9 nH) had to be incorporated in series with the feedback resistance in order to match the curves.

The simulated transimpedance is in good agreement with the measured one. Only at high frequencies (above 15 GHz) the slope of the simulated curve becomes steeper. This is due to the IC-CAP parameter extraction, which was performed only up to 20 GHz. Also it has to be remembered that the IC-CAP parameters were simulated for several different bias conditions, which means that the extracted parameters might not be optimally fitted to the voltages used in the measurements.

In Figure 4.16 is presented dB(S_{21}) as a function of frequency for an e-beam circuit. The result is very good: frequency at 0 dB-level is measured to be 9.45 GHz, and $|S_{21}|$ exhibits 7.25 (17.2 dB) at 250 MHz.

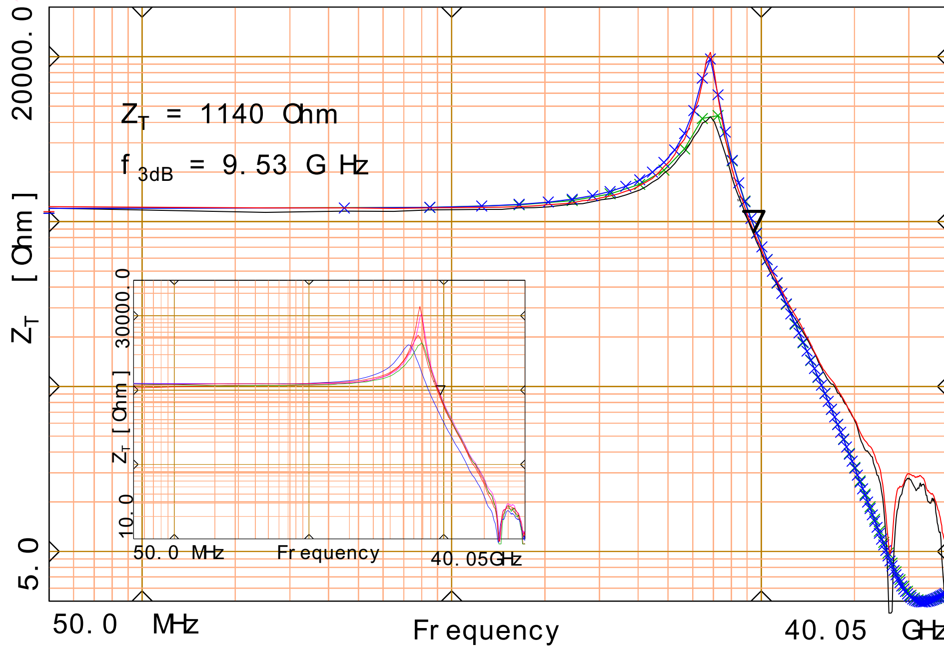


Figure 4.15: Transimpedance from electrical S-parameter measurements for e-beam receivers on pHEMT2. The bias probe was not connected to the MSM-pad. Measurement (solid line), fitting (crosses). V_{dd} = 4.5 V, V_{ss} = -2.5 V (upper curve); V_{dd} = 5 V, V_{ss} = -3.1 V (lower curve). For both receivers V_{msm} = 0 V. l_g = 0.2 μm, l_{DS} = 1 μm. The inset: several receivers measured on the same wafer.

Comparison between standard and e-beam receivers

A comparison of the transimpedance between a standard and an e-beam circuit is plotted in Fig. 4.17. The simulation was done using R_f = 1350 Ω, C_f = 1 fF, R_s = 3 Ω, R_{dark} = 50 kΩ. C_{msm} = 9.6 fF (A = 22 x 28 μm^2, s = w = 2 μm) and 98 fF (A = 22 x 40 μm^2, s = 0.3 μm, w = 0.3 μm) for

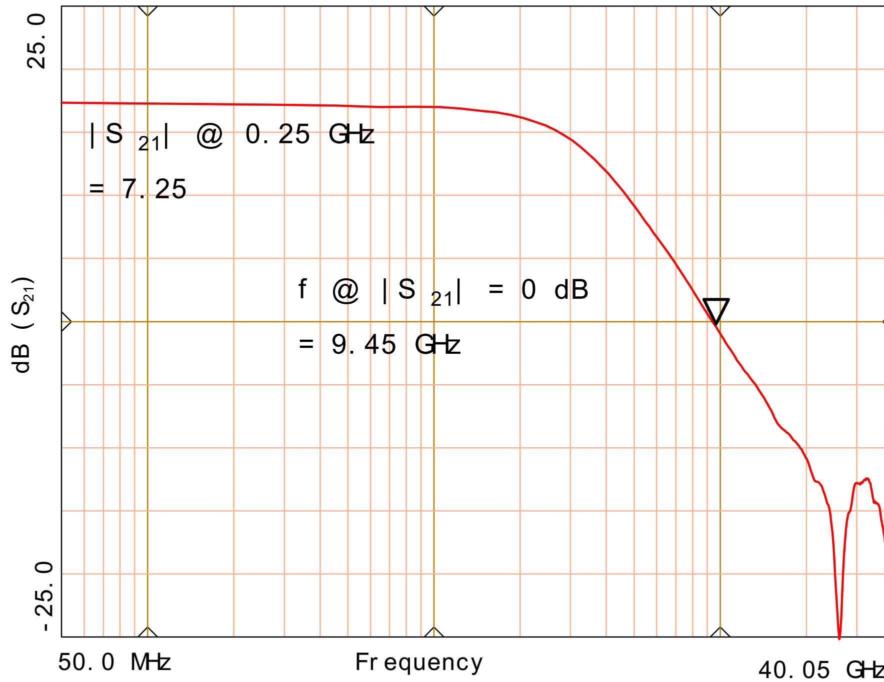


Figure 4.16: dB(S_{21}) for an e-beam receiver on pHEMT2. V_{dd} = 4.5 V, V_{ss} = -2.5 V, V_{msm} = 0 V. l_g = 0.2 μm, l_{DS} = 1 μm. f_{3dB} = 9.45 GHz for Z_T = 1.2 kΩ.

the standard and e-beam circuit, respectively. Measuring the e-beam circuit, the MSM bias pad was floating. Therefore, a high ohmic resistance ($1 \cdot 10^{12}$ Ω) in parallel to a fringing capacitance (from the pad to the metal frame, 0.035 pF) was added to the simulated circuit model. The good agreement found in the figure confirms the validity of the equivalent circuit.

A comparison of Z_T between standard and e-beam receivers fabricated on different wafers is seen in Fig. 4.18. The exact measurement conditions, and the obtained transimpedance and the 3 dB bandwidth values are summarized in Table 4.1. The e-beam circuit fabricated on pHEMT2 has clearly the highest bandwidth (9.53 GHz).

Table 4.1: Measurement conditions, Z_T and f_{3dB} for different receivers (see Fig. 4.18).

Device	V_{dd} [V]	I_{dd} [mA]	V_{ss} [V]	I_{ss} [mA]	V_{in}/V_{out} [V]	Z_T [kΩ]	f_{3dB} [GHz]
pHEMT1 (standard)	4.0	31.34	-2.0	-26.65	-0.1/-0.046	1.185	7.88
pHEMT2 (standard)	4.5	44.37	-2.5	-38.1	0.11/0.15	1.254	8.37
pHEMT3 (standard)	6.5	7.72	-2.0	-6.6	-0.17/0.23	1.159	6.75
pHEMT2 (e-beam)	5.0	47.9	-3.1	-41.1	-0.12/0.55	1.139	9.53

Receivers with feedback transistor

Receivers with a feedback transistor (W = 5 μm) were fabricated also; mask design by J. Wellen [27]. The benefit of utilizing an active feedback instead of a passive one (i.e. fixed resistor) is the possibility to tune the gain and bandwidth by varying the feedback voltage V_f. The transimpedance was measured for several receivers, Fig. 4.19. In (a) Z_T ranges from 344 to 422 Ω at V_f = 0 V, and f_{3dB} is between 8.7 to 10.1 GHz. In (b) Z_T ranges from 332 to 411 Ω at V_f = 0 V, and f_{3dB} from 8.5 to 9.9 GHz.

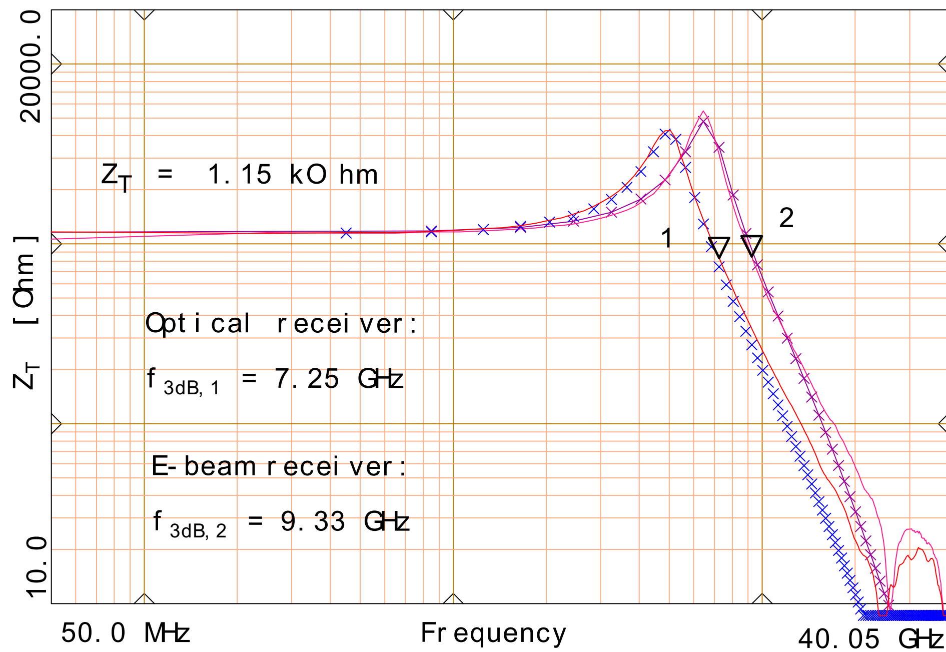


Figure 4.17: Measured (solid line) and simulated (crosses) transimpedance from electrical S-parameter measurements for a standard receiver on pHEMT1 and an e-beam receiver fabricated on pHEMT2. V_{dd} = 4 V, V_{ss} = -2 V (standard); V_{dd} = 4.5 V, V_{ss} = -2.5 V (e-beam). For both circuits V_{msm} = 0 V. l_g = 0.2 μm, l_{DS} = 1 μm.

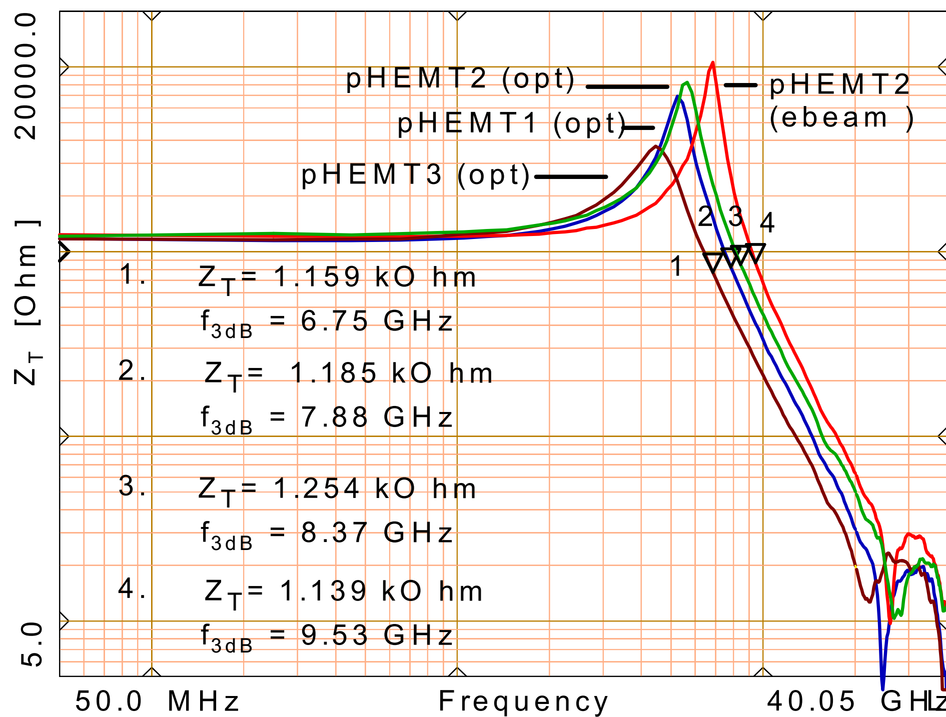


Figure 4.18: Transimpedance from electrical S-parameter measurements for receivers fabricated on different wafers: pHEMT1, pHEMT2 and pHEMT3, using both optical and e-beam lithography. $l_g/l_{DS} = 1/4$ μm, $l_g/l_{DS} = 0.2/1$ μm for standard and e-beam circuits, respectively.

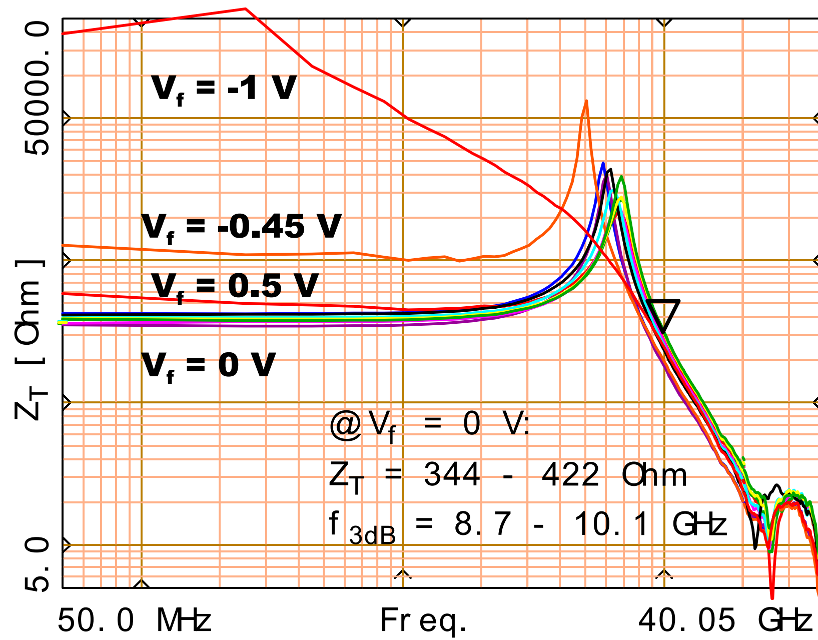
The Z_T at V_f = 0 V is as low as 400 Ω, which is a result of the fact that the transistors at V_{gs} = 0 V already have an almost fully conducting channel, i.e. a low value for R_f. Making V_f more negative raises Z_T, while for V_f being positive, Z_T barely changes. When V_f = -1 V, it means that the feedback transistor is pinched off and has a high resistance, hence the gain is large and approximates the open loop gain of the receiver. As a conclusion it can be said, that the feedback transistors showed promising results considering the bandwidth. However, the transimpedance was low, thus leading to a considerably lower gain-bandwidth product than compared to passive receivers reported in the previous. Redesign of circuits with feedback transistors is necessary with this wafer structure, in order to optimize the R_f value.

Summary of results

Tables 4.2 and 4.3 record the high-performance receivers fabricated in this work, showing $|S_{21}|$ at 250 MHz, the frequency at $|S_{21}|$ = 0 dB, the 3 dB bandwidth and Z_T. Clearly best performance is achieved for e-beam circuits fabricated on pHEMT2. From the standard receivers ($l_g \sim 1$ μm) the circuits fabricated on pHEMT2 show superior characteristics compared to those on pHEMT1 or pHEMT3. This is an indication that the 1 μm buffer layer used in pHEMT2 is of advantage compared to that of 0.5 μm in pHEMT1 and pHEMT3. Furthermore, the DBR-type SL-structure in pHEMT3 may have caused parallel conduction, leading to a decreased velocity in the channel, and thus a reduced overall bandwidth. Also the feedback resistance may have changed drastically, due to process variations leading to structural and dimensional differences. Conclusions given here are, however, only indicative and would require a much larger characterization work for appropriate accuracy. Furthermore, optical measurements should be performed for all different structures in order to get full confirmation of the influence of the substrate layers on the MSM responsivity, and hence on the overall performance of the total receiver.

Table 4.2: Results of electrical measurements for various receivers.

Receiver Material	l_g [μm]	V_{dd}/I_{dd} [V, mA]	V_{ss}/I_{ss} [V, mA]	V_{in}/V_{out} [V](open)	Z_T [kΩ]	f_{3dB} [GHz]	$Z_T f_{3dB}$ [Ω THz]
pHEMT2	0.45, 1.1	5.0 / 37.0	-2.5 / -30.8	0.01 / -0.02	1.36	8.05	10.9
pHEMT2	0.25, 1.1	4.5 / 39.9	-2.5 / -34.1	-0.02 / -0.03	1.21	9.45	11.5
pHEMT2	0.25, 1.1	4.5 / 43.1	-2.5 / -36.8	-0.03 / -0.07	1.21	8.05	9.7
pHEMT2	0.2, 1.1	4.5 / 42.4	-2.5 / -35.2	-0.01 / -0.02	1.21	9.45	11.5
pHEMT2	0.2, 1.1	5.0 / 47.9	-3.1 / -41.1	-0.12 / 0.55	1.14	9.45	10.8
pHEMT2	0.2, 1.1	4.5 / 44.5	-2.5 / -36.1	0.05 / 0.21	1.15	9.33	10.8
pHEMT1	1.1	4.0 / 34.6	-2.0 / -29.8	-0.188 / -0.233	1.16	7.3	8.4
pHEMT1	1.1	4.0 / 30.8	-2.0 / -28.1	-0.390 / -0.376	1.18	7.25	8.6
pHEMT1	1.1	4.0 / 31.8	-2.0 / -26.7	-0.100 / -0.046	1.19	7.9	9.4
pHEMT2	1.1	4.5 / 44.37	-2.5 / -38.1	0.11 / 0.15	1.25	8.4	10.5
pHEMT2	1.1	4.5 / 37.3	-2.5 / -32.0	0.08 / 0.11	1.25	7.34	9.2
pHEMT3	1.1	6.5 / 7.72	-2.0 / -6.6	-0.17 / 0.23	1.22	6.45	7.8
pHEMT3	1.1	6.5 / 7.72	-2.0 / -6.6	-0.17 / 0.23	1.16	6.75	7.8



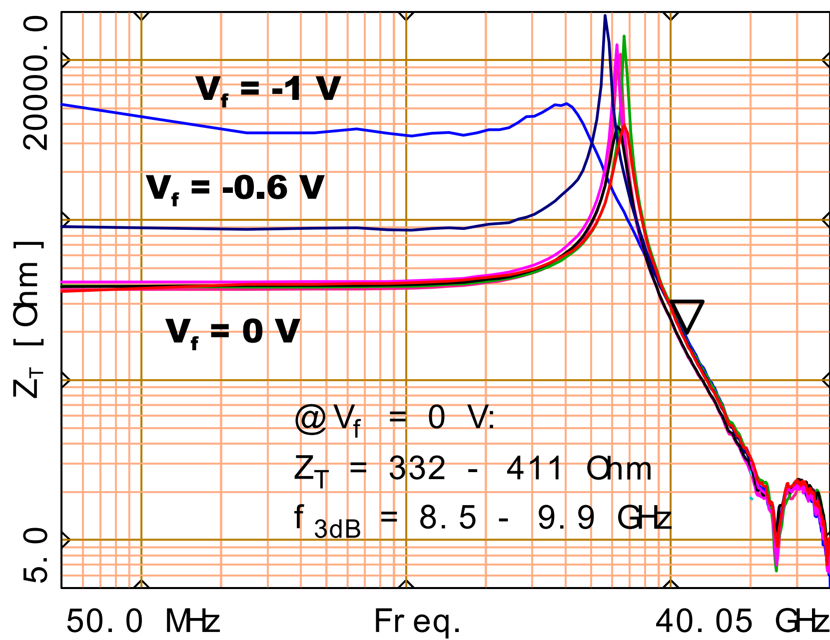


Figure 4.19: Transimpedance for receivers with a variable feedback transistor fabricated on pHEMT1. l_g/l_{DS} = 1/4 μm, V_{dd} = 5 V, V_{ss} = -3 V, V_{msm} = 0 V, the feedback voltage is V_f = 0 V for (a) 9, (b) 7 measured receivers, and varied for one receiver in both (a) and (b).

Table 4.3: Results of electrical measurements for various receivers.

Receiver Material	l_g [μm]	V_{dd}/I_{dd} [V, mA]	V_{ss}/I_{ss} [V, mA]	V_{in}/V_{out} [V](open)	$\|S_{21}\|$ @ 0.25 GHz [/dB]	f @ $\|S_{21}\| = 0$ dB [GHz]
pHEMT1	0.25, 1.1	4.0 /	-2.0 /	/	7.92 / 18.0	6.45
pHEMT2	0.45, 1.1	5.0 / 37.0	-2.5 / -30.8	0.01 / -0.02	9.88 / 19.9	8.45
pHEMT2	0.25, 1.1	4.5 / 39.9	-2.5 / -34.1	-0.02 / -0.03	6.86 / 16.7	9.05
pHEMT2	0.25, 1.1	4.5 / 43.1	-2.5 / -36.8	-0.03 / -0.07	6.63 / 16.4	9.05
pHEMT2	0.2, 1.1	4.5 / 42.4	-2.5 / -35.2	-0.01 / -0.02	7.25 / 17.2	9.45
pHEMT2	0.2, 1.1	5.0 / 47.9	-3.1 / -41.1	-0.12 / 0.55	5.11 / 14.2	9.25
pHEMT2	0.2, 1.1	4.5 / 44.5	-2.5 / -36.1	0.05 / 0.21	5.64 / 15.0	8.45
pHEMT3	0.65, 1.1	5.0 / 41.4	-2.5 / -37.0	-0.21 / -0.18	7.78 / 17.8	6.05
pHEMT1	1.1	4.0 / 31.2	-2.0 / -26.7	-0.217 / -0.247	6.68 / 16.5	8.45
pHEMT1	1.1	4.0 / 30.0	-2.0 / -25.4	-0.220 / -0.087	6.84 / 16.7	8.85
pHEMT1	1.1	4.0 / 34.4	-2.0 / -29.4	-0.037 / 0.008	7.41 / 17.4	8.05
pHEMT1	1.1	4.0 / 30.8	-2.0 / -28.1	-0.390 / -0.376	8.61 / 18.7	7.85
pHEMT1	1.1	4.0 / 31.8	-2.0 / -26.7	-0.100 / -0.046	7.08 / 17.0	8.85
pHEMT2	1.1	4.5 / 44.37	-2.5 / -38.1	0.11 / 0.15	7.99 / 18.1	9.25
pHEMT2	1.1	4.5 / 44.41	-2.5 / -38.4	0.08 / 0.15	8.17 / 18.2	9.05
pHEMT2	1.1	4.5 / 44.1	-2.5 / -37.6	0.09 / 0.24	8.34 / 18.4	8.65
pHEMT2	1.1	4.5 / 43.6	-2.5 / -37.4	0.09 / 0.15	8.53 / 18.6	8.45
pHEMT2	1.1	4.5 / 37.5	-2.5 / -32.1	-0.02 / 0.05	8.54 / 18.6	8.25
pHEMT2	1.1	4.5 / 37.7	-2.5 / -31.9	0.02 / 0.04	8.85 / 18.9	8.05
pHEMT2	1.1	4.5 / 37.5	-2.5 / -32.1	-0.02 / 0.05	8.46 / 18.6	8.45
pHEMT2	1.1	4.5 / 37.7	-2.5 / -31.9	0.02 / 0.04	16.4 / 24.3	8.85
pHEMT2	1.1	4.5 / 37.7	-2.5 / -31.9	0.02 / 0.04	10.5 / 20.4	8.45
pHEMT3	1.1	4.5 / 26.9	-2.5 / -23.5	0.076 / 0.09	6.47 / 16.2	6.45
pHEMT3	1.1	4.5 / 23.7	-2.5 / -20.5	-0.14 / -0.19	6.77 / 16.6	6.65
pHEMT3	1.1	5.5 / 15.3	-2.0 / -13.1	0.09 / 0.20	9.22 / 19.3	7.45
pHEMT3	1.1	6.5 / 8.65	-2.0 / -7.3	-0.11 / 0.39	8.71 / 18.8	6.25
pHEMT3	1.1	6.5 / 7.72	-2.0 / -6.6	-0.17 / 0.23	5.92 / 15.5	6.65

4.6.2 Opto-Electrical Response

Circuit diagram for OE-characterization

The opto-electrical (OE) characterization of the receivers was done according to the circuit diagram drawn in Fig. 4.20. The microwave signal coming out from the Network Analyzer port 1 is connected to the AC-port of a bias-T. At the output connector of the bias-T the modulating microwave signal is superimposed on a DC-current that sets the laser diode in its working range. Varying of the modulation frequency is done with the signal generator that is a part of the network analyzer system. The DC-current applied to the laser diode and the case temperature of the chip determines to a large extent the modulation bandwidth of the laser module (direct intensity modulation). From the output of the receiver under test (or from the MSM in case of a single MSM OE measurement) a microwave probe makes the connection to port 2 of the Network Analyzer.

The laser diode emits light at a wavelength of 855 nm, the bandwidth being ca. 8.5 GHz. Only S_{21} is being measured. Electrical and electro-optical RF characterizations are performed on chip using GSG RF probes (Cascade Microtech. probes) and a HP 85107A Network analyzer system.

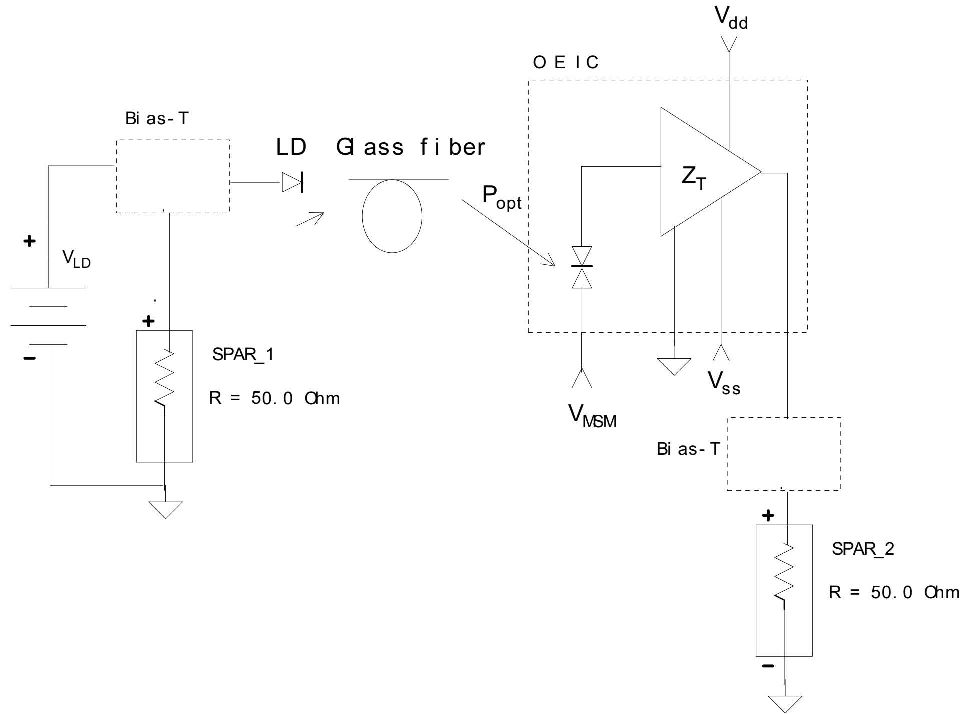


Figure 4.20: Circuit diagram for measurements of the opto-electrical HF characteristics of the integrated photoreceiver. The measured response comprises the total path as follows: laser diode, optical path (lens and glass fibre), MSM detector and transimpedance amplifier, microwave output probe.

Standard receivers

A standard receiver fabricated on pHEMT1 is measured in Fig. 4.21, the bias voltage on the MSM being either 0 V or 5 V. This proves, that a bias voltage of at least 5 V is necessary, otherwise the detector produces only leakage current, which is comparable to the noise level of the system.

Figure 4.22 shows the measured and simulated opto-electrical characteristics of standard receivers (i.e. gate length $\sim$ 1 μm) fabricated on pHEMT1. Two different circuits are measured; one with a large area MSM PD (A = 101 x 108 μm^2), the other with a smaller area (A = 21 x 28 μm^2). For both receivers the MSM PD has the dimensions $w = s = 1$ μm. The measurement is done by illuminating the MSM PD with a laser beam at $\lambda = 855$ nm.

In the simulation an AC simulation is done according to the circuit diagram shown in Fig. 4.20. Now, however, the S-parameter ports are removed and a 50 Ω load is added to the output. The output voltage V_{out} is simulated over the frequency range from 50 MHz to 10.05 GHz. The transistor parameters used in the EEHEMT1-model are listed in Fig. D.1. The MSM detector is modelled as presented in Fig. 2.20, i.e. a variable current source connected in parallel to C_{msm} and R_{dark}. A small series resistance R_s is included also to account for the finger electrode resistance. Values used in the fitting are as follows: $R_{dark} = 50$ kΩ, $R_s = 3$ Ω, $R_f = 1000$ Ω, $C_f = 1$ fF, $V_{dd} = 3.5$ V, $V_{ss} = -2$ V. For the MSM capacitances theoretical 2D conformal mapping values are used: C_{msm}(small area) = 20 fF and C_{msm}(large area) = 340 fF. The AC current generated from the MSM PD is 13 μA and 40 μA for the small and large area detector, respectively.

The transimpedance is calculated by dividing the simulated output voltage by the current generated from the MSM PD. For the small area MSM-circuit: Z_T = 5.84 mV / 13 μA = 449 Ω, for the large area MSM-circuit: Z_T = 18.04 mV / 40 μA = 451 Ω.

The plot 4.22 shows that the smaller area MSM-circuit has, as expected, a lower dB-level, i.e. a lower output voltage. However, since the capacitance for the smaller area MSM is less, the 3 dB bandwidth of this circuit is shifted to a higher frequency, i.e. from 2.59 GHz (large MSM) up to 4.86 GHz (small MSM). The discrepancy between measurement and simulation at low and high frequencies is due to the

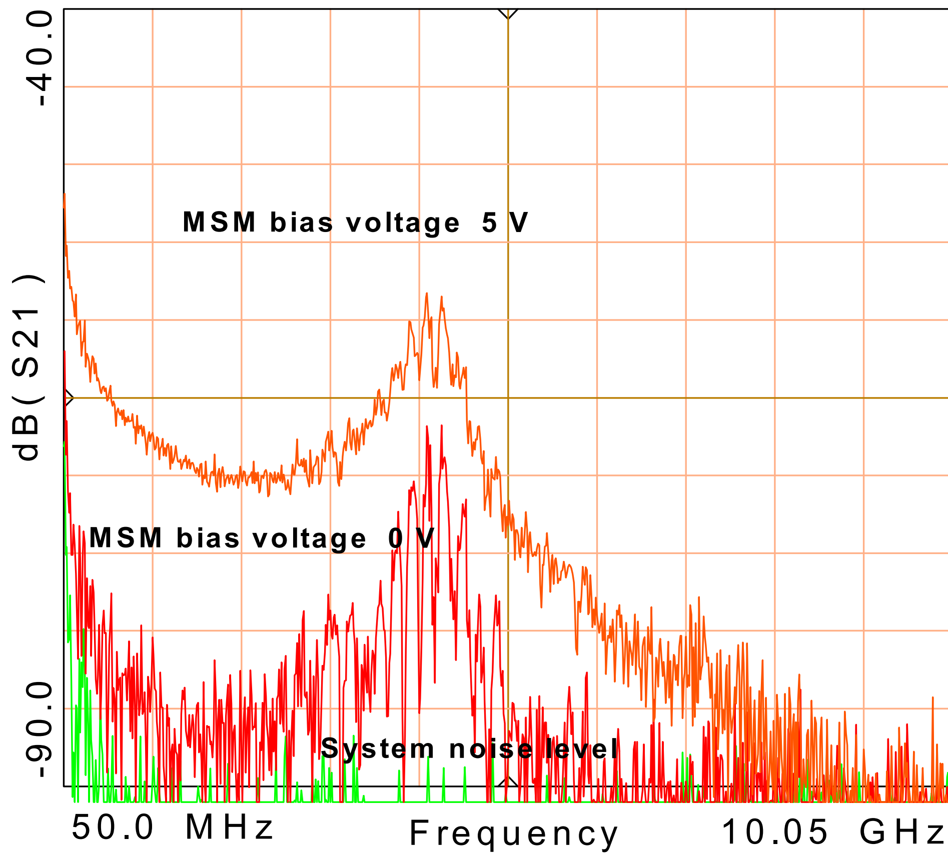


Figure 4.21: OE response for a standard receiver fabricated on pHEMT1 measured at λ = 855 nm (l_g = 1 μm, l_{DS} = 4 μm, MSM PD: A = 11 x 18 μm^2, $s = w$ = 1 μm). The MSM is biased at 0 V and 5 V. V_{dd} = 4 V and V_{ss} = -2 V.

laser diode characteristics used in the measurement. The laser diode has a higher modulation efficiency at low frequencies, and starts to fall off above 7.5 GHz.

The simulated curve for the smaller MSM-circuit extends to a 3 dB frequency of 5.35 GHz. This higher frequency compared to that obtained in the measurement suggests that the 20 fF finger capacitance value used is an underestimation. In fact, measurements on separate same size MSMs obtained values in the range of 35 fF. A circuit simulation using C_{msm} = 35 fF gave a better fit, and a 3 dB bandwidth of 4.80 GHz at -47.3 dB.

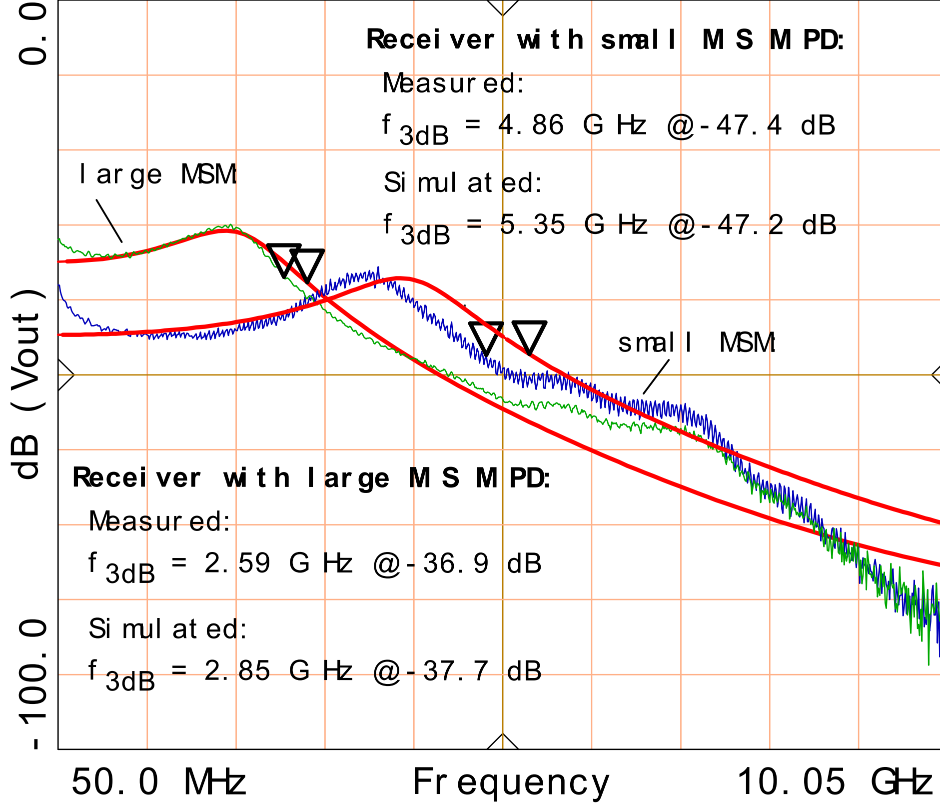


Figure 4.22: OE response for standard receivers fabricated on pHEMT1 with different sizes for the MSM PD. Simulated response is shown by the solid line. l_g = 1 μm, l_{DS} = 4 μm, MSM(large): A = 101 x 108 μm^2, MSM(small): A = 21 x 28 μm^2, for both s = 1 μm, w = 1 μm. V_{dd} = 3.5 V, V_{ss} = -2 V, V_{msm} = 2 V. See Table 4.4 for details about measurement conditions.

Table 4.4: OE measurement for receiver pHEMT1: V_{dd} = 3.5 V, V_{ss} = -2 V, V_{msm} = 2 V, see Fig. 4.22.

pHEMT1	I_{dd} [mA]	I_{ss} [mA]	I_{msm} [mA]	V_{out} [V]	$\lvert S_{21}\rvert$ [dB]	f_{3dB} [GHz]
Small MSM (21 x 28)	23.4	-20.0	0.144	-0.276	-47.4	4.86
Large MSM (101 x 108)	24.6	-20.6	0.186	-0.403	-36.9	2.59

E-beam receivers

The opto-electronic response at λ = 855 nm is measured for e-beam circuits fabricated on pHEMT2, Figs. 4.23 (referred to as circuit 1) and 4.24 (referred to as circuit 2). The receiver dimensions are the same for the two circuits, the difference being in the position on the wafer. Standard gates are used: l_g = 1.1 μm, l_{DS} = 3.9 μm, and e-beam gates (in the amplification stage): l_g = 0.2 μm, l_{DS} = 1.3 μm, MSM: A = 11 x 22 μm^2, s = 0.3 μm, w = 0.2 μm. Figs. 4.23 (a), 4.24 (a) plot dB(S_{21}) vs. frequency for the receiver, and for an MSM PD on S.I. GaAs (indicated as 'detector path', A = 100 x 100 μm^2, $w = s$ = 2 μm, V = 5 V). Figs. 4.23 (b), 4.24 (b) show the response of the receiver relative to the MSM PD response. The straight line corresponds to the detector, indicated as 'detector path' (i.e. MSM response normalized to its own response). There is a difference in height of the fiber end above the MSM surface and the receiver which leads to a difference in optical power supplied to both samples. In addition, since the receiver and the MSM sample have different thicknesses, the figures do not represent the exact gain of the receiver compared to a single MSM, but rather show the shape of the response vs. frequency.

The reason for measuring the single MSM PD along with the receiver is to obtain knowledge of the laser diode bandwidth. Since the MSM is assumed to exhibit a bandwidth of several tens of GHz, the bandwidth of the laser is read from this single MSM measurement.

The laser current was 160 mA, and the case temperature of the laser module -3 °C and -9 °C for circuit 1 and 2, respectively. It is also emphasized that the responses plotted in Figs. 4.23 and 4.24 are not comparable in absolute sense, since the glass fiber probe was almost touching the sample with circuit 2, and this distance was larger for circuit 1. The exact measurement conditions, and the electrical (-3 dB) as well as optical bandwidth (-6 dB) are recorded in Table 4.5. The bandwidth data are obtained with the 0-dB reference level taken at 2 GHz. The optical measurements demonstrate lower bandwidth than the electrical characterizations, which may partly be explained by stray light to transistors resulting in deterioration of the amplifier behaviour.

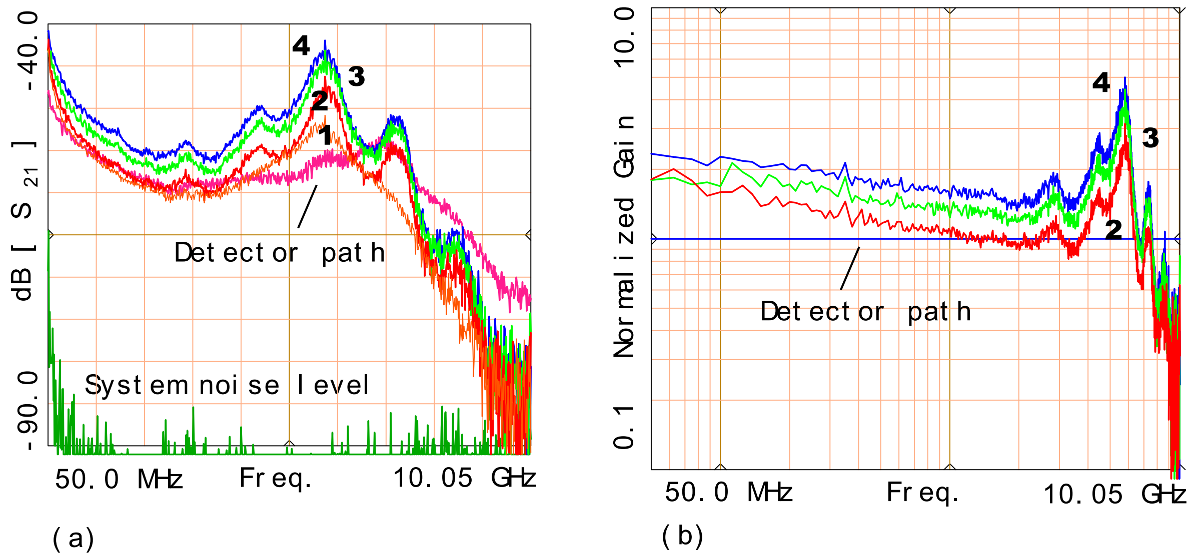


Figure 4.23: OE response measured at λ = 855 nm for an e-beam receiver on pHEMT2 (Circuit 1). (a) dB (S_{21}), also is shown the response for a separate MSM PD. (b) Normalized Gain = Receiver $|S_{21}|$ relative to MSM PD response. Numbers 1 - 4 refer to different measurement conditions, see Table 4.5.

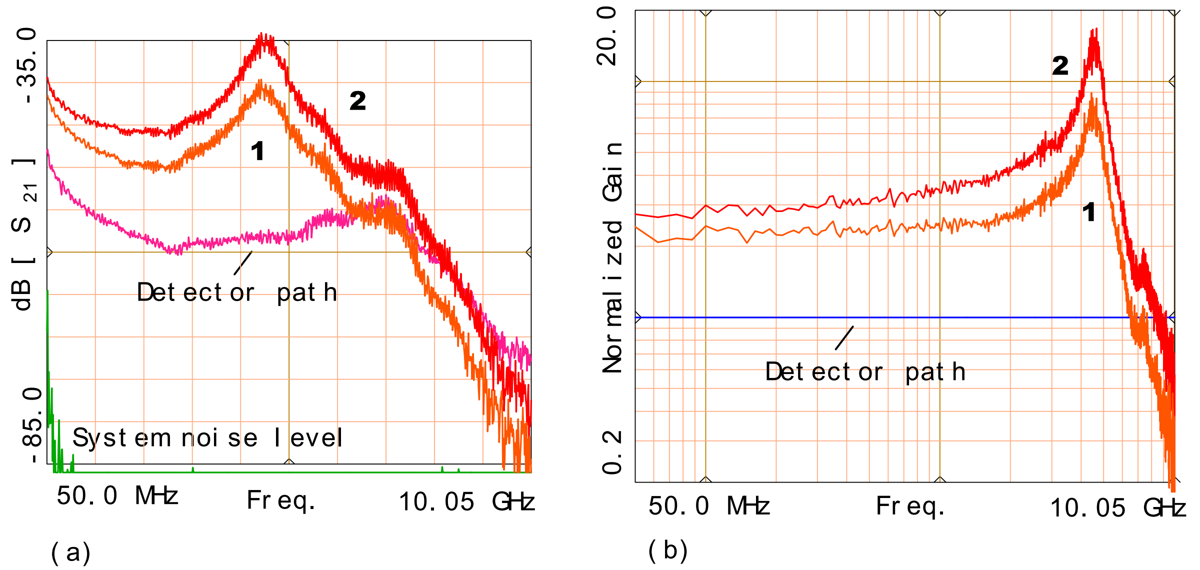


Figure 4.24: OE response measured at $\lambda = 855$ nm for an e-beam receiver on pHEMT2 (Circuit 2). (a) dB (S_{21}), also is shown the response for a separate MSM PD. (b) Normalized Gain = Receiver $|S_{21}|$ relative to MSM PD response. Numbers 1 and 2 refer to different measurement conditions, see Table 4.5.

Literature comparison

In Table 4.6, there is a comparison of results from the literature for photoreceivers realized on different material systems, and operation wavelengths. The receiver fabricated in this work is compatible with the other published results, considering the material system (GaAs instead of InP), and the transistor dimensions. The level-shift and buffer-stage transistors were defined optically ($l_g \sim 1.1$ μm), whereas only the amplification stage gates were written by e-beam (submicron gate length).

Table 4.5: OE measurement for e-beam receivers on pHEMT2 (see Figs. 4.23, 4.24).

pHEMT2	V_{dd} [V]	I_{dd} [mA]	V_{ss} [V]	I_{ss} [mA]	V_{out} [V]	V_{msm} [V]	I_{msm} (DC) [mA]	f_{3dB}/f_{6dB} [GHz]
Circ. 1 / 1	4.75	49.3	-3.0	- 42.1	0.28	2.0	0.192	7.29/7.64
Circ. 1 / 2	4.85	49.1	-3.0	-42.1	0.26	2.0	0.229	7.63/7.74
Circ. 1 / 3	4.85	49.1	-3.0	- 42.1	0.20	2.5	0.313	7.69/7.81
Circ. 1 / 4	4.85	49.1	-3.0	-42.1	0.15	3.0	0.387	7.64/7.74
Circ. 2 / 1	4.55	47.6	-2.58	- 39.4	- 0.17	2.0	0.108	6.0-6.15/7.40
Circ. 2 / 2	4.58	48.6	-2.53	- 39.8	- 0.19	3.0	0.157	6.1-6.7/7.54

Table 4.6: Comparison of different receivers from literature.

Receiver type, technology Material (operation λ)	l_g [μm]	f_t/f_{max} [GHz]	Z_T or Responsivity	f_{3dB} [GHz]	$Z_T f_{3dB}$ [Ω THz]	Data rate [Gbit/s]	Year/ ref.
• pHEMT/MSM PD InGaAs/GaAs (0.855 μm)	1	22/43	1 kΩ	6.5	6.5		1997/[27]
• pHEMT/PIN PD InGaAs/InP (1.55 μm)	0.2		407 V/W	8.3		12	1998/[147]
• HEMT/PIN PD InGaAs/InP (1.55 μm)	0.12	110/	6 kΩ	2.5	0.15	7	1998/[148]
• MODFET/MSM PD InGaAs/GaAs (0.85 μm)	0.25	66/70	300 Ω	10.0	3		1993/[149]
• HEMT/MSM PD InGaAs/InP (1.55 μm)	0.26	58/120	175 V/W	7.0			1998/[150]
• HEMT/PIN PD InGaAs/InP (1.55 μm)	0.3	90/200	39 dBΩ	37		50	1999/[151]
• HEMT/MSM PD InGaAs/InP (1.3 μm)	0.5	45/85	100 V/W	7.0		10	1996/[152]
• HEMT/MSM PD AlGaAs/GaAs (1.55 μm)	0.2	60/	12 kΩ	17	204	20	1998/[153]
• HEMT/MSM PD AlGaAs/GaAs (1.55 μm)	0.2	60/	14 kΩ	16	224	20	1998/[154]
• HEMT/PIN PD InGaAs/InP (1.55 μm)	0.1, 0.8		160 - 890 V/W	9 - 10		10	2000/[155]
• pHEMT/MSM PD passive feedback InGaAs/GaAs (0.855 μm)	0.35, 1	59/127	1.2 kΩ	9.5	11.5		2001/ this work
• pHEMT/MSM PD active feedback InGaAs/GaAs (0.855 μm)	0.2, 1	86/67	422 Ω	10.1	4.3		2001/ this work

Chapter 5

Discussion

5.1 Conclusions and Evaluation of Results

Two different electronic devices were investigated in this work, the MSM diode (fabricated both on SOI-structures and on S.I. GaAs) and the pseudomorphic InGaAs-channel HEMT. Furthermore, the MSM PD was monolithically integrated with a GaAs-based transimpedance amplifier, comprising a complete photoreceiver circuit. The main goal was to develop the processing technology using e-beam exposure in order to achieve submicron devices with good frequency performance.

1. **MSM PDs**

   • The results suggest that the planar Schottky barrier MSM diode is suitable for picosecond optoelectronics, and for monolithic integration with high-speed FET amplification stages. The fast response time is mainly attributed to the interdigitated electrode geometry, i.e. small intrinsic capacitance per area and series resistance resulting in low RC times, and small electrode separation leading to fast carrier transit times. In addition, the planarity of the device makes the fabrication simple, fast and reproducible.

   • MSM PDs have been fabricated on SOI-substrates with different top Si-layer thicknesses by using optical lithography, and on S.I. GaAs applying e-beam direct writing. DC characterization exhibits for SOI-based diodes a low detector dark current (11 pA at 10 V) and a saturation capacitance of 0.48 pF. The low leakage current was achieved by growing a 100 nm thick isolation layer underneath the contact pads, and a SiN passivation layer on top of the finger structure.

   For submicron GaAs-based detectors the dark current was measured to be 67 pA at 2 V, corresponding to a dark current density of only 18 μA/cm^2. The capacitance of GaAs MSM PDs with nanoscale finger dimensions was measured to be 32, 50, 85 and 125 fF for areas of 10 x 35, 15 x 35, 25 x 35 and 35 x 35 μm^2, respectively. The electrical parasitics extracted from S-parameter measurements agreed very well with these experimental results.

   • The transient measurements indicate that high speed performance can be achieved for SOI-structures in the infrared region, depending on the active top Si layer thickness. The advantage of implying SOI diodes is the fact that at long wavelengths the active layer can be made much smaller than the light penetration depth, causing the detector's speed to be independent of the light wavelength. At a wavelength of $\lambda = 800$ nm the measurement setup limited rise time was 64 ps (5.5 GHz), 77 ps (4.5 GHz) and 198 ps (1.8 GHz) for detectors with top layer thicknesses of 0.5 μm, 1 μm and 4 μm, respectively. The submicron MSM on S.I. GaAs (finger spacing 0.3 μm, finger width 0.2 μm) exhibited a rise time of 18 ps (19.4 GHz), which was the resolution limit of the measurement equipment. In SOI structures the tail due to slow mobility holes was effectively reduced, attributed to the buried isolating oxide layer underneath the top Si layer. For GaAs-based detectors the full recovery time of the pulse extended beyond 0.2 ns.

   • Theoretical investigation showed, that for SOI detectors with finger spacings above 1 μm the bandwidth is limited by the transit time of the charge carriers, whereas for nanoscale GaAs detectors the limitation comes from the RC-time constant.

• From the experiments done on SOI MSM PDs it can be concluded that the thin top Si-layer (ranging from 0.2 μm up to 4 μm) confines the photogenerated carriers very effectively into this area, thus leading to fast carrier collection time. However, a severe trade-off exists between the achieved high speed and the sensitivity of the detector. Utilizing such thin top Si-layers, only a fraction of the incident light is absorbed in the active area, causing a responsivity in the mA/W range. Values of 3, 7, 24, 43 and 93 mA/W were achieved for Si top layer thicknesses of 0.2, 0.5, 1, 2 and 4 μm, respectively (bias voltage 6 V, λ = 800 nm.) For S.I. GaAs the measured responsivity was higher and according to theory, $\sim$ 0.25 A/W (bias voltage 3 V, λ = 780 nm).

• DC gain was observed for both detector-types, most probably attributed to hole trapping in surface/interface states close to the cathode, leading to subsequent electron injection from the metal into the semiconductor, either by tunneling or by thermionic-emission.

• Both SOI- and GaAs- MSM PDs exhibited good DC and transient characteristics. However, a trade-off must be made according to requirements of a particular application, i.e. high-speed performance versus responsivity.

2. **pHEMTs**

• The experiments done on pHEMTs resulted in good DC and HF characteristics, and met the design goals as defined at the beginning of the project. The e-beam lithography was developed using different PMMA resist stacks, and both a triangular shape and a mushroom shape gate technology were optimized. Lift-off was successful for resist thicknesses of 580 nm (triangular shape, 2-layer resist stack), 680 nm (mushroom shape, 2-layer resist stack) and 740 nm (mushroom shape, 3-layer resist stack), and subsequent metal depositions with thicknesses of 300 nm, 400 nm ad 400 nm, respectively. Considering the ratio of resist to the metal, this is a remarkable result.

• Several gate recess etching experiments were performed, utilizing ammonia/H_2O2 and CA/H_2O_2-based solutions. The results suggest, that both etchants are suitable for GaAs/AlGaAs-systems with an AlAs etch stop layer.

• The extrinsic transconductance was observed to increase with decreasing gate length, as expected from the theory: 539 mS/mm and 403 mS/mm were measured for pHEMTs with l_g of 0.34 μm and 0.61 μm, respectively (W = 40 μm). The transistors with decreasing gate length showed a larger output conductance, thus having a smaller DC voltage gain A_o compared to devices with larger gate lengths. The maximum voltage gain for a transistor with l_g = 0.85 μm (W = 160 μm) exhibited g_m = 56 mS, g_o = 0.9 mS, hence A_o = 61.

• The cut-off frequency was proven to scale with the gate length. A triangular shaped transistor with a gate length of 0.19 μm demonstrated an extrinsic f_t/f_{max} of 86 GHz/67 GHz in contrast to 42 GHz/78 GHz for a transistor with l_g = 0.51 μm. A mushroom-shaped gate pHEMT (top part 0.4 μm, footprint $\sim$ 0.2 μm) obtained frequencies of 75 GHz/102 GHz.

3. **Monolithically integrated MSM PD/pHEMT photoreceiver**

• Receivers were fabricated both optically, and using combination of optical and e-beam lithography (referred to as e-beam circuits). The processing of the e-beam circuits was complex due to two subsequent gate alignment and gate recess etching steps needed; i.e. to define the optical (standard) gates and the submicron gates. Nevertheless, good performance, and bandwidths comparable with results from literature could be achieved.

• For a standard receiver with gate lengths of 1 μm a 3 dB bandwidth of 8.4 GHz (Z_T = 1.3 kΩ) was measured. An e-beam receiver (the amplification stage consisting of submicron transistors with gate lengths of 0.25 μm, and the level shift and buffer stage consisting of transistors with a gate length of 1 μm) performed a 3 dB bandwidth of 9.5 GHz (Z_T = 1.2 kΩ). The receivers fabricated on pHEMT2-layer structures demonstrated superior characteristics compared to those fabricated on pHEMT1 and pHEMT3. Simulations done with MDS were in good agreement with the experimental results.

• The results for the discrete devices as well as for the photoreceiver are comparable with results recorded in literature. Simulations confirmed, that realizing a receiver with the same mask except replacing all standard 1 μm-gate transistors with submicron gates would increase the receiver bandwidth up to $\sim$ 17 GHz. This proves the significance of utilizing submicron technology.

5.2 Recommendations

In future work a circuit consisting of solely submicron transistors could be fabricated. This would in great degree facilitate the processing technology, because only one gate recess step would be required. In the circuits fabricated in this work, first a gate recess was performed for the standard gates, and a second gate recess etch for the e-beam written gates (amplification stage gates). Considering how critical the gate definition is for the performance of the whole receiver (threshold voltage shift, frequency characteristics etc.) the gate etching should be done only once. According to simulations performed in Section 4.5 a circuit consisting of submicron transistors yields an electrical 3 dB bandwidth of 16.9 GHz, which means that the optical bandwidth is in excess of this value. Attention should be drawn to avoiding the high frequency gain peaking, i.e. by means of optimizing the MSM capacitance/resistance and feedback resistance in such a way that the response is balanced. An extra feedback capacitance should be added in parallel to the feedback resistance in order to get the compensated response, or the shape of the feedback resistance R_f could be redesigned.

Totally new receiver design could be realized with special optimization drawn to the interconnections in the circuit. Using coplanar lines instead of microstrips the performance could probably be enhanced. In addition, in order to tune the transimpedance and 3 dB bandwidth a circuit with active feedback transistor should be applied instead of a fixed feedback resistor. The results for standard receivers (l_g = 1.1 μm) with active feedback showed higher bandwidth (8.7 - 10.1 GHz for Z_T = 344 - 422 Ω) compared to passive feedback receivers with same transistor dimensions (7.9 GHz for Z_T = 1.2 kΩ). However, it is noticed, that the gain-bandwidth product for the active feedback receivers is less, 3 - 4.3 ΩTHz, than that of 9.5 ΩTHz for the passive receiver. Therefore, designing a receiver with an active feedback with combination of e-beam fabricated submicron transistors attention should be drawn to optimizing the transimpedance also.

In the transistor design some changes could be performed also. Measurements performed on common-source pHEMT transistors showed that these transistors have a high level of amplification at low frequencies, but a fast decay of the response, thus low amplification at high frequency and a slightly lower 3 dB bandwidth than 'standard' common-gate transistors. The opposite characteristic was observed for common-gate transistors, i.e. low level of amplification at low frequencies, but a high gain peak at a higher frequency, and larger 3 dB bandwidth. Therefore, utilizing a common-gate transistor in combination with a common-source transistor would be a good chance to enhance both the amplification over the whole frequency range, and the 3 dB bandwidth.

Appendix A

Layer Structures

A.1 pHEMT

Tables A.1 and A.2 show the used pseudomorphic-HEMT layer structures.

Table A.1: Layer structures for pHEMT1 and pHEMT2 (with GaAs buffer layer thicknesses of 0.5 μm and 1 μm, respectively). An AlGaAs/GaAs SL is grown on the S.I. GaAs substrate.

Material	Layer type	Thickness [nm]	n-Doping [cm^{-3}]
GaAs	capping	20	$2 \cdot 10^{18}$
AlAs	etch-stop	3	$2.5 \cdot 10^{18}$
$Al_{0.23}Ga_{0.77}As$	Schottky	30	-
Si - delta			$5 \cdot 10^{12}$ cm^{-2}
$Al_{0.23}Ga_{0.77}As$	spacer	3	-
$In_{0.20}Ga_{0.80}As$	channel (strained)	12	-
GaAs	buffer	50	-
AlAs	etch-stop	3	-
GaAs	buffer	500 / 1000	-
$Al_{0.5}Ga_{0.5}As$	super lattice	10 $\times$ 10	-
GaAs	super lattice	10 $\times$ 10	-
GaAs	buffer	30	-
GaAs	buffer	20	-
S.I. GaAs	(100) substrate	625 μm	-

Table A.2: Layer structure for pHEMT3 (GaAs buffer layer with a thickness of 0.5 μm). An AlAs/GaAs DBR-type SL is grown on the S.I. GaAs substrate.

Material	Layer type	Thickness [nm]	n-Doping [cm^{-3}]
GaAs	capping	20	$2 \cdot 10^{18}$
AlAs	etch-stop	3	$2.5 \cdot 10^{18}$
$Al_{0.23}Ga_{0.77}As$	Schottky	30	-
Si - delta			$5 \cdot 10^{12}$ cm^{-2}
$Al_{0.23}Ga_{0.77}As$	spacer	3	-
$In_{0.20}Ga_{0.80}As$	channel (strained)	12	-
GaAs	buffer	50	-
AlAs	etch-stop	3	-
GaAs	buffer	500	-
GaAs	super lattice	6×57.7	-
AlAs	super lattice	6×70.2	-
GaAs	buffer	30	-
GaAs	buffer	20	-
S.I. GaAs	(100) substrate	625 μm	-

Appendix B

Fabrication Overview

B.1 Processing Steps for MSM PDs

• Metal fingers and metal pad contacts: photolithography (Table B.3)

Table B.1: MSM fabrication for SOI MSM detectors.

• Metal fingers: e-beam lithography (Table B.4)
• Metal pad contacts: photolithography (Table B.5)

Table B.2: MSM fabrication for S.I. GaAs MSM detectors.

• Cleaning	T [° C]	time [min:sec]
Rinsing in acetone		5:00
Rinsing in isopropanol		5:00
Rinsing in D.I. H_2O		1:00
Drying with N_2-blow		
Baking	120	30:00
• Growth of isolation layer and definition of the active area	T [°C]	time [min:sec]
Wet-oxide, thickness ~ 100 nm		120:00
Vapor coating of HDMS (to improve resist adhesion)		10:00
Resist (AZ 5214E) coating, spinning speed: 4000 rpm		0:25
Prebake	90	20:00
Mask exposure (active MSM area); UV 300		0:08
Development with AZ 400K : H_2O (1:4)	21	1:00
Rinsing in D.I. H_2O		2:00
Drying with N_2-blow		
Wet etching in BHF (Sioetch)		1:30
Resist removal in acetone / isopropanol		5:00
Rinsing in D.I. H_2O		2:00
Baking	120	30:00
• Definition of MSM fingers and contact pads	T [°C]	time [min:sec]
Vapor coating of HDMS (to improve resist adhesion)		10:00
Resist (AZ 5214E) coating, spinning speed: 4000 rpm		0:25
Prebake	90	20:00
Mask exposure (MSM fingers and pads), UV 300		0:08
Development with AZ 400K : H_2O (1:4)	21	1:00
• Metal Deposition	T [°C]	time [min:sec]
p-type SOI: E-beam evaporation Ti/Au = 50/100 nm or 50/120 nm		
n-type bulk Si/SOI: Thermal evaporation of Al = 90 nm / 120 nm		
Lift-off in acetone		10:00
• Growth of ARC layer	T [°C]	time [min:sec]
PECVD, Si_3N_4 thickness ~ 100 nm	200	8:00
• Reversal bake	T [°C]	time [min:sec]
Vapor coating of HDMS (to improve resist adhesion)		10:00
Resist (AZ 5214E) coating, spinning speed: 4000 rpm		0:25
Prebake	90	20:00
Mask exposure (active MSM area); UV 300		0:06
Waiting		20:00
Baking	120	15:00
Flood exposure (soft contact); UV 300	21	0:20
Development with AZ 400K : H_2O (1:4)		2:30
• RIE etching	Power [W]	time [min:sec]
SF_6, 5 sccm, 17 mTorr, etch speed 15 nm/min	50	7:00
Resist removal in acetone / isopropanol		5:00
Rinsing in D.I. H_2O		2:00
Drying with N_2-blow		

Table B.3: SOI-detectors using optical lithography.

• **Cleaning**	T [° C]	time [min:sec]
NH_3(25%) : H_2O (1:10)	20	1:00
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
Rinsing in acetone		1:00
Rinsing in isopropanol		1:00
Drying with N_2-blow		
• **E – beam lithography**	T [°C]	time [min:sec]
Resist coating		
- 1-layer PMMA: 495KA4		
rpm: 2000. Thickness: 200 nm		0:30
- 3-layer PMMA: 495KA4/50K05/495KA4		
rpm: 2000/1500/2000. Thickness: 200/180/200 nm → 580 nm		0:30
Baking for 1-layer	175	60:00
Baking for 3-layer-system (inbetween layers)	175	30:00
Electron beam writing: 20 kV, dose 160 - 180 $\mu C/cm^2$		
Development with MIBK:isopropanol (1:3)	22	0:30
Stopping in isopropanol		0:15
• **RIE etching for clearing resist traces**	Power [W]	time [min:sec]
O_2-plasma: 100 mTorr, DC-bias 100 - 115 V,	20	0:30
temperature of plate T = 20 ° C		
→ Resist thinning: 25 - 45 nm		
• **Metal Deposition**	T [°C]	time [min:sec]
For 1-layer: E-beam evaporation of Ti/Au = 30/40 nm		
For 3-layer: E-beam evaporation of Ti/Au = 50/250 nm		
Lift-off in acetone		10:00

Table B.4: Metal-finger formation using e-beam for MSM detectors on S.I. GaAs.

• **Cleaning**	T [° C]	time [min:sec]
Rinsing in acetone		1:00
Rinsing in isopropanol		1:00
Drying with N_2-blow		
• **Photolithography**	T [°C]	time [min:sec]
Resist (AZ 5214) coating, spinning speed: 5000 rpm		0:30
Prebake (softbake)	95	5:00
Flood exposure, UV 300		0:02
Reversal bake	105	5:00
Mask exposure (Interconnect), UV 300		0:45
Development with AZ:H_2O (1:1)	21	1:15
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
• **Metal Deposition**	T [°C]	time [min:sec]
Evaporation of Ti/Au = 50/200 nm		
Lift-off in acetone		10:00

Table B.5: Metal-pad formation for MSM detectors on S.I. GaAs.

B.2 Processing Steps for pHEMTs

• Mesa etch (Table B.7)
• Ohmic contacts (Table B.8)
• Gate: optical and e-beam lithography (Tables B.9, B.10 and B.11)
• Interconnections (Table B.12)

Table B.6: pHEMT fabrication.

• Cleaning	T [° C]	time [min:sec]
NH_3(25%) : H_2O (1:10)	20	1:00
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
Rinsing in acetone		1:00
Rinsing in isopropanol		1:00
Drying with N_2-blow		
• Photolithography	T [°C]	time [min:sec]
Resist (S 1805) coating, 3000 rpm		0:30
Prebake (softbake)	95	5:00
Mask exposure (Mesa); UV 300		0:30
Postbake	105	5:00
Development with MP 2401 : H_2O (1:10)	21	1:00
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
Hardbake	105	10:00
• Non – selective wet etching	T [°C]	time [min:sec]
H_2SO_4 : H_2O_2 : H_2O (1:1:6), etch speed 1.4 nm/sec	20	1:00
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
• Resist removal	T [°C]	time [min:sec]
Spraying with acetone		2:00
Spraying with isopropanol		2:00
Drying with N_2-blow		

Table B.7: Mesa definition.

• **Cleaning**	T [° C]	time [min:sec]
NH_3(25%) : H_2O (1:10)	20	1:00
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
Rinsing in acetone		1:00
Rinsing in isopropanol		1:00
Drying with N_2-blow		
• **Photolithography**	T [°C]	time [min:sec]
Resist (AZ 5214) coating, 5000 rpm		0:30
Prebake (softbake)	95	5:00
Flood exposure ; UV 300		0:02
Reversal bake	105	5:00
Mask exposure (Ohmic); UV 300		0:45
Development with AZ:H_2O (1:1)	21	0:40
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
• **Surface de − oxidation before evaporation**	T [°C]	time [min:sec]
NH_3(25%) : H_2O (1:10)	20	0:30
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
• **Metal Deposition**	T [°C]	time [min:sec]
Evaporation of Ge/Ni/Au = 20/15/150 nm		
Lift-off in acetone		10:00
• **Rapid Thermal Annealing (RTA)**	T [°C]	time [min:sec]
Temperature ramp profile:	400	0:30
22 → 100 °C in 45 sec		
100 → 400 °C in 10 sec		
30 sec constant at 400 °C		
400 → 100 °C in 2 min 30 sec		
100 → 60 °C in 1 min 30 sec		

Table B.8: Ohmic contacts.

• **Cleaning**	T [° C]	time [min:sec]
NH_3(25%) : H_2O (1:10)	20	1:00
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
Rinsing in acetone		1:00
Rinsing in isopropanol		1:00
Drying with N_2-blow		
• **Optical lithography**	T [°C]	time [min:sec]
Resist (S 1805) coating, 3000 rpm		0:30
Prebake (softbake)	95	5:00
Mask exposure (Gate), UV 300		0:30
Postbake	105	5:00
Development with MP 2401 : H_2O (1:10)	21	0:50
Rinsing in D.I. H_2O (5 MΩ)		2:00
• **Selective GaAs etch**	T [°C]	time [min:sec]
Dip in D.I. H_2O		
NH_3(25%) : H_2O_2, pH 8 adjusted:	21	0:06
(5 drops NH_4OH + 50 ml H_2O_2, etch speed 8 nm/sec)		
Rinsing in D.I. H_2O (5 MΩ)		2:00
• **Selective AlAs etch**	T [°C]	time [min:sec]
Dip in HCl(32%) : H_2O (1:10)	21	0:01
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
• **Surface de − oxidation before evaporation**	T [°C]	time [min:sec]
NH_3(25%) : H_2O (1:10)	20	0:30
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
• **Metal Deposition**	T [°C]	time [min:sec]
Evaporation of Ti/Au = 50/150 nm		
Lift-off in acetone		10:00

Table B.9: Gates using photolithography.

• **Cleaning**	T [° C]	time [min:sec]
Rinsing in acetone		1:00
Rinsing in isopropanol		1:00
Drying with N_2-blow		
• **E – beam lithography**	T [°C]	time [min:sec]
Resist coating		
- 3-layer-PMMA for triangular gates: 495KA4/50K05/495KA4		
rpm: 2000/1500/2000. Thickness: 200/180/200 nm → 580 nm		0:30
- 2-layer-PMMA/MAA for T-gates: MMA(8.5)MAA EL10/950K0.25		
rpm: 2000/2500. Thickness: 550/130 → 680 nm		0:30
- 3-layer-PMMA for T-gates: 50K05/MMA(8.5)MAA EL10/950K0.25		
rpm: 1500/3500/2500. Thickness: 180/430/130 → 740 nm		0:30
Baking (inbetween layers)	175	30:00
Electron beam writing: 20kV, dose depending on layer stack and linewidth		
- 3-layer system (triangular gates): dose 180 - 250 $\mu C/cm^2$		
- 2-layer system (T-gates): dose for SPL 250, for top exp. 80 - 100 $\mu C/cm^2$		
- 3-layer system (T-gates): dose for SPL 260, for top exp. 90 - 110 $\mu C/cm^2$		
Development with MIBK:isopropanol (1:3)	22	0:30
Stopping in isopropanol		0:15
• **RIE etching for clearing resist traces**	Power [W]	time [min:sec]
O_2-plasma: 100 mTorr, DC-bias 100 - 115 V,	20	0:30
temperature of plate T = 20 ° C		
→ Resist thinning: 25 - 45 nm		
• **Wetting before etching**	T [°C]	time [min:sec]
HCl(32%) : H_2O (1:1)	21	0:30
Rinsing in D.I. H_2O (5 MΩ)		2:00
• **Selective GaAs etch**	T [°C]	time [min:sec]
NH_4OH(25%) : H_2O_2, pH 8 adjusted	21	0:06
(5 drops NH_3 + 50 ml H_2O_2, etch speed 8 nm/sec)		
OR CA : H_2O_2 (1:1), etch speed 1.7 nm/sec		00:30 or 0:45
Rinsing in D.I. H_2O (5 MΩ)		2:00
• **Selective AlAs etch**	T [°C]	time [min:sec]
Dip in HCl(32%) : H_2O (1:10)	21	0:01
Rinsing in D.I. H_2O (5 MΩ)		2:00
• **Surface de – oxidation before evaporation**	T [°C]	time [min:sec]
H_3PO_4 : H_2O_2 : H_2O (1:1:200)	20	0:04
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
• **Metal Deposition**	T [°C]	time [min:sec]
Triangular gates: E-beam evaporation of Ti/Au = 50/250 nm		
T-gates: E-beam evaporation of Ti/Au = 50/350 nm		
Lift-off in acetone		10:00

Table B.10: Gates using e-beam lithography.

Linewidth: **Resist stack**	600 nm Dose	400 nm Dose	300 nm Dose	200 nm Dose	160 nm Dose
Triangular 3-layer	180-190	190-200	210-220	225-240	235-250
Mushroom 2-layer	80-90	95-100			
Mushroom 3-layer	90-100	105-110			

Table B.11: Dose $[\frac{\mu C}{cm^2}]$ for achieving different linewidths at 20 kV. Step size = 14 nm. The dose-values for the mushroom-gates, i.e. the T-gates, apply for the top-part exposure (low dose). The dose for the footprint exposure (SPL with high dose) and step size for mushroom-gates are: 250 $\frac{\mu C}{cm^2}$ / 6 nm and 260 $\frac{\mu C}{cm^2}$ / 10 nm for the 2- and 3-layer system, respectively.

• **Cleaning**	T [° C]	time [min:sec]
Rinsing in acetone		1:00
Rinsing in isopropanol		1:00
Drying with N_2-blow		
• **Photolithography**	T [°C]	time [min:sec]
Resist (AZ 5214) coating, 5000 rpm		0:30
Prebake (softbake)	95	5:00
Flood exposure ; UV 300		0:02
Reversal bake	105	5:00
Mask exposure (Interconnections), UV 300		0:45
Development with AZ:H_2O (1:1)	21	1:15
Rinsing in D.I. H_2O (5 MΩ)		2:00
Drying with N_2-blow		
• **Metal Deposition**	T [°C]	time [min:sec]
Normal gates: Evaporation of Ti/Au = 50/200 nm		
Lift-off in acetone		10:00

Table B.12: Interconnections.

Appendix C

Measurements

C.1 Power loss in the pulsed optical beam experiment for GaAs MSM PDs

The path between the DUT (i.e. the MSM PD) and the sampling oscilloscope is composed of the probe head, the bias-T, the cable and the coaxial adapters. In order to estimate the power loss due to the cable assembly (input port: CPW head, output port: 3.5 mm coaxial connector) three separate one-port measurements for three different coaxial load conditions were performed using a calibrated analyzer with only one microwave test probe. This test probe (ANA port 1) is connected to one side of a 1 ps THRU-line on a calibration substrate belonging to the probe station. The other side of this 50 Ω CPW line on the substrate is connected to the probe head of the cable assembly. The free cable end with the coaxial connector, usually connected to the sampling oscilloscope, is in sequence terminated by a 50 Ω load, an open and a short calibration standard from the coaxial calibration set. The reflection coefficient at the input (at the position of the DUT) is then measured for the three above mentioned situations. The relationship between the input reflection Γ_{in} and the reflection of the load Γ_L is given by:

$$\Gamma_{in} = S_{11} + (S_{12}S_{21}\Gamma_L)/(1 - S_{22}\Gamma_L) \ ,$$

where S_{ij} are the four S-parameters of the cable assembly. Applying three different known Γ_L's: a perfect 50 Ω load, an open and a short calibration standard with Γ_L=0, +1, -1, respectively, will result in three measured Γ_{in}'s , here denoted as Γ_{tm} (termination), Γ_{om} (open) and Γ_{sm} (short).

Solving the equations, gives for the cable assembly the product:

$$S_{12}S_{21} = 2\frac{(\Gamma_{\rm tm} - \Gamma_{\rm sm})(\Gamma_{\rm om} - \Gamma_{\rm tm})}{(\Gamma_{\rm om} - \Gamma_{\rm sm})}. \tag{C.1}$$

In the actual situation the reflections of the MSM diode (=source) and the oscilloscope (=load) have to be taken into account. Assuming that $|S_{12}| = |S_{21}|$ and applying Eq. (3.76) with the approximation $\Gamma_s = \Gamma_L = 0$ (reflection coefficient of the MSM diode, input reflection coefficient of the oscilloscope, respectively), Eq. C.1 directly represents the power loss due to the cable assembly. The power loss in dBs is plotted in Fig. C.1. The voltage gain A_v (or voltage attenuation in this case) as defined in Eq. (3.75) (approximating that $\Gamma_L = 0$, i.e. the oscilloscope perfectly matched) is achieved by taking the square root of the absolute value of Eq. (C.1), and using $S_{11} = \Gamma_{tm}$. Thus the voltage loss of the cable becomes: $A_v = \frac{S_{21}}{1+S_{11}} = \frac{S_{21}}{1+\Gamma_{tm}}$.

The power loss is a function of frequency. Therefore, in order to correct the time dependent pulse response Fourier transformation is needed. In the following the steps for correction are described in detail:

- Transformation of the measured transient response into frequency domain.
- Calculation of the correction factor $C(f) = \frac{1}{|S12S21|}$ for each separate frequency (e.g. correction factor at the low frequency of 50 MHz is 1, while at 40.05 GHz it is 10, see Fig. C.1).

• Inverse Fourier transform into pulse domain. As the result of the correction the rising slope of the pulse becomes steeper, and demonstrates the rise time of the MSM detector.

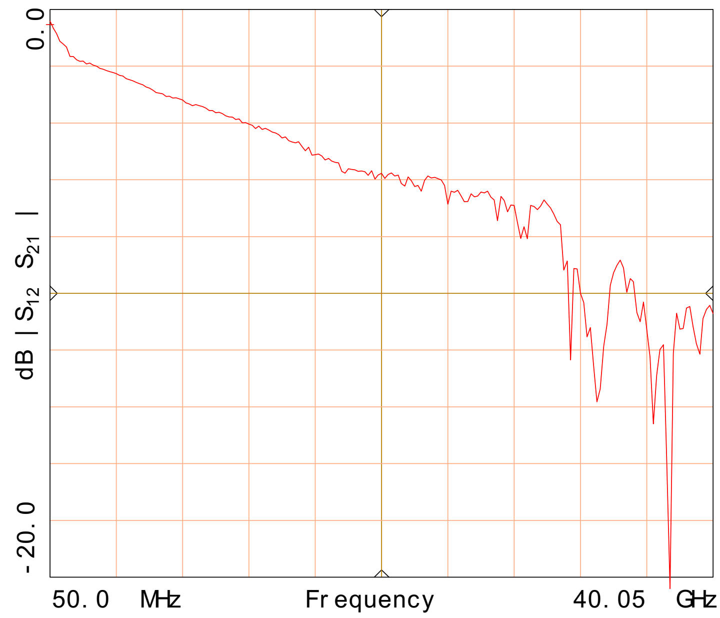


Figure C.1: Losses due to the measurement setup (transient response measurement for submicron GaAs MSM PDs with the Titanium-Sapphire laser.)

Appendix D

Modelling

D.1 EEHEMT1-model Parameters

IC-CAP parameter extraction results using the EEHEMT1-model for a standard and submicron transistor are recorded in Figs. D.1 and D.2, respectively.

* EEHEMT1 MODEL *

IDS model

VTO = -1.032
GAMMA = 0.001
VGO = -0.2928
VCH = 0.02041
GMMAX = 0.02506
VDSO = 1.5
VSAT = 1.001
KAPA = 0.001481
PEFF = 84.55
VTSO = -100
VCO = -0.04639
MU = 0.0001
VBA = 0.5827
VBC = 1.029
DELTGM = 0.01498
ALPHA = 0.155

IDB model

RDB = 1e9
CBS = 1.6e-13
GDBM = 1.573e-6
KDB = 10
VDSM = 100
GMMAXAC = 0.02086
VTOAC = -0.920
GAMMAAC = 0.03781
KAPAAC = 0.07639
PEFFAC = 200
VTSOAC = -100
DELTGMAC = 0.006917

Gate model

IS = 21.21e-12
N = 2
KBK = 0.03
IDSOC = 1.893
VBR = 25
NBR = 2

Parasitics

RS = 3.602
RG = 5.0
RD = 2.205

UGW = 80e-6
NGF = 1

Charge model

C11O = 231.7e-15
C11TH = 44.97e-15
VINFL = -0.4243
DELTGS = 1.089
DELTDS = 0.8348
LAMBDA = 0.047
C12SAT = 13.22e-15
CGDSAT = 48.59e-15
RIS = 13.14
RID = 1e-10
TAU = 5.42213e-12
CDSO = 1e-17

Figure D.1: Parameters extracted with IC-CAP (EEHEMT1-model) for a standard transistor ($l_g = 1$ μm, $W = 80$ μm, T-configuration).

* EEHEMT1 MODEL *

IDS model

VTO = -0.8949
GAMMA = 0.0187
VGO = -0.383
VCH = 0.8607
GMMAX = 0.04950
VDSO = 1.5
VSAT = 0.9176
KAPA = 0.02327
PEFF = 8.014
VTSO = -100
VCO = -0.3218
MU = 0.0001
VBA = 0.5132
VBC = 0.4739
DELTGM = 0.073
ALPHA = 0.2301

IDB model

RDB = 1e9
CBS = 1.6e-13
GDBM = 100e-6
KDB = 10
VDSM = 100
GMMAXAC = 0.04813
VTOAC = -0.8854
GAMMAAC = 0.02410
KAPAAC = 0.01226
PEFFAC = 200
VTSOAC = -100
DELTGMAC = 100e-6

Gate model

IS = 7.801e-15
N = 1.184
KBK = 0.03
IDSOC = 1.893
VBR = 25
NBR = 2

Parasitics

RS = 7.213
RG = 6.5
RD = 1.565
UGW = 80e-6
NGF = 1

Charge model

C11O = 135.2e-15
C11TH = 1e-18
VINFL = -1.647
DELTGS = 3.992
DELTDS = 0.9563
LAMBDA = 0.06736
C12SAT = 22.66e-15
CGDSAT = 24.89e-15
RIS = 0.5663
RID = 1e-10
TAU = 1.5e-12
CDSO = 26.08e-15

Figure D.2: Parameters extracted with IC-CAP (EEHEMT1-model) for a submicron transistor ($l_g = 0.42$ μm, $W = 80$ μm, T-configuration).

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