DEVELOPMENT OF PROCEDURES FOR PERFORMANCE MEASUREMENTS AND LIFETIME TESTING OF THIN FILM PHOTOVOLTAIC DEVICES

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Dissertation for the degree of Doctor of Science in Technology to be presented with due permission for public examination and debate in Auditorium F1 at Helsinki University of Technology (Espoo, Finland) on the 25th of January, 2002, at 12 o'clock noon.

ABSTRACT

In this work single junction a-Si, CdTe and CIGS modules and prototype modules and mini-modules were investigated to reliably be able to characterize these technologies for electrical performance and to find out potential failure mechanisms in accelerated lifetime testing. Thin film modules may increase their share of the market in the future. A-Si modules have been manufactured already for several years and CdTe and CIGS modules are shortly entering the market. However, there is a lack of characterization and testing methods to reliably predict the power output and service lifetime of these technologies.

In this work physics, material and manufacturing issues related to a-Si, CdTe and CIS thin film technologies were reviewed to understand possible failure mechanisms in reliability testing. The calibration measurement procedures and in particular the choice of the reference device for the thin film photovoltaic materials was investigated. The results enable correctly to define if the modules have passed or failed qualification tests and to predict the power output of the module during its lifetime. A-Si, CdTe and CIGS devices were exposed to accelerated lifetime testing. The potential failure mechanisms were investigated by testing them in thermal cycling and humidity freeze cycles, in damp heat, in dry heat and in light soaking. Laser scanning was used to further investigate the observed failure mechanisms after accelerated lifetime testing. The method enables non-destructive determination of position dependent photocurrent throughout the module.

It is suggested to use a reference device with a spectral response similar to that of the sample material to reliably measure the electrical characteristics of a-Si, CdTe and CIGS devices. It is demonstrated that the major cause for failure in accelerated lifetime tests of a-Si, CdTe and CIGS devices is humidity penetration into the module encapsulation. However, the a-Si modules were not very sensitive to humidity penetration. For CdTe prototype modules even small amounts of humidity penetration caused changes in the back contact composition, resulting in electrical degradation. The CIGS prototype mini-modules were not as sensitive to humidity penetration as the CdTe devices were. In case of light soaking the a-Si photovoltaic modules degraded as expected and the degradation stabilized towards the end of the light exposure. In the CdTe, a decrease in maximum power was observed. In the CIGS samples, an increase in maximum power and fill factor was observed which, may however be dependent on material quality. In the laser scanning it is concluded that the method can be used as a powerful non-destructive tool to investigate the short circuit current performance of thin film photovoltaic modules. It is demonstrated that laser scanning can be used to correlate the causes of short circuit current degradation after accelerated lifetime testing with the visual defects observed.

It was shown in this work that the current standards for measurement and testing photovoltaic devices may not necessarily be applied as such, especially for CdTe and CIGS thin film technologies. The results also demonstrate that it is important to design proper and reliable encapsulation to increase the service lifetime of the thin film modules.

PREFACE

The work reported in this dissertation has been done over a period of three years from 1997 to 2000 at the European Commission Joint Research Center in Ispra, Italy in the Renewable Energies unit. Most of the work was carried out for the European Commission project ANTHEM. I would like to gratefully acknowledge the European Commission for financing my stay in Ispra.

I would like to thank my colleagues at JRC ESTI for all the help, discussions and sharing of knowledge. I would especially like to thank Wim Zaaiman for the help in setting up the various measurements and for sharing all the most valuable knowledge that he has in the field of solar cell measurements. I would also like to especially thank Antonella Realini for all the help with the accelerated lifetime testing. Guido Agostinelli deserves special thanks for all the help with the laser scanning system. I would also like to thank Dr. Heinz Ossenbrink and Dr. Ewan Dunlop for supervising my work in Ispra.

This work would never have been completed if I had not the chance to work at the Helsinki University of Technology Technical Physics/Advanced Energy Systems Laboratory for a couple of months in spring 2001. For making that possible and for all the supervision in finishing the work, I would like to express my special thanks to Prof. Peter Lund. I would also like to thank Fortum for giving me the chance to concentrate on finishing this dissertation.

Finally, I would like to express my deepest gratitude to my husband Martti. He has been supporting me through all the good and bad times that the work with this dissertation has involved. He also endured for three years the separation of thousands of kilometers that we had between us.

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1. INTRODUCTION

1.1   Current status of photovoltaics

The photovoltaic industry growth rate was in average 21 % per annum between 1982 and 1997, and during the late 1990's the growth was as high as 40 % per annum. Almost all PV producers have invested in the last 3 years in expansion of production facilities. New start up companies in Europe and in the USA increase world's production capacity additionally. Remarkable is the last years' increase of shipment in Japan with almost 50 % per year. Japan manufactures today about close to half of the world PV market. Totally, the current solar cell production capacity is estimated to be approximately 280 MW_p per year.[1], [2].

The resource potential for photovoltaics is enormous. Apart from conventional energy sources, the efficiency of photovoltaics does not depend on the size of a photovoltaic plant. For that reason photovoltaics can be regarded as a very flexible power source which can be applied in small, decentralized plants as well as in large, central power plants. Since photovoltaics does not generate any emissions during operation, the environmental impacts are mainly associated with emissions generated during production of the photovoltaic technology and the disposal of modules and cells at the end of their useful life.[1], [2].

The most common cell technology is wafer based crystalline silicon. However, the availability of cheap silicon feedstock will be a major barrier for a further cost reduction. Thus, photovoltaic technology may be on the verge of a major transition from first-generation silicon wafer based technologies to a second-generation thin film product. In 1999, thin film solar cell production accounted for about 13 % of all photovoltaic production. The remaining 84 % of the production is evenly distributed between single-crystalline and multi-crystalline silicon technologies. Other crystalline technologies such as ribbon growth or thin silicon films contributed with slightly more than 3 %. The main barriers of thin film technologies, which need to be overcome through are the bad image from the first generation amorphous silicon modules, the relatively low efficiency compared to crystalline technologies, toxicity of materials in production and disposal, and expected lifetime. All five problems have to be addressed simultaneously if thin film technology is to take a major share of the growing market.[1], [3], [2], [4].

1.2   Thin film solar cells

Thin film technologies hold considerable promise for a substantial reduction of the manufacturing costs of solar cells due to the reduction of material costs and the deposition on large area substrates [5], [6], [7], [8], [9]. The thin film technologies for photovoltaic applications include a-Si:H alloys, CdTe, Cu(In,Ga)Se$_2$ (CIGS), poly-Si, μc-Si/Poly-Si and dye/TiO$_2$. The most advanced technologies are a-Si-alloys, CdTe and CIGS [6], [5].

Thin films for solar cells and modules can be deposited by a variety of different processes that lead to different deposition rates and widely varying material quality. Thin film technology generally provides high production capacity at reduced material consumption and energy input in the fabrication process and integrated module structures with deposition processes which normally are suitable for mass production. The practical efficiency of different thin films becomes the crucial determinant of their competitive potential. It has been estimated that thin films can reach the cost limit of 0.6 €/W$_p$ at a capacity of 60 MW$_p$ per year, whereas crystalline silicon modules can achieve this cost level only at capacities well above 500 MW$_p$ per year.[6], [9].

For a-Si the goal is to reach a stable module efficiency on large areas of 10 %, which represents a tough condition for competitiveness with other thin film options. A major problem of the amorphous silicon technology has been the degradation of the amorphous films and devices under illumination, or the so-called Staebler-Wronski effect. A-Si modules have considerably penetrated the market mainly in the consumer electronics segment rather than in large-scale power generation.[6], [5].

CdTe appears to be an ideal material for thin film solar cells because its energy gap is direct and is 1.45 eV which is ideal for solar energy conversion. Efficiencies of 10-16 % have been obtained for CdTe solar cells depending on the process used. A major issue in the CdTe cell technology is the formation of good ohmic contacts of high stability.[5], [9]. CdTe is at the transition from pilot production to manufacturing. Two ventures are aiming at large scale production of CdTe thin film solar module: BP Solarex is introducing the Apollo® thin film CdTe technology at its Fairfield production plant in California and ANTEC Solar is starting production of CdTe modules in Germany. Both are aiming at a nominal production capacity of 10 MW$_p$ per year. Production of small CdTe modules for consumer products with an output of about 1 MW$_p$ is ongoing at Matsushita Inc. in Japan. If CdTe thin film solar cells are to become a commercially successful product, they have to fulfill the criteria of having a high efficiency of at least 10 to 15 %, to be manufactured at high production speed and with robust processes, to be deposited on cheap substrates with low materials consumption and to reach a long term stability.[9].

The Cu(In,Ga)Se$_2$ (CIGS) have reached record laboratory efficiencies of close to 19 %, larger modules of 30 x 30 cm^2 size have been fabricated and there are announcements to proceed with pilot production. Würth Solar in Germany is building a

pilot manufacturing line for CIGS thin film modules with the aim that the capacity will be raised to around 10 MW_p per year.[10], [11]. Major problems which might prevent commercialization of CIGS thin film photovoltaic modules have not yet been identified. Prospective modules costs of $Cu(In,Ga)(Se,S)_2$ modules range from about 0.28 to 1.7 €W_p^{-1}.[5], [6], [10].

1.3 Objective and contents of this work

Thin film modules are likely going to increase their share of the growing photovoltaic industry. Amorphous silicon modules have been manufactured already for several years but the short lifetime of the first generation modules has given them somewhat bad reputation. CdTe and CIGS modules are shortly entering the market. However, there is a concern about the service lifetime expectations of these thin film module technologies. There is lack of proper electrical performance measurement and accelerated lifetime testing procedures and knowledge of failure mechanisms of these thin film technologies. The methods in use are based on standards developed for measurement and testing of crystalline silicon modules. In this work the objective is to develop methods to reliably determine electrical characteristics and durability of thin film single junction amorphous silicon, CdTe and CIGS photovoltaic modules, and gain knowledge of their potential failure mechanisms in accelerated lifetime testing.

This work was mainly done as part of the European Commission project (Contract No. JOR3-CT970154). Some of the results were reported as JRC Ispra technical notes [12], [13], [14], [15], [16], [17], [18] and published as conference articles [19], [20]. The literature review on thin film technologies (Chapter 2) and the calibration measurement results (Chapter 3) were partly reported in the licentiate thesis of the author [21].

The work was done at the Joint Research Center (JRC) of the European Communities which is a European scientific and technical research center operated by the European Commission. The European Solar Test Installation (ESTI) belongs to the Renewable Energies Unit of the Environment Institute and is located in Ispra, in Italy. Because of its experience in developing testing and measurement standards and its proper facilities for this kind of work, ESTI was a natural and appropriate choice to realize this study. The services available at ESTI include qualification testing and certification of commercial PV modules to IEC standards, support to industry by conducting tests on prototype devices in the development process, calibration of reference devices for irradiance monitoring, device analysis, development of test equipment and methods, recommendations for harmonized testing methods, and support to standards organizations. The ESTI laboratory conforms to the European standard EN45001 General criteria for the operation of testing laboratories and the International Standards Organization (ISO) Guide 25 General requirements for the competence of calibration and testing laboratories. The ESTI laboratory is accredited by the Comite Francais d'Accreditation (COFRAC), as a result of which the instrument calibration laboratory is equipped with two primary standards for solar irradiance measurements and secondary standards for voltage - current, resistance and temperature measurements.

Calibration measurement services for thin film photovoltaic materials are available apart from ESTI at some extent at least at the National Renewable Energy Laboratories (NREL) in the USA and at the Fraunhofer Institute of Physics in Germany. However, the publications that exist to the author's knowledge on calibration measurements of a-Si,

CdTe and CIGS devices are published mainly on the work done at ESTI laboratories in Ispra [22], [23]. The problems pointed out in this work on the calibration measurements are also mentioned in [24] (published after the author's own publication on the subject [19]). For the first time however, comparisons on the choice of the reference device for calibration measurements for a-Si, CdTe and CIGS technologies are reported here in this study. Uniquely, the comparisons are based on I_{sc} vs. irradiance measurements, a technique developed at ESTI.

Apart from ESTI, NREL in the USA is one of the few laboratories in the world reknown for its knowledge and test facilities for accelerated lifetime testing of photovoltaic modules. They have tested also thin film modules, however the results have not been published in such a detail as reported in this work [25]. Some manufacturers have done their own accelerated tests but the results are reported very briefly [26], [27], [28]. At the Uppsala University Ångström Solar Center and at ZSW in Stuttgart some work has been done on finding the failure mechanisms of CIGS devices in damp heat [29], [30]. For the first time failure modes of thin film PV modules are reported in detail in this work and module encapsulation improvements are suggested. The adequacy of the existing standard test procedures questionned and corrections to the testing methods are suggested accordingly in this work.

The laser scanning measurement method has been used in a similar manner at NREL in the USA as at ESTI and there are several publications on the subject [31], [32], [33], [34], [35], [36]. In this work, however, for the first time the method has succesfully been used to investigate thin film modules after accelerated lifetime testing and subsequently to correlate the visual defects observed with the degradation in electrical performance of the modules.

Chapter 2 reviews some physics, material and manufacturing issues related to amorphous silicon, CdTe and CIS thin film photovoltaic technologies in order to understand possible failure mechanisms in accelerated lifetime testing. In Chapter 3 the validity of existing standard calibration measurement procedures for a-Si, CdTe and CIGS thin film photovoltaic materials is studied and improvements to increase the measurement reliability of these technologies are suggested. In Chapter 4 a-Si, CdTe and CIGS modules, prototype modules and prototype mini-modules are exposed to accelerated lifetime testing according to the IEC standard procedures. The purpose of this study is to investigate potential failure mechanisms in thin film photovoltaic modules rather than to qualify the samples. Suggestions to change the current standard to be able to improve the current test methods are made according to the test results. Also improvements to module construction to improve service lifetime are suggested. In Chapter 5 the technique of laser scanning is used to investigate the failure mechanisms in the tested a-Si, CdTe and CIGS samples and to correlate visual defects with electrical performance after accelerated lifetime testing. Laser scanning was chosen because it is a non-destructive way to determine current output uniformity of thin film modules.

2. THIN FILM A-SI, CDTE AND CIGS SOLAR CELLS

In this Chapter some physics, device manufacturing techniques and module construction matters are reviewed from the literature for a-Si, CdTe and CIGS technologies. These subjects give important background knowledge which is essential in order to understand the failure mechanisms such as corrosion and thus to draw conclusions from the lifetime test results reported in Chapter 4.

2.1 Amorphous silicon

Photovoltaic amorphous silicon material has various strengths.[37], [38], [39], [40]. Silicon materials are abundant and are not regarded as environmentally dangerous (at the product level). As far as material resources (In) and environmental hazards (Cd, Se) are concerned open questions remain for CIS and CdTe thin film solar applications. These problems do not exist with silicon based thin film technologies.

Substantial knowledge of a-Si is being developed outside the photovoltaics for non-PV a-Si applications, such as thin-film transistors. Progress in a-Si technology has been based on concurrent developments in the areas of new materials, novel cell designs and large area deposition techniques suitable for mass production. The advances made in materials and cell design could utilize the advantages offered by the outstanding optoelectronic properties of a-Si:H, its ability to form germanium and carbon alloys and the relatively low film deposition temperatures (250-300 °C). These intrinsic materials are incorporated as the intrinsic layers in p-i-n solar cells.[41]. A bandgap E_G<1.7 eV results using amorphous silicon germanium alloys a-SiGe:H. Bandgaps of E_G>1.9 eV represent amorphous silicon carbon alloys a-SiC:H. The bandgaps 1.7 eV<E_G<1.9 eV correspond to a range of amorphous silicon intrinsic materials with varying hydrogen concentration. Compared to crystalline silicon the optical gap is larger and the optical absorption coefficient in the visible range is much higher, the latter being the prerequisite for using this material as absorber in thin film solar cells. A thickness of 1 μm suffices to absorb the solar radiation efficiently.

Drawbacks of this material are the rather high density of midgap electronic states arising from unsaturated silicon bonds usually called dangling bonds, and the low carrier drift mobilities especially for holes. Another deleterious phenomenon observed quite generally in amorphous semiconductors relates to light induced increase of dangling bond states. Enhanced recombination and trapping of majority carriers in defect states lead to decreasing photo- and dark conductivity. This so-called Staebler-Wronski effect saturates and can be reversed upon annealing at around 150 °C. Besides the action of recombination centers dangling bond states can cause space charge regions in device structures because of multiple charge states depending on Fermi level position.

A big advantage of amorphous silicon technology is that it is possible to scale up the sizes of modules relatively quickly without significant losses in performance. For example, the stabilized efficiencies of the single and double junction a-Si:H panels are essentially independent of the module size. Deposition of amorphous silicon is much

faster than crystalline silicon growth and can be carried out over much larger areas.

Issues that affect the future of the a-Si technology are low device efficiencies, the Staebler-Wronski effect, and manufacturability of innovations. For long term competitiveness, 12-15 % stabilized efficiency for a-Si will be required. The maximum theoretical efficiencies are 22 % for a 1.7 eV single gap cell, 29 % for a 1.95/1.4 eV dual tandem cell and 33 % for a 2.1/1.7/1.25 eV triple tandem cell. In practice these efficiency values will be hard to achieve because of reflection and absorption losses and recombination of photogenerated carriers. A more realistic upper limit to the triple-stacked cell efficiency may be about 18 %.

2.1.1   Single junction a-Si device structure

Doped layers with large defect concentrations exhibit high recombination rates.[40]. Therefore, amorphous silicon solar cells are designed as p-i-n diodes. In p-i-n, single junction devices the p- and n-type doped layers are made thin and the absorber layer is the intrinsic layer.[37]. The majority of device makers deposit the p-layer, doped with boron, on a glass substrate that is coated with a conducting transparent oxide (TCO). To increase the light transmission of the p-layer, a-Si:H is alloyed with carbon, which increases the bandgap. The n-type layer is doped with phosphorus. The absorber layer is too thin to absorb much of the solar spectrum beyond 650 nm. Using a thicker absorber layer reduces the efficiency because of poor photocarrier collection. The simplest method to increase the amount of absorbed light is to make a light trapping structure producing multiple internal reflections in the absorber layer. Usually the tin oxide coated glass is textured on the scale of the wavelength of the absorbed light. Because the TCO dictates the growth of subsequent layers in the device, its morphology is a compromise between an extremely rough surface that might give the best light trapping, and a smoother surface that produces pin-hole free growth of the p-layer. This pin hole free growth is important because pinhole can produce shunts in the devices. These shunts occur because the pinhole region permits contact of the i-layer to the n-type TCO. In this situation normal p-layer barrier is absent, causing an increase in the dark current. The substrate structure achieves its light trapping ability through the silver/TCO layer deposited on the conducting substrate, usually stainless steel. The transparent top contact, indium tin oxide, to the device is chosen for its conductivity and low optical absorption. This structure permits a microcrystalline p-type top contact that gives a high open circuit voltage. The substrate design requires no front glass.

A conventional single junction a-Si solar structure is presented in Figure 2.1 below.[40]. The intrinsic layer of about 500 nm thickness serves as the light absorbing layer and the electric field set up by the much thinner p- and n-doped regions supports the separation of the photogenerated carriers and their drift to the contact layers. A transparent conductive oxide coating (TCO) on the glass substrate forms the front contact and exhibits a rough surface structure to enhance light absorption especially relevant for the long wavelength region of the solar spectrum. The back contact layer consists of silver whose reflectivity can further be improved by an additional TCO layer of

appropriate thickness. p-doped amorphous silicon – carbon alloys are used as p-layer. The higher bandgap reduces the absorption in the front part of the solar cell and shifts the corresponding carrier generation into the i-layer. For an efficient carrier collection the electric field should be as high as possible over the whole i-layer thickness. The defect concentration depends on the Fermi level position and hence the defect concentration varies appreciably from the p- to the n-region of the p-i-n diode structure being largest close to the doped layers. The concentration of positively charged defects sharply increases towards the p-region and the concentration of negatively charged defects increases towards the n-layer. Therefore, appreciable space charges build up at the respective interfaces and lead to regions of high electric field. Consequently, the field strength in the middle of the i-layer is decreased. The electric field distribution will be of major importance to understand and to reduce the amount of light induced degradation of amorphous silicon solar cells.

In [42] the authors have deposited a-Si photovoltaic device on flexible plastic film substrates. Both sides of the plastic films are covered with metal electrode layers called metal and back-side electrodes, respectively. These metal layers prevent gas evolution from the flexible plastic substrate and avoid deterioration of semiconducting layers. Hydrogenated amorphous silicon layers are deposited on the metal electrode and covered with transparent electrode of indium tin oxide (ITO).[43]. There are two kinds of apertures: one is for the electrical connection between the transparent electrode and the back-side electrode and the other is between the metal electrode and the back-side electrode. The former contact apertures help to collect the current at the transparent electrode by flowing the current into the back-side electrode. The transparent ITO electrode has relatively high resistivity comparing with metal electrode. This structure with collecting current through apertures decrease the series resistance at the ITO electrode. Both sides of the deposited layers are divided into each unit cell by a laser-scribing technique and each cell is electrically connected in series by the apertures contacting the metal electrode and the back-side electrode.

	Layer thickness
glass	1-2 mm
TCO	500 nm
p-layer	20 nm
i-layer	500 nm
n-layer	25 nm
metal contact	500 nm
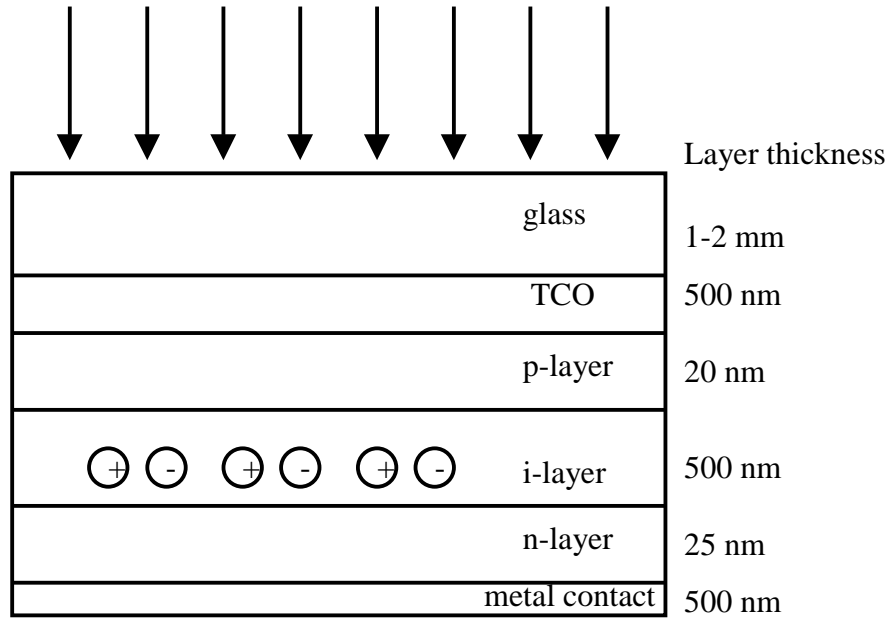
Figure 2.1 *The p-i-n diode structure of single junction amorphous silicon solar cell [40].*

2.1.2 Structure of different a-Si device layers

Conducting transparent oxide TCO

As an electrical contact, the requirements for the TCO layer are quite stringent.[44], [45]. While a low sheet resistance, the requirement for low contact resistance in the p-layer is equally critical. A large contact barrier usually results in a low open circuit voltage and a low fill factor. One such parameter which strongly affects the contact resistance between the SnO_2 and the a-SiC p-layer is the deposition temperature.

ZnO is potentially a superior TCO material, than SnO_2 as a front contact. The transparency of SnO_2 is reduced under exposure to reactive plasma due to chemical reduction. This causes a thin layer of highly absorbing Sn to be formed. Furthermore, SnO_2 has a peak transmission of only approximately 94 % in the visible spectral range. ZnO is inherently more transparent (97 %) than SnO_2 resulting in as much as 10 % increase in J_{sc} for a-Si:H based multijunction solar cells. Additional advantages of ZnO are controllability and ease of manufacturing. Some difficulties using ZnO include the fact that there is a contact barrier at the ZnO/a-SiC:H p-layer interface which causes a lower FF and V_{oc} if the same p-layer is used, that it is difficult to scribe ZnO cleanly and reliably by laser, and that higher shunt currents occur with ZnO.

The optical confinement technique with textured SnO_2 transparent electrodes is very effective in improving the conversion efficiency of the tandem solar cell under the limited i-layer thickness.[46]. Application of a highly textured SnO_2 electrode leads to a drop in V_{oc} in the tandem cells with thinner i-layers. The cause of the drop in V_{oc} is

related to defect creation in the i-layer. For a-Si solar cells formed on the SnO_2 electrode it is well known that V_{oc} decreases with decreasing p-layer thickness.

p-i-n layer

Because for single junction cells, an optimum band gap is around 1.7, open circuit voltages up to 0.9 V can be obtained as well as fill factors around 0.75.[38], [44]. The ability to generate high currents with thinner absorber layers lowers the requirements on the carrier transport required for their efficient collection. Reducing i-layer thickness would also increase the fill factor, the open circuit voltage as well as the stability of the solar cell. The concomitant decrease in carrier recombination in these thinner structures reduces the rate at which Staebler-Wronski defects are created and hence the degradation in the cell performance.

Of the many different approaches that have been attempted to improve the quality of i layers, hydrogen dilution of the gas mixtures seems to be the most successful.[47]. Hydrogen also plays a role in determining the optical gap of the alloys. Films grown from a dilute mixture of silane in hydrogen showed an improvement in stability against light induced degradation. Presence of excess hydrogen during deposition passivates the growing surface.

The doped layers play an important role in terms of providing high built-in potential in the bulk and also facilitating junctions between the adjacent cells without resistive loss.[47], [38]. Since the doped layers are inactive as far as conversion of light to electricity is concerned, they must also be optically transparent. The p-a-Si:H achieved with heavy boron doping usually results in larger absorption in the material, and the conductivity is also low resulting in large junction loss between the p and the n layers. B-doping of a-Si alloy also exhibits gap shrinkage so that p-type hydrogenated amorphous carbon and microcrystalline silicon were developed. Microcrystalline p layer with low optical loss is highly conducting as to provide high built-in potential and low tunnel junction loss. Hydrogenated amorphous silicon carbide (a-SiC:H) with optical bandgaps up to about 3 eV was initially introduced as a wide bandgap, p-type heterojunction contact for a-Si:H solar cells. The wider bandgap contact offers the advantage of generating a higher open circuit voltage as well as higher optical transmission to the a-Si:H absorber layer. The range of bandgaps that can be utilized in solar cells is limited by the increase in the gap states that accompanies the incorporation of carbon. The widening of the gap achieved even after doping significantly increases the transmission of the p-type window layer. Highly electron injecting, n-type contacts can be made with phosphorous doped a-Si:H.

Both V_{oc} and FF are adversely affected if the first p-layer is locally too thin or if component layers of the "tunnel" junction are locally too thin in a tandem a-Si device.[48]. Non-uniformities in the performance can also be caused by variations in the germanium concentration in the back junction. In an a-Si:H/a-SiGe:H tandem device structure the fill factor and the stability are improved by increasing the H_2 dilution in the vicinity of the p/i interface, but V_{oc} is reduced due to a decrease in the bandgap of the

interface layer.[49].

Back contact

The back reflector should perform two important functions.[47], [49]. It must be highly reflecting and it should also scatter light at an angle higher than the critical angle for total internal reflection. Ag is usually used to obtain high reflectivity. The interface between Ag and Si, however, is not highly reflecting because of intermixing of the two elements, and a buffer layer of ZnO is deposited in between to prevent intermixing. The required texture for optimum scattering is obtained by depositing Ag and ZnO at a high temperature in the range between 100 and 400 °C.

However, the reflectivity of the ZnO/Ag contact appears to degrade with time and results in a 3-4 % loss in J_{sc} after long-term light soaking. Zinc oxide/aluminum rear contacts do not show any difference in IV or quantum efficiency data between the initial values and those obtained after light soaking and annealing of the cells. The performance of the cells with zinc oxide/aluminum rear contacts was better than that of cells with the zinc oxide/silver contacts after long term light soaking.

In order to take advantage of the higher reflectivity of ZnO/Ag rear contact and hence gain J_{sc} and efficiency without jeopardizing module yield due to shunting, the authors in [44] explored ways to combine ZnO/Ag with other metal and/or metal-oxide layers to make composite back contact, ZnO/Ag/X, where X is some protective layer or layers. The idea is to make ZnO/Ag behave like an extension of the a-Si:H n-layer as far as laser scribing and electrical curing are concerned. The protective layer X must satisfy several conditions, such as being electrically conductive, shunt-resistant, and compatible with Ag in terms of adhesion and absence of inter-diffusion. Ideally, in the ZnO/Ag/X contact, the ZnO/Ag should dominate the optical but not the electrical behavior of the contact as to minimize Ag-related shunting.

Substrate/superstrate

The low processing temperature of a-Si:H solar cells allows a variety a substrates and cell structures to be used.[38], [40], [45]. Single (and multijunction) p-i-n and n-i-p cells are fabricated with either a-SiC:H or microcrystalline silicon p-layers on substrates such as glass/TCO, stainless steel and plastics. High efficiency cells utilize optical enhancement obtained by texturing these substrates. This increases the already high optical absorption in the a-Si:H cells. The non-transparent substrate material such as steel or plastic foils necessitate the inverse sequence of layer deposition with the p-doped layers facing the incoming solar radiation (because of the smaller hole mobility). Superstrate devices use the configuration glass substrate/textured TCO/p-i-n/p-i-n/smooth TCO/metal and the substrate devices the configuration stainless steel substrate/textured Ag/smooth TCO/n-i-p/n-i-p/smooth TCO.

The superstrate device requires a thick transparent front contact to achieve both the light trapping structure and low electric series resistance.[37]. This results in a significant light loss. The superstrate design is easier to manufacture in large area

modules because of the ease of monolithic interconnections, whereas the substrate presents difficulty in connecting different submodules together in a monolithic panel.

Module interconnection

Large area photovoltaic modules consist of solar strips separated by laser scribing or other techniques and interconnected in series. The typical interconnection scheme is shown in Figure 2.2 below. The benefit of such integrated structures results from a reduction of resistive losses by higher output voltages and lower currents of the modules.
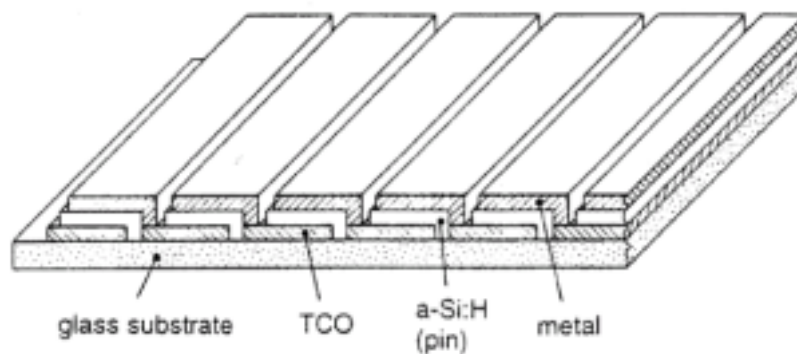
Figure 2.2 *Series connection of amorphous silicon solar cells for module integration [40].*

2.1.3 Staebler-Wronski effect as a degradation mechanism

Properties and causes of the effect

That sunlight creates light induced metastable defects in a-Si:H was discovered very soon after the first cells were made. This light induced degradation is called Staebler-Wronski effect. The Staebler-Wronski effect involves an optically induced decrease in both the photoconductivity and dark conductivity and restoration to the original state by annealing above 150 °C.[50], [38]. A lot of articles have been written discussing this effect, but the physical causes of the effect still seem somewhat uncertain. Already in their article [50], Staebler and Wronski suggested that a localized defect undergoes a metastable structural change (e.g., local bond reorientation) when it traps or acts as a recombination center for photogenerated charge carriers in extended states. In discharge produced a-Si, however, where compensation of dangling bonds by hydrogen atoms is thought to play an important role, a bond reorientation could have a large influence on the effective density of gap states. In the light induced degradation, about two-thirds of the degradation is due to degradation of the fill factor FF, and one-third is due to V_{oc}.[46]. The degradation in I_{sc} is negligible. Experiments have also shown that the magnitude of the light induced change depends on whether the cell is under open circuit, short circuit, or load conditions. The results generally show that the largest and smallest changes occur under open- and short-circuit conditions, respectively.[51].

Most studies of the Staebler-Wronski effect have concluded that optical exposure causes metastable states in the gap.[39], [37], [52], [51]. The main result of these metastable changes is an increase in the density of neutral dangling bond defects, the dominant recombination center. The added dangling bonds shift the dark Fermi level toward midgap, resulting in a decrease in the dark conductivity. It has also been shown conclusively that these metastable defects in undoped hydrogenated amorphous silicon are produced by a recombination of excess carriers, after these excess carriers are created either by illumination or by carrier injection. The formation of dangling bonds reduces the efficiency of the devices until the formation rate of the dangling bonds in equal to their annealing rate, which is increasing with temperature. Consequently, the stabilized efficiency is higher at higher device temperatures.

In a-Si:H films, the rate of the recombination that creates the defects is determined only by the light intensity.[53]. In a-Si:H solar cells, however, the recombination rate is determined by the bias voltage in addition to the light intensity. Both the light intensity and the bias voltage determine the increase in the defect density and the degradation characteristics of the solar cells. The degradation is accelerated according to the light intensity. Under the open circuit condition, all the photogenerated carriers were recombined in the cells. Under the load condition, the bias voltage is controlled so that one-third of the photogenerated carriers are recombined in the cell. Namely, the bias voltage controls the recombination ratio that is defined as the ratio of the recombined carriers to the photogenerated carriers in the cell. The degradation is accelerated according to the forward bias voltage. A monomolecular recombination process is dominant in a-SiC:H and a-Si:H, a bimolecular recombination process is dominant in a-SiGe:H. In the paper the authors have derived a relation in which they express the light induced degradation by a function that does not depend on the exposure condition when it is expressed as a function of total defect density instead of time. Part of the relation depends on the i-layer material.

The usual method for lessening the light-induced degradation is reduction of the thickness of the device.[39]. The resulting higher electric field removes the carriers more effectively, reducing the recombination that causes defect formation. However, the thinner device absorbs less light. To capture more of the light, the a-Si cells use a back reflector (such as silver-coated zinc oxide) or the device is modified to become a multijunction device consisting of many layers with different band gaps. Consequently, the stabilized efficiency of single-junction amorphous silicon devices usually peaks for thickness around 2000 Ångströms, whereas the initial efficiency peaks at a larger thickness. The cell exposed directly to sunlight is thin in a multi-junction device, resulting in less degradation. The second (and third cell if present) are exposed to lower intensities of light, also resulting in a lower rate of defect formation. Also hydrogen dilution results in a higher relative stabilized state which is reached much more rapidly than without dilution.

Another precaution to reduce the degradation except using the stacked cell

structure, concerns the design of the p-i interface region of each single cell.[40]. Usually an undoped buffer layer is inserted between the highly p-doped a-SiC:H and the intrinsic a-Si:H absorber layer. The buffer, whose band gap lies between those of the adjacent layers, yields higher V_{oc} values but this benefit is often offset by higher long term degradation. Mainly the fill factor (FF) is affected by degradation indicating a reduced carrier collection. This in turn results predominantly from a reduced field within the i-layer because of an increase of positively charged defects at the p-i interface and hence a major drop of the electric field strength. Couterdoping in this region by insertion of a weakly p-doped interface layer and hence partial charge compensation avoids the strong electric field drop and provides higher field strength throughout the i-layer.

Light soaking indoors

Some indoor light soaking results observed in literature, are discussed in the following. Material grown from hydrogen diluted silane by rf glow discharge is shown to have a better stability against light induced degradation.[43]. It is believed that hydrogen dilution controls the growth mechanism and leads to an increase of the microscopic density. The H-diluted a-Si:H solar cells out perform the undiluted a-Si:H solar cells in both V_{oc} and FF after 600 hours of light soaking. A thin layer of H-diluted a-Si:H between p and n interface stabilize V_{oc} after 600 hours of light soaking just as with H-dilution of the bulk solar cell. This implies that the stabilization of H-diluted a-Si:H solar cell is through controlling p and i interface.

A-Si solar cells experience permanent degradation at elevated temperatures due to hydrogen motion.[48]. Since hydrogen diffusion is much faster in p-type material than in undoped or n-type material, the degradation occurs mainly in the short wavelength portion of the spectral response. Moreover, the degradation is accelerated in the presence of a strong electric field which induces proton motion in the vicinity of the p/i interface.

Light soaking outdoors

Results of some outdoor light soaking are presented below. After controlled light-soak testing of multijunction a-Si modules, some of the modules were installed outdoors.[54]. Under outdoor exposure, the modules degrade further in performance approximately 10 %, possibly due to lower outdoor temperatures and varying spectra. Single junction modules experienced approximately 25-30 % degradation in normalized power during the first 5 months of exposure. Approximately 10 % seasonal performance variation has been observed. Dual junction modules experienced an initial light induced degradation of approximately 20-25 % in normalized power during the first few months of exposure with seasonal performance variations of approximately 10 %.

When a-Si solar modules with p-i-n single junction structure were exposed outdoors, the module efficiency exhibits a marked degradation after the two first months of sunlight exposure.[55]. Due to the higher temperatures that the a-Si solar cells experience during summer, an improvement occurs in material characteristics (increase in charge carrier lifetime and decrease in band gap) as well as in device characteristics

(increase in spectral photoresponse). The favorable spectral distribution of solar irradiation during summer, especially in the ultraviolet region, which is caused by the decrease in air mass, also supports the increase in the PV module efficiency. In winter, the solar spectral irradiance shifts to longer wavelengths (the red region) where the a-Si material shows a poor spectral response and the efficiency gradually decreases together with the PV module operating temperature. The PV module efficiency is almost completely stabilized after two years of sunlight exposure and reaches and apparent steady state with seasonal variations.

In [56] when the authors have analyzed experimental data, the stabilized performance seems to depend on the light intensity I: $\eta(stable) = 1-AI^{1/8}$, where A = fractional power loss at 1-sun intensity. NREL outdoor stability data on dual junction modules show that the degradation during winter months is higher than during summer months. The degradation increases by 2.5 to 4 percentage points for each 10 °C lower temperature than the 50 °C. The temperature coefficients change with light soaking. Also the initial performance under the solar simulator is generally higher than that under outdoor conditions. After light soaking the degradation as measured outdoors is generally lower than that measured under the solar simulator.

The tandem junction module described in [57] experienced light induced degradation of ~16 % after 600 hours under AM1.5 illumination. The efficiency loss of a single-junction a-Si device with a comparable device thickness is about 27 %. The outdoor tested modules were divided into two groups, one group operated approximately at the maximum power point with a load during light soaking while the other were set at open circuit condition. There was no significant difference between the two groups.

2.1.4 Other degradation mechanisms

Other possible a-Si module degradation mechanisms include module thin film corrosion due to inadequate encapsulation.[39]. Also the incorporation of Ge in amorphous silicon alloy cells is known to deteriorate the cell performance.[58]. The fill factor of a-SiGe alloy cells is poorer than that of a-Si alloy cells. The reason for the poorer performance of a-SiGe alloy cells is considered to be the lower adatom mobility of GeH_3 molecules on the growing surface. This may cause higher microvoid density for a-SiGe alloys and will contribute to the poorer quality.

2.1.5 Deposition techniques

Several methods have been used to deposit amorphous silicon from silane or other silicon carrier gases.[37], [59]. These include: chemical vapor deposition (CVD), direct current (DC) and radio frequency (RF) glow discharge (plasma enhanced chemical vapor deposition), microwave glow discharge, electron-cyclotron resonance glow discharge, remote plasma-assisted CVD, controlled plasma magnetron (CPM) glow discharge, photolytic decomposition (photo-CVD), sputtering, cluster beam evaporation and hot-wire decomposition. Of these, RF and DC glow discharge depositions are the most common and are those used by industry. The optimum a-Si:H material has

traditionally been produced at a substrate temperature of around 250 °C and contains about 10 at.% H. Some gas mixtures used to deposit a-Si:H contain SiH_4, Si_2H_6, SiF_4 and H_2, while others may use only SiH_4. The most recent route to obtain higher quality films is to use H-dilution of the feedstock gases. This improves the initial film quality in some systems and leads to less light induced degradation in solar cells. To decrease the bandgap, mixtures of silane and germane with or without disilane and hydrogen are typically used to make a-Si:Ge:H alloy. Methane and silane are the most common mixtures to produce a-Si:C:H alloy. Phosphine and silane mixtures are the best for the n-layer, whereas diborane, boron trifluoride or trimethylboron produce a p-type dopant. The best glow discharge material is produced at a deposition rate between 0.1 and 0.2 nm/s. Because most device absorber layers are about 500 nm thick, it takes up to 1 h to grow the i-layer.

Plasma enhanced chemical vapor deposition (PECVD)

The conventional way of obtaining amorphous silicon layers is by plasma enhanced chemical vapor deposition (PECVD).[40]. Silane is fed into the reaction chamber containing two capacitor plates for plasma excitation, the grounded one being heatable and used for carrying the substrate. At substrate temperatures in the range of 150 to 250 °C and gas pressure in the 0.1 Pa regime deposition rates of 0.1 to 0.5 nm/s are obtained. The amorphous layers likewise deposited on glass, steel, or plastic foils contain 10 to 15 at.% hydrogen. For preparation of doped layers phosphine or diborane are added to the silane flow, for the preparation of silicon alloys germane or methane are added.

Roll-to-roll process

Continuous roll-to-roll manufacturing technology at Energy Conversion Devices, Inc., utilizes a thin flexible stainless steel substrate.[60], [61]. The stainless steel substrate is rugged and this improves production yield by eliminating substrate breakage. The transport mechanism on a thin flexible stainless steel is mechanically simpler and less expensive than the transport mechanism for conventional glass substrates. Heating and cooling of the substrate during solar cell deposition can be accomplished quickly compared to glass substrate manufacturing. The stable module efficiency for a module manufactured with the process described above is 8 %.

The triple junction two bandgap a-Si alloy solar cells are deposited in a continuous roll-to-roll process on a 5 mil thick, 14 in wide and 600 ft long web of stainless steel at speed of 1 ft/min. The back-reflector machine deposits a textured reflective metal layer and a metal oxide layer using a multiple target DC magnetron sputtering chamber. The metal adheres to the stainless steel and texturizes the surface to provide a diffuse, reflective layer with high reflectivity. The metal and oxide layers provide ohmic contact to the solar cell as well as improved infrared response.

Amorphous silicon alloy deposition machine deposits nine layers of doped and undoped amorphous silicon alloy semiconductor materials using PECVD process.

Mixtures of feedstock gases are decomposed in a series of RF CVD plasma chambers to continuously deposit layers of amorphous silicon alloy material onto the coated stainless steel substrate heated to approximately to 250 °C to 300 °C. The process gas mixtures in each section are dynamically isolated from adjacent sections by proprietary gas gates. Substrate passage through the process chambers is such that deposition takes place on the underside, which minimizes film defects due to particulate accumulation.

Transparent conductor deposition machine deposits a transparent, electrically conductive layer on top of the solar cell structure as an electrical top contact and as an anti-reflective coating using reactive evaporation of metal in an oxygen atmosphere.

An advancement of the process described above is the serpentine deposition process using RF plasma processor. The deposition takes place on the substrate as it travels vertically through the deposition chamber. In the deposition chamber, a single RF cathode will generate plasma which will produce film deposition on regions of substrate facing both sides of the cathode. There will be equipment cost savings, reduced heat loss and consequently electric power consumption, and improved gas utilization efficiency due to the serpentine process. Also the hardware design is simpler than with the present deposition machines.

In [42] a-Si solar cells are deposited on flexible plastic film substrates with an improved roll-to-roll deposition technique named stepping roll (SR) film deposition technique. The SR apparatus overcomes a problem of doping gas contamination in roll-to-roll plasma chemical vapor deposition (PCVD) apparatus, and enables to set sputtering reactors in the same vacuum system to perform in-situ fabrication of transparent conductive oxide electrode layer on the PCVD a-Si layers. The contact apertures are made on the plastic substrate by a punching unit and the substrate is cleaned in a roll-to-roll pretreatment apparatus. Then the metal electrode and the back-side electrode are sputter deposited by a roll-to-roll electrode deposition apparatus. After the electrode formation, a-Si:H layers and ITO electrode are in-situ fabricated by SR film deposition apparatus composed of 6 CVD reactors and 2 sputtering reactors set in a common chamber. The successive deposition of a-Si and ITO layers avoids generation of short-circuit points. Finally, these layers formed on both sides of the film substrate are laser scribed into unit cells by a roll-to-roll laser scriber.

Electron-cyclotron-resonance plasma CVD process

Two types of p-i-n a-Si devices were fabricated with ECR [59] plasma-CVD growth technique, superstrate devices on tin oxide substrates, and substrate devices on bright-polished stainless steel.[59]. The ECR plasma-CVD growth technique uses microwaves and magnetic fields to create a highly ionized beam of either hydrogen or helium atoms, which streams towards the substrate. The streaming beam of hydrogen reacts with silane to create primarily SiH_3 species, which leads to the growth of the material. During growth, the material is subjected to controlled ion bombardment and etching by the H ions and radicals, thus achieving the condition of etching-during-growth. This etching-during-growth should lead to better localized microctructure and

hence, better stability. It is easier to get higher voltages in substrate geometries than in superstrate geometries. The stability of both types of cells, when deposited using the H-ECR technique, is better than the stability of comparable quality glow discharge cells.

2.2 CIS

The three component compound of copper and indium diselenide, $CuInSe_2$, with chalcopyrite structure is considered to be one of the most promising compounds to be employed in solar cells.[62], [63]. The CIS is a square-gap, direct band gap semiconductor with gap width (~1.04 eV) acceptable for photoconverters. The band gap has been shown to decrease linearly with increasing temperature between 77 and 300 K. Devices usually achieve optimum performance after air heat treatments at 200 °C for times ranging from 15 min to 16 h. The CIS-based solar cells are simple to produce, feature chemical stability, their parameters are stable in time, and it is possible to produce both p- and n-type conduction material.

The absorbing layer is the key element of solar converters, which is produced mainly from the p-type semiconductor. It is likely that improvements in short circuit current, I_{sc}, and fill factor, FF, can be achieved by improved device design. In contrast, improvements in V_{oc} may require modifications of the cell materials. Further, graded band gap structures could be developed which could result in an improvement in V_{oc} without reduction in I_{sc}. In general, high Ga contents have produced devices with high values of V_{oc}. It is of interest to use the solid solutions of the type $CuIn_{1-x}Ga_xSe_2$ or sometimes $CuIn(Se_{1-y}S_y)_2$ instead of or together with CIS.[64]. Varying x, the gap width can be changed from 1.04 eV for CIS to 1.68 eV for $CuGaSe_2$. Employing $CuInGaSe_2$ together with CIS extends the spectral range to the IR region. Also the fractional loss of V_{oc} for increasing temperature is seen to become smaller as Ga is added to CIS.[65]. Similarly, the fractional loss of V_{oc} as irradiance is reduced through the addition of Ga.

2.2.1 Defects in CIS

Chalcopyrite structure CIS has been reported to form at temperatures below 810 °C.[63]. The chalcopyrite structure is retained for variations from the stoichiometric composition in the direction of excess In and Se but not for excess Cu at equilibrium. The chalcopyrite structure is stable over the widest composition range. The observed microstructures typically exhibit equiaxed, <1μm in diameter, when viewed perpendicular to the film, and contain significant numbers of line, plane, and volume defects. These defects include dislocations, stacking faults, microtwins, and intergranular pores. Compositions in most films have been found to be completely uniform with depth below the surface despite changes in the incident atom fluxes by several percent during deposition. In-rich region is occasionally present near the film surface. In three source evaporated films there is a surface modified layer. The composition of the altered layer depends on the average composition of the film and whether a single-layer or bilayer growth process was used. The resistivity of CIS films depends on the average composition of the deposited layers.

The major donor level in the CIS is associated with Cu vacancies; the major acceptor, with Se excess and In at Cu sites.[63], [66]. The dominant defect is the Cu vacancy and it is considered the major defect responsible for the n-type doping. Cu-at-

In-sites-defects are responsible for bandgap levels that are identified as donors. In-at-Cu-sites and In vacancies have been identified as acceptors.

Type conversion and changes in conductivity occur by changing the populations of the two defects by controlling the relative defect chemical potentials, for example, by interaction of one defect with oxygen at the film surface or at grain boundaries. This may, in part, explain the broad range of compositions over which high efficiency solar cells can be produced and the effect of air annealing on both CIS films and devices.

2.2.2 The effect of oxygen and sodium on CIS

Annealing as-deposited films produced by a variety of techniques in air or oxygen typically leads to changes in resistivity and the conversion of n-type layers to p-type.[63]. Air annealing of completed $CuInSe_2/CdS$ cells is used to optimize the performance of the device, and the improvements in the cells have been correlated with changes in electric properties of the film.

According to the defect chemical model of oxidation effects, surface (including grain boundary) formation in CI(G)S is accompanied by the formation of donor defects, which are due to the "dangling bonds" resulting from the bonds that need to be broken to form the surface.[67]. These can be viewed as Se vacancies and the vacant sites can be occupied by O atoms. From an electrical point of view, the grain boundary donors are detrimental to solar cell performance in two ways: first, they act as traps for the recombination of photo-generated electrons with holes, which has been identified as a major loss mechanism in polycrystalline photovoltaic devices in general and in CIGS-based photovoltaic devices in particular. Second, they result in a positive surface charge, situated at the grain boundaries. This positive charge results in a depletion region and a potential barrier for electrons in the vicinity of the grain boundary. Thus, the effective p-type doping of the CIGS layer is decreased, because a non-negligible portion of each grain is depleted of holes, and the inter-grain transport of photo-generated electrons is impeded. The placement of O as a substitute for the missing Se immediately cancels both effects and explains why oxidation is beneficial.

The interface between the CIGS and CdS layers is a special case of a grain surface.[67]. Therefore, both oxidation effects, namely removal of recombination centers and decrease in positive surface charge, are expected there as well. The removal of interface recombination centers is beneficial, because the presence of such centers increases the solar cell leakage current and thus decreases its V_{oc}. Much of the oxidation-induced improvement in photovoltaic performance of early CIS-based solar cells had to do with the reduction of interface recombination. A decrease in the positive interface charge implies a decreased band bending in the CIGS layer. Because the free holes and electrons in this layer are repelled from or attracted to the positive charge, respectively, a decrease of this charge causes the space charge layer to become less depleted or less inverted. As opposed to all oxidation effects discussed so far, this one is detrimental to the photovoltaic performance, because V_{oc} decreases with a decreasing band bending in the absorber layer. Donor defects situated at internal CIGS grain boundaries are highly

detrimental to photovoltaic conversion, because they act both as recombination centers and as an impediment to inter-grain charge transport. However, when states of essentially the same nature are situated at the CdS/CIGS interface, their positive contribution to the band bending may eclipse their negative effect on the interface recombination. Thus, a relatively unusual case where defect states are actually beneficial to device operation may arise.

Na has been found to increase the open-circuit voltage, V_{oc}, of ZnO/CdS/CIGS solar cells.[67]. In some cases, an improvement in the short-circuit current, I_{sc}, or the fill factor has also been noted. Low cost soda lime glass (SLG) is an alkali containing substrate from which sodium diffuses into the CIS layer during semiconductor formation and improves grain growth and cell performance.[68]. SLG also shows a near optimum match in the thermal expansion coefficient with $CuInSe_2$ (CIS) and $Cu(In_{0.84}Ga_{0.16})Se_2$ (CIGS). The soda lime substrate acts as a sodium source for the CIS thin film and the molybdenum exhibits controlled sodium permeability. The amount of sodium ending up in the final CIS layer depends on the sodium concentration in the soda lime glass, the permeability of molybdenum and on the thermal budget used for film formation. Sodium incorporation is clearly accompanied by a morphological change of the CIGS thin films i.e. significantly larger grains.

Upon production of the CIGS film, much of the passivation of donor defects at grain boundaries is achieved by Na-catalyzed oxidation.[67]. Unfortunately, the same effect also passivates the free surface of the CIGS film after the latter is removed from the vacuum chamber. Therefore, an important role of the CDB-CdS layer is to restore the band bending by re-introducing donor defects at the CdS/CIGS interface. Another possible role of the CdS buffer layer is to partially "protect" against oxidation of the interface. Na increases the open-circuit voltage of ZnO/CdS/CIGS cells but decreases it at otherwise identical ZnO/CIGS buffer-free cells. A reasonable hypothesis is that in the absence of CdS, the detrimental Na-catalyzed interface oxidation dominates over the beneficial grain boundary one.

As mentioned above, the electronic effects of Na and of oxidation are connected.[67]. The fundamental reason for this relation is the well-known catalytic effects that alkali metals in general, and sodium in particular, have on the surface oxidation of semiconductors. The catalytic effect stems from alkali-induced polarization of the O-O bond in the physisorbed O_2 molecule, as well as enhanced tunneling from the substrate due to alkali metal-induced lowering of the surface work function, which result in increased formation of O_2. The latter is considerably easier to dissociate into atomic oxygen than the O_2 molecule. Since the dissociation of molecular oxygen into atomic oxygen is a prerequisite for occupation of a Se site by oxygen, a catalytic effect is obtained. For confirming the defect chemical model, on the chemical side, one must establish that Na is primarily associated with grain boundaries and that Na and O concentrations are correlated. On the electrical side, one must verify that Na induces elimination of gap states acting as recombination centers, and induces and increase in the

free hole density.

Another subtle relation between sodium and oxygen is that sodium is also known to induce Cu liberation.[67]. Surface oxygenation of CIGS results in a reduction of the surface Cu content. Cu is well-known to be a mobile constituent in CIS. Therefore, the Cu atoms that are released can migrate. The built-in field drives the excess Cu^+ ions away from the surface. Because interstitial Cu is a donor, the net acceptor density in the space charge region and the neutral volume of the grain is decreased. This increases the width of the space charge region.

In conclusion, the beneficial effect of oxidation is the passivation of Se-vacancy donor states at grain boundaries by oxygen atoms.[67]. Na-effects are related because Na catalyzes the oxidation. However, the oxidation of CIGS-based solar cells has also detrimental effects: first, a reduction of the band bending in the CIGS film (and hence a reduction of V_{oc}), due to the reduction of the positive CdS/CIGS interface charge. Second, a decrease in the effective hole density in the CIGS film, due to oxidation-induced Cu liberation and migration. Therefore, Na and O treatments must be carefully optimized to balance the beneficial and detrimental effects.

2.2.3 The effect of illumination on CIS

The electrical properties of CIGS and $CuInSe_2$ (CIS) solar cells significantly change after illumination, after electrical bias, or after extended storage in the dark.[69], [70]. It is found that the performance improves in general when the cell is brought to operation conditions. The CIS device has two different states, the "high free electron density in CdS" (HFE) and the "low free electron density in CdS" (LFE). The latter state is the intrinsic state of the device, i.e. without external excitation the device will relax to this state. Exposure to white light or blue or green light all can cause the device to change from LFE state to the HFE state. The cutoff wavelength of the light that can cause this change is experimentally verified to be 550 nm which coresponds to the cutoff wavelength of CdS optical absorption. Thus, the HFE state is created by the free electrons derived from photons absorbed in the CdS. When a device is in the HFE state and the light needed to sustain it is removed, the device will return to the LFE state, but slowly, due to the slow release of trapped charge. The red light illumination, on the other hand, is seen to result in a kink in the J-V characteristics around open circuit voltage (V_{oc}). The low free electron density results in low current to voltage sensitivity. Thus the "red kink" appears at voltage around V_{oc} because the current is almost zero in the region.

The benefit of blue part of the solar spectrum is mainly given by the increase of the fill factor which is often observed during light soaking. The open circuit voltage of CIGS based solar cells increases slightly during illumination. Light soaking treatments are also used to re-establish fill factor losses which have occurred during thermal cycling of the cell. The fill factor degradation under red illumination sensitively depends on the preparation conditions of the buffer layer as well as on those of the window layer and, in general, is less pronounced. The illumination effect leads to fill factor

degradation/recovery cycles upon storing the cell in the dark and illuminating it with the full solar spectrum. If the solar cell is operated at normal working conditions, i.e., is exposed to the full solar spectrum, the device also approaches its optimum performance. Fill factor degradation/recovery and open circuit voltage relaxation are perfectly reversible. Thus, these metastable effects do not contradict the long term stability of CIGS –based solar modules.

Also cross-overs of the dark and illuminated IV-curves of chalcopyrite based heterojunctions are frequently observed.[71]. In an ideal device the effect of illumination is taken into account by an additional photocurrent and consequently the dark and illuminated curves never cross. The occurrence of the cross-over depends on the spectrum of the illumination, i.e. the absorption of photons in the CdS buffer layer results in a cross-over of the dark and illuminated IV-curves. If only photons are absorbed in the $Cu(In,Ga)Se_2$ absorber layer, such a behavior is not present.

2.2.4 CIS device structures

Solar cells based on $CuInSe_2$ use heterojunctions between a p-type (absorber) layer of $CuInSe_2$ or a related alloy, and a transparent n-type CdS, ZnSe, ZnO, or related compound layer.[63]. Substrate is generally glass. The active device is deposited on a base electrode, typically >1 µm of Mo, which provides a low resistance contact to the CIS and good adhesion to the glass. Top contacts are usually transparent conducting oxides, sometimes combined with a metal. The transparent conductor also serves as an antireflection layer. The average composition of the absorber layer is typically near-stoichiometric $CuInSe_2$. A schematic cross section of a typical single device such as produced by three source evaporation is shown in Figure 2.3 below.
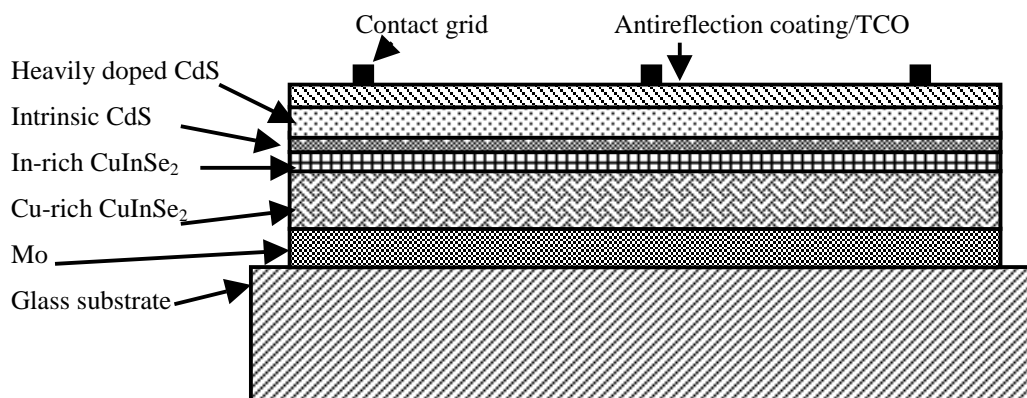

Figure 2.3 *A schematic cross section of a typical single device such as produced by three source evaporation (layers not drawn in scale, e.g. the CdS layer is made very thin).*

An alternative device structure involves fabrication of cells in an inverted superstrate configuration.[63]. The major difficulty with this structure is that the highest

temperature processing step, deposition of CIS (T>300 °C), may lead to interdiffusion across the heterojunction, particularly with CdS window layers. Devices using the superstrate configuration have been fabricated by depositing ITO and CdS on glass, followed by CIS, and finally Pt for the back contact metallization. The grain size of the superstrate configuration CIS was found to be considerably smaller than in the bilayer CIS films deposited on Mo. The most significant loss in performance resulted from the low V_{oc}, which may be due to the interface or smaller grain structure.

In Ga containing CIGS devices four configurations can be used to incorporate the Ga-containing absorber layer into the solar cell structure.[72]. In the first Ga is incorporated in a homogeneous $CuIn_{1-x}Ga_xSe_2$ quaternary CIGS structure. In the second, Ga is completely separated from the CIS in a distinct Ga (or Ga_xSe_y) layer (CIS/Ga). In the third model Ga is graded into the lattice as $CuInSe_2/CuIn_{1-x}Ga_xSe_2$ (CIS/CIGS) and in the fourth model segragated as a bilayer $CuInSe_2/CuGaSe_2$ structure (CIS/CGS).

Window layer

Several materials have been considered for the n-type window layer on $CuInSe_2$-based heterojunctions, including CdS, CdS:In, CdZnS, ZnSe, and ZnO.[63], [62], [73]. CdS is the most compatible material for optic windows due to close values of their electron affinity. The edge of heterojunction conduction band has practically no discontinuities. A slight divergence of lattice constants (~1%) enhances effective division of light generated charge carriers. Another advantage of CdS is the simple production processes for layers with properties specified in advance. Devices using ZnO window layers have exhibited low efficiencies with high short circuit current but low open circuit voltage.

In common thin film solar cells of CIS/CdS type, losses are high due to radiation absorption by the CdS front layer in the short wavelength region, and to short circuit current density losses. The main drawback, which limits the growth of efficiency in solar cells based on the CdS optic window, is its narrow gap (2.42 eV).

Transparent conductor (TCO)

Transparent conductors, which also function as anti-reflection coatings, have been shown to provide high quality top contacts.[63]. The most popular choices for these conductors are indium-tin oxides (ITO) or doped ZnO. Transparent electrodes contribute slightly to the series resistance observed in active devices, but the resistance is offset by improvements in the overall quantum efficiency through reductions in surface reflection losses.

Back contact

The Mo film is typically used as the CIS front and back contacts.[62], [63]. The thermal expansion coefficient of Mo is close to that of CIS and Mo shows inertness to the CIS cells, and hence it is indifferent to the CIS stoichiometry and electric properties in the processes of film deposition, device manufacture, and various heat treatments. Mo is

neutral to T=600 °C and can diffuse into CIS at higher temperatures and interact with Se with the formation of $MoSe_2$.

However, because Mo has a relatively low conductivity and is expensive when compared to materials such as Al, it is not an ideal contact material. A large number of alternate conductors have been examined including Al, Ni, Cu, Pt, and Au, but none of these has proven superior to Mo. There has been some evidence of diffusion of Cu, In, and Se, at approximately equal rates, into the underlying metal. However, no Mo was observed to move into the CIS layer. This diffusion probably occurs along column boundaries in the Mo and thus does not mix the metal and CIS layers.

2.2.5   CIS deposition options

The general guidelines for the CIGS recipe are: (1) material is delivered to the substrate in a sequential manner, (2) substrate temperatures of 450 °C or lower are used during the deposition of the metal selenides, and (3) substrate temperatures of 500 °C or higher are used only during (In,Ga,Se) vapor treatments.[74], [63]. A wide variety of techniques have been used to fabricate $CuInSe_2$, including three source evaporation, laser annealing, flash evaporation, vapor transport, spray pyrolysis, sputtering, liquid phase epitaxy, electrodeposition, screen printing, and selenization of metal layers. Common elements to the different processes are the requirement for the formation chemistry to pass through the Cu-rich, CIGS:CS two phase region where, at substrate temperatures greater than 500 °C in a Se activity, the CIGS absorber quality is optimized by a liquid-phase sintering/recrystallization process, and that an activity of (In,Ga,Se) is required to convert the excess CS to CIGS.

In the I-III-IV$_2$ family of semiconductors, it is during the thin film or crystalline formation process that the semiconductor properties are determined by native defects, alloying, and the presence of secondary phases.[75], [65], [74]. Various rules have been generated regarding compound formation. For example, finishing the precursor with Cu (or copper selenide) generally leads to low V_{oc}, while higher V_{oc}'s are obtained by finishing with In. Starting the precursor with gallium selenide against the Mo has been found to lead to superior adhesion, while finishing with Ga can lead to improved V_{oc} and FF. A high surface concentration of Ga should enhance V_{oc}, and the increasing band gap toward the rear should enhance collection of carriers generated outside the space charge region. Improvements in device performance can be attributed to higher substrate temperatures and the strategic inclusion of Ga and/or S in the absorber to increase in the band gap. The higher substrate temperature ($T_{sub} \geq 500$ °C) helps to create enhanced grained structures. With the increase in grain size comes an enhancement of crystallite quality, a decrease in free-surface area, and an associated decrease in free-surface states. The net benefits are lower O_2 sensitivity (i.e., the devices do not require an air anneal to optimize performance), fewer grain boundary shunts, and more planar surfaces, and, hence, lower forward currents and diode-quality factors with higher V_{oc}'s and FF's. Deleterious effects of the high temperature process include enhanced reactivity of the substrate to Se and higher thermal expansion mismatch, producing both electrical and

mechanical complications for the device.

Important chemical relationships in the CIGS thin film processing are the Cu/(In+Ga) ratio, which controls the formation chemistry and phase nature, the Ga/(In+Ga) ratio, which determines the fundamental band gap, the Se/total metal ratio, which controls the chemical reaction path, and the substrate temperature, which influences the formation chemistry and adatom mobility during growth.[76], [77]. A non-uniform Ga/(Ga+In) depth profile within the absorber produces superior devices in comparison to those incorporating homogeneous absorbers. The optimal profile, however, is difficult to achieve because of enhanced interdiffusion of In and Ga at higher temperatures. In band gap profiling, V_{oc} and J_{sc} are enhanced by a "back-surface field" that is created by inserting higher band gap absorber material at the back contact. With this structure, recombination at the back contact is reduced, and a quasielectric field improves carrier collection deep within the absorber. J_{sc} is improved by limiting the extent of Ga diffusion from high Ga regions to lower Ga regions. V_{oc} and FF are improved by proper grading of the band gap at the heterointerface. This results in reduced space-charge recombination and improved conduction band line-up.

Coevaporation of the precursor

In three source evaporation the Cu and In fluxes determine the film composition and growth rate.[63]. Typically, the Se atom flux exceeds the combined Cu and In fluxes and the excess Se desorbs from the film surface. The first layer is typically ~2 µm thick, deposited at 350 °C, with an average composition of approximately 26 % Cu, 25 % In, and 49 % Se. The Cu-rich film is capped by a 1-µm $CuInSe_2$ layer grown at 450 °C with a typical average composition of 21 % Cu, 28 % In, and 51 % Se which grows pseudoepitaxially on the Cu-rich layer. Diffusion during growth mixes the two layers completely forming a near-stoichiometric film. The resulting material has larger grains than a single-layer film of comparable composition.

In [78] the system for deposition of CIS and CIGS onto larger area substrates uses the in-line principle by moving the evaporation sources relative to the substrates. Substrates are mounted on the inside of a hexagonal holder, which can be loaded with a maximum of 12 pieces of 30 x 30 cm^2 substrates. The entire hexagonal holder rotates inside a cylidrical 3-zone substrate heater, each zone being heated by 8 IR-lamps of 1 kW each. Evaporation is done from elemental, temperature controlled sources. Transport of the sources into the substrate heater arrangement is accomplished by having the sources mounted on a long rod, which moves at a constant speed of about 1 cm/min. The evaporation rates are measured prior to the deposition by using a quartz-crystal microbalance individually on each source.

A manufacturing line based on precursor coevaporation is described in the following.[79], [80]. An in line system was used with line sources having a homogeneous distribution of the vapor across the total width of the substrate. The system consists of a deposition chamber with four line sources for Cu, Ga, In, Se, a preheating and a cooling stage and two load lock chambers. Rate profiles can be

adjusted by the positions of the sources. High substrate temperatures close to the softening point of the glass are required for the production of films with high quality. In order to facilitate the transport, the substrates are supported by carriers. A new design which evaporates downwards has been developed. An important issue is the control of deposition rates and final composition of the film. Several methods are investigated for this purpose including various types of spectroscopies and in-situ measurements of film properties.

In an example production line, soda lime glass substrates with a thickness of 1-2 mm are used. The molybdenum back contact is deposited by sputtering or electron beam evaporation. For the separation of cells, patterning by laser scribing is used which leads to modules with good performance. For the formation of the heterojunctions, a thin buffer layer of CdS is produced by chemical path deposition. ZnO electrode is fabricated by sputtering, ALE or activated reactive evaporation (ARE). For large scale production, deposition rates of RF sputtering process are too low for low cost and thus reactive DC sputtering process is used. Also ALE was found to be a process which can produce high quality ZnO films on large area. The process is basically a batch process but a large number of substrates can be processed in one batch, so that high throughput can be achieved. The second patterning step after absorber deposition and the third step after ZnO is done by mechanical scribing. Limitation of the scribing width is due to the limited adhesion of the CIS film on the Mo layer.

Selenization of Cu/In bilayers

There are three important steps in fabricating a CIS solar cell using the selenization process: deposition of the Cu-In precursor films, selenization of the Cu-In precursor films, and deposition of the window layers for junction formation.[73]. The way in which the selenization process is carried out affects the morphology, stoichiometric uniformity, and the resistivity of the CIS films. As a result of compositional differences in which some grains contain Cu-rich alloys and others have In-rich compositions, the kinetics of selenization vary from grain to grain. In-rich grains, for example, selenize earlier than the Cu-rich regions because of the existence of a liquid phase. Formation of In and Cu binary selenides in grains consisting mostly of In and Cu-rich phases respectively, makes it difficult for these large grain films to homogenize during the selenization period. As a result, CIS layers with poor compositional uniformity are obtained. The morphology of the CIS films obtained by the selenization technique also depends on the selenization process. Films with non-uniform grain sizes because they have been grown under Se-deficient conditions, yield solar cells with low V_{oc} values. This is due to the fact that Cu-rich secondary phases present in the large grains of such films give rise to shunting paths through the cells.

The precursor layer in [81] was selenized with elemental Se vapor in vacuum. Elemental Se vapor is supplied continuously from the 5 min ramp-up stage to the selenization stage. The selenization stage was carried out at 400 to 500 °C for 60 min with elemental Se vapor in vacuum. Se content of at least 30 to 40 at.% was required to

prepare a uniform precursor layer with sufficiently large grains. Careful control of Se content, which was directly linked to the control of In content, was required to fabricate device quality CIS films. A sufficient amount of Se is needed in the precursor layer to be supplied onto the precursor surface during the selenization stage for progression of a smooth reaction of In with Se.

Sputtering

Sputtering is probably the most readily scalable deposition technology for large-area coatings.[63], [62]. For example reactive magnetron sputtering has been found to be suitable for production of large solar cells uniform over the entire surface area. Films prepared by rf-sputtering of stoichiometric, cold-pressed, $CuInSe_2$ targets have been observed to be of a single-phase chalcopyrite structure with grain sizes of ~1μm when grown at temperatures above 500 °C. The grain size depends on the rf power and voltage, which probably results from modification of the energy distribution at atoms striking the growth surface. Energetic neutral atoms reflected from the target may account for the loss of Se at low gas pressures observed for Ar^+ rf-sputtering of $CuInSe_2$. The addition of substrate bias has been found to decrease the Cu/In atom ratio in the films and to lead to type conversion from p to n, accompanied by a large increase in film resistivity near the conversion point. Another sputtering technique used to produce is hybrid sputtering.

An example of pilot line consisting of two systems, one for sputtering of metals and the TCO and the other for selenization for manufacture of $Cu(In,Ga)(S,Se)_2$ thin film photovoltaic modules, is presented in [77]. Molybdenum and copper are deposited by DC magnetron sputtering. Selenium and the binary selenides of In and Ga are deposited independently by physical evaporation from linear deposition heads. The binary sources are preferred over the elemental ones because a significantly lower temperature is required for an identical vapor pressure. An advantage of sequential deposition stages is that each step may be optimized independently for uniformity.

Close spaced vapor transport

Close-spaced vapor transport technique in a closed reactor is a low cost and potentially large area growing method to deposit $CuInSe_2$-type thin films.[82]. The bulk materials were obtained from crushed powder of ingots made of the stoichiometric mixture of the Cu, In(Ga) and Se(S) elements. Solid iodine was used as the reagent. The temperature gradient between the source and the substrate is adjusted. The reaction begins when the iodine pressure is high enough. The source and substrate temperatures are thus stabilized and remain rather constant during the deposition. The iodine pressure is determined by the lowest temperature in the reactor.

The microstructure of the films is determined by the source and substrate temperatures, the temperature gradient, and also by the crystallinity of the substrate. The electrical conductivity of the films strongly depends on the source and substrate temperatures and the iodine pressure. At low source temperature (< 500 °C) the films are

degenerated p-type. When the source and substrate temperatures increase, the p-type conductivity decreases and the films become insulating. The n-type conductivity increases with the source and substrate temperatures. The transition temperatures strongly depend on the pressure in the reactor, i.e. the iodine pressure: the temperatures are decreased when the iodine pressure decreases.

2.2.6 Degradation mechanisms

In [83] an investigation on the influence of humidity on the CIGS absorber is reported. Two different Na species can be found on CIGS thin film surfaces. The first, "passivated" species is detected after air exposure and segregation at room temperature, while the second, "metallic" species with a bonding character intermediate between ionic and metallic, is found after thermally activated segregation and after deposition of metallic Na. The passivation of Na under ambient conditions is due to an interaction with H_2O, leading to a reacted species and a passivation against further chemical reactions. The Na concentration has an influence on film morphology and also on the electronic structure. In ambient conditions, in general the Na concentration is reduced by H_2O exposure. When increasing H_2O exposure without additional Na deposition, the work function is reduced as well, and can be attributed to a change of surface dipoles, as is consistent with the large dipole moment of H_2O. Na influences the electronic structure of a solar cell device when operated under humid conditions such that reaction products increase the work function, reduce surface (and interface) dipoles, and lead to an upward shift of the electronic bands. This will affect not only surface properties but bulk measurements of CIGS samples as well, provided they are sensitive to grain boundary effects.

Exposure to reverse bias may occur for single cells within a series connected module by the partial shading of the module.[69]. Significant Cu-electromigration can occur in CIS/CIGS cells at temperature of 340 K and under electrical bias, because of the built-in electric field at the junction and by the application of additional voltage bias. The increased electrical field at reverse bias drives more Cu out of the space charge region and displaces the space charge minimum farther away from the surface. However, after one hour of annealing at 340 K the system recovers the initial space charge distribution. The fact that Cu ions are driven into the absorber by reverse bias in not critical because they return under zero bias. Thus it is concluded, that Cu-migration does not degrade the long term stability of $Cu(In,Ga)Se_2$ and $CuInSe_2$ based devices.

2.3   CdTe

The first CdTe based solar cells were made as CdTe/Cu$_2$Te composition but instabilities caused by Cu diffusion lead to the presently most common heterojunction composition of CdTe/CdS. The main drawback of this composition was the insufficient p-doping level and as a consequence, a rectifying back contact [84]. The deposition techniques used for obtaining above 10 % efficiencies on small cells are electrodeposition, close-based sublimation, chemical spraying and atomic layer epitaxy (ALE). The raw materials, Cd and Te, are relatively inexpensive and available in reasonable quantities [85]. However, cadmium is classified as an environmentally harmful material.

CdTe has been considered as one of the more promising solar cell materials because of its 1.45 eV direct band gap [84]. As a consequence of the direct energy gap the absorption edge is very steep, and thus 90 % of the incident solar light will be absorbed in a few micrometers of the material. The maximum photocurrent available from a CdTe cell under the standard global spectrum normalized to 100 mW/cm^2 is 30.5 mA/cm^2 [86] and the theoretical maximum efficiency of CdTe is over 27 % [85], [26].

2.3.1   CdTe film properties and device structure

When growing good films for solar cell application, the following basic properties are important: stoichiometry, growth morphology and grain boundary behavior, doping, and contacting.[84]. Stoichiometry can be easily established if the films are deposited or post-annealed at elevated temperatures at which the compound has a very low vapor pressure compared to the elements. The favorable growth properties of CdTe films are mainly due to the crystal structure. If viewed perpendicular to the (111) direction, the lattice exhibits alternate layers of hexagonally arranged Cd and Te ions. These layers have a strong tendency to grow parallel to the substrate, largely independent of the nature of the substrate. The II-IV films also show only very small grain boundary influence on overall electronic properties.

Due to low thickness of the CdTe films, very high doping is not needed and thus doping levels around 10^{15} cm^{-3} do not produce significant series resistance. In, Ga, Al, Cl, Br and I form donors, P, As, Sb and Cu are more commonly used as acceptors for intentional doping. At elevated substrate temperatures, native p-doping is observed, which can still be enhanced by the presence of oxygen during growth. There has been some problems in attaining good ohmic contacts to p-type films.

All solar cells involving CdTe as active material contain a highly transparent and n-conducting partner to CdTe which induces a depletion region in the mostly p-conducting CdTe film.[84], [87]. This partner may be a metal or a transparent conductor or a highly doped semiconductor such as CdS or ZnO. The most common combination is p-CdTe/n-CdS. In spite of relatively high lattice mismatch between CdTe and CdS (~10%), the interface seems to behave well, and especially recombination centers seem to be considerably reduced in comparison to the clean surface. CdS acts as a filter for

solar light, having a cut off at 514 nm. The theoretical loss in short circuit current is around 5 mA/cm^2. This can be avoided to a certain extent by using a very thin CdS film as partner to CdTe, which will preserve the major properties of the cell such as the open circuit voltage.

The electrical resistivity of CdS film is an important factor affecting the solar cell characteristics. The increase in conductivity under illumination is due to the excess carriers in the grains introduced by the absorption of above bandgap radiation and the lowering of potential barriers at grain boundaries. The dark resistivity of as-deposited CdS films of 1000 Å thickness is usually on the order of 10^4-10^5 ohm-cm. This type of CdS film is suitable for solar cell purposes. CdS is suitable as a transparent electrode because it can be easily n-doped with rather high conductivity by introducing substitutional donors or creating donor-type S-vacancies. Its use as TCO reduces the requirements with respect to the grid spacing for low resistance current collection. If the CdS thickness is reduced for increased photocurrent, an additional transparent electrode must be used, most commonly SnO_2 or ITO (Indium-Tin-Oxide). ZnO layers deposited onto CdTe crystals have also been studied in order to form heterojuctions. Also the ZnO films can be highly n-doped and thus used as transparent conductors.

When depositing the thin film layers in the case of CdS/CdTe cells, the stacking order can be changed.[84]. If the transparent semiconductor is looking away form the substrate, the cell is called frontwall type and can be produced on opaque substrates. If the transparent conductor is adjacent to the substrate, the cell is said to be backwall type and needs to be produced on a transparent substrate. The properties of thin II-IV films are different depending on whether they are grown on a neutral substrate such as glass covered with a metal back contact film or on a CdS film of a given crystal structure and morphology. Similarly, a difference has been observed between the ohmic contacts when depositing CdTe onto the contact material or depositing the contact material onto CdTe. Usually the backwall cell is considered as a better alternative (Figure 2.4).
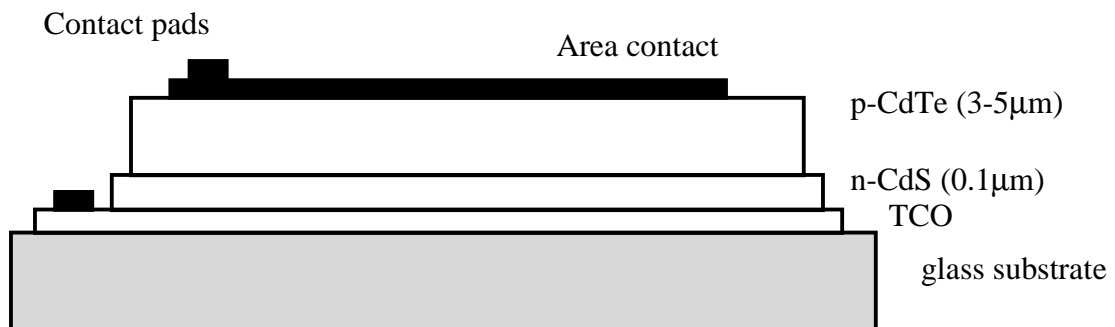

Contact pads

Area contact

p-CdTe (3-5μm)

n-CdS (0.1μm)

TCO

glass substrate

Figure 2.4 *Most common layer sequence of the CdS/CdTe thin film solar cell [84].*

It has been determined that the dominant current transport mechanism in the CdTe cells is recombination in the space charge region.[88]. Dark and light IV have been consistently modeled using Equation 2.1:

$$J = J_0 \left(e^{\frac{q(V-Jr_S)}{AkT}} - 1 \right) + \frac{(V - Jr_S)}{r_{SH}} - J_L \qquad \textbf{2.1}$$

where r_S and r_{SH} are the series and shunt resistance respectively, A is the diode quality factor, J_L is the photocurrent, and J_0 is the reverse saturation current. The reverse saturation current is given by Equation 2.2:

$$J_0 = \frac{kTn_iW}{2(V_{bi} - V)\tau} \qquad \textbf{2.2}$$

where k is the Boltzman's constant, T is the temperature, n_I is the intrinsic carrier concentration, W is the space charge width, V_{bi} is the built-in voltage and τ is the lifetime. Typically the diode quality factor was found to be in the range of 1.4-1.9, and the reverse saturation current in the range of 10^{-12}-10^{-9} A/cm^2. The best cells are characterized by low A's and J_0's. As cell performance degrades both A and J_0 increase.

2.3.2   The back contact problem

One of the principal barriers to obtaining high efficiency CdTe solar cells is the resistive and/or unstable contact to p-type CdTe. The difficulties come from the compensation mechanism of II-VI semiconductors and of the large work function for p-type CdTe.[89], [90], [26], [91], [92]. In these cases, contact schemes that rely on quantum-mechanical tunneling at the contact interface are typically investigated. These types of contacts are usually produced by doping the semiconductor heavily at the contact interface. Unfortunately, this approach is limited by the inability to produce a p-CdTe layer with sufficiently high p$^+$ doping because of acceptor compensation.

An alternative technique to form ohmic contacts is to use a separate interfacial layer between the metal contact and the p-CdTe, such as CdTe:Te, Cu$_2$Te, ZnTe:Cu, or HgTe or by processes in which the contact materials such as Cu/Au layers or carbon paste containing Hg or Cu salts are applied to a suitably prepared surface and then heated. The interfacial layer must provide both a negligibly small valence-band discontinuity with the p-CdTe, and also be able to be doped highly p-type (~10^{18}-10^{19} cm^{-3}) at the outer metal contact to facilitate low resistance tunneling.

Pseudo-ohmic contacts to CdTe films for thin film CdS/CdTe solar cells have been made by evaporation of Au-Cu alloy, and by evaporation of the Au-Cu$_2$Te layer. The Cu diffusion into CdTe probably forms a heavily p-type doped surface layer to promote tunneling through the metal-semiconductor barrier, leading to an ohmic contact behavior. During the stability test at room temperature, an appreciable amount of Cu and Te diffused out through the Au layer and accumulated at the surface. The compositional change of the Au-Cu$_2$Te/CdTe interface resulted in degradation due to an increase in the series resistance of CdS/CdTe solar cells with Au-Cu$_2$Te contacts to CdTe film.

The diffused Cu contact process consists of deposition of a Cu layer on the CdTe surface, heat treatment of the entire structure, etching, and application of the desired current-carrying contact material. After rinsing in methanol the samples were contacted with the different current carrying conductors such as Ni, Cr, Pt, Mo, carbon paste, and indium-tin oxide (ITO). The choice of contact materials can be also based on manufacturing issues instead of on CdTe requirements. The diffused Cu contact yields similar performance to that obtained with the baseline Cu/Au contact. Optimum V_{oc} is obtained when sufficient Cu is diffused into CdTe. The reaction with $Br_2:CH_3OH$ forms a conductive layer on the CdTe consisting of either elemental tellurium or copper telluride of composition Cu_xTe. The contacting process discretely separates Cu diffusion doping of the CdTe layer from the formation of a conductive surface, permitting independent control of each step. The process is applicable to CdTe devices made by different methods. V_{oc} and bulk series resistance, which are related to doping of the CdTe layer, can be controlled by the treatment time.

Copper acts as a substitutional acceptor for Cd, thus increasing the doping concentration near the surface of p-type CdTe to form a good ohmic contact. Cu also may form interstials or Cu defect complexes which can act as recombination centers. Cu in CdTe can diffuse into the underlying CdS layer, causing a decrease in cell performance. The use of Cu forms a better ohmic contact on CdTe, but excess Cu may diffuse into the CdTe film and short the device. Cu diffusion could form shunt paths or recombination centers to degrade cell performance. The Cu observed in the CdTe arrives by diffusion during the metallization process and not as result of heat treatment. For polycrystalline CdTe solar cells, the penetration of the Cu into the CdTe may be enhanced by diffusion along grain boundaries. The thickness of Cu plays a critical role in the CdTe solar cell performance with Au/Cu contacts. Increase in Cu thickness results in a better ohmic contact which reduces the R_s, but the excess Cu causes shunt paths or recombination centers, which tend to lower the R_{sh} and cell performance. Thus a greater thickness of Cu increases Cu density in the cell, reduces R_{sh} and leads to degradation in cell performance.

Also tellurium has been tried as a back contact material for CdS/CdTe solar cells but it caused stability problems. In such cells the primary mode of degradation was a loss of open circuit voltage, the degradation rate was strongly dependent on temperature and the degradation was not reversible. Similar results were obtained using gold or nickel electrodes. A graphite electrode indicates good stability when adequately encapsulated. The principal mode of degradation, which an unencapsulated cell using this improved electrode can exhibit, is an increase in series resistance due to an overexposure to humidity.

2.3.3 Module fabrication after film deposition

In the monolithic series interconnect the available device area is divided into individual cells which are then connected into series.[93]. The isolation and interconnection can be achieved by laser scribing. A first laser cut penetrates to the glass

isolating cells and the second cut stops on the tin oxide (Figure 2.5). The area occupied by the three cuts does not generate power and therefore it is important to minimize the width of this inactive region.

Initial packaging techniques in for CdS/CdTe solar modules employed a conventional ethylene vinyl acetate (EVA)/Tedlar lamination method in which the EVA was fully adhered to the back contact of the device. This lamination process produced an increase in the series resistance. This led to the development of edge seal techniques on which the active area is not in physical contact with the sealant. The glass substrate was laminated to an oversize front cover glass with the border created being used for the edge seal.
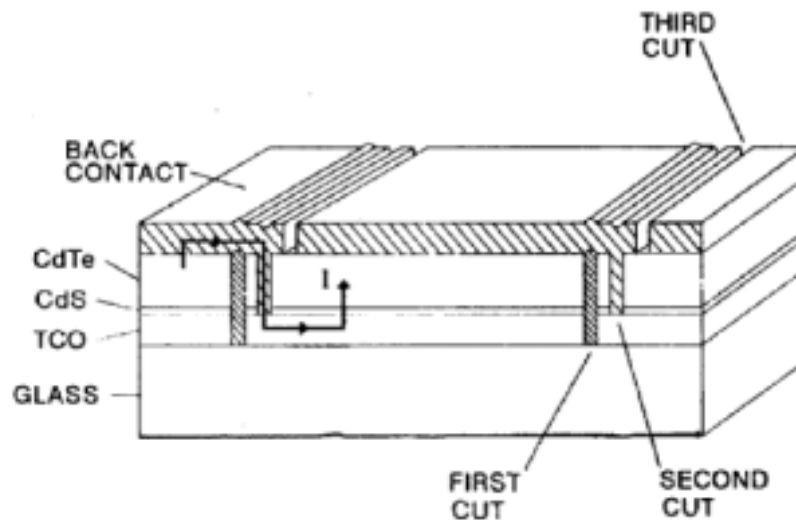

Figure 2.5 *Cross sectional view of the monolithic series interconnect [93].*

2.3.4 Production methods

Any process that can deliver a near-stoichiometric ratio of Cd and Te onto a substrate can yield polycrystalline CdTe films provided that the deposited layer has mechanical integrity.[94]. The following general design rules concerning the window layers and the ohmic contacts are generally followed in processing high efficiency thin film CdTe/CdS solar cells. First, cells have the superstrate device configuration in which the CdTe film is deposited over a transparent CdS/TCO/glass substrate. Second, the thickness of the CdS layer is minimized to improve the short wavelength response of the cell. Third, CdTe layers are chemically treated before an appropriate contact material is deposited on them. The etchants typically leave a low-resistivity p-type Te-rich surface which allows the formation of a tunneling contact to the high resistivity p-CdTe film. A p-type dopant such as Cu is usually introduced at the contact/CdTe interface. Most widely used contact materials are graphite and Ni. An annealing step after the contact deposition generally lowers the contact resistance due to the activation of the Cu dopant at the contact/film interface.

In addition a high temperature heat treatment, oxygen and $CdCl_2$ are also

important ingredients in CdTe solar cell fabrication process.[94], [95]. It is well known that electrical properties of CdTe are dominated by impurities in the material as well as its native defects and defect impurity complexes. The relatively open crystal structure and the ionic nature of this compound allow easy formation of native vacancy and interstitial defects that are highly mobile even at low temperatures. Therefore, properties of CdTe thin films can readily be altered through thermal treatments. Oxygen is known to enhance the p-type character of CdTe thin films when such films are annealed in oxygen containing atmosphere at elevated temperatures. Oxygen is present in type conversion/junction formation (TCJF) which is the key step in processing thin film CdTe/CdS heterojunctions. Cd vacancy generation is the major mechanism responsible for the type conversion. The presence of oxygen in the film, on its surface and in its grain boundaries, helps the Cd vacancy generation process by acting as a sink for Cd.

Another important ingredient in the CdTe cell fabrication process, $CdCl_2$, is a well established fluxing agent for both CdS and CdTe and thus good quality CdTe crystals have been successfully grown from $CdCl_2$ solutions.[95], [96], [97], [94], [98]. High temperature processing or post deposition annealing in the presence of $CdCl_2$ results in both CdTe grain growth and interdiffusion of the CdS and CdTe films. 400 °C $CdCl_2$ heat treatment recrystallizes the CdTe and interdiffuses the CdS and CdTe layers. The amount of the diffusion of Te into CdS depends on the CdS thickness and structure. The device structure is most likely $CdS_{1-y}Te_y/CdTe_{1-x}S_x$ with the $CdS_{1-y}Te_y$ reducing the short wavelength spectral response and the $CdTe_{1-x}S_x$ enhancing the long wavelength spectral response. According to [99], $CdCl_2$ treatment is important in improving the CdTe/CdS performance. It appears to introduce a V_{oc} and efficiency limiting defect due to V_{Cd}-Cl complexes. V_{oc} and fill factor are a strong function of the $CdCl_2$ concentration while I_{sc} shows a weak dependence on $CdCl_2$ concentration. However, there has also been arguments against the $CdCl_2$ treatment. According to [100], $CdCl_2$ process mainly leads to an improvement of the electronic defect structure of the diodes and not to grain growth. The $CdCl_2$ process leads to a decrease of interface state density, but also produces unwanted defects in the space charge region.

The condition of the CdTe surface affects the resulting device efficiency as a result of its contribution to contact resistance.[26]. Therefore treatment of the surface, using various chemical rinses and etches, is of major importance for good device efficiency and stability. Understanding the growth and removal steps of the oxide at the surface is both a performance and stability issue. That is why in the end of the process the cell is exposed to Br_2CH_3OH treatment which increases both V_{oc} and FF.[96], [97]. Cell performance improves significantly following immersion in Br_2CH_3OH for five seconds at room temperature. The bromine reacts with Cd in the near surface region, producing excess Te which may react with Cu, to form Cu_2Te, and with Au, if that is used as back contact material, forming an ohmic contact with p-type CdTe. The treatment increases V_{oc} and FF but no change can be observed in I_{sc} or spectral response. The increase in V_{oc} is attributed to a chemical interaction along the CdTe grain

boundaries and the increase in FF results because of reduction in the series resistance.

Even though borosilicate glass has better properties than soda lime glass (thermal expansion coefficient, impurity content, optical transmission etc.) in order to keep material costs down it is necessary that thin film PV modules are fabricated using inexpensive soda lime glass.[88]. It therefore becomes necessary to maintain processing temperatures below 550 °C. The most significant change affecting device performance was found to be a change in the structural properties and density of CdTe films.

2.3.5   CdS layer deposition

In [93], the CdS films for CdS/CdTe solar cells are deposited with chemical bath deposition. The chemical bath deposition or electroless technique is based on the reaction of a cadmium salt, a complexing agent and a sulphur compound in an aqueous solution. The process therefore relies on slow release of Cd^{2+} ions and S^{2-} ions in solution. The formation of CdS takes place heterogeneously on a suitable substrate placed in the bath and homogeneously in the solution.

Rf-sputtering and close spaced sublimation have also been used to deposit CdS.[88]. These processes offer manufacturing advantages over chemical bath deposition, and do not generate large amounts of liquid waste that add to manufacturing costs. Continuous and pinhole free CdS films were deposited with rf-sputtering. The films consist of small grains but the grain size increase with increasing substrate temperature. The most critical close spaced sublimation (CSS) process parameters for the deposition of CdS films are the substrate/source temperatures and the ambient conditions. For inert ambients such as those containing He, it was found that the films contained pinholes for low substrate temperatures (400°C) and high deposition rates. Increasing the substrate temperatures (500°C) resulted in pinhole free films. Considerable changes in film structure were observed when the depositions were carried out in the presence of O_2. Oxygen may act as a transport agent as well as be incorporated in the films to form defect complexes. The use of O_2 was found to be beneficial since it yielded pinhole free films over a wide range of deposition conditions. The presence of O_2 however also reduces the deposition rate and increased the thickness variation over the substrate area.

2.3.6   CdTe layer deposition

Close spaced sublimation

In close-spaced sublimation (CSS) CdTe is sublimed from a solid source.[100], [87], [98], [101]. The deposition of CdTe films by CSS method is based on the reversible dissociation of CdTe at high temperature in an inert gas ambient at a pressure of ≤ 1 mbar. The CdTe dissociates into its elements $(2CdTe(s) \rightarrow 2Cd(g) + Te_2(g))$ which recombine on the substrate surface to form the CdTe film. The source material is maintained at a higher temperature than the substrate. The source CdTe dissociates into its elements, which recombine on the substrate surface depositing CdTe films. Since the

rate of sublimation depends strongly on the source temperatures and the gas pressure in the reaction tube, the rate of CdTe deposition varies similarly. At low substrate and evaporation temperatures, the films grow disoriented, however, at evaporation temperatures greater than 650 °C, the films become highly oriented. CdTe layers deposited at low evaporation temperature grow oriented if the substrate temperature is greater than 350 °C. The substrate and source, separated about 0.2 cm and supported by appropriate holders, are enclosed in a controlled atmosphere in a fused silica tube with gas inlet and outlet tubes. They are maintained at desired temperatures of about 600 °C by using quartz lamps, and thermocouples inserted into the holders were used to control their temperatures. The close-spacing of source and substrate provides direct transport of each component of the source across the space to the substrate. The microstructure CdTe films is determined by the substrate temperature, source-substrate temperature gradient, and the crystallinity of the substrate. In general, the grain size increases with increasing substrate temperature and increasing film thickness. However, higher temperatures not only promote larger grain sizes, but also increase the size of voids or pinholes between grains. Voids between grains effectively reduce V_{oc} by providing shunt paths between the back and front contacts. The changes in the chemical composition of the CdTe thin films are caused by variations in the substrate and evaporation temperatures and could be attributed to the different sublimation temperatures and condensation rates of the Cd and Te species. Growth rates of 5 to 10 μm/min are easily achieved with CSS.

Electrodeposition

Thin film electrodeposition of CdTe offers an inexpensive and easily scalable means of producing large area devices utilizing a technology readily adaptable to an industrial manufacturing process.[100], [93], [102]. Aqueous electrodeposition is an attractive method for large scale use because it is a technique used in industry for various purposes. It uses relatively cheap equipment, minimizes material usage, clean-up from spent solutions is readily accomplished, and it reduces the health hazards of the toxic components used. Furthermore, solutions can be used for long periods. In electrodeposition films of CdTe and similarly CdS are formed from aqueous solutions of $CdSO_4$ and Te_2O_3 at temperatures of around 90 °C. In general terms the overall deposition process may be represented by two steps: tellurium reduction $HteO_2^+ + 3H^+ + 4e^- \rightarrow Te + 2H_2O$, and the reaction of deposited tellurium with the Cd^{2+} ions in the solution $Te + Cd^{2+} + 2e^- \rightarrow CdTe$. In the electrodeposition process there is a substantial number of variables whose influence needs to be understood and controlled. These include the type and concentration of species in solution, the electrodeposition method chosen and its parameters, the design of the deposition system, the flow geometry and the solution temperature. Grain size enhancement and improvement of microstructure be thermal annealing processes lead to films of high photoelectronic quality. Low deposition rates can be compensated by parallel deposition.

Screen printing

The screen printing process consists of subsequently screen printing, drying and sintering of first CdS, then CdTe films and back contact, e.g. graphite, layers.[100], [103], [104]. As compared to other technologies, screen printing usually leads to thick layers (10-20 μm compared to some μ), and requires rather high fabrication temperatures. The sintering is performed in a belt type furnace, under N_2 atmosphere at temperatures ranging from 575 °C to 700 °C. The CdS paste is obtained by mixing CdS powder and $CdCl_2$ powder with propylene glycol. The $CdCl_2$ acts as a flux to promote particle fusion and granule regrowth of CdS. The CdS film thickness is about 30 μm. During sintering the $CdCl_2$ is evaporated from the film. The paste for CdTe layer contains Cd and Te powders which are milled in H_2O, and $CdCl_2$ powder and propylene glycol. The simplicity of the production process is the special aspect of this technique.

In CdS-CdTe solar cells prepared by the screen printing and sintering technique, a certain number of intermixing of CdS and CdTe layers occur during the sintering of the CdTe layer on top of the CdS layer base. It is a consequence of the high sintering temperatures (600 °C and up) and is strongly associated with the presence of liquid $CdCl_2$, which is used as a sintering flux. Interdiffusion has to be minimized if one is to obtain high V_{oc} and good response in the short wavelength region, and hence a high short circuit current. For all heat treatment temperatures the presence of copper in the graphite paste significantly enhances both V_{oc} and I_{sc}, and in most cases also FF. Copper, which acts as a p-type dopant to CdTe, diffusing into the CdTe during the heat treatment of the carbon electrode is significantly altering the semiconductor properties. Even in the vicinity of the junction it affects such properties as collection of light generated current and V_{oc} buildup. The morphology of the structure of screen printed and sintered cells benefits from the particular properties of sintering (high temperature and the presence of liquid $CdCl_2$): micrometer sized grains are in contact at the junction.

Atomic layer epitaxy

Atomic Layer Epitaxy (ALE) is a thin film growth method, which is based on sequential chemical reactions on the surface.[100], [105], [85]. It is very suitable for II-VI compounds thin film deposition. Characteristics of thin films produced by ALE are good crystallinity, excellent uniformity over a large area and a low pinhole density. ALE offers the possibility to grow both CdS and CdTe layers in a single process. Low pressure type ALE reactor is based on reactant transport and valving with computer controlled inert gas flow. The reactor is equipped with four individually controlled sources for solid reactants inside the reactor body and a definable number of external sources for gas and liquid reactants. The reaction zone consists of a 1-3 mm space between two 50 x 50 mm^2 substrates. The lateral flow through the reaction zone ensures an effective reactant/substrate interaction resulting in high material efficiency. Cadmium sulphide films are grown using elemental Cd and S as reactants. A possible process temperature range is 300–500 °C. CdTe layers are grown in the temperature range

between 350 °C and 440 °C using elemental Cd and Te as reactants. All the layers are processed in one run and at the same reaction temperature. To minimize the effects from the lattice mismatch between CdS and CdTe on the electrical function of the heterojunction, a graded layer is processed between CdS and CdTe in which the CdS/CdTe proportion is gradually changed from pure CdS to pure CdTe.

Chemical vapor deposition

In chemical vapor deposition volatile, thermally decomposable organic compounds of Cd and Te are transported in gaseous form by a carrier gas at ambient pressure towards the heated substrate where they decompose and form CdTe.[100].

High-vacuum evaporation

High-vacuum evaporation creates films by evaporation of CdTe from a heated crucible and its condensation on the heated substrate in high vacuum.[100]. Grain-size enhancement and recrystallization by thermal annealing processes have led to moderate efficiencies. High-vacuum equipment is technically mature and commercially available.

Chemical spray pyrolysis

In chemical spraying an aerosol of water droplets containing heat decomposable compounds of Cd and Te is sprayed onto a heated substrate forming a CdTe film. A CdS film for generating heterojunctions is created in a similar way.[100]. Due mainly to very small grain size cells with rather low efficiency have been obtained.

An example of a large area CdS/CdTe prototype module fabrication process based on spray pyrolysis is presented in [26]. A 0.5 – 1.2 µm film is deposited on commercial 3-mm float glass of tin oxide by spray pyrolysis. The deposition temperature is ca. 480 °C. A CdS film of 6 µm thickness is deposited on top of the tin oxide and subsequently approximately 6 µm of CdTe is deposited onto the CdS. CdTe is made conductive with phosphorus. After Br_2/MeOH etch and subsequent NaOH soak to remove the surface oxide, a graphite electrode is deposited on top of the CdTe to a thickness of ca. 10 µm. A more-conductive electrode containing tin is evaporated on top of the structure to complete the device.

2.3.7   Efficiency loss mechanisms

When comparing the solar spectrum and the spectral response of CdTe material, some efficiency loss mechanisms can be identified.[86]. Near the bandgap cutoff the associated loss is assumed to be due to photons that penetrate sufficiently deep that the electron-hole pair generated is not collected. At mid-wavelengths the curves generally have a reflection loss component. A major loss, due to window absorption of photons with greater energy than the window bandgap, dominates the short wavelength curves.

The quantum yield spectra of the electrodeposited CdTe cells showed that the better cells had fewer losses in the higher wavelength region at forward bias compared with less efficient cells.[102]. The loss mechanisms operating for the better cells were

related to interface rather than bulk processes. The growth conditions of the CdTe affects the number of grain boundaries and hence increases the likelihood of loss mechanisms.

2.3.8 Degradation mechanisms

The CdTe/CdS cells are known to be sensitive to moisture induced degradation.[99], [7]. Use of Cu-Au contacts has shown noticeable degradation in high efficiency cells. This degradation in efficiency is associated with significant reduction in V_{oc} and fill factor and a modest decrease in I_{sc}. After the rapid initial degradation the cell efficiency nearly stabilizes. The oxidation of Cu or Te is the probable cause of cell degradation. Br:MeOH etch is able to reduce oxides and restore both V_{oc} and fill factor values to almost 90 % of the original values.

The remarkable effect of oxygen on the photovoltaic properties seems to be common for II-VI and I-III-VI$_2$ compounds. A certain amount of oxygen is essential for the module to maintain its initial properties at a high temperature.[106], [104]. When modules that were protected from permeation of moisture and outer environmental gases are exposed to a strong light or to a high temperature, the component materials used in the modules decompose to form organic radicals that react with oxygen surrounding them. When the concentration of oxygen is gradually degreased by the reaction and finally decreased to a critical value. The recovery of photovoltaic properties by sufficient oxygen when first degraded due to oxygen deficiency in a sealed module, may be the same phenomenon as increase in p-type characteristics in high resistivity CdTe by heat treatment in air in other fabrication processes. It is most probable that chalcogen elements are responsible to the effect. Oxygen is also a chalcogen element and it may be rather easy that oxygen occupies the Te position in CdTe, by replacement or by filling of existing chalcogen defects.

The most delicate feature of the CdTe/CdS device is believed to be the low loss back contact.[107], [95], [104]. Some devices subjected to stress testing or life testing display high series resistance and/or evidence of a reverse diode – both characteristics which could be attributed to the back contact. For example, increases in the series resistance of C back contact cells have been seen to result from an increase in the contact resistance between CdTe and carbon in the high temperature and humidity test and from an increase in the resistance of the carbon layer in the humidity test. The increase in the contact resistance was caused by a decrease in the adhesion between CdTe and carbon and the increase in the carbon resistance was due to a swelling of the carbon layer with water absorption. Reversible degradation effects in the CdTe/CdS devices include increases in series resistance and decreases in J_0 of the reverse diode upon application of reverse bias (with opposite changes upon forward bias). Permanent effects include an additional increase in series resistance and a reduction in collected photocurrent. Devices stressed in reverse bias display effects associated with degradation of bulk properties while devices stressed at forward bias display effects associated with a reverse diode. The light-dark crossover after reverse bias is interpreted as a manifestation of light induced changes in the internal electric field distribution due to changes in trap

occupancy or transient charge distribution. Thus, crossover is associated with bulk properties of the device including grain boundary effects. Forward bias results in the strengthening of a reverse diode. Forward bias may oxidize the surface $CdTeO_3$ and produce a rectifying contact on CdTe.

3. CALIBRATION MEASUREMENTS

3.1 Theory on calibration measurements

According to the IEC standard 6904-3 [108] the current practice to determine the photovoltaic performance of a solar cell or module is by exposing it at a known temperature to stable sunlight, natural or simulated, and tracing its current-voltage characteristic while measuring the magnitude of the incident irradiance. The measured performance is then corrected to Standard Test Conditions (STC). The STC conditions are defined to be such that the cell temperature is 25 ± 2 °C and the irradiance as measured with a reference device 1000 W/m^2 with the reference solar spectral irradiance distribution.

The calibration measurements at ESTI consist of the IV-curve calibration and the calibration of I_{sc} and V_{oc} values.[22]. The IV-curve is calibrated by measuring the electrical characteristics with two different pulsed solar simulators, SpectroLab LAPSS and Pasan LAPSS. In order to be able to correct the results to STC-condition also measurements of spectral response and temperature coefficients are performed. The calibration of I_{sc} and V_{oc} values is done by measuring them over the flash decay. This techniques shows the cell linearity with variable irradiance levels and the I_{sc} and V_{oc} values can be determined exactly at 1000 W/m^2. A comparison of the measurements is presented in the summarizing table Table 3.I below.

When following the IEC standards in the calibration procedure, as is done at ESTI, it has to be noted that the standards are made mostly for the measurements of c-Si materials and it is expected that the material being measured behaves linearily. This is also assumed in this work when measuring thin film samples since no other more specific standard exists for the measurements of these materials. However it is not implicit that the thin film materials behave linearly.

Table 3.I *Summarizing table of the measurements included in the calibration measurement procedure.*

Measurement	Parameters obtained/usefulness
IV/SpectroLab	IV parameters
IV/Pasan	IV parameters
I_{sc} vs. Irradiation	Reference cell material suitability, I_{sc} calibration
V_{oc} vs. Irradiation	V_{oc} calibration
Spectral response	Spectral mismatch factor
T coefficient	Temperature correction

3.1.1 IV-measurements

According to the IEC standard 6904-1 [109] in the following are some general current-voltage characteristics measurement requirements. The measurement connection should be done according to Figure 3.1 below. The irradiance measurements shall be made using a calibrated reference device which essentially shall have the same relative spectral response as the device under test. Short-circuit currents shall be measured at zero voltage using a variable bias to offset the voltage drop across the external series resistance. Alternatively, they may be determined by measuring the voltage drop across a precision 4-terminal fixed resistor provided that a measurement is made at a voltage not higher than 3 % of the device open-circuit voltage within the range where there is a linear relationship between current and voltage and the curve is extrapolated to zero voltage. When measuring with pulsed simulated sunlight the test device shall be mounted as near as possible to the reference device with their active surfaces in the test plane. When applying temperature and irradiance corrections to the measured IV-characteristics the procedures determined by the standard are applicable over an irradiance range of $\pm$ 30 % of the level at which the measurements were made. The measured current-voltage characteristics shall be corrected in case of irradiance to Standard Test Conditions or other selected irradiance value by applying the following Equation 3.1 [110]:

$$I_2 = I_1 + I_{SC}\left[\frac{I_{SR}}{I_{MR}} - 1\right] + \alpha(T_2 - T_1) \qquad\qquad \textbf{3.1}$$

in which I_1 is the coordinate of the measured characteristics point, I_2 is coordinate of the corresponding point of the corrected characteristics, I_{sc} is the measured short-circuit current of the test device, I_{MR} is the measured short-circuit current of the reference device and I_{SR} is the short-circuit current of the reference device at the standard or other desired irradiance. T_1 and T_2 are the measured and desired temperatures and α is the current temperature coefficient of the test device. When the measurement is effectuated at 25 $\pm$ 0.5 °C the last part of the equation disappears.

The IV-curves are measured with SpectroLab and Pasan large area pulsed solar simulators [111] which both conform the Class A simulator standards in IEC 904-9 [112]. The measurements are performed in dark rooms with either black curtains or black screens positioned between the lamp and the test plane in order to avoid reflections. An example of the arrangements can be seen in Figure 3.2 [113] below. With both SpectroLab and Pasan LAPSS a four terminal differential connection is used both the test and the reference device connections. The measured irradiance level is adjusted such that it does not exceed $\pm$ 20 % from 1000 W/m^2.
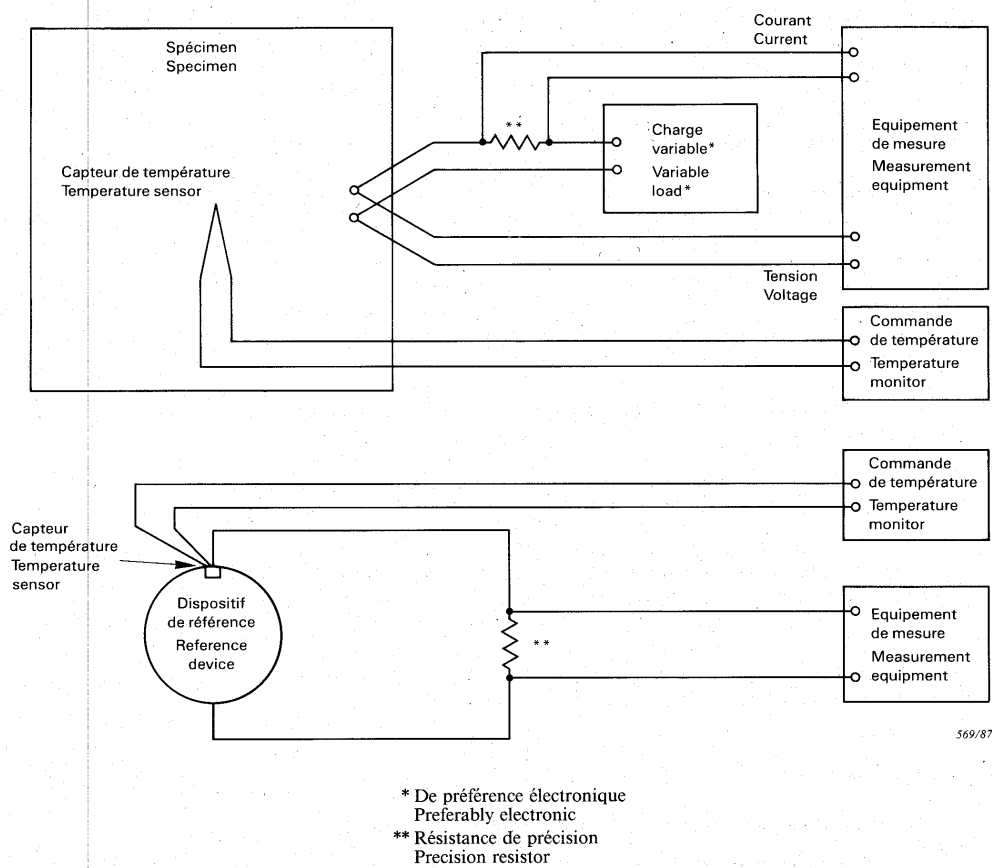
Figure 3.1 *Measurement connection for current-voltage characteristics measurement.*
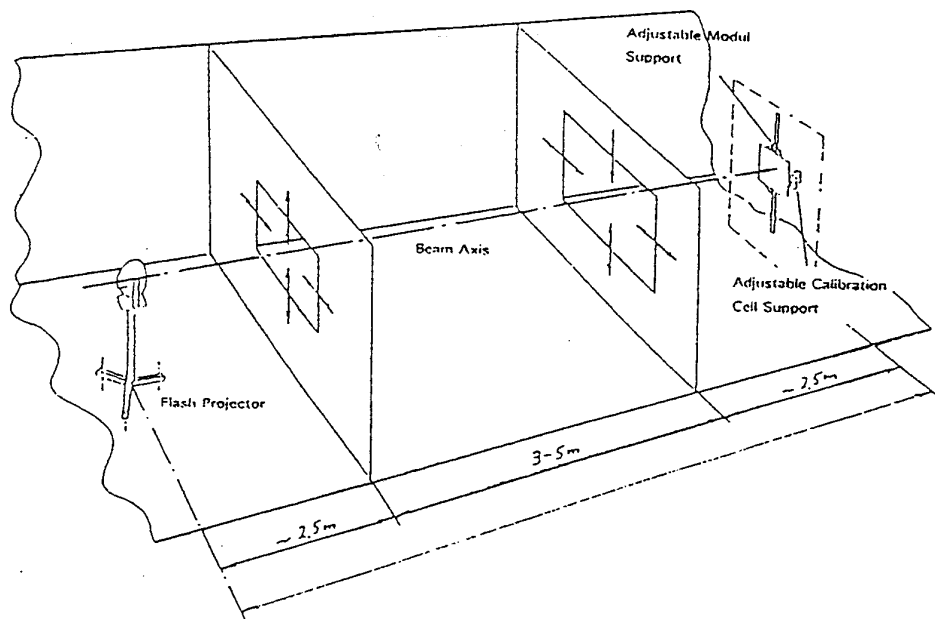*[109].*

Figure 3.2 *Darkroom arrangements for Pasan LAPSS measurement set up [113].*

SpectroLab LAPSS

The general measurement principle for SpectroLab LAPSS can be seen in Figure 3.3 below.[113]. The measurement system consists of two Xenon pulse flash tube lamps at 13 m distance from the test plane with possible irradiance range between 0.5 and 1.4 kW/m^2. The irradiance uniformity is ± 1.5 % on a test plane of the size 2.5 x 2.5 m^2 or ± 3 % on test plane of 5 m diameter. The flash generator operates such that when a pulse is required the generator is charged until the voltage level of 3 kV is exceeded and after approximately 3 s the pulse is released. The control unit has a voltage range of 1.0 - 100 V and a current range of 0.1 - 20 A with the accuracy of ± 1 % of full-scale. The shape of SpectroLab LAPSS pulse is rectangular, illustrated in Figure 3.4 [23] below. The flat part of the pulse at 1000 W/m^2 lasts for approximately 2 ms. The data is recorded with a 12-bit Krenz transient recorder which has four channels (4 x 8 kB) and the sample time can be varied between 1.0 μs and 20 ms. The test and reference device temperatures are measured with resistance temperature sensors Sigma Pt-100.
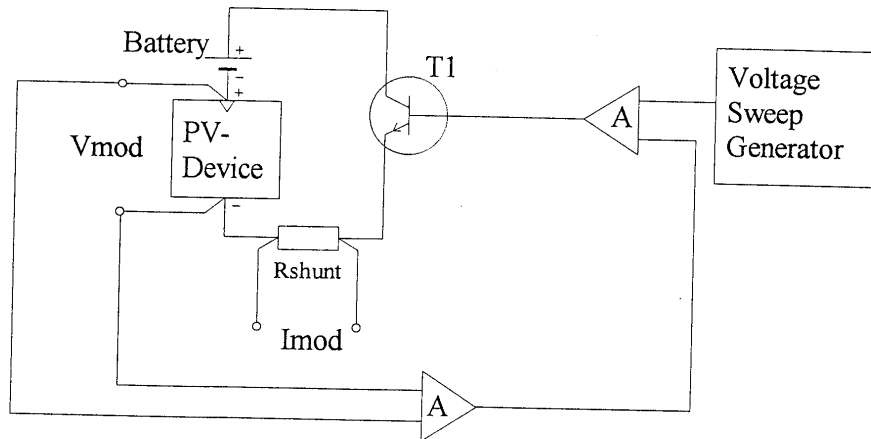

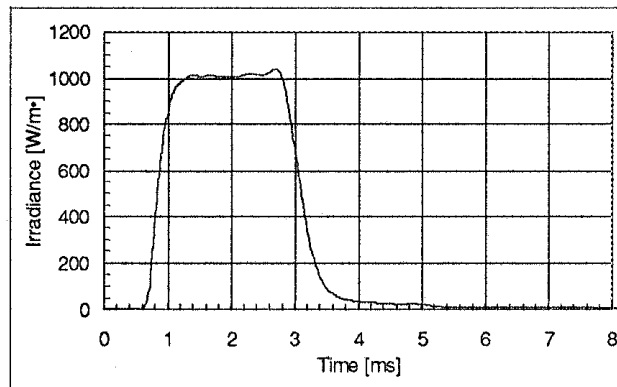**Figure 3.3** *Measurement principle of SpectroLab LAPSS [113].*

Figure 3.4 *The pulse shape of SpectroLab LAPSS [23].*

The actual measurement is effectuated as follows.[113], [23]. The IV-curve is measured at 25 ± 0.5 °C. During the 2 ms light pulse of the simulator and electronic load imposes a voltage ramp across the test device forcing it to deliver the corresponding current. The voltage and current ranges as well as the duration of the ramp electronic load are adjusted according to the test device size. The current is measured across a precision shunt and the voltage with separated contacts directly on the test device as can be seen in Figure 3.3 [113]. These measurement signals together with the irradiance signal of the reference cell are recorded by the fast transient recorder. The sample rate of the data aqcuisition system is set to 1 MHz per channel resolving the light pulse to a maximum of 1500 data samples depending of the duration of the voltage ramp (1.5 - 2.0 ms). In the beginning of the voltage ramp the test device is short-circuited whereafter the current decreases until at the end of the ramp the device is in open circuit and the IV-trace is completed. The software directly corrects the data to an average irradiance level of 1000 W/m^2 and creates the IV-curve.

Pasan LAPSS

The Pasan LAPSS IV characteristic measurement set up is very similar to that of SpectroLab LAPSS. The general set up for Pasan LAPSS can be seen in Figure 3.5 [114] below. The measurement system can be described as follows. The lamp used is a Xenon helical pulse low-pressure tube lamp. The lamp to test plane distance is set to 8 m and the irradiance can be varied between 0.25 and 1.2 kW/m^2. The irradiance uniformity is ± 1 % in test plane of 1.5 m diameter. The flash generator has a nominal energy of 12 kJ at 1300 V and when a pulse is required the generator charges about 30 s until the adjustable voltage level has been achieved and the pulse is released. The data is recorded with a similar Krenz 12-bit transient recorder to that of SpectroLab LAPSS with four channels available. The voltage range of the control unit is between 0.7 and 100 V and the current range between 0.1 and 30 A with an accuracy of ± 1 % of full-scale. The test and the reference device temperatures are measured with Sigma Pt-100 temperature sensors. The Pasan LAPSS pulse shape is a fast, a 3 ms long rising pulse followed by an exponentially for 40 ms decaying tale. The Pasan LAPSS pulse shape is represented in Figure 3.6 [23] below.

The IV-curve is obtained with Pasan LAPSS in a similar way to SpectroLab LAPSS. The IV-characteristics are measured at 25 ± 0.5 °C. The tracing of the IV-curve is started before the pulse reaches its peak value and ended after it thus using the pulse irradiance values closest to the 1000 W/m^2 values. Similarily to SpectroLab LAPSS the electronic load of the Pasan LAPSS imposes a voltage load on the cell or module. In the electronic load power circuit the current is measured over a shunt. In order to maintain a good voltage signal a shunt value as big as possible is chosen. However the shunt introduces some error to the measurement and thus the voltage drop across the shunt should not exceed 3 % of the open-circuit voltage or [113], [114]:

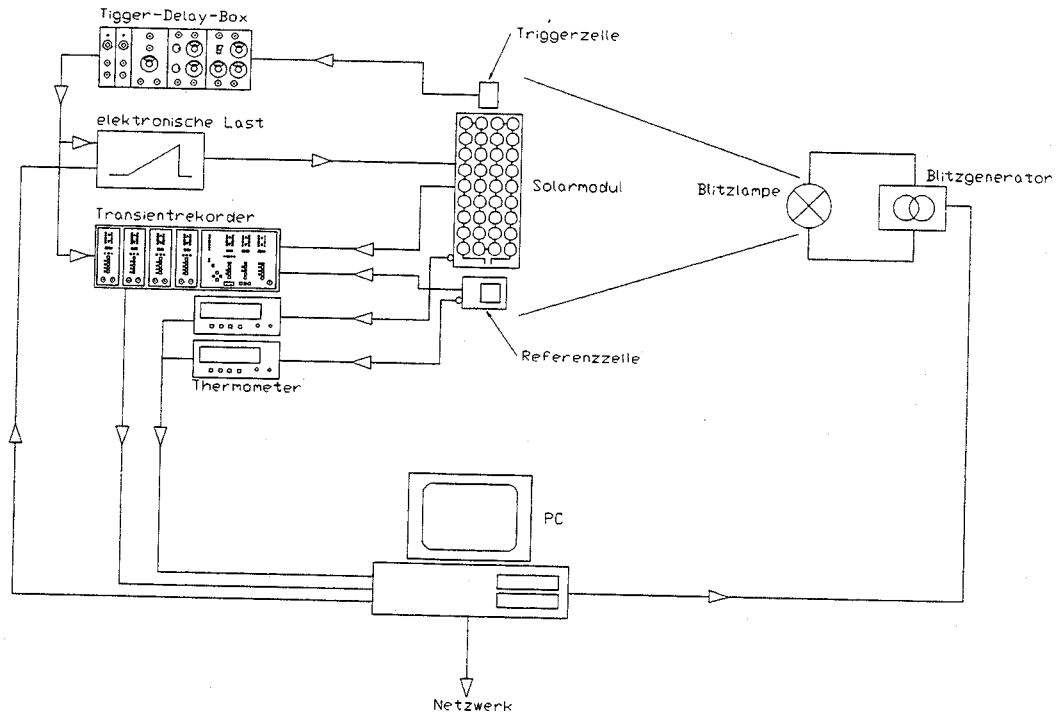$$R_{shunt} \leq 3\% \cdot \frac{V_{oc}}{I_{sc}}$$

3.2

Figure 3.5 *The general measurement set up for Pasan LAPSS solar simulator [114].*
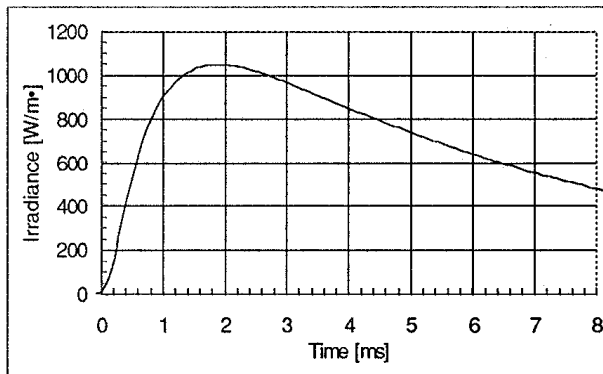
Figure 3.6 *The Pasan LAPSS pulse shape [23].*

3.1.2   Isc and Voc vs. Irradiation measurements

In addition to the IV-curve characterization the I_{sc} and V_{oc} values are calibrated by simultaneously reading the I_{sc} and V_{oc} signals of the test device and the irradiance signal of the reference device throughout the duration of the Pasan LAPSS light pulse decay. This technique results in electrical characteristics over a wide range of irradiance levels,

from about 1020 W/m^2 to about 150 W/m^2 and reduces the possible time effects during the relatively short IV-characteristics measurement. A linear least square fit of the I$_{sc}$ values yields the fitted I$_{sc}$ value at 1000 W/m^2.

The V$_{oc}$ values measured at different irradiance are plotted against the natural logarithm of the normalized signal of the reference device. As can be seen from the equations below the curve interception point with the y-axis represents the V$_{oc}$ value at 1000 W/m^2. By fitting a straight line through Equation 3.3 also the diode ideality factor n and the diode saturation current I$_0$ can be obtained.

$$V_{oc} = a \cdot x + b \qquad\qquad\qquad \textbf{3.3}$$

$$a = nkT / q \qquad\qquad\qquad \textbf{3.4}$$

$$x = \ln \frac{I_{sc\_ref}}{I_{sc\_ref\_1000}} \qquad\qquad\qquad \textbf{3.5}$$

$$b = -\frac{nkT}{q} \ln \frac{I_0}{I_{sc\_ref\_1000}} \qquad\qquad\qquad \textbf{3.6}$$

This method of obtaining the calibration factors assumes a linear relationship between the short-circuit currents of the test device and the reference cell especially at high irradiance levels.[23], [115], [116].

3.1.3 Spectral response measurements

Measurement procedure

According to the IEC standard the spectral response is measured as follows. The relative spectral response of a photovoltaic device is measured by irradiating it by means of a narrow-bandwidth light source at a series of different wavelengths covering its response range and measuring the short-circuit current density and irradiance at each of these wavelengths. As an alternative to the irradiance monitor is a previously calibrated reference photovoltaic device whose relative spectral response covers the required range. In this case the relative spectral response of the test specimen is computed as follows:

$$k_2 \cdot s_{2\lambda} = k_1 \cdot s_{1\lambda} \cdot \frac{J_{mt\lambda}}{J_{mr\lambda}} \qquad\qquad\qquad \textbf{3.7}$$

where k$_1$·s$_{1\lambda}$=the relative spectral response of the reference photovoltaic device at wavelength λ, k$_2$·s$_{2\lambda}$=the relative spectral response of the test specimen at the same wavelength, J$_{mr\lambda}$=the measured short circuit current density of the reference photovoltaic device at wavelength λ, and J$_{mt\lambda}$=the measured short circuit current density of the test specimen at the same wavelength. Special attention should be given to the uniformity of irradiance at the test plane and to the linearity of response of the short-circuit current of the device versus the light intensity at all illumination levels and all wavelengths. For

linear devices the bias light is also necessary unless there is proof that the obtained spectral response will not change significantly when the bias light is not used.[117].

The actual measurement set up for spectral response measurement at ESTI can be seen in Figure 3.7 [114] below. As indicated in the figure the Pasan LAPSS measurement system is used for the measurement. As a light source a 10000 J flash lamp is used in front of which a filter wheel is mounted. The filterwheel construction can be seen in Figure 3.8 [118] below. In the filter wheel (Figure 3.8) there are 18 interference filters each having a bandwidth of less than 50 nm covering a spectral area from 350 nm to 1100 nm.[113], [23], [114], [119]. Each filter assembly consists of four filters of the same wavelength assembled together into an aluminum frame and installed directly in front of the flash bulb. Since the monochromatic irradiance is always at least 10 W/m^2 the presence of bias light does not have practically any influence to the measurement result or the carrier generation in case of c-Si material and thus is not used. For thin film materials the need of bias light will be investigated but currently it is not used. The test plane covered has a diameter of 1 m on which a uniformity of ± 1.5 % is achieved.

The measurement is done by a relative spectral response method in which calibrated reference cell is used to monitor irradiance according to the standard described above. The short-circuit current of the test device is compared to that produced by the reference device according to the Equation 3.7 above when both are illuminated by the same monochromatic light. In the measurement set up the outputs of the test device and reference cell are recorded as voltage signals and thus no electronic load is used but instead some amplifiers to amplify the small signal of one wavelength band at a time. The triggering is done by a trigger cell mounted directly in front of the lamp and not into the test plane as in case of a normal IV-curve measurement.
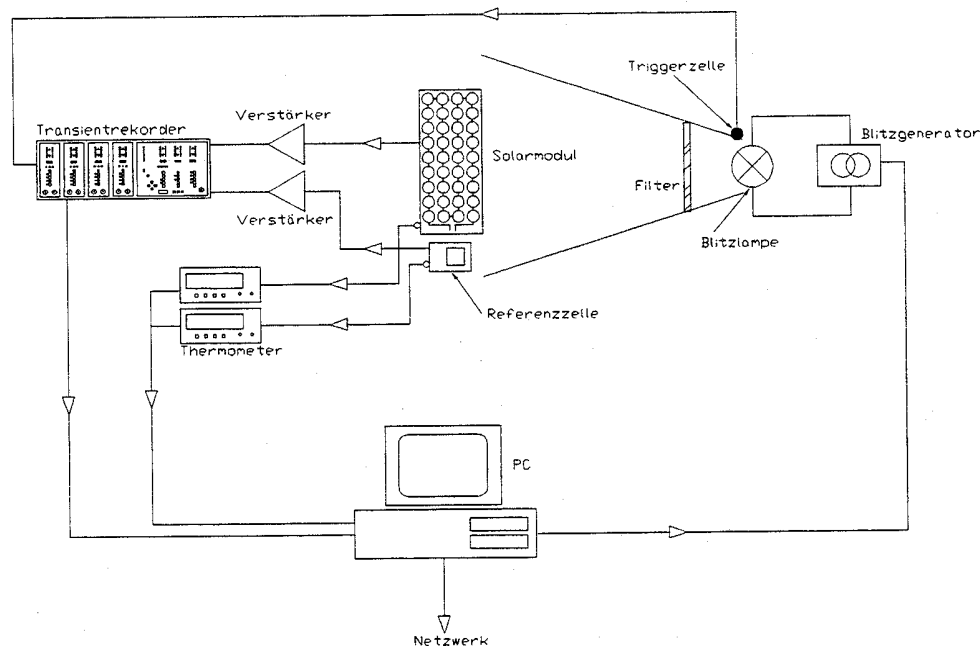

Figure 3.7   *The measurement set up at ESTI for spectral response measurement [114].*
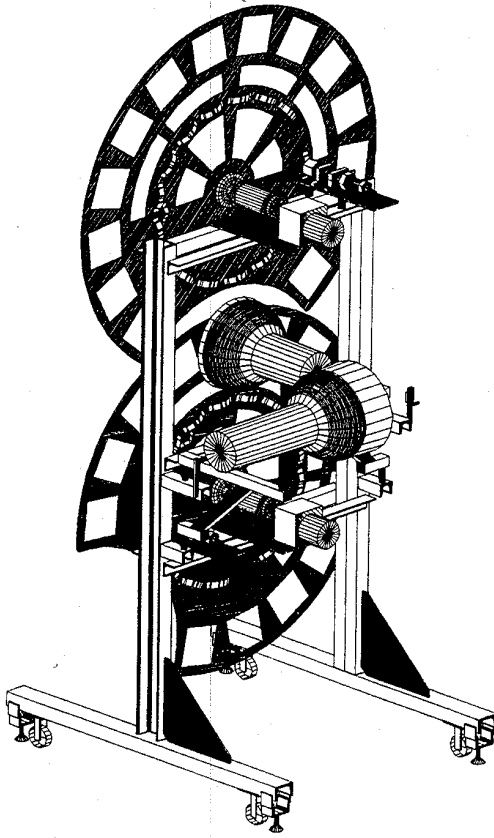
Figure 3.8   *The filter wheel used in spectral response measurement at ESTI [118].*

Spectral mismatch calculation

According to the IEC standard 904-7 [120] the spectral mismatch is defined and calculated as follows. The spectral mismatch error is calculated to correct for the error introduced in the testing of photovoltaic devices caused by the interaction of the mismatch between the spectral responses of the test specimen and the reference device, and the mismatch between the test spectrum and the reference spectrum. The error is computed from the integrated products of the relative spectral responses of the reference device and the test specimen and the relative spectral irradiances of the simulator and the reference solar spectral irradiance distribution.

The short circuit currents of the device under test and the reference device can be written in the following way:

$$I_{CS} = \sum E_{Si} R_{Ci} \Delta_i$$

$$I_{RS} = \sum E_{Si} R_{Ri} \Delta_i$$

$$I_{CA} = \sum E_{Ai} R_{Ci} \Delta_i$$
  3.8

$$I_{RA} = \sum E_{Ai} R_{Ri} \Delta_i$$

in which R_{Ri}=response of the reference device R and R_{Ci}=response of the cell C or test

sample at spectral position i and Δ_i=ith spectral interval width. In [120] and [121] the mismatch factor is determined according to Equation 3.9 below when using the relationships 3.8:

$$M = \frac{I_{CS} / I_{RS}}{I_{CA} / I_{RA}} \qquad\qquad \textbf{3.9}$$

When the source S is set so as to make $I_{RS}=I_{RA}$ and the parameter I_{CS} is being measured the current value for the sample under test can be determined for AM1.5G spectrum by applying 3.10:

$$I_{CA} = \frac{I_{CS}}{M} \qquad\qquad \textbf{3.10}$$

when M is according to Equation 3.9. However at ESTI the relationship 3.11 as below is used to calculate the mismatch factor. Equation 3.11 is actually a definition related to M in Equation 3.9 by: MMF=1/M and thus when implementing the factor it is rather multiplied by I_{CS} than devided by it as in Equation 3.10.

$$MMF = \frac{I_{RS} / I_{RA}}{I_{CS} / I_{CA}} \qquad\qquad \textbf{3.11}$$

3.1.4 Temperature coefficient measurements

The procedure to determine the temperature coefficients of modules according to the IEC 1215 standard [122] is the following. The temperature of the sample module should be monitored with a temperature sensor measuring to an accuracy of $\pm$ 0.5 °C. The measurement should be effectuated in a chamber capable of accomodating the module, equipped with transparent window and means for evenly heating and cooling the contents over the temperature range of interest. The sample should be mounted into the chamber and a suitable irradiance monitor or reference device outside the chamber within the simulator beam. When starting the measurement the short-circuit current of the module is first determined at the desired irradiance at room temperature the door of the chamber being open. Then the chamber is closed and the irradiance set so that the test module produces the short-circuit current determined when the door was open. This irradiance setting is monitored and maintained throughout the test. The module is then heated to the maximum temperature of interest, the heater switched off and the module allowed to cool evenly. As the module cools the measurements should be taken of the I_{sc} and V_{oc} at 5 °C intervals over a range of interest of at least 30 °C. The measurements are preferably effectuated with simulated sunlight of a pulsed simulator in order to create as little as possible additional heat that could affect the cell during the measurement. The measured I_{sc} and V_{oc} values are then plotted as a function of temperature and a least squares fit curve is constructed through the data. From the slopes of the current and voltage curves and at a point midway between the minimum and maximum temperature of interest the temperature coefficients α and β are calculated.

The current temperature coefficient α is applied according to Equation 3.1 and the voltage temperature coefficient β according to Equation 3.12 below:

$$V_2 = V_1 - R_S(I_2 - I_1) - KI_2(T_2 - T_1) + \beta(T_2 - T_1) \qquad \textbf{3.12}$$

in which I_1 and V_1 are co-ordinates of points on the measured characteristics, I_2 and V_2 are co-ordinates of the corresponding points on the corrected characteristics, T_1 and T_2 are the measured and desired temperatures, R_S is the internal series resistance of the test device, K is a curve correction factor and β is the voltage temperature coefficient of the test device.[110].

According to [123] systematic influences that occur during testing or system operation often result in apparent temperature coefficients that differ from anticipated values. For example physical irregularities such as junction boxes, metal module frames, or mounting brackets can introduce non-uniform temperature across the module (cells) during testing, which in turn results in measured temperature coefficients that are often smaller than the true values. Also the temperature coefficients for V_{oc} and V_{mp} are usually assumed to be independent of the solar irradiance level. Although this assumption is not strictly correct, it is a reasonable simplification at least for c-Si material. The temperature coefficient for I_{sc} and I_{mp} must be scaled by the ratio of the actual irradiance level to the irradiance level used for determining the coefficients. Contrary to practice in obtaining the temperature coefficients for the voltage and current parameters by calculating the derivative of the parameters versus temperature function, the derivative of maximum power with respect to temperature should not be considered a constant for a given irradiance level. The maximum power, P_{mp}, is the product of two factors, I_{mp} and V_{mp}, both of which vary with temperature and irradiance. Therefore the derivative or temperature coefficient should be calculated as in the following Equation 3.13 [123]:

$$\frac{dP_{mp}}{dT} = V_{mp} \cdot \frac{dI_{mp}}{dT} + I_{mp} \cdot \frac{dV_{mp}}{dT} \qquad \textbf{3.13}$$

At ESTI the temperature coefficients are measured with a measurement set-up shown in Figure 3.9 [114] below. For the measurement Pasan LAPSS flash simulator is used and the sample module is enclosed into a temperature controlled cabinet with a glass door to permit the cell to be illuminated. The reference device is mounted outside the cabinet but as close to the sample module as possible. When beginning the measurement a correction factor for the irradiance attenuation due to the glass is calculated and applied to the measured I_{sc} and V_{oc} data. As during the determination of α and β full IV-curves are measured a similar correction procedure allows the curve correction factor κ also to be determined.[113], [23]. On the contrary to the recommendation above of IEC 1215 [122] at ESTI the IV-curves are measured at different temperatures when heating up the module. The measurements are made at the temperatures of 25 °C, 30 °C, 35 °C, 40 °C, 45 °C, 48 °C, 50 °C, 55 °C and 60 °C. The temperature is monitored with a temperature sensor Sigma Pt-100. The temperature

coefficients are calculated according to the standard by constructing the least squares fit through the measurement data and calculating the slope of the fit.
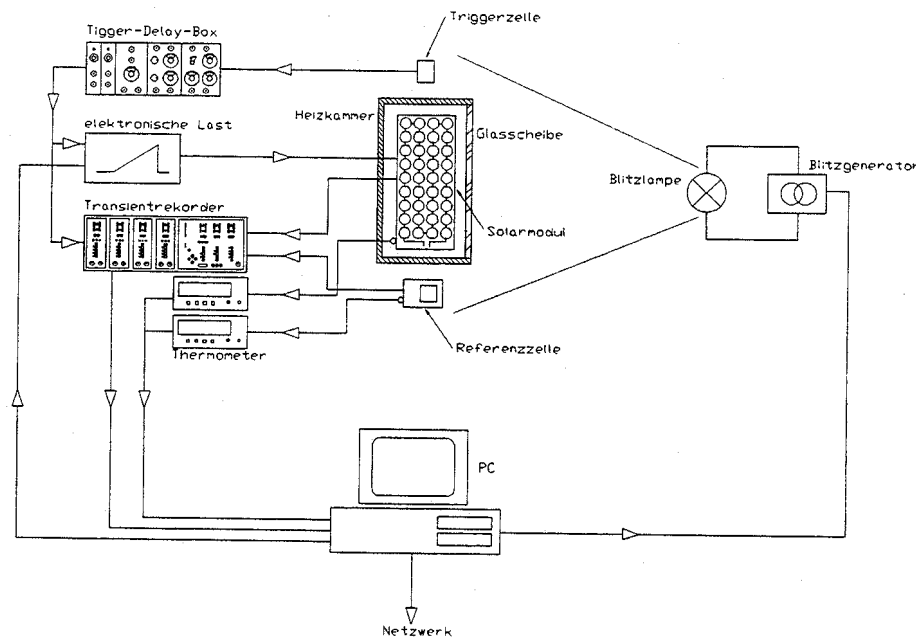

Figure 3.9 *Measurement set up for temperature coefficients measurement at ESTI [114].*

3.1.5 Reference cells

The definition of a reference cell is the following. A reference cell is a specially calibrated cell which is used to measure irradiance or to set simulator irradiance levels in terms of a reference solar spectral irradiance distribution. There are two types of reference cells: a primary reference cell is a cell whose calibration is based on a radiometer or standard detector conforming to the standard World Radiometric Reference (W.R.R.). A secondary reference cell is calibrated in natural or simulated sunlight against a primary reference cell.[124]. In this work three different reference cells, RRC14, PX204A and MB51 were used. RRC14 consists of a crystalline silicon solar cell. Its spectral resposivity can be seen in Figure 3.10. PX204A is a reference device with also a crystalline silicon solar cell but it is filtered to give a spectral response, also illustrated in Figure 3.10, close to that of amorphous silicon material. MB51 is a reference device consisting of a GaAs cell grown on germanium and its spectral responsivity is also illustrated in Figure 3.10. The all three reference devices used had been calibrated against at ESTI existing secondary standard reference devices. The secondary standard devices had been calibrated in the World Photovoltaic Scale (WPVS) calibration round robin. As the determination of the WPVS calibration factor includes calibration measurements against Absolute Cavity Radiometers the traceability link is

garanteed between WPVS and WRR. Thus the three reference devices used are treated as production standards at ESTI. The calibration factors used can be seen in Table 3.II.
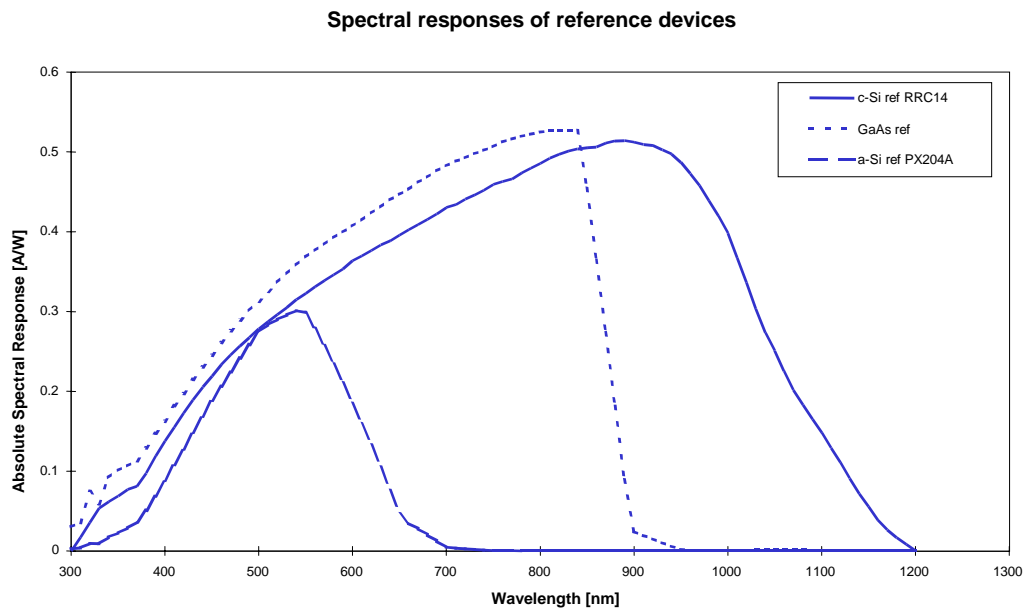
Spectral responses of reference devices

Figure 3.10 *Spectral responses of the reference devices used.*

Table 3.II *Calibration factors of the reference devices used.*

Reference device	Calibration date	Calibration temperature [°C]	Calibration value for I_{sc} [A]	I_{sc} standard deviation
RRC14	PEP83	25	0.1121	1.00
PX204A	Jan 97	25	0.0299	1.00
MB51	May 98	25	0.433	1.00

3.1.6 The ESTI calibration procedure

The ESTI calibration procedure, discussed in detail above, is shown in Figure 3.11 below. The modules are measured for their IV characteristics with two different pulsed solar simulators, SpectroLab LAPSS and Pasan LAPSS. The IV-measurements of the modules are done against a reference device detecting the irradiance. The I_{sc} and V_{oc} values are separately calibrated by simultaneously reading I_{sc} or V_{oc} signals of the test device and the irradiance signal of the reference device throughout the duration of the Pasan LAPSS pulse decay. The spectral responses of the module materials are measured using the Pasan LAPSS. The measurement is done with a relative spectral response method in which reference device was monitoring the irradiance. The I_{sc} values are

corrected to AM1.5G by multiplying with the mismatch factor calculated from the spectral response measurement. Finally the temperature coefficients are measured.

The final calibration values are determined as follows. The I_{sc} value is obtained by first multiplying the I_{sc} values from the SpectroLab LAPSS, Pasan LAPSS and I_{sc} calibration measurements with the spectral mismatch factor and then averaging the results. The final value is thus AM1.5G corrected. The final calibration value for V_{oc} is averaged from the SpectroLab LAPSS, Pasan LAPSS and V_{oc} calibration measurement results. The final value for the fill factor is averaged from the SpectroLab LAPSS and Pasan LAPSS measurement results and finally the final calibration values for P_{max} and efficiency are calculated from the other values.
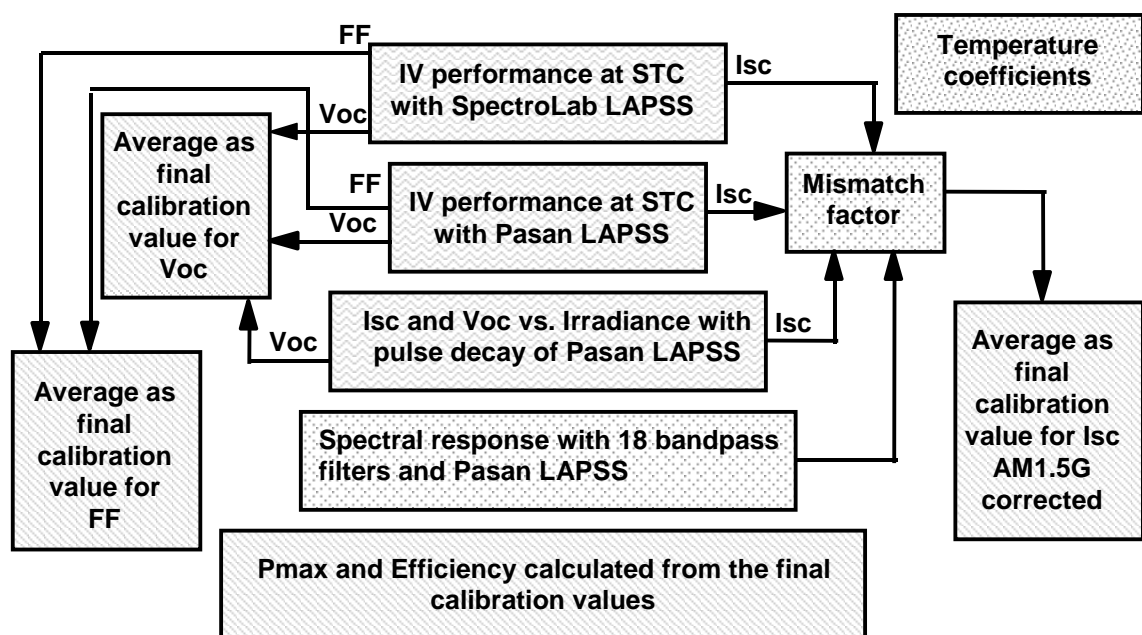

Figure 3.11 *The ESTI calibration procedure.*

3.2   Calibration measurement results

3.2.1   Sample description

The samples measured in the first round of measurements are described in Table 3.III. Three different thin film materials were studied, single junction amorphous silicon, $Cu(In,Ga)Se_2$ and CdTe. For CdTe there were sample from two different manufacturers. The samples from the first manufacturer were done with close spaced sublimation (BB501) and the samples from the second manufacturer with electrodeposition (XA504 and XA512). The a-Si samples were encapsulated, plastic framed modules of size 30 x 30 cm^2 having 29 cells in series. The module structure was a double glass laminate laminated with acrylic resin. The CIGS samples were encapsulated, unframed minimodules of size 10 x 10 cm^2 with 13 cells in series. These samples were double glass laminates laminated with EVA. The CdTe encapsulated, unframed minimodule of manufacturer 1 (BB501) was of size 5 x 5 cm^2 and had five cells in series. Also this sample was a double glass laminate with EVA. The CdTe samples from manufacturer 2 included both a tedlar back, unframed minimodule of size 5 x 5 cm^2 having four cells in series (XA504), and encapsulated, aluminum framed module of size 30 x 30 cm^2 having 31 cells in series (XA512). The small sample had a structure of glass-EVA-tedlar and the larger sample was a double glass – EVA laminate.

Table 3.III *Explanation of the samples measured.*

ESTI ID code	Material	Module size	Module construction
AB501 - AB505	a-Si	30 x 30 cm^2	glass-glass laminated with acrylic resin, polyurethan frame
BB501	CdTe (manuf. 1)	5 x 5 cm^2	glass-glass laminated with EVA, no frames
CB501 - CB505	CIGS	10 x 10 cm^2	glass-glass laminated with EVA, no frames
XA504	CdTe (manuf. 2)	5 x 5 cm^2	glass-tedlar laminated with EVA, no frame
XA512	CdTe (manuf. 2)	30 x 30 cm^2	glass-glass laminated with EVA, aluminum frame

3.2.2 Results of the first set of measurements

IV measurements

The first set of measurements was done using c-Si reference device RRC14. The samples were first measured with SpectroLab LAPSS, then with Pasan LAPSS and finally the Pasan LAPSS results were mismatch corrected. The average deviation in I_{sc} between measurements with SpectroLab LAPSS and Pasan LAPSS in the first round of IV measurements was for a-Si 7%, for CdTe 4% and for CIGS 0.3%. In V_{oc} the average deviation was for a-Si 0.8%, for CdTe 3% and for CIGS 0.1%. In fill factors the average deviation was 1% for a-Si, 5% or 1% for CdTe depending on the manufacturer and 4% for CIGS. After applying the mismatch factors to the with Pasan LAPSS measured I_{sc} values there was an average deviation of 2% for a-Si, 7% for CdTe and 1% for CIGS. The deviations for I_{sc} and V_{oc} are shown for the samples measured in the second measurement round in Figure 3.18 in the next section.

The ESTI measurement accuracy in for c-Si samples is in $I_{sc} \pm 2.2$ % and in $V_{oc} \pm 0.8$ %. The V_{oc} values fall within the measurement accuracy for a-Si and CIGS materials but not for CdTe. The I_{sc} values for CIGS samples are within the measurement accuracy both before and after the application of the mismatch correction. In case of a-Si and CdTe samples there is a considerable deviation in the measured values. For a-Si samples the difference was reduced to be barely within the measurement accuracy when the mismatch correction was applied. For CdTe samples the correction resulted in a too large a difference to the opposite direction when compared to the situation before the mismatch factor application. In fill factors there was no considerable deviation for a-Si and for the CdTe samples of the other manufacturer. In this parameter the CIGS samples showed some deviation together with the CdTe samples of the other manufacturer when measured with the two pulsed flash simulators. The P_{max} deviations corresponded to the fill factor deviations. The ESTI measurement accuracy for P_{max} is ± 2.4 %.

I_{sc} and V_{oc} calibrations

In I_{sc} calibration the I_{sc} values were measured at different irradiances from the decaying pulse tale of Pasan LAPSS. The results of I_{sc} calibration were plotted as relative normalized I_{sc} ratios against normalized irradiance (Figure 3.12). In the first measurements the c-Si reference device RRC14 and filtered c-Si reference device PX204A were used. Both the I_{sc} and the irradiance values have been normalized to 1000 W/m^2. It has to be noted that no mismatch correction has been applied in Figure 3.12 to correct the possible differences in the lamp spectra at different irradiance levels.

The normalized figures can be considered to show how well the reference device suits for the measurement of the sample. The closer the curve is to one at different irradiance levels the better is the suitability. In the first round of measurements, when c-Si reference device RRC14 was used, a strong deviation from one was observed for a-Si and CdTe samples but not for CIGS samples. When doing the same measurement with

filtered c-Si reference device PX204A a strong deviation from one was still observed for CdTe samples but not for a-Si samples.

In V_{oc} calibration the V_{oc} values were measured at different irradiances from the decaying pulse tale of Pasan LAPSS. The c-Si reference device RRC14 was used. The V_{oc} behavior indicates the solar cell behavior in the junction. When the results are drawn against the natural logarithm of irradiance values that have been normalized to 1000 W/m^2, the ideality factor of the material can be determined from the slope of the curve. In the first measurement round the results of V_{oc} calibration were compared with the V_{oc} values obtained from the IV measurements with SpectroLab LAPSS and Pasan LAPSS. A deviation of 2% against SpectroLab LAPSS and 3% against Pasan LAPSS for a-Si sample, of 1% for CIGS sample with both simulators, and of 1% against SpectroLab LAPSS and 1% or 2% depending on the manufacturer against Pasan LAPSS for CdTe samples was observed.
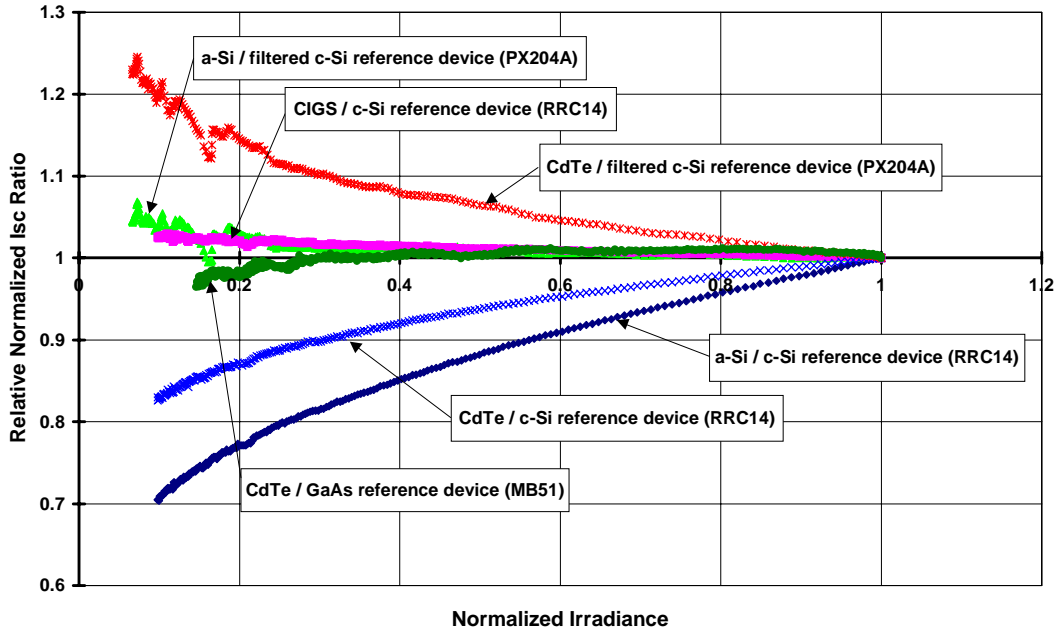

Figure 3.12 *The measured and estimated curves of the I_{sc} values as measured against the irradiance decay of the Pasan flash pulse with the c-Si reference device RRC14.*

The spectral response measurement

The spectral responsivity curves of the reference devices and the measured samples are shown in Figure 3.13. Also the Pasan LAPSS and AM1.5G spectra are shown. All the spectral responses on the first measurement round were measured against the c-Si reference device RRC14.

As also indicated in Table 3.IV in the next section, the mismatch factors calculated for each material, when the spectral response measurement was done against c-Si reference device RRC14, were 5% for a-Si, 11% for CdTe and 0.7% for CIGS.
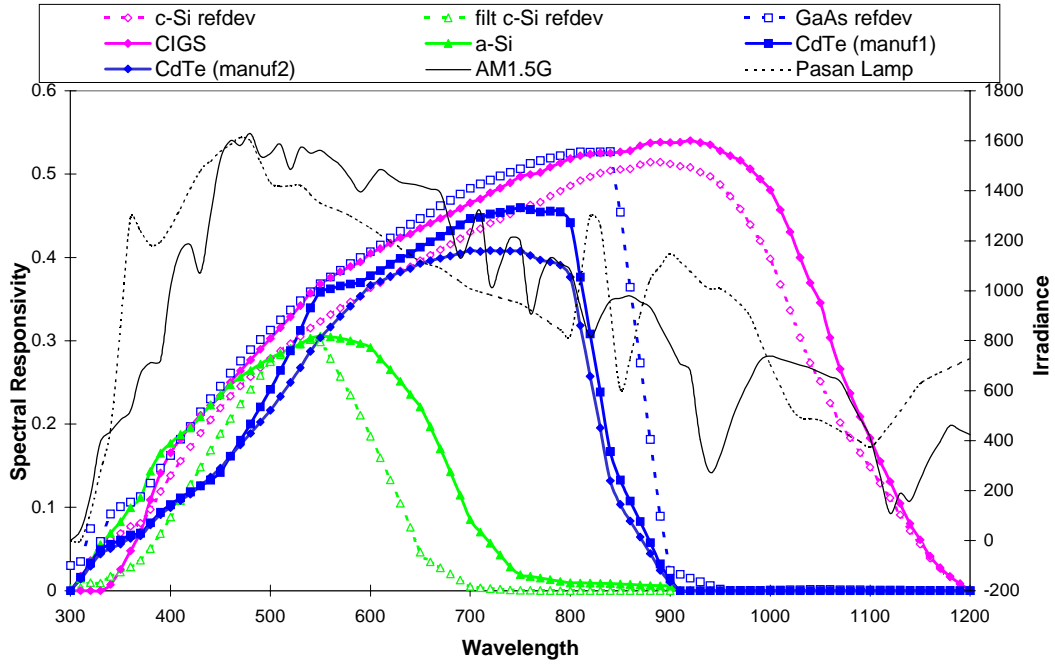
Figure 3.13 *The spectral response curves of the reference devices and the sample materials. Also shown are the Pasan LAPSS lamp and the AM1.5G spectra.*

Temperature coefficients

The temperature coefficients α and β for current and voltage respectively are shown in Table 3.IV for each material. The temperature coefficients were measured with the c-Si reference device RRC14.

Table 3.IV *Temperature coefficients for a-Si, CIGS and CdTe materials measured against c-Si reference device RRC14.*

Sample material	α	β
	$[\mu A\,°C^{-1}cm^{-2}]$	$[mV\,°C^{-1}]$
a-Si	4.2	-2.2
CIGS	-5.1	-1.7
CdTe (manufacturer 1)	9.0	-2.3
CdTe (manufacturer 2)	9.9	-2.4

The temperature coefficient measurement results are also plotted as temperature vs. normalized temperature dependence for each material in Figures 3.14-3.17 below. For a-Si (Figure 3.14) the V_{oc} and V_{mp} are decreasing with increasing temperature. P_{max} is quite constant towards temperature change showing only some decrease with increasing temperature. I_{sc}, I_{mp} and FF are also quite stable towards temperature changes showing

slight increase with increasing temperature. For CdTe material of both manufacturers (Figures 3.15 and 3.16) the temperature behavior is very similar to that of the a-Si material. V_{oc} and V_{mp} are decreasing and P_{max} quite constant or slightly decreasing with increasing temperature, and I_{sc}, I_{mp} and FF slightly increasing with increasing temperature. For the CIGS material all the parameters are decreasing with increasing temperature (Figure 3.17). In P_{max} the decrease is strongest.
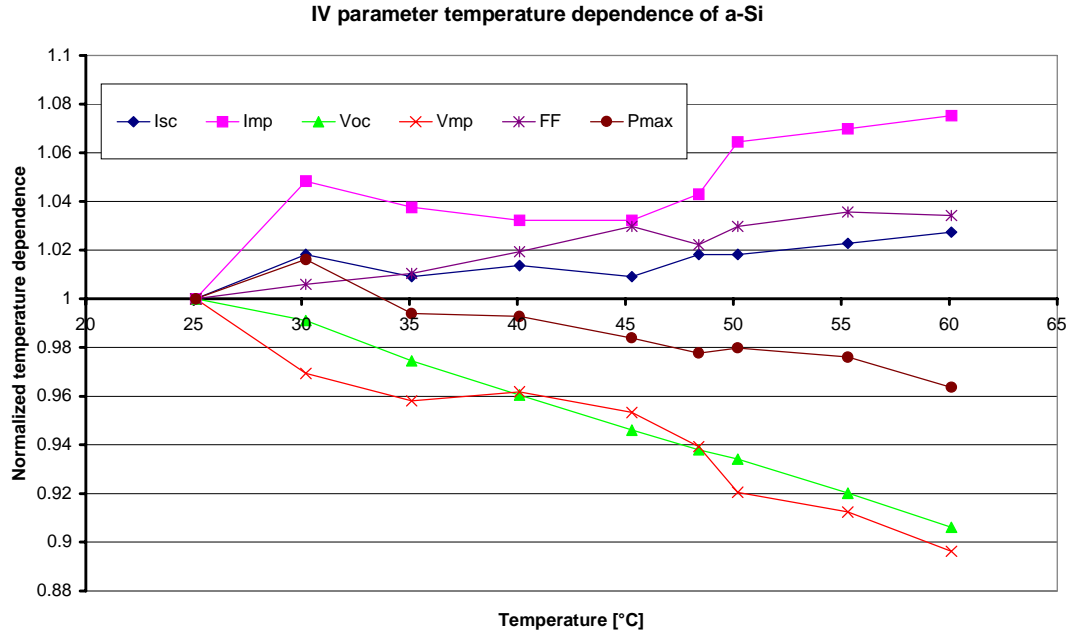

Figure 3.14 *The normalized temperature dependence of the IV parameters I_{sc}, I_{mp}, V_{oc}, V_{mp}, FF and P_{max} for a-Si material.*

Figure 3.15 *The normalized temperature dependence of the IV parameters I_{sc}, I_{mp}, V_{oc}, V_{mp}, FF and P_{max} for CdTe material of the first manufacturer (BB501).*

Figure 3.16 *The normalized temperature dependence of the IV parameters I_{sc}, I_{mp}, V_{oc}, V_{mp}, FF and P_{max} for CdTe material of the second manufacturer (XA512).*

IV parameter dependence of CIGS

Figure 3.17 *The normalized temperature dependence of the IV parameters I_{sc}, I_{mp}, V_{oc}, V_{mp}, FF and P_{max} for CIGS material.*
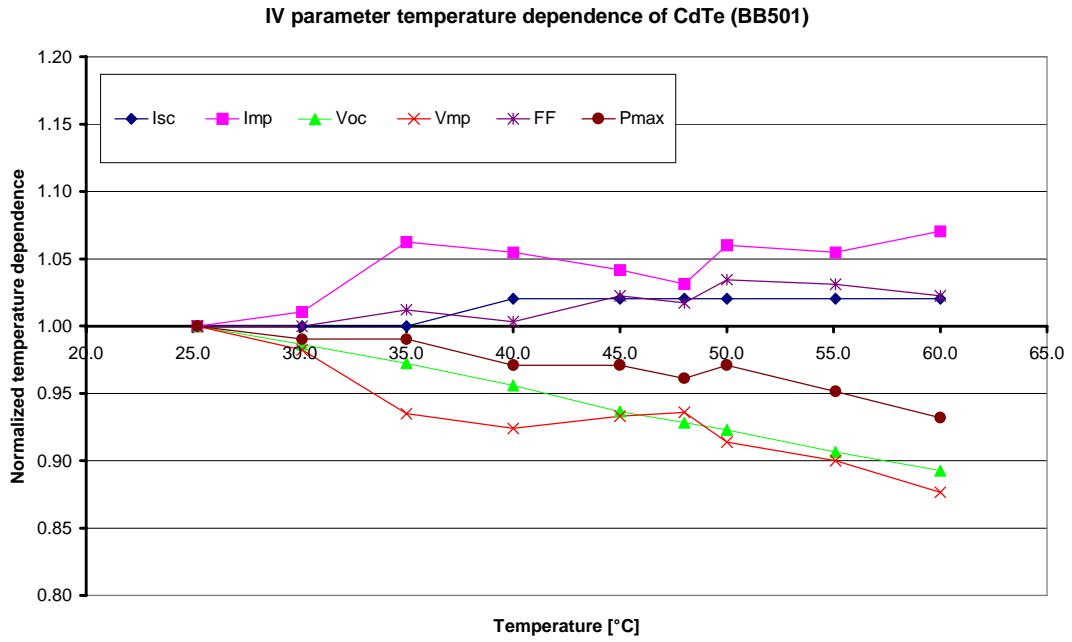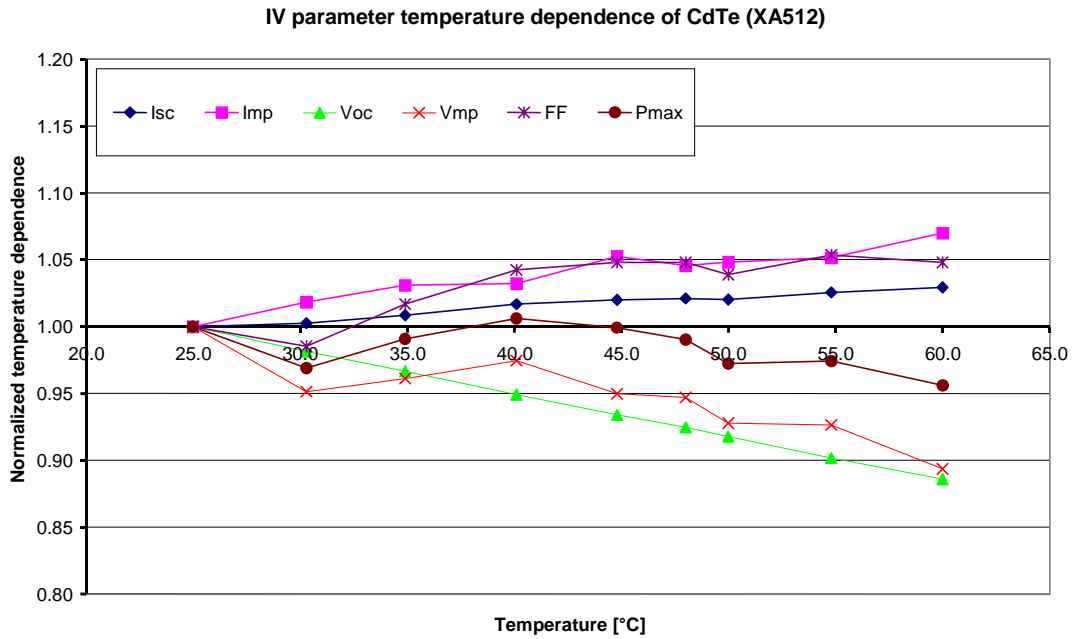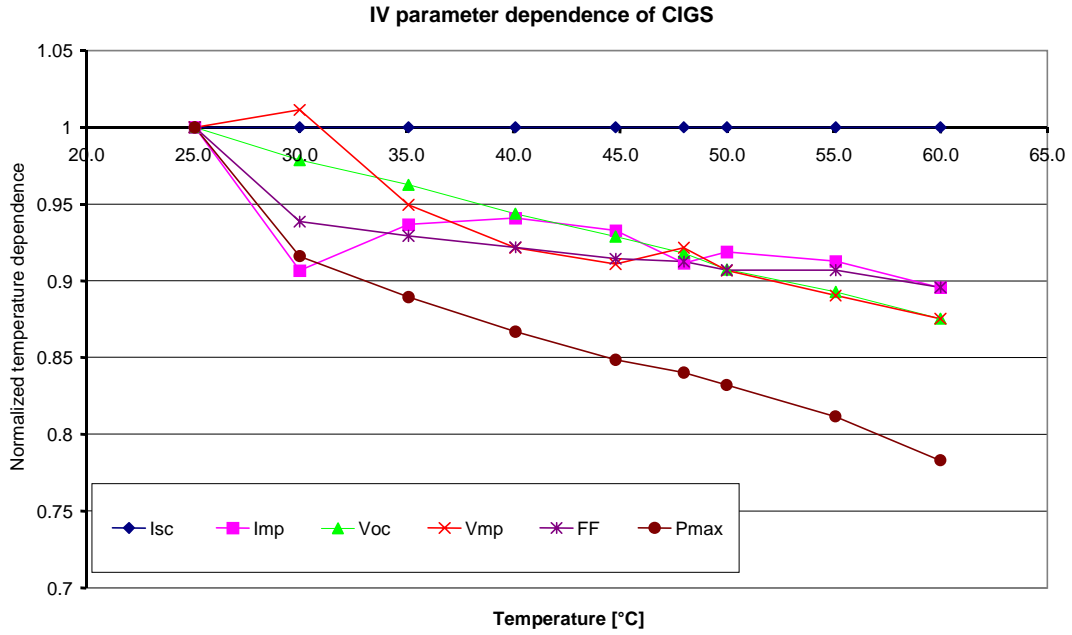
3.2.3 Results of final calibration measurements

From the second round of measurements the final calibration factors or calibrated IV parameters were determined for one sample of each material according to the calibration procedure discussed in Section 3.1. For measurements of a-Si material, filtered c-Si reference device PX204A was used, and for the CdTe samples GaAs reference device MB51 was used. The CIGS samples were not re-measured on this second measurement round.

The deviations in I_{sc} for the samples when measured with Pasan LAPSS and SpectroLab LAPSS, compared with the final calibration value, are shown in Figure 3.18. The results in Figure 3.18 for CIGS are based on the measurements on the first measurement round. On this second measurement round the deviation in I_{sc}, when comparing the IV measurements with SpectroLab LAPSS and Pasan LAPSS against the final calibration values, is around 1 % to 3 % for a-Si and both CdTe samples. The mismatch correction reduces the deviation for a-Si to 0.3 % and for CdTe to 1 %. In V_{oc} the deviations were 0.8 % for a-Si, and 7 % or 3 % for CdTe depending on the manufacturer. The deviations in fill factors were 1.4 % for a-Si, and 5 % or 2 % for CdTe again depending on the manufacturer.

The CdTe samples were I_{sc} calibrated against the pulse decay of Pasan LAPSS using GaAs reference device MB51. With this MB51 reference device, the relative normalized I_{sc} ratio as plotted against the normalized irradiance, is close to one for all irradiance values (Figure 3.12).

The a-Si and CdTe samples were V_{oc} calibrated against the pulse decay of Pasan

LAPSS. For a-Si sample filtered c-Si reference device PX204A and for CdTe samples GaAs reference device MB51 was used. The normalized V_{oc} curves are plotted as the function of the natural logarithm of irradiance normalized by 1000 W/m^2 in Figure 3.19. The deviation in the V_{oc} calibration results against the final calibration value was 0.7% for a-Si sample, 0.2% for CdTe samples and 0.8% for CIGS sample.

Difference in Isc and Voc against the final calibration value (FCV) when different simulators and different reference
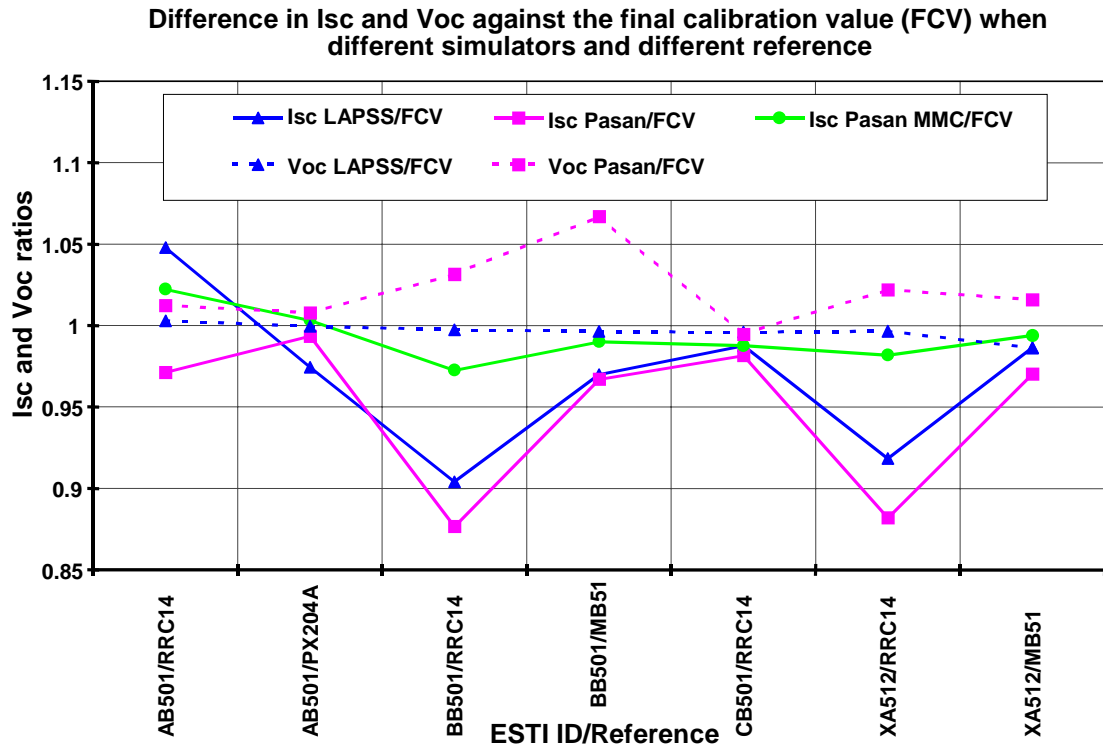
Figure 3.18 *Differences between the I_{sc} and V_{oc} values when measured with two different pulse solar simulators and three different reference devices as compared with the final calibration values.*
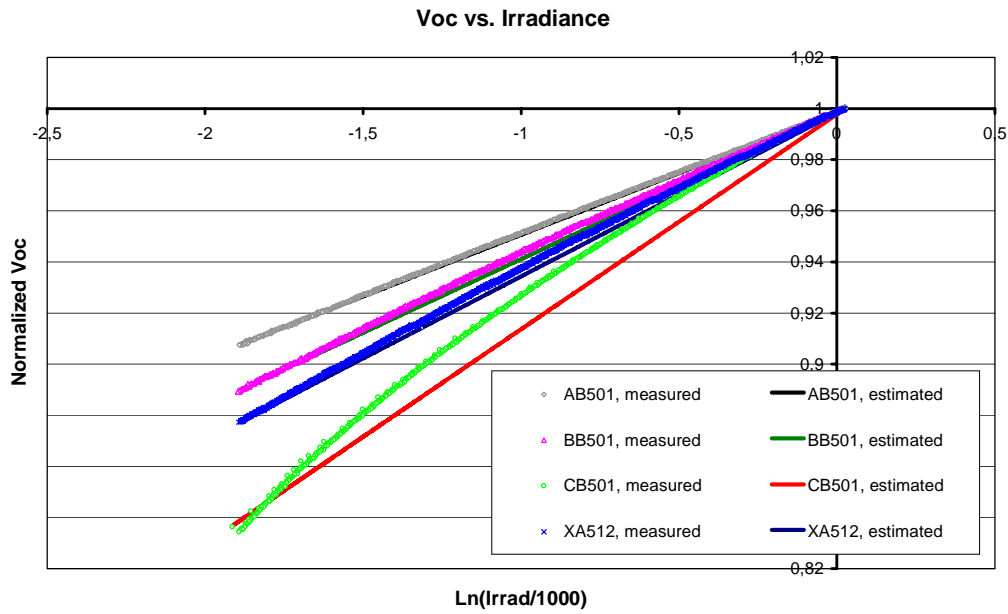
Voc vs. Irradiance

Figure 3.19 *The measured and estimated V_{oc} values as measured against the irradiance decay of the Pasan LAPSS flash pulse with three different reference devices. (For AB501 and BB501 the estimated curves are barely visible because of good correlation).*

The mismatch factors measured on the second measurement round are shown in Table 3.V below. The a-Si sample was measured with the filtered c-Si reference device RRC14 and the CdTe sample with the GaAs reference device MB51. The CIGS results are from the previous measurement round as measured with c-Si reference device RRC14. Also shown in Table 3.V are for comparison the mismatch factors obtained from the first measurement round.

The temperature coefficients were not re-measured with different reference devices because the coefficients are calculated from the slope of the measurement points and thus absolute values are not needed.

Table 3.V *Mismatch factors for different materials.*

Material	Mismatch factor, 1st round	Mismatch factor, 2nd round
a-Si	5.0 % (RRC14)	1.0 % (PX204A)
CdTe (BB501)	11.0 % (RRC14)	2.4 % (MB51)
CIGS	0.5 % (RRC14)	0.5 % (RRC14)
CdTe (XA512)	11.0 % (RRC14)	2.5 % (MB51)

3.3   Discussion on calibration measurements

The electrical characterization of PV modules made of conventional materials like c-Si is well established and relatively straight forward procedure since the material properties and the behavior of these materials under illumination are well known and the measurement procedures and the correction methods well documented and standardized. However for thin film materials there is a need to establish reliable characterization methods since no international standards are yet available. To be able to objectively judge the test results for qualification testing of PV modules reliable and repeatable measurements are essential.

a-Si, CdTe and CIGS samples were IV calibrated in this study by measuring them for IV parameters with three different ways using three different reference devices. Also spectral responsivities and temperature coefficients were measured. In Figure 3.12 the relative normalized I_{sc} ratios are drawn against normalized irradiance. This kind of presentation should indicate how well the reference device suits for the IV characterization of the sample under measurement. The closer the curve is to one for all irradiance values the better the suitability. It has to be noted that no corrections are made for the possible differences in the lamp spectra at different irradiances. In Figure 3.13 the spectral responsivities of the sample materials and the reference devices used are shown. Also the AM1.5G and Pasan LAPSS lamp spectra are shown. The mismatch factor corrects for differences between the lamp and the AM1.5G spectra and for differences between the spectral responsivities of the sample and the reference device.

3.3.1 I_{sc} calibration

a-Si

After the first set of measurements there was considerable deviation between the SpectroLab LAPSS and Pasan LAPSS measurement results for I_{sc}. The first measurements were done using c-Si reference device RRC14. After the mismatch correction, the average deviation reduced to 2 %. However, the mismatch correction of 5 % is too large to be reliable in general. The cause for this large mismatch factor is visible in Figure 3.13, in which the spectral responses of the a-Si material and the reference device RRC14 are shown. The mismatch factor corrects for the differences between the sample material and the reference device spectra as well as the differences between the lamp and the AM1.5G spectra. The spectral response of a-Si material extends to around 750 nm as opposed to the c-Si reference device spectral response which covers the wavelength range up to 1200 nm. There are also some large differences between the lamp and the AM1.5G spectra from 750 nm to 1200 nm which affect the spectral correction for the reference device but not for the sample material. Thus the mismatch factor become large and can not be considered to give a reliable correction to the measurement result.

In Figure 3.12 the relative normalized I_{sc} values are plotted against the irradiance decay of the Pasan LAPSS flash pulse tale. This representation should indicate the

spectral suitability of the reference device to be used in the measurement of the sample material. As can be seen, there is a deviation in the curve from one when a-Si sample is measured with RRC14. Thus the c-Si reference device RRC14 does not give reliable measurement results in the I_{sc} calibration when used for measuring a-Si material.

In the second set of measurements the filtered c-Si reference device PX204A was used for the measurements of a-Si material. The filter of this reference device is such that the spectral response of the device is changed to be close to that of single junction a-Si material. Thus in the second measurements with this reference device the deviation in I_{sc} values when measured with the two different solar simulators was reduced to be within the ESTI measurement accuracy. Also the mismatch factor was reduced to 1 %. In Figure 3.13 it can be seen that the spectral responses of the a-Si material and PX204A are rather close together resulting in the reduced mismatch factor. Some error to the mismatch factor determination is caused in this case by the drop in the spectral response of the reference device around shorter wavelengths than where the response of a-Si is dropping. This is because the spectral response was measured relative to the reference device. However, this error is not larger than the measurement system accuracy and can thus be ignored.

In the final calibration value calculation also the SpectroLab LAPSS measured I_{sc} value and the I_{sc} from the irradiance decay measurement are mismatch corrected and the averages of these results is taken as the final calibration value. As can be seen in Figure 3.18 there is a deviation between the different measurement results and the final calibration value when using c-Si reference device RRC14 but when using filtered c-Si reference device PX204A the values are adequately close to each other. Thus it can be concluded that the final calibration value of a-Si samples in I_{sc} can be reliably determined using the filtered c-Si reference device PX204A.

CIGS

For CIGS samples there was practically no deviation after the first set of measurements in I_{sc} when measured with SpectroLab LAPSS and Pasan LAPSS against the c-Si reference device RRC14. When the relative normalized I_{sc} values are plotted against the irradiance decay of the flash pulse (Figure 3.12), the curve is close to one indicating that the RRC14 reference device is suitable for the measurement of the CIGS material. When the spectral mismatch factor is determined, it results in a spectral correction of only 0.5 %. This is due to the close match of the spectral responsivities of the CIGS material and the c-Si reference device RRC14 (Figure 3.13). In Figure 3.18 it is shown the comparison of the different measurements with the final calibration value and practically no deviation in the values can be observed. Thus no second measurement round for the CIGS samples was needed and it could be concluded that the c-Si reference device RRC14 is suitable for the I_{sc} final calibration value determination of the CIGS material.

CdTe

After the first set of measurements there was a considerable deviation in the I_{sc} values when measured with SpectroLab LAPSS and Pasan LAPSS and with the c-Si reference device RRC14. The deviation was consistent for the CdTe samples of the two different manufacturers. After the mismatch correction the deviation increased to be 7 %. The mismatch factor obtained was 11 % and thus too large to give a reliable correction. The reason, visible in Figure 3.13, is the large spectral responsivity difference between the reference device RRC14 used and the CdTe material. The CdTe spectral response cuts off around 900 nm compared to the RRC14 response which covers wavelengths up to 1200 nm. Again, as in the case for the a-Si material, the mismatch correction corrects for the differences between the sample material and the reference device and thus the differences in the lamp and AM1.5G spectra from 900 nm to 1200 nm affect the reference device correction but not that of the sample.

The relative normalized I_{sc} decay over the irradiance decay for CdTe against c-Si reference device RRC14 is shown in Figure 3.12. The curve is deviating downward from one, slightly less than the curve of a-Si when measured with RRC14, but enough to show that RRC14 is not a reliable reference device for the measurement of CdTe material. The I_{sc} decay over the irradiance decay was also measured against the filtered c-Si reference device PX204A and the result curve having a deviation upward from one is plotted in Figure 3.12 as well. The spectral response curves in Figure 3.13 show that the problem with PX204A for the measurement of CdTe is a response of the reference device that covers much smaller part of the wavelength region than the CdTe materials. Thus the problem is opposite to that of the problem with the measurement with RRC14. Also the mismatch factor can not be accurately determined with the relative spectral response measurement used since the division by zero for the wavelengths between 750 nm and 900 nm causes too large an error in the mismatch factor calculation.

A possible reference device for the calibration measurements of the CdTe materials was calibrated from a GaAs cell. This new reference device MB51 has rather similar spectral response to the CdTe material (Figure 3.13). The deviation of the I_{sc} results when measured with the different simulators was reduced to be within the ESTI measurement accuracy, when GaAs reference device MB51 was used. Also the mismatch factor was reduced to be 2.5 % giving a reasonable correction to the I_{sc} measurements. In Figure 3.18 the I_{sc} values for both CdTe samples are reasonably close to the final calibration value, showing consistency with the different measurement equipment when using the GaAs reference device MB51. The relative normalized I_{sc} decay over irradiance decay curve is close to one (Figure 3.12) implying that the MB51 reference device is suitable for a reliable measurement of CdTe material.

3.3.2 V_{oc} calibration

In the first round of measurements the differences in V_{oc} values measured for a-Si and CIGS samples with SpectroLab LAPSS and Pasan LAPSS were well within the

ESTI measurement accuracy. Also in second round of measurements the V_{oc} values measured with both solar simulators are close to the final calibration value (Figure 3.18). The first round was measured against c-Si reference device RRC14 and in the second round filtered c-Si reference device PX204A was used for the a-Si sample measurements. However, in the V_{oc} measurement the choice of the reference device is not crucial.

For the CdTe samples there was a considerable deviation in the first round of measurements between the V_{oc} values obtained with SpecroLab LAPSS and Pasan LAPSS. Also on the second measurement round quite large or very large difference from the final calibration value could be observed when compared against the Pasan LAPSS measurements (Figure 3.18). Again, even though the choice of the reference device is not crucial in the V_{oc} measurements, the first round was measured with the c-Si reference device RRC14 and the second round with the GaAs reference device MB51. One possible reason for this deviation is stated in [125]. The authors argue that I_{sc} values appear to be independent of the pre-biasing sensitivity condition but V_{oc}, and therefore the calculated parameter of fill factor, appears to be quite dependent on the pre-biasing condition. The voltage effect is dependent on voltage history, not illumination history. Physically, the effect is almost certainly the result of changing the occupation of traps in the junction. This voltage effect is expected to be significantly reduced as the junction quality is improved (lower diode ideality factor). This argument might also explain the difference noticed between the samples of the two manufacturers. In V_{oc} of the sample from the first manufacturer (BB501) there was a 7 % difference between the final calibration value and the measurement with Pasan LAPSS. For the sample of the second manufacturer (XA512) this difference was only 3 %. Even though the diode ideality factor is possible to be determined from the V_{oc} decay over the irradiance decay measurement discussed in the next section, its determination is not within the scope of this study and thus it was not determined. Another reason for the observed large difference in the V_{oc} measurement of the sample of the first manufacturer might be a, for some reason, more inaccurate measurement than the normal ESTI measurement accuracy.

The V_{oc} was also calibrated against the pulse decay of Pasan LAPSS flash pulse tale and the values obtained were averaged to the final calibration value. In the first measurement round some deviation was observed with the V_{oc} values compared with the SpectroLab LAPSS and Pasan LAPSS measurements in a-Si and CdTe. For the CIGS sample the deviation was within the ESTI measurement accuracy. On the second measurement round the deviation for a-Si and CdTe samples were reduced also to be within the ESTI measurement accuracy. In principle, the diode ideality factor n and the diode saturation current I_0 could be determined from this measurement but they are not determined in this study since it is out of the scope of this study. However, the measured and estimated curves of the normalized V_{oc} decay against the normalized natural logarithm of the Pasan LAPSS flash pulse tale decay are shown in Figure 3.19. According to [126], a major advantage of this technique is that series resistance is

eliminated which allows direct observation of the main junction right up to and through one sun V_{oc}. As also is visible in Figure 3.19, the data curves for most of the samples are not straight lines. Thus there is no single n, I_0 pair to describe the given curve, although over smaller intervals of voltage one could adequately fit a single line and determine an apparent n, I_0 descriptor. Thus the integral of the deep states in the gap determines the recombination at one sun and hence V_{oc}. The larger range in V_{oc} observed at lower intensities is indicative of the detailed properties of the density of states profile.

A factor that should be taken into account in the further studies of the V_{oc} measurements of polycrystalline CdTe and CuInSe$_2$ (CIS) solar cells is that when the cells are illuminated, the voltage continues to increase during the time range 1 ms to > 10 ks in some cases.[127]. For an ideal solar cell, the voltage will stabilize in a few microseconds. Deep traps located near the metallurgical junction in the absorber material that effectively increase the barrier height V_{bi} are thought to be the primary mechanism responsible. ΔV has been found to result from the cell being in forward bias and is not directly due to the cell being illuminated. The recommended way to prevent an artificially low efficiency measurement is to apply a bias near the maximum power voltage in the dark for the order of 30 minutes and then sweep the IV-curve from high to low bias so that the relaxation during the IV measurement is minimized. Biasing near the open circuit voltage may increase the voltage slightly more than at the maximum power voltage. However, the time dependence of the voltage was not studied in the scope of this work but the possibility of the dependence should be taken into account when determining the final V_{oc} calibration values for CdTe and CIS or CIGS samples.

3.3.3 Final calibration values of fill factor

In the first round of measurements some difference was observed in the fill factor values of CIGS and CdTe samples when comparing the measurements with SpectroLab LAPSS and Pasan LAPSS. In the a-Si samples the average deviation was negligible. In the second measurement round again hardly no difference could be observed in the a-Si samples but a considerable difference was present in the CdTe samples. A possible explanation is presented in Section 3.1.4 at least for CIGS samples. In that section it is argued that blue light might increase the fill factor in CIGS samples. Although both the simulators, SpectroLab LAPSS and Pasan LAPSS, are equipped with xenon lamps, there might still exist some differences between the spectra of the lamps. These differences, when appearing especially in the blue part of the spectrum, could cause some difference to the measured fill factor values. Since in Section 3.1.4 it is also argued that the enhancement of the fill factor in the CIGS samples under blue light is mainly caused by the behavior of the CdS window layer, the same might apply to the CdTe samples also having CdS window layer.

3.3.4 Temperature coefficients

The measured voltage and current temperature coefficients are presented in Table 3.IV for the different samples. All the IV parameters are also plotted as a function of

temperature in Figures 3.14-3.17. What could be noted from these figures is that even though V_{oc} is decreasing with increasing temperature for all the thin film materials, P_{max} is rather stable with increasing temperature for a-Si and CdTe samples. This implies that the a-Si and CdTe module output power should be very stable in different outdoor temperature operation conditions. For CIGS material P_{max} is decreasing with the increasing temperature.

3.4 Conclusion on calibration measurements

In conclusion the use of c-Si reference device when characterizing modules made of CIGS material was found to give reliable measurement results in the I_{sc} calibration. In case of a-Si material the use of the filtered c-Si reference device the spectral response of which resembles that of a-Si gives more reliable results than the use of the c-Si reference device. In case of CdTe a reference device made of GaAs cell, having similar spectral response to that of CdTe material can be used.

In order to obtain consistent I_{sc} values when measuring with the different simulators, a correction based on the difference in the slopes for the reference device and the sample in the normalized I_{sc} decay over the irradiance decay could be applied if the lamp spectrum was assumed to be constant at different irradiance levels. When the irradiance level is decreased the drop in the normalized current for the material with the spectral response covering a wider wavelength range is less than for the other material. Since the correction to 1000 W/m^2 irradiance level is based on the smaller drop in the normalized current of the reference device the correction for the sample in this case is too small. In SpectroLab LAPSS the irradiance correction is smaller due to the flatter pulse shape than in Pasan LAPSS. However the SpectroLab LAPSS was operated as a class A simulator [112] and due to the timing settings the Pasan LAPSS was in class B simulator mode (temporal instability in irradiance $> \pm 2$ %). Thus the values measured with SpectroLab LAPSS might in general be considered more stable. However the spectrum is not constant and the response of the sample material not necessarily linear at different irradiance levels. Thus at ESTI the problem is solved by using a reference device with a spectral response similar to that of the sample material. In that case also a mismatch factor closer to one is obtained.

4. ACCELERATED LIFETIME TESTING

4.1 Introduction to accelerated lifetime testing

4.1.1 Basic principles of accelerated lifetime testing

According to the American Society for Testing and Materials (ASTM), the service lifetime of materials, devices, or systems is the time at which their performance degrades below a prescribed or required value, i.e. a total failure or a failure to perform at a pre-assigned value. Durability or reliability is the ability of a unit to maintain a sustained performance for a specified period of time. Because the desired PV module lifetimes are greater than 30 years, accelerated lifetime testing in (simulated) weather environments and service lifetime prediction methodology must be used.[128], [129]. Thus the aim of accelerated lifetime testing is to help improve photovoltaic (PV) module long-term performance and reliability. This is accomplished by designing, developing and implementing test methods and techniques for PV modules, as well as performing actual testing on them from commercially available products to R&D prototypes. The results should help manufacturers, test facilities and end users to understand and improve PV module design, performance, long-term reliability and safety.[130]. Research and development using accelerated lifetime testing at an early state can reduce the cost of developing advanced PV technologies. In addition to accelerated lifetime testing, the experimental approach needs to include monitoring the real time testing performance. Only then a service lifetime prediction becomes possible.[129], [131], [132].

Accelerated lifetime testing can be divided to qualification testing and reliability testing. The qualification test sequence aims to judge the suitability of a module design for long term (15-20 years) operation in general open air climates. The test sequence is not oriented towards tropical, polar, or marine environment.[133]. Every module tested to the qualification specification sequences is expected to pass, providing evidence that the module type can withstand the level of stress defined in the test and therefore is expected to have some minimum lifetime in normal operation.

Having well accepted qualification test sequences can result in two problems. First of all everyone starts believing that the qualification tests tell them everything they need to know about their modules reliability and so do not perform additional reliability tests. Secondly the same qualification tests are applied to all PV technologies without determining if the test sequences are really relevant for anything but the module type that the modules were developed for, the type being crystalline silicon in most cases. Thus reliability tests are used to develop a scientific understanding of how the module performs under various environmental stresses.[134], [130].

In module qualification testing the accelerated tests are run one after the other in series or parallel. There is no attempt to determine what happens if one or more stresses are applied at the same time. Reliability tests go beyond the ranges used in qualification tests, for example running the tests for longer duration or by applying higher stress

levels. Module reliability testing should include combinations of stresses. Combination of tests can be selected from the knowledge of PV operating conditions or from analysis of observed field failures. One example of this is accelerated weathering, which attempts to look at the synergistic effects of solar radiation, temperature, and moisture of PV modules, using both indoor, artificial test methods, as well as outdoor, natural exposure. Often these tests are continued until failure in an attempt to understand what failures can occur and therefore what changes in module construction or design will ultimately improve module reliability and lifetime.[134], [130].

When considering testing of electronic materials in general there are four types of accelerated environmental tests: STRIFE or stress life tests, burn-in tests, environmental stress screening (ESS) and highly accelerated life tests (HALT). The stress life tests use aggressive stress to force failures of prototype units. The resulting failures are due to product or process design flaws. The burn-in tests eliminate early failures typically associated with manufacturing defects. The level of burn-in stress must not be high enough to damage the non-defective units. The environmental stress screening tests units at system or subsystem level. It uses milder but more complicated stress regimen. The tests screen out defective items without harming the system. The highly accelerated life tests are useful when inferences about life at use conditions are not needed. These tests include inspection sampling of new lots of materials/components and burn-in screening tests. The tests provide the scope of information useful in planning more extensive accelerated lifetime tests and explore relevance of failure modes discovered in stress life tests.[132]. When interpreting the test results, failure mechanisms are considered to fall into two broad classes: generic and statistical. Generic problems must be solved by design or process changes, statistical failures are effectively solved through redundancy and quality control.[131].

In designing accelerated environmental tests, it must be insured that the tests relate to both acceleration of the environment that the product is to be exposed to as well as to the mechanisms by which the environmental stress causes failure in the product. Solar energy conversion systems are subjected to a unique set of stresses that may alter their stability and, hence, their performance and life cycle costs in addition to the initial costs of the systems. These stresses include UV radiation, temperature, atmospheric gases and pollutants, the diurnal and annual thermal cycles. In addition, rain, hail, condensation and evaporation of water, dust, wind, thermal expansion mismatches, etc. may impose additional losses in the performance of a photovoltaic system. Models for extrapolation should have a basis in or be derived from the physics and chemistry of the important failure mechanisms.[131], [132], [134], [128], [135], [129].

It is also important to define failure. Since degradation processes generally proceed faster at higher temperatures, increased temperature is most commonly used as an accelerator of chemical degradation mechanisms. Typically used acceleration theorem is that of Arrhenius which claims that there is a factor of 2 increase per every 10 °C. Although aging tests at very high sample temperatures bring a further acceleration,

they may lead to unrealistic results, because other aging processes, thermally dependent, are initiated, which do not occur at practical use. Thus the elevated stress levels in temperature, relative humidity (RH), and cycle frequency must be carefully chosen.[131], [132], [134], [128], [135], [129].

It is implicit that the reactions studied under accelerated conditions simulate the reality of the reactions under normal operating conditions; e.g. a free-standing polymer exposed in air cannot simulate reaction of a polymer in an encapsulated, multi-layer PV device. In making service lifetime predictions, a number of criteria are necessary. These include, that the accelerated test must not alter the degradation mechanisms, and the activation energies and mechanisms of the dominating reactions at normal operating conditions and accelerated test conditions must be the same. Also both the specimens and accelerating parameters must simulate reality, that is full-sized cells and/or modules must be used in the accelerated tests. Finally the time-dependent performance loss must be correlated with the degrading reactions.[128], [129].

4.1.2   History and evolution of testing procedures in use

Increased array life and reliability directly influence the economic viability of photovoltaics as an energy source. Based on the economic sensitivity to plant life, a 30-year life was chosen as the target of the crystalline Si module development effort. To achieve this high level of reliability a systematic reliability program was undertaken in 1975 by the Jet Propulsion Laboratory Flat Plate Solar Array Project to develop the technology base required.[131]. The JPL Block V sequence of tests was developed during the 1970's to "qualify" PV modules for performance monitoring and deployment in the field. This work, performed by JPL, was principally designed for crystalline silicon photovoltaic modules. The JPL test sequence included the following tests: temperature cycling, humidity-freeze cycling, cyclic pressure loading, wind resistance, hail impact, electrical isolation and hot spot endurance. SERI subsequently developed an interim series of qualification tests and procedures which included, but went further than (with additional and more rigorous tests), the Block V sequence.[25]. Thus the present module testing sequence is the result of extensive work that began with the JPL (Jet Propulsion Laboratory) Block V test sequence and was continued through the UL (Underwriters Laboratories) Standard 1703, and then the SERI (Solar Energy Research Institute) Interim Qualification Tests and Procedures. Also European Commission Joint Research Center (JRC) worked on developing module testing standards. Their Specification No. 501 [136] was based on the JPL Block V test sequence. This sequence was developed further to become Specification No. 502 [137]. In 1989 JRC published qualification test procedures for crystalline silicon modules, Specification No. 503 [138]. The current IEC standard 61215 [122] is in theory equal to this JRC standard. In 1989 JRC also published recommendation for thin film module testing, Specification No. 701 [139].

The current qualification test sequence for thin film photovoltaic modules is illustrated in Figure 4.1 below. It is based on the IEC International Standard 61646:

Thin-film terrestrial photovoltaic (PV) modules - Design qualification and type approval [140]. The qualification test sequence for thin film modules is based on and thus is very similar to the qualification test sequence for crystalline silicon modules.[122]. Each of the accelerated tests in the qualification test sequence is designed to evaluate the module's performance against a known module failure mechanism in c-Si photovoltaic modules. Temperature cycling and humidity tests are workhorse tests with good correlation to field failures, they are generally the most difficult to pass.[131]. Daily changes in module temperature produce stresses on the interconnects between cells and on the bonds between the interconnects and the solar cells. Early PV modules suffered open circuit failures, especially when deployed in desert environments where the temperature extremes were large. The thermal cycling test was developed to simulate this failure mechanism. The lower extreme (-40 °C) was selected because it represented the typical worst case for terrestrial environments and it was the lowest temperature easily achieved by a standard refrigeration unit. The upper extreme (+90 °C or 85 °C) was selected because flat plate modules are unlikely to experience higher temperatures and because higher temperatures would likely damage many of the plastics used in PV module construction. If necessary, the thermal cycling test should only be extended by increasing the number of thermal cycles.[134]. The qualification tests however do not necessarily manage to correlate with the real outdoor performance. For example in [141] the author reports that some c-Si modules were thermal cycled without any power degradation. However, outdoors the same modules continued to experience problems, which could be duplicated by running peak power current through the modules during thermal cycling test.[141].

The damp heat test is designed to evaluate the ability of the module to withstand long term penetration of moisture. Even though in some point of development replaced by a cycling test, the damp heat and humidity freeze tests actually test for different failure mechanisms. Long term exposure to damp heat is testing the ability of the module metallization system to withstand moisture-induced corrosion. The condition of 85 °C and 85 % relative humidity (RH), was selected to accelerate the phenomena, but at an humidity level that can usually be controlled without resulting in condensation of liquid water in the chamber. It was estimated that 200 hours at 85 °C, 85 % RH represented 20 years of exposure in Miami, Florida. A range of probable acceleration factors was calculated and it was concluded that a 20 year field exposure could be simulated with up to 400 hours of exposure at 85 °C, 85 % RH. So it appears that the 1000 hours qualification test included in IEC-61215 is more than adequate to test module reliability for a 30 year life.[134].

In the humidity freeze test moisture is pumped into the encapsulant during the high temperature, high humidity part of the cycle. This moisture is then frozen during the low temperature portion of the cycle. This is a test of the strength of the encapsulation system, particularly the adhesion of various layers. Inadequate priming of the glass, inadequate curing of the encapsulant or the wrong selection of back sheet

adhesive are all conditions that can result in field failures that will be observed in this test. A good encapsulation system does not appear to suffer any damage during the humidity freeze test. There is no evidence to indicate that running more cycles of the humidity freeze test will provide any additional information about the long-term reliability of the module. However, there is evidence that extending the time for moisture to enter the encapsulation system may increase the severity of the test.[134].

Other important tests in the qualification test sequence are among others the hot spot endurance test, mechanical load test and UV endurance test. Hot spot heating occurs in a PV module when the current carrying capability of a particular cell or cells is lower than the operating current of the cell string. This condition results in the affected cells going into reverse bias and absorbing power equal to the product of the reverse voltage and the string current. This condition can be caused by transient events such as local shadowing or soiling or by permanent degradation of the cells such as cell cracking or interconnect failure.[134].

The purpose of the dynamic mechanical loading test is to simulate wind or other changing mechanical loads that a module might experience in the field. The static loading test simulates exposure to static mechanical loads, such as snow and ice, which may cause a PV module to bend or undergo stress for extended periods of time.[25], [134].

The discoloration of EVA in c-Si modules was the first indication that UV and high temperature caused module degradation. Laboratory tests showed that while temperature accelerated the process, UV was necessary for the discoloration to occur. The major issue with establishing an accelerated UV test is the spectrum of the light source. While there are many sources of UV, most produce a significant amount of their light at wavelengths shorter and therefore more damaging than the UV spectrum experienced in outdoor exposure. Three sources have been identified that can match the outdoor UV spectrum, xenon, UV fluorescent and concentrated sunlight.[134].

The IEEE standards committee had voted to eliminate the wet hi-pot test from the test sequence, believing it to be both redundant and too dangerous. However, several modules (both thin film and c-Si) that had passed the wet megger test subsequently failed the wet hi-pot test. This demonstrates that the wet hi-pot test is still needed to expose severe failures in some modules that only occur under wet, high-voltage conditions.[130].

8 modules

Visual inspection

Performance at STC

Insulation test

Wet leakage current test

1 module

Control module

3 modules

Light soaking

4 modules

1 module

Measurement of temperature coefficients α and β

2 modules

UV test under consideration

Annealing

2 modules

Thermal cycling test 200 cycles -40°C to +85°C

NOCT

Annealing

Performance at NOCT

Thermal cycling test 50 cycles -40°C to +85°C

2 modules

Damp heat test 1000 h 85°C, 85% RH

Performance at low irradiance

Humidity freeze test 10 cycles -40°C to +85°C

Outdoor exposure test 60 kWhm^2 total irradiance

1 module

Robustness of terminations test

1 module

Mechanical load test

1 module

Hail test

Hot spot endurance test

1 module

Twist test

Repeat highlighted tests for control

Wet leakage current test

Light soaking

NOCT=nominal operating cell temperature

Figure 4.1 *Test sequence for qualification testing of thin film photovoltaic modules according to the IEC standard 61646 [140].*

4.1.3 Thin film photovoltaic module qualification test procedures according to IEC standard

According to the IEC thin film module qualification standard 61646 [140], it is written with amorphous silicon technology in mind, but may also be applicable to other thin film PV modules. Modifications to the test sequence described in the standard may be necessary due to the specific characteristics of these other new technologies. For example a wet leakage current test has been added to this standard because all types of thin film modules are susceptible to moisture induced corrosion. Also modules are annealed before thermal cycling and damp heat tests in order to separate the annealing effects from any degradation resulting from these tests. For thin film technologies other than amorphous silicon, pre-treatments such as light soaking and annealing may differ or may prove unnecessary.[140]. In the following there are more detailed descriptions of

the tests that are considered most relevant in the scope of this study. Also some general pass-fail criteria according to the standard are presented.

A module design shall be judged to have passed the qualification tests, and therefore, to be IEC type approved, if each test sample meets all the following criteria:
a) the degradation of maximum output power at standard test conditions (STC) does not exceed the prescribed limit after each test;
b) after the final light soaking, the maximum output power at STC is not less than 90 % of the minimum value specified by the manufacturer;
c) no sample has exhibited any open circuit or ground fault during the tests;
d) there is no visual evidence of a major defect;
e) the requirements of insulation test and wet leakage current test are met.
If two or more modules out of eight do not meet these test criteria, the design shall be deemed not to have met the qualification requirements.[140].

For the purposes of design qualification and type approval, the following are considered to be major visual defects:
a) broken, cracked, bent, misaligned or torn external surfaces;
b) voids in, or visible corrosion of any of the thin film layers of the active circuitry of the module, extending over more than 10 % of any cell;
c) bubbles or delamination forming a continuous path between any part of the electrical circuit and the edge of the module;
d) loss of mechanical integrity, to the extent that the installation and/or operation of the module would be impaired.[140].

In the scope of this study the most relevant tests are thermal cycling, humidity freeze and damp heat tests. The purpose of the thermal cycling test is to determine the ability of the module to withstand thermal mismatch, fatigue and other stresses caused by repeated changes in temperature. In the test the modules are subjected to cycling between module temperatures of -40°C±2°C and +85°C±2°C. The rate of change in temperature between the low and high extremes shall not exceed 100°C/h and the module temperature shall remain stable at each extreme for a period of at least 10 min. The cycle time shall not exceed 6h. There shall be no evidence of major visual defects and the degradation of maximum output power at STC shall not exceed 5% of the value measured before the test.[140].

The purpose of humidity freeze test is to determine the ability of the module to withstand the effects of high temperature and humidity followed by sub-zero temperatures. The modules are subjected to 10 complete cycles. During one cycle, which lasts for 24 h the modules are kept at 85 °C with 85 % relative humidity for 20 h minimum and at -40 °C 0.5 h minimum. There shall be no evidence of major visual defects and the degradation of maximum output power at STC shall not exceed 5 % of the value measured before the test.[140].

The purpose of damp heat test is to determine the ability of the module to withstand the effects of long term penetration of humidity. The modules are subjected to

85 °C with 85 % RH for a duration of 1000 h. There shall be no evidence of major visual defects and the degradation of maximum output power at STC shall not exceed 5 % of the value measured before the test.[140].

Light soaking is used to separate light induced degradation from other degradation mechanisms, and to provide the maximum power at the end of the test sequence as an estimate of the long-term performance of thin film modules. Light soaking is not really considered as a test but rather a pre-treatment of the modules. The purpose of light soaking is to stabilize the electrical characteristics of thin film modules by means of simulated solar irradiation. Using the reference device, the irradiance is set between 800 Wm^{-2} and 1000 Wm^{-2}. It has to be ensured that the module temperature does not vary by more than ±2°C within the range of 40 °C to 50 °C during the course of the test. The modules are subjected to irradiation until their maximum power values, measured over three consecutive periods of at least 48 h, are all within 2 % of each other. There shall be no evidence of major visual defects. After the final light soaking the maximum output power at STC shall not be less than 90 % of the minimum value specified by the manufacturer.[140].

The purpose of hot spot endurance test is to determine the ability of the module to withstand hot spot heating effects, for example deterioration of the encapsulation. This effect could be provoked by mismatched or cracked cells, interconnect failures, partial shadowing or soiling. Hot spot heating occurs in a module when its operating current exceeds the reduced short circuit current of a shadowed or faulty cell or group of cells within it. When such a condition occurs, the affected cell or group of cells is forced into reverse bias and dissipates power, which can cause overheating.[140]. Unfortunately the hot spot endurance of thin film PV modules was not studied in this work. However, it is included in the introduction to point out the discussion about the necessity of this test to be included in the qualification of thin film modules.

4.1.4   Module degradation vs. encapsulation

When designing a module to pass the qualification test sequence most consideration must be given to the encapsulation scheme. The cost effective deployment of PV systems is partly limited by the durability and life cycle cost of the module encapsulation materials used and thus encapsulation material is one of the most critical components of the PV module. The encapsulation material is also an important contribution to thin film photovoltaic module manufacturing costs. It is primarily designed to provide structural support, optimal optical coupling, reliable electrical isolation, and environmental protection for PV module components. The encapsulation must protect the cell from the environment, providing a cushion for thermo-mechanical stresses, while maintaining good optical properties, and chemical compatibility. The secret to success is to perform these functions while not degrading the intrinsic reliability of the cells themselves.[142], [128], [131], [133], [143].

Research on the encapsulation materials and studies that address the influence of materials degradation on cell performance are greatly needed, especially to understand

degradation of polymeric materials, the effects of water vapor permeation, corrosion, and degradation at interfaces. A good test sequence should aim to provoke chemical reactions between the cell and the encapsulant, and mechanical fatigue of the cell-encapsulant combination, and of the electrical interconnections. The ultimate need is to identify module materials that will not decrease the cell performance during exposure to actual use conditions for 30 years.[142], [128], [131], [133], [143].

Degradation of photovoltaic module in use can occur by weathering and/or soiling of the cover glass or photothermal, oxidative, or other degradation of the pottant or interdiffusion of ions into the pottant. It can also occur as matallization corrosion or electric field induced ion migration or degradation, and as polymer/metal oxide interface reactions or delaminations. Many of these processes may depend on initial impurity concentrations and trapped gases (vapors), concentration changes during use, and the introduction of reaction products during use [128]. Long term degradation mechanisms usually result from complex synergistic reactions between the environment and PV cell or module materials. The predominant degradative reactions may change during the module life. For example, degradation of polymeric materials can be catalyzed by their own reaction products, by solar cell metallization materials, or from ion transport into them that can eventually result in enhanced discoloration, cracking, moisture ingress, and failures in other module component materials. An increase of moisture in the encapsulant may facilitate electrochemical corrosion and progress to the point where dielectrical breakdown occur between the cell circuit and the module ground.[142].

The processing conditions of polymer materials such as injection molding, extrusion, polymerization of casting resin, as well as mounting conditions of the finished component part, may influence the aging behavior in a high degree.[135]. Migration of plastisizers and stabilizers through glassy polymers is accelerated by increases in temperature. A buildup of stabilizers on the surface of the polymer is often manifested by the appearance of a hazy layer or "bloom". For hydrophilic polymers, and increase in the relative humidity can result in an increase in the permeability of both water vapor and other permeant gases. Bulk optical properties of polymers typically are not influenced by changes in temperature or the application of stress. However, if these two environmental stresses cause a change in polymer morphology, i.e. crystallization, there can be a dramatic decrease in the polymer's clarity.[128]. From a technological perspective, absolute stability of component materials is not a requirement, but the rate of reaction, i.e. the relative stability, is crucial to the service lifetime of a device.[128].

Although the exact configuration of the encapsulation scheme may vary depending on the kind and design of the PV modules, the need for a suitable insulating encapsulant remains paramount. To be economically and practically useful, the encapsulant material has to meet the requirements of low cost, good processability, high optical transmission, high dielectric constant, low water absorptivity and permeability, high resistance to UV degradation and thermal oxidation, good adhesion, mechanical strength, and chemical inertness. Even though some groups suggest the use of silicon based materials [144], the

material that is considered to best up to date meet these criteria and is thus most commonly used is EVA or a random copolymer of ethylene and vinyl acetate. EVA is also being used in the encapsulation of thin film modules.[128].

However, there are certain concerns in the use of EVA, too. The stability of EVA is affected by UV insolation, temperature and its cycling, stabilizing additives and their concentrations, and other impurity ions present. Also degradation products and contact with interfaces including adhesives and primers, processing during manufacture, extrusion, lamination, and curing, and the synergism of all these variables affect the EVA stability.[145]. One of the fundamental parameters in PV module reliability is the adhesion of the encapsulant EVA to various module surfaces. Contamination of the surfaces in a PV module has a dramatic effect on adhesion. However, the most significant effect on EVA adhesion to module surfaces comes with environmental exposure. While thermal effects are minimal, in [146] significantly lower peel strengths were obtained after both humidity freeze and damp heat exposures. Thus humidity has a large impact on the adhesion values. Some EVA formulas have substantially more silane primers incorporated into their recipes. There is concern that higher primer concentrations may cause the PV module to be more moisture sensitive due to excess silane at the bondline, which can in fact reduce bond strength rather than promote adhesion.[146]. Also in [128] the authors reported that EVA has showed in some studies accelerated browning and loss of adhesion on glass samples containing vanadium oxide, antimony oxide, or a mixed copper/nickel oxide. Metal catalyzed degradation in the presence of Cu was the most severe. EVA degraded rapidly to a complete loss of tensile strength, elongation, and transmittance in 400 h for samples without primer, but the induction period was extended to 1000 h for EVA with a primer. Deacetylation occurred only in the EVA in direct contact with Al, Ni, or Ta surfaces when heated in the presence of water vapor. The degradation resulted in decreased adhesion.[128].

Another degradation mechanism detected with some EVA types is its browning due to UV radiation. The solar spectrum cut-off at sea level is 285 nm, and radiation between 290 nm and 300 nm is routinely incident at the Earth's surface. UV radiation at these wavelengths can damage polymers severely if their activation spectra are in this regime, which is thought to be the case for some EVA types. With some modified EVA types, however, this problem has been cured.[128]. Recently some other encapsulation schemes have been investigated which use conformal polymer coatings and organic varnishes, which are also frequently used in the automotive and electronics industries [143].

4.1.5   Lessons learned from crystalline silicon module testing

Crystalline silicon modules have been several years in market and thus a lot of testing experience has been gained on them. In c-Si modules most module reliability problems are related to the encapsulant system: soiling, cracking, yellowing, delaminating, accelerated corrosion, voltage breakdown, laminating stresses and differential expansion stresses. Second most frequent module reliability problems in c-Si

modules are related to circuit integrity: fatigue due to differential expansion stresses and poor solder joints.[131]. In [128] the authors report that the early failure modes in c-Si modules included delamination at interfaces, penetration of liquid water, short circuits and arcing, cracking of the solar cells from expansion/contraction stresses, cell interconnect failures, charring and melting of solder from hot spots, and excessive soiling.[128]. According to [133] the 200 thermal cycle test provoked the largest number of power loss failures of any test in c-Si modules, which clearly demonstrates the fatigue caused by this test. These power losses are caused by the thermo-mechanical stresses causing fatigue in the electrical interconnections, or damage to cells. The conditions in the damp heat test accelerate corrosion processes, leading to reductions in IV curve fill factor.[133].

New cell materials and monolithic structures require new device processing techniques, but the package function and design evolves to a lesser extent. Although there are new encapsulants optimized to take advantage of the mechanical flexibility and low temperature processing features of thin films, the reliability and life degradation stresses and mechanisms remain mostly unchanged. Thin film module failure/degradation mechanisms are as follows. Corrosion is main failure mechanism since layers are so thin. Therefore it is very important to prevent adhesive failures or delamination in the package and humidity penetration especially if EVA and Tedlar is used. Corrosion of output leads is also critical because this is the easiest single point failure mode. Thus key reliability technologies in common between crystalline and thin film modules include hot-spot heating, galvanic and electrochemical corrosion, hail-impact stresses, glass breakage and mechanical fatigue. Also photothermal degradation of encapsulants, operating temperature, moisture sorption, circuit design strategies, product safety issues, and the process required to achieve a reliable product from a laboratory prototype have to commonly be considered for all PV devices.[131], [141].

However, corrosion-type issues are clearly different between c-Si and thin film modules, although data from electrochemical corrosion studies indicate there is not much difference between the resistance of thin film modules and those of crystalline modules. When there is a micrometer of material and half a micrometer of it is lost, practically a whole cell is lost. On a crystalline cell you can loose a lot of the metallization system, there are bulk amounts of material that you ca corrode away and still leave an active solar cell.[131]. Another difference is the hot spot endurance. In [147] the hot-spot phenomenon in c-Si solar cells is studied. In a c-Si cell array the interconnected electrical generators or solar cells must be electrically matched, i.e. they must develop the same current when connected in series, or the same voltage when connected in parallel. A mismatched generator, such as a cracked or shadowed cell, acts as an internal load, dissipating power and producing a hot-spot, while reducing the power output of the array.[147]. On the contrary, when hot-spot testing of a-Si modules in [111] the hot-spot temperatures usually did not exceed 120 °C. It was difficult to find cells with a back-bias voltage high enough to provide power dissipation leading to a significant hot-spot

temperature. The power dissipation obtained in the cells tested was not enough to produce a hot-spot problem.[111].

New materials and processes in thin-film modules will require a diliquent reliability program which should include the establishment of mechanism-specific reliability goals, quantification of mechanism parameter dependencies, prediction of expected long-term degradation, identification of cost-effective solutions, and testing and failure analysis of trial solutions.[131]. For each new PV module technology, reliability testing requires a baseline of outdoor exposure testing to identify failure mechanisms for which accelerated tests can be developed. Until this field work has been completed, there is no basis for believing that passing the crystalline silicon qualification test sequence means anything for a new technology module. At this stage of development the accelerated tests should be considered reliability not qualification tests. New technologies will likely suffer from failure mechanisms that are not even tested for in the crystalline test sequence. In addition, care must be taken when interpreting failures of new module technologies in the tests designed for crystalline silicon.[134]. Probably the most important lesson learned from the crystalline program is that honest conscientious working of reliability and safety issues can significantly affect the economic viability and public acceptance of the product. Resolving the issues is not cheap, and cannot be accomplished overnight.[131].

4.1.6 Overview of this study on accelerated lifetime testing

In this study single junction amorphous silicon photovoltaic modules and CdTe and CIGS prototype modules were tested. Thermal cycling and humidity freeze tests were executed according to the standard procedures. During the damp heat test the test was interrupted after every certain time periods and the modules were visually inspected and measured for their electrical performance. Otherwise also the test methods for damp heat test were according to the IEC qualification standard 61646 [140]. Additionally dry heat test, which is not listed in the qualification test sequence, was executed for one CdTe prototype module. Also light soaking was done for a-Si modules, CdTe prototype modules from two different manufacturers and for CIGS modules from two different batches. Light soaking was not considered in this study as a pre-conditioning step according to the standard, but rather as a study of the light behavior of the different thin film technologies.

The general conclusion for all the thin film photovoltaic technology modules included in this study is that the major cause for failure in accelerated lifetime tests is humidity penetration into the module encapsulation. In amorphous silicon modules humidity penetration caused major visual defects but the electrical performance was not affected very much. In CdTe prototype modules humidity penetration caused changes in the back contact composition which could be visually detected and which lead to degradation in electrical performance. In CIGS prototype minimodules humidity penetration caused corrosion of cell interconnect areas. Back contact Mo and connection between the front contact ZnO and back contact Mo lay relatively unprotected on these

cell line areas. This corrosion could be observed both visually and as degradation in the electrical performance.   In thermal cycling no major degradation was observed. The degradation in humidity freeze resembled degradation in damp heat but was less in quantity since the modules were exposed to humidity for a shorter time period than in the damp heat test. In dry heat test some degradation in the CdTe module was observed but further investigations would be needed to confirm the phenomenon and to find causes for it.   In light soaking two series of samples of a-Si, CdTe and CIGS modules and prototypes were tested.   The electrical performance of the samples was measured frequently during the exposure.   As a result the a-Si degraded in performance, as expected from the literature. The CdTe samples degraded in maximum power but all the samples did not behave consistently during the exposure time. The CIGS samples mostly gained in maximum power although there were inconsistencies in the behaviour also within these samples.

4.2 Thermal cycling and humidity freeze tests

4.2.1 Test sequence description

The thermal cycling and humidity freeze tests were done to thin film photovoltaic modules according to the IEC standard testing procedure 61646 [140]. In the thermal cycling test the modules were exposed to 50 thermal cycles. The test chamber used for both thermal cycling and humidity freeze was a Weiss Technik climatic chamber. One thermal cycle is completed in four hours. During one cycle the modules stay at +85 °C and –40 °C about 20 min in each. The rate of change in temperatures during one cycle is according to the standard requirements.

After the thermal cycling test the modules were exposed to humidity freeze test. The humidity freeze test consists of ten cycles and each cycle lasts 24 hours. During one cycle the modules are kept for 20 hours at a temperature of +85 °C and a relative humidity of 85 %. After this period the temperature is dropped to –40 °C and the modules are kept at this temperature for one hour before raising the temperature and starting the cycle again. Again the rate of change in temperatures confirm to the standard requirements. In both thermal cycling and humidity freeze the modules were continuously monitored for their open circuit voltage.

The modules were visually inspected and electrically measured before and after thermal cycling and after humidity freeze tests. As measurement equipment SpectroLab large area pulsed solar simulator was used and a crystalline silicon reference cell was used as reference device for measurements of all modules.

4.2.2 Sample description

Table 4.I below indicates the modules exposed to the thermal cycling and humidity freeze tests. The a-Si modules were 1 x 1 ft^2 or 1 x 3 ft^2 modules with polyurethan (PUR) frame and acrylic resin encapsulant between the two glasses. The smaller modules had a symmetric frame on the edge at the back and front of the module. In the larger modules the frame on the back was covering a wider area on the side edges than on the front side. The CdTe modules were 30 x 30 cm^2 prototype modules with aluminum frames and the two glasses were laminated with EVA. The CIGS samples were 10 x 10 cm^2 prototype mini-modules and the two glasses were laminated with EVA. The CIGS samples were unframed but there was a 1.2 cm area between the module edge and the active thin film. The humidity tightness of the connections coming out from between the glasses was enhanced by protecting them with plastic molds.

Table 4.I   *Description of the samples exposed to thermal cycling and humidity freeze.*

ESTI ID	Thin film material	Module size	Module description
AB506	a-Si	1 x 1 ft^2	PUR framed glass-glass module
AB507	a-Si	1 x 1 ft^2	PUR framed glass-glass module
AB512	a-Si	1 x 3 ft^2	PUR framed glass-glass module
AB513	a-Si	1 x 3 ft^2	PUR framed glass-glass module
CB507	CIGS	10 x 10 cm^2	Glass-glass unframed prototype mini-module
CB508	CIGS	10 x 10 cm^2	Glass-glass unframed prototype mini-module
ZB504	CdTe	30 x 30 cm^2	Al-framed glass-glass module
ZB505	CdTe	30 x 30 cm^2	Al-framed glass-glass module

4.2.3   Results

Visual inspection

In the a-Si modules no major defects were observed after thermal cycling or humidity freeze tests. In the small a-Si modules some start of delamination was visible along the side edges after thermal cycling. Photograph of this pattern can be seen in Figure 4.2 below. In the large a-Si modules no defects were observed after thermal cycling nor humidity freeze tests.

In the two CdTe modules included in the thermal cycling and humidity freeze tests the back contacts differed initially in color. In the other module ZB505 the junction box upper material had melted during the thermal cycling test. After humidity freeze more melting of the junction box plastic in ZB505 was observed (Figure 4.4(a)). In the other module ZB504 the junction box showed deformation by cracking but only after the humidity freeze test (Figure 4.3(b)). In ZB504 in the front color changes forming black dotted areas around the corners were observed (Figure 4.3(a)). In ZB505 bubbles and some delamination appeared in the back around the center tedlar piece situated under the junction box (Figure 4.4(b)). In ZB505 also the back contact changed color to dark gray radially around the corner areas (Figure 4.5). Photographs of the defects in CdTe modules after thermal cycling and humidity freeze tests are shown in Figures 4.3-4.5 below.

As a visual defect in the CIGS modules after the humidity freeze test the EVA

between the glasses changed from being transparent to white or looking like foggy. This defect could be detected in both samples CB507 and CB508. This change was visible only outside the active film part of the module. However in both of the samples the middle active area of the front film appeared to look somewhat darker colored than the edge part of the film after humidity freeze testing. Photographs of the defects are shown in Figure 4.6 below for the modules CB508.

Figure 4.2   *Starting of delamination on the side edge of the back contact on 1 x 1 ft² a-Si module AB507 after 50 cycles of thermal cycling test.*
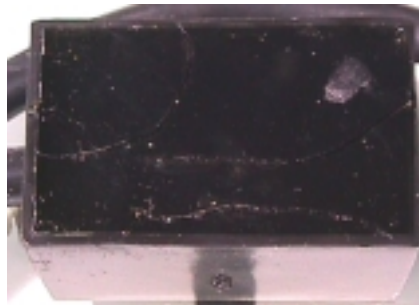
| (a) | (b) |

Figure 4.3   *Defects in CdTe module ZB504 after humidity freeze testing. (a) The front contact color changed forming black dots on the corner areas. (b) The junction box cover plastic cracked.*
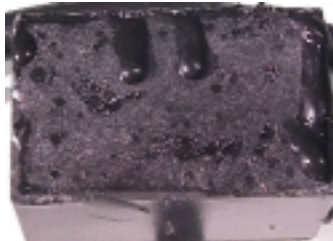
| (a) | (b) |

Figure 4.4   *Defects in CdTe module ZB505 after thermal cycling and humidity freeze tests. (a) Junction box deformation by plastic melting after thermal cycling test. (b) Bubbles and delamination on the back of the module after humidity freeze testing.*
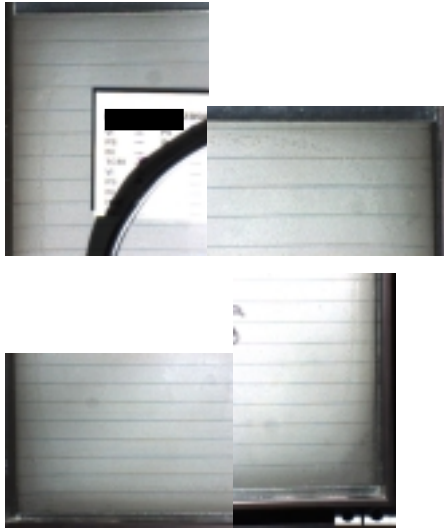
Figure 4.5 *Darkening of the back contact around the corner areas in CdTe module ZB505 after humidity freeze testing.*

| (a) | (b) |
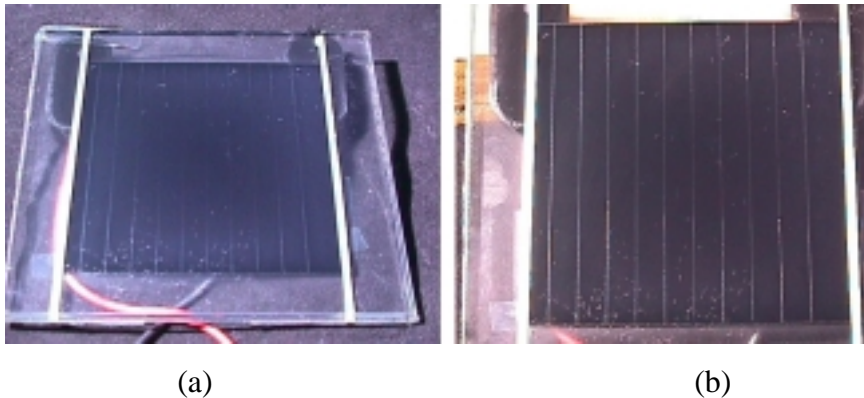
Figure 4.6 *Visual defects observed in the CIGS sample CB508 after humidity freeze testing. (a) The EVA around the active area of the sample turned white or foggy. (b) The middle of the active area appears somewhat of darker color than the edge area.*

Electrical performance

The average normalized degradation of 1 x 1 ft^2 a-Si modules after thermal cycling and humidity freeze tests is illustrated in Figure 4.7 below. On average no degradation was observed in short circuit current or fill factor. After thermal cycling 2 % degradation was seen in open circuit voltage and 3 % degradation in maximum power. After humidity freeze the V_{oc} had increased back to the initial values and in P_{max} the degradation had reduced to 2 %. After thermal cycling the other module had degraded slightly more in V_{oc} and especially in P_{max} than the other one but after humidity freeze test their performance was even. In general the modules can not be said to have degraded in the thermal cycling or humidity freeze tests.

The average normalized degradation of 1 x 3 ft^2 a-Si modules in thermal cycling and humidity freeze is shown in Figure 4.8 below. On average there were no changes in

the electrical performance after thermal cycling or humidity freeze tests. Both modules behaved the same way and thus no degradation in either of them was observed after the tests.

The normalized average degradation of CdTe modules in thermal cycling and humidity freeze is shown in Figure 4.9 below. In the CdTe modules about 5 % degradation in fill factor was observed after thermal cycling. No degradation in the other IV parameters was observed after thermal cycling. After the humidity freeze test a degradation of 22 % was detected in maximum power and in fill factor but no degradation in I_{sc} or V_{oc}. A somewhat differing behavior was seen between the two modules tested. In I_{sc} after thermal cycling neither of the modules showed any degradation. After humidity freeze the other module ZB504 degraded in I_{sc} 2 % and the other one ZB505 4 %. In V_{oc} no degradation was observed in either of the modules after both tests. In P_{max} ZB504 had degraded 8 % after thermal cycling and ZB505 not at all. However after humidity freeze the degradation for ZB504 was 12 % and for ZB505 34 %. In fill factor the module ZB504 had degraded after thermal cycling 9 % and the module ZB505 2 %. After humidity freeze the degradation in fill factor for ZB504 was 10 % and for ZB505 33 %.

The normalized average degradation of CIGS prototype mini-modules after thermal cycling and humidity freeze is shown in Figure 4.10 below. On average no degradation was observed in any of the IV parameters after thermal cycling. After humidity freeze no degradation was observed on average in short circuit current or open circuit voltage. In maximum power the CIGS samples degraded on average 12 % and in fill factor the degradation was 11 %. After thermal cycling none of the two CIGS modules showed any changes in performance and thus the average describes their behavior well. After humidity freeze in I_{sc} neither of the samples showed any changes. In V_{oc} the other sample CB507 showed no changes in performance and the other one CB508 degraded 2 % after humidity freeze. In P_{max} CB507 degraded after humidity freeze test 8 % and CB508 15 %. In fill factor the degradation of CB507 was 10 % and of CB508 13 % after humidity freeze testing.
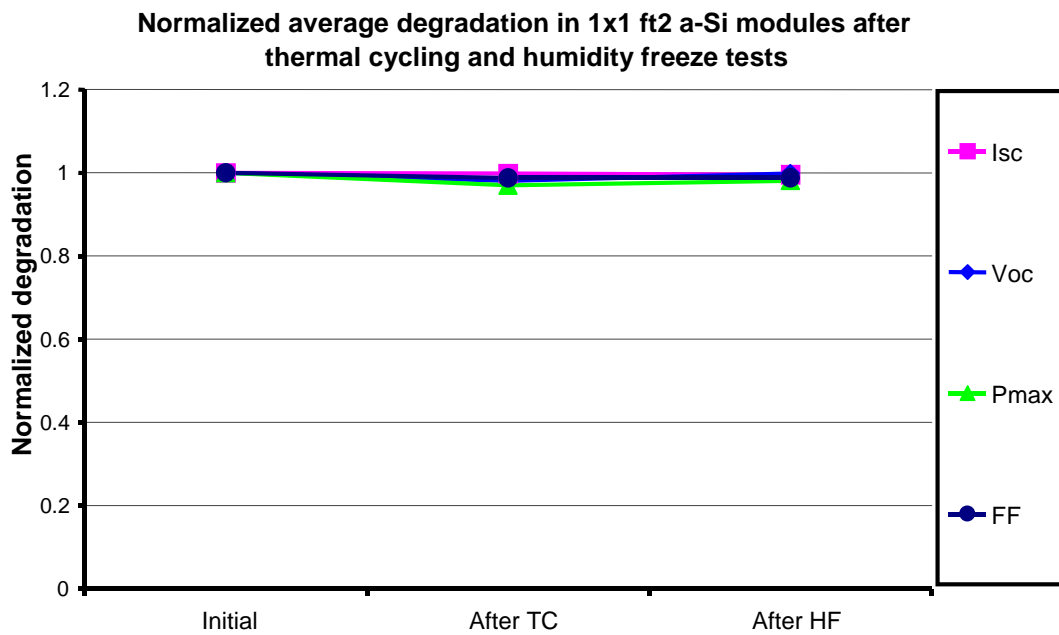
Figure 4.7 *Normalized average degradation of the 1 x 1 ft² a-Si modules after thermal cycling and humidity freeze tests.*
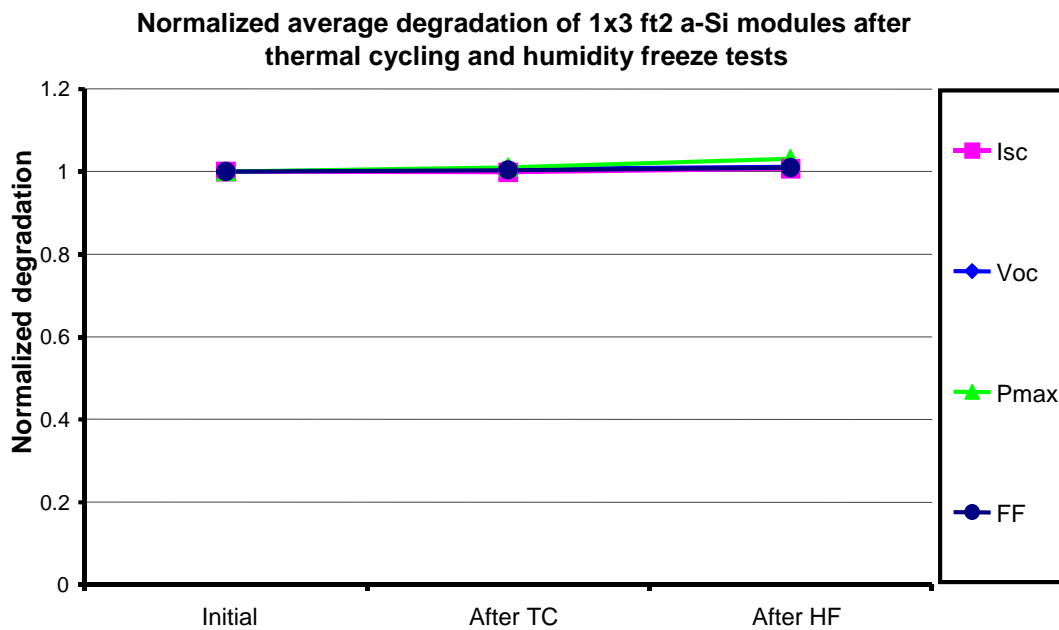
Figure 4.8 *Normalized average degradation of the 1 x 3 ft² a-Si modules after thermal cycling and humidity freeze tests.*
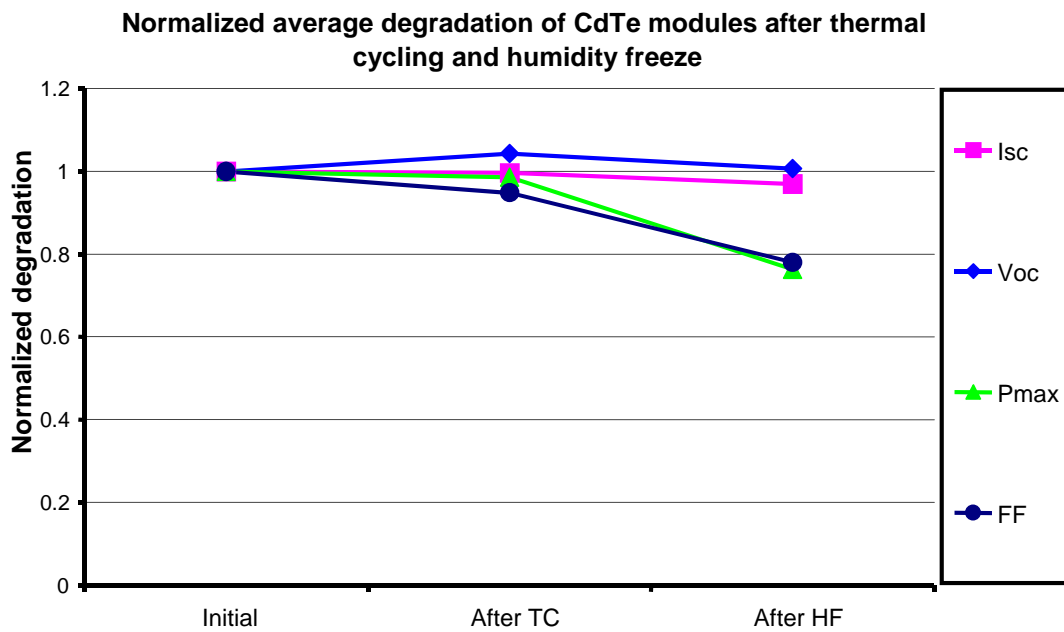
Figure 4.9 *Normalized average degradation of the CdTe modules after thermal cycling and humidity freeze tests.*
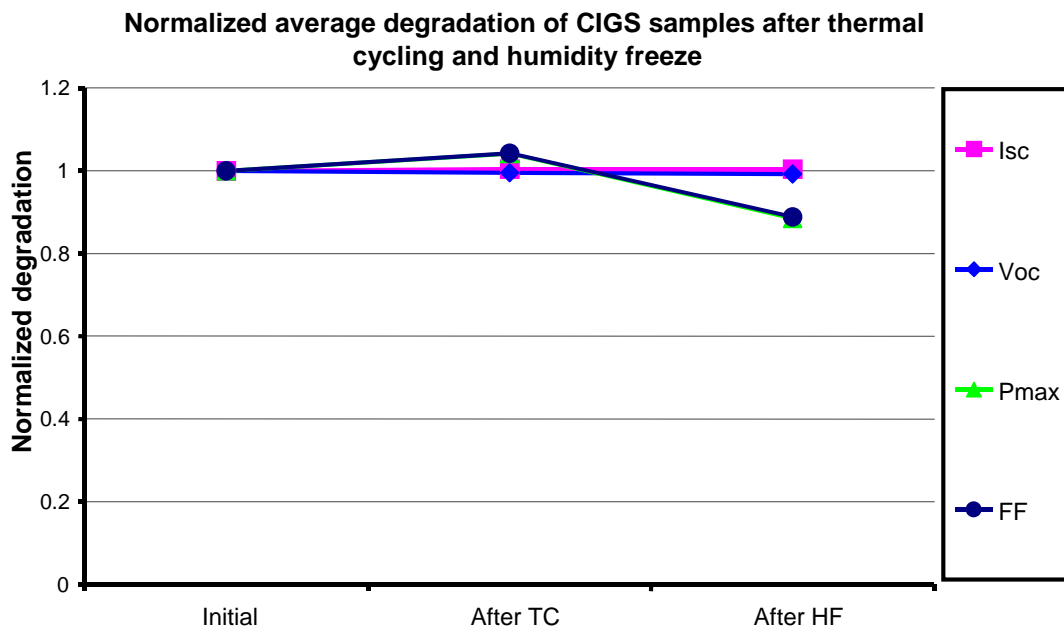

Figure 4.10 *Normalized average degradation of the CIGS prototype mini-modules after thermal cycling and humidity freeze tests.*

4.3   Damp heat testing

4.3.1   Test sequence description

In the damp heat tests the modules were kept at a temperature of +85 °C and a relative humidity of 85 % totally for 1000 hours. Weiss Technik climatic chamber was used. Open circuit voltage of the modules and the humidity within the chamber were continuously monitored during the test.

To check the performance of the modules during the test, visual inspection and electrical characterization was done by interrupting the test after certain time periods. The electrical performance was measured with SpectroLab Large Area Pulsed Solar Simulator (LAPSS). As a reference device a crystalline silicon reference cell was used for all the measurements presented in here. For all module technologies tested in the two consequent damp heat exposures there was always a reference module for each technology. This reference module was kept in dark and measured in the beginning and end of the test run. Thus any possible larger distortions in the measurement accuracy between the first and the last measurements were eliminated.

Visual inspection was done under photographic halogen lamps and photographs were taken with digital cameras. Also a microscope was used when necessary. The climatic chamber was loaded at ambient conditions and then brought to the operating temperature and humidity conditions over a period of two hours. When cooling the chamber to room temperature at the end of each test step, four hours were allowed to avoid possible thermal shock for the modules.

In the first round of damp heat testing all the a-Si, CdTe and CIGS modules included in the test were visually inspected and electrically characterized before and after the test as well as during the exposure according to the following sequence: before test, then after 10, 30, 60, 110, 185 testing hours, then after every 100 hours until 885 test hours and finally in the end of testing time after 1000 hours of damp heat exposure.

In the second round of damp heat testing the a-Si and CIGS modules were IV measured for the electrical performance and visually inspected before and after the test and after every 100 test hours up to 400 test hours and then every 200 test hours until the end of the test. The CdTe modules in the second test round were IV measured and visually inspected before and after the test and during the test after every 100 test hours throughout the entire testing period. Two a-Si modules from the first damp heat test round were included in the second test run also. These modules were IV measured for electrical performance as described for a-Si and CIGS modules above but visually inspected only in the end of the test.

4.3.2   Sample description

The modules included in the first damp heat test round are listed in Table 4.II below. The a-Si modules were 1 x 1 ft^2 modules with polyurethane (PUR) frame and acrylic resin encapsulant between the two glasses. The CdTe modules were 30 x 30 cm^2

prototype modules with aluminum frames and the two glasses were laminated together with EVA. The CIGS sample was a prototype mini-module of 10 x 10 cm^2, the two glasses laminated with EVA. The CIGS sample had no frame but there was a glass edge of about 1.5 cm wide before the active cell area started. The Al-busbars came out unprotected from between the glasses.

Table 4.II   *Description of the samples exposed to damp heat testing in the first round of testing.*

ESTI ID	Thin film material	Module size	Module description
AB504	a-Si	1x1 ft^2	PUR framed glass-glass module
AB505	a-Si	1x1 ft^2	PUR framed glass-glass module
CB505	CIGS	10x10 cm^2	Glass-glass unframed prototype mini-module
ZB501	CdTe	30x30 cm^2	Al-framed glass-glass module
ZB502	CdTe	30x30 cm^2	Al-framed glass-glass module

Table 4.III below indicates the modules exposed to the damp heat test in the second round of testing. The small a-Si modules (AB504 and AB505) continued from the first round of damp heat testing and thus after this second testing period were exposed totally to 2000 hours of damp heat. The large a-Si modules were PUR framed and had acrylic resin between the glasses. In the large a-Si modules the frame on the back was covering a wider area on the side edges than on the front side. The CIGS modules were unframed glass-glass prototype mini-modules laminated with EVA. The humidity tightness in the interconnections had been enhanced by protecting the outcoming from between the glasses with plastic molds. Compared to the CIGS sample in the first set of testing the active area for the samples in the second set was smaller and consequently there was a wider protective area around the edges. The CdTe modules were Al-framed glass-glass prototype modules laminated with EVA. The humidity tightness in the CdTe modules had been enhanced using resin between the back contact and the EVA.

Table 4.III *Description of the samples exposed to damp heat test in the second set of testing.*

ESTI ID	Thin film material	Module size	Module description
AB504(old)	a-Si	1 x 1 ft^2	PUR framed glass-glass module, continuing from the previous test round
AB505(old)	a-Si	1 x 1 ft^2	PUR framed glass-glass module, continuing from the previous test round
AB514	a-Si	1 x 3 ft^2	PUR framed glass-glass module
AB515	a-Si	1 x 3 ft^2	PUR framed glass-glass module
CB509	CIGS	10 x 10 cm^2	Glass-glass unframed prototype mini-module
CB510	CIGS	10 x 10 cm^2	Glass-glass unframed prototype mini-module
ZB510	CdTe	30 x 30 cm^2	Al-framed glass-glass module
ZB511	CdTe	30 x 30 cm^2	Al-framed glass-glass module

4.3.3   Results

Visual inspection

In the first round of damp heat testing in the a-Si modules the major visual defects detected were some pinholes and white dots along the edge areas in the front side. In the back side some small bubbles were detected as well as delamination along the side edges and Al back contact discoloration especially along the cell lines along the edges of the modules. Also the polyurethan frame suffered some deformation on places were the module had been leaning to the rack structure in the climatic chamber. Photographs of the visual defects in a-Si modules after 100 hours of damp heat testing are illustrated in Figure 4.11 below.

In the CdTe modules after the first round of damp heat testing yellow patterns and some white dots were observed in the front of the module. In the back of the module bubbles around the junction box area were detected as well as cracking and deformation of the junction box. Around corners of the module the back contact changed color from light to

dark gray. On the frame the bolts for mounting oxidized in one of the modules. Photographs of the visual defects in CdTe modules after 1000 hours of damp heat testing are presented in Figure 4.12 below.

In the CIGS module in the first round of damp heat testing the only visual defect observed was that the cell lines became transparent starting from the edges after 60 hours of exposure. The transparency continued to proceed from the edge towards the center of the active area throughout the testing time. After the test the center part of the module appeared slightly lighter in color than the edge parts. Photograph of the visual defects in one of the two exposed CIGS samples is shown in Figure 4.13 below.

Table 4.IV below summarizes the visual defects of the first round of damp heat testing correlating them with the defects listed in the IEC standard 61646 [140] for thin film module testing. The defects listed in the standard disqualify the modules going through the type approval testing according to the standard testing procedure.

Table 4.IV *Summary of the visual defects in the first set of damp heat testing in correlation with the IEC standard 61646 [140].*

Defect description in IEC 61646	Corresponding defect in first round of damp heat testing		
	a-Si	CIGS	CdTe
broken, cracked, bent, mis-aligned or torn external surfaces	one leaning corner slightly deformed	none	junction box plastic cracked
faulty interconnections or joints	none	none	none
voids in, and visible corrosion of any of the thin-film layers of the active circuit	corrosion/humidity dots	transparency in cell lines	humidity patterns
visible corrosion of output connections, interconnections and bus bars	none	none	none
failure of adhesive bonds	none	none	none
tacky surfaces of plastic materials	none	none	none
faulty terminations, exposed live electrical parts	none	none	none
any other conditions which may affect performance	none	none	none
bubbles, delamination or any kind of defect forming a continuous path between a cell and the edge of the module	bubbles but not continuous path, delamination	none	bubbles forming path with cell lines nearby junction box area

(a)   (b)

(c)   (d)

(e)   (f)

(g)
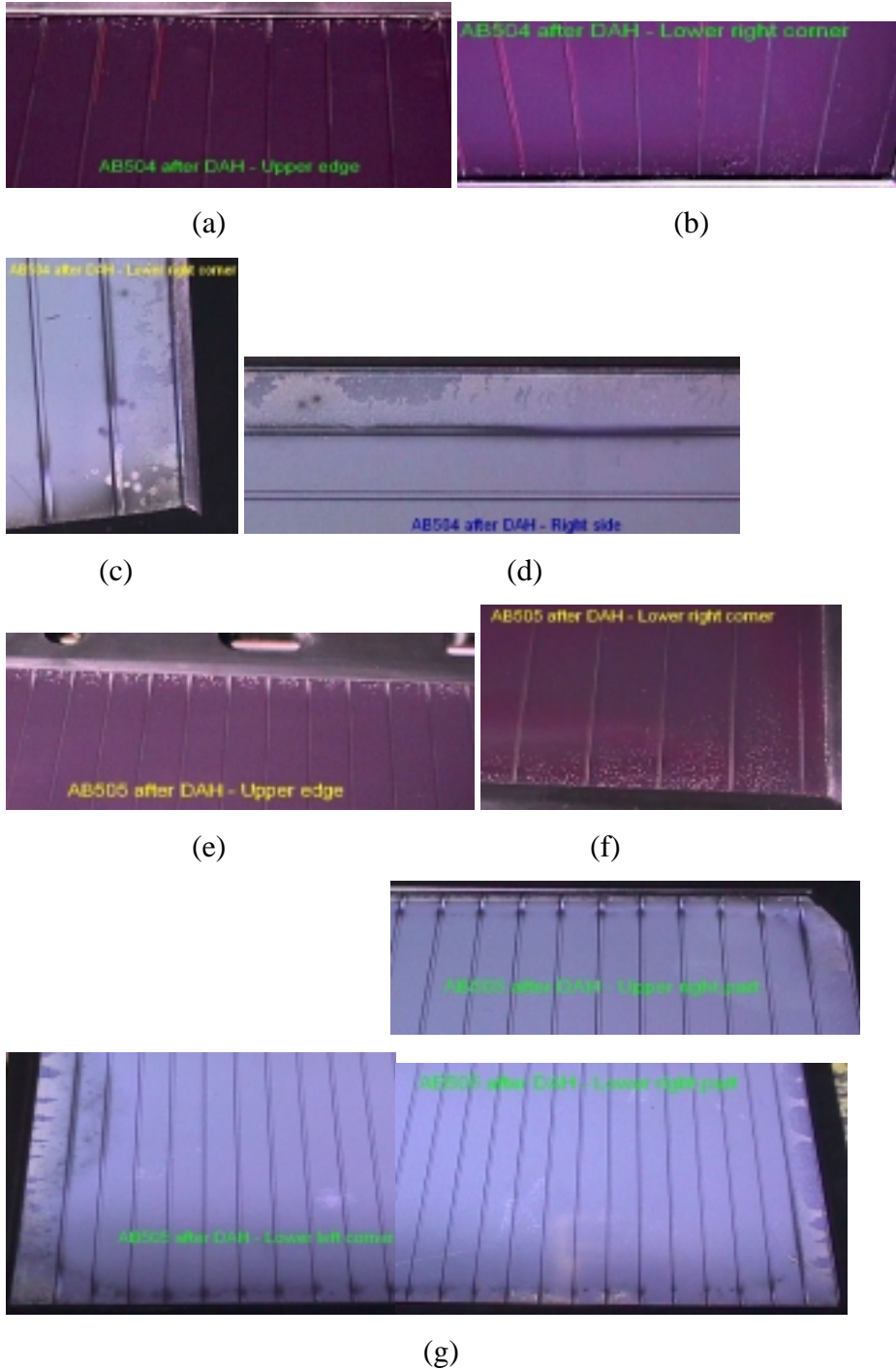
Figure 4.11 *Photographs of visual defects in a-Si modules after 1000 hours of the first round of damp heat testing. (a) and (b) White dots in the front film on upper and lower edges of the module AB504. (c) and (d) Delamination along the side edge and Al-back contact discoloration or corrosion around one corner in AB504. (e) and (f) White dots in the front film on upper and lower edges of the module AB505. (g) Delamination and Al-back contact discoloration along the edges on the back of module AB505.*
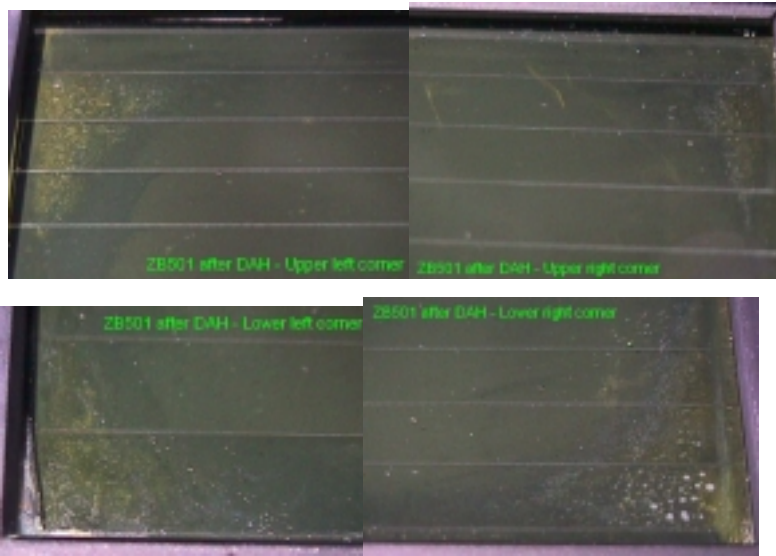
(a)
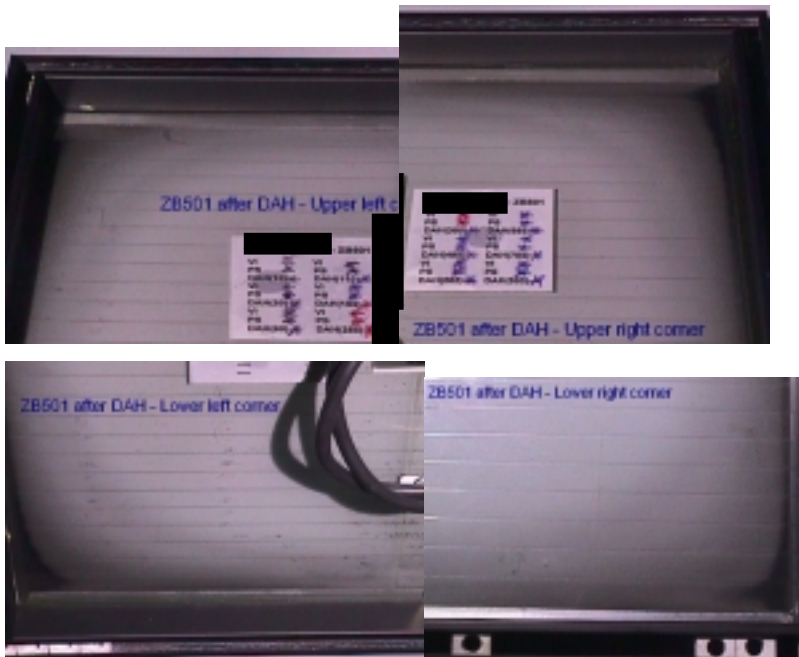
(b)

(c)
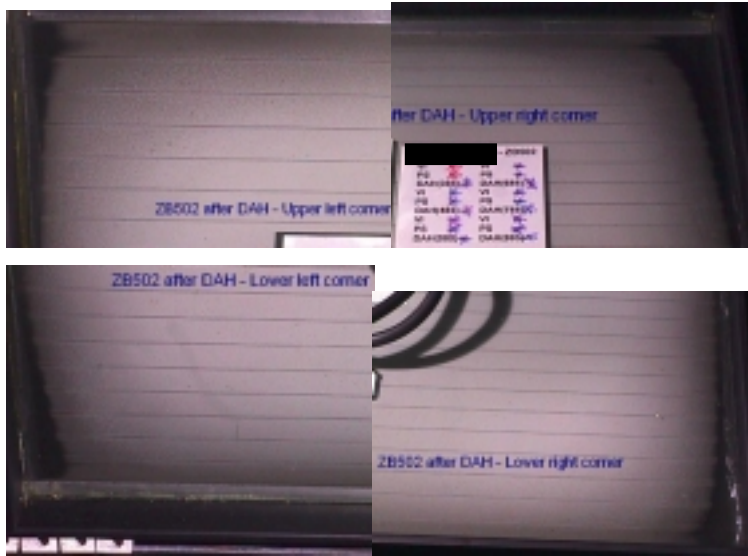
(d)

Figure 4.12 *Photographs of visual defects of CdTe prototype modules after 1000 hours of damp heat testing. (a) Color changes in the front film as yellow and white dots around the corner areas in ZB501. Similar changes occurred in ZB502 s well. (b) Color changes in the back contact around the edges and corner areas in ZB501. (c) Bubbles and delamination around the junction box area in the back contact of ZB501. (d) Color changes in the back contact around the edges and corner areas in ZB502.*
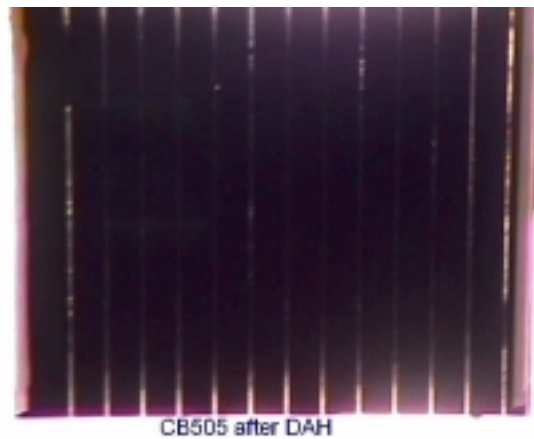
Figure 4.13 *Photograph of the visual defects after 1000 hours of damp heat exposure in CIGS prototype mini-module CB505. The photograph is taken towards bright light and thus the cell line transparencies around the edges are visible.*

In the second round of damp heat testing only a few visual defects were detected in the 1 x 3 ft^2 a-Si modules. Some white dots appeared along the upper and lower edges in the front film of the modules and the number of pinholes increased. Photographs of the visual defects in the a-Si modules after second round of damp heat testing are shown in Figure 4.14 below.

In the CIGS samples in the second round of damp heat testing the transparent edge outside the active film area became very white like foggy. The cell lines became somewhat transparent starting along the film edges. By the end of the test the transparent cell line part had a slight yellow color and overall the module appeared darker colored in the middle and lighter around the active film edges. Photographs of the visual defects in the CIGS prototype modules after 1000 hours of the second round of damp heat testing can be seen in Figure 4.15 below.

As visual defects in the CdTe prototype modules after the second round of damp heat testing the back contact of the Al film showed darkening in a peeling like patterns along the edges but not starting right from the edge. In the front around the corner areas white-bluish curly shaped lines, like delamination, appeared. In the other module (ZB510) the front glass nest to the frame was broken after 300 test hours. The upper part of the junction box melted to form big crater like holes already during the initial testing hours. In the front film the color appeared to change leaving the corner areas radially to be of very dark green shade and the middle part to be of light green colored. Photographs of the major visual defects in the CdTe modules after second round of damp heat testing are shown in Figure 4.16 below.

In the a-Si modules continuing from the first round of damp heat testing to this second round of testing the same visual defects, observed already after the first 1000 hours of damp heat test, continued to grow. The worst defect towards the 2000 test hours was that the plastic material of the electrical wires became hard and cracked on several places short-circuiting the module. Only when replacing the wires the modules could be measured by the end of 2000 test hours. Photographs of the a-Si modules after 2000 hours of damp heat testing are shown in Figure 4.17 below.

Table 4.V below summarizes the visual defects in the second set of damp heat testing and correlates them to the visual defects listed in IEC standard 61646 [140]. In table 4.V the modules indicated for a-Si material are those 1 x 3 ft^2 modules having taken part only in the second set of damp heat testing. The a-Si modules that continued testing after the first set of damp heat are not included.

Table 4.V *Summary of the visual defects in the second set of damp heat testing according to the IEC standard 61646 [140]. The a-Si modules included in this table are the 1 x 3 ft^2 modules tested in the second set of damp heat.*

Defect description in IEC 61646	Corresponding defect in second round of damp heat testing		
	a-Si	**CIGS**	**CdTe**
broken, cracked, bent, mis-aligned or torn external surfaces	none	none	junction box deformation, broken front glass
faulty interconnections or joints	none	none	none
voids in, and visible corrosion of any of the thin-film layers of the active circuit	corrosion/humidity dots	transparency in cell lines	humidity patterns in back and front
visible corrosion of output connections, interconnections and bus bars	none	none	bus bar oxidization
failure of adhesive bonds	none	none	none
tacky surfaces of plastic materials	none	none	none
faulty terminations, exposed live electrical parts	none	none	none
any other conditions which may affect performance	none	none	none
bubbles, delamination or any kind of defect forming a continuous path between a cell and the edge of the module	none	none	bubbles
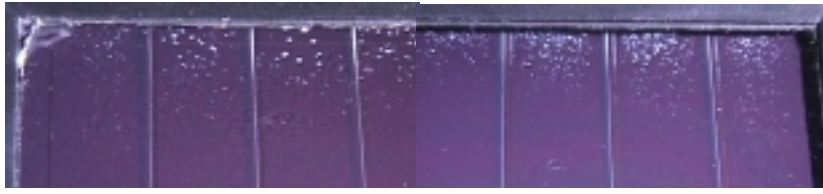
(a)
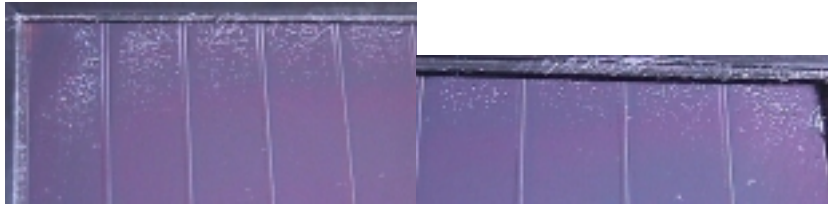
(b)

Figure 4.14 *Photographs of the a-Si 1 x 3 ft^2 modules after the second set of damp heat testing. White dots appearing on the upper and lower edges in the front film of the a-Si module (a) AB514 and (b) AB515 after 1000 hours of damp heat.*
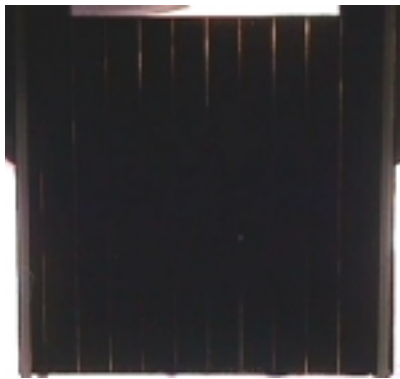
(a)

(b)

Figure 4.15 *Photographs illustrating (a) transparency in the cell lines in CB509 and (c) white or foggy looking edge areas in CB510 after 1000 hours of the second round of damp heat testing in the CIGS prototype mini-modules.*
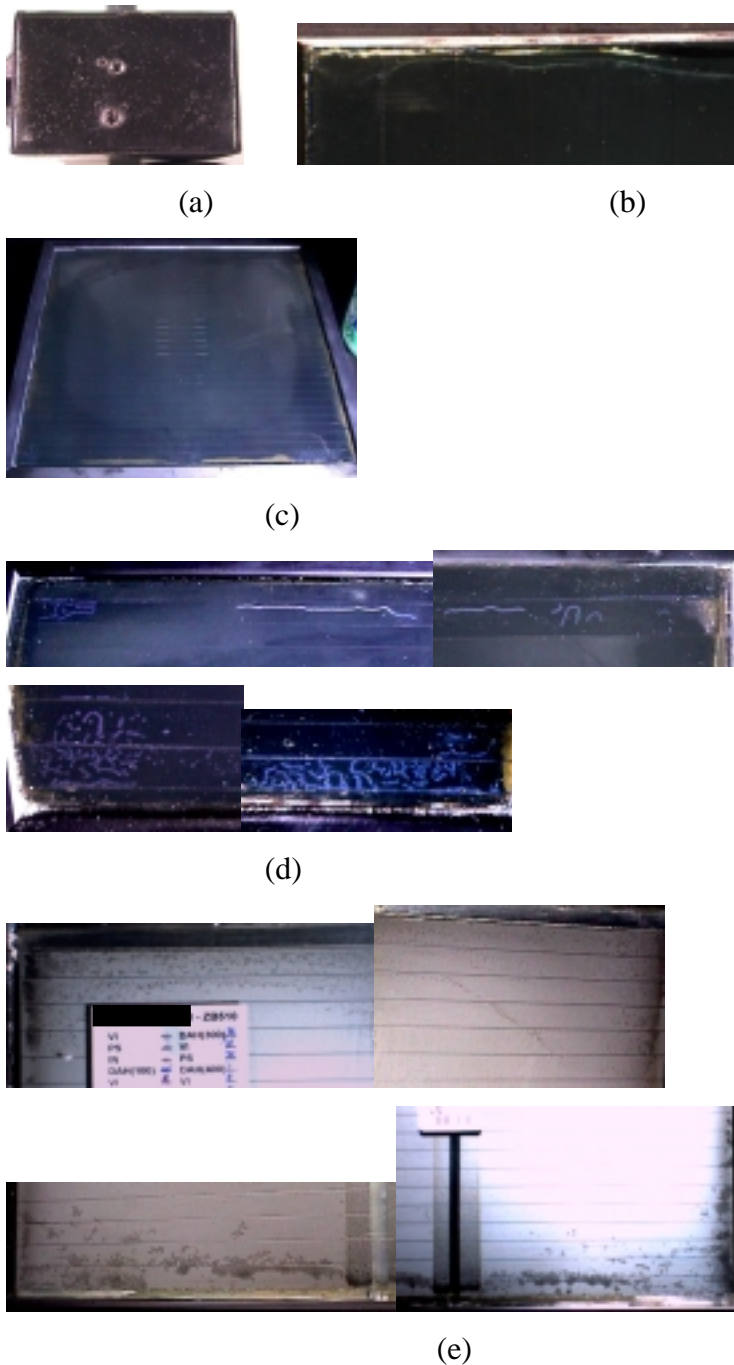
Figure 4.16 *Photographs of visual defects in the ZB510 CdTe module in the 2nd set of damp heat test. (a) Junction box deformation after 100 h of testing. (b) Cracking of the front glass after 300 h of testing. (c) Non-uniform front color after 900 h of testing. Darker areas can be seen radially around the edges and lighter color in the middle. (d) White lines and spots in front contacts after 1000 h of testing, looking like delamination. (e) Darkening of the back contact around the edge areas after 1000 h of test. Similar defects were detected in the other module ZB511 except for the glass cracking.*

<div align="center">(a)   (b)</div>
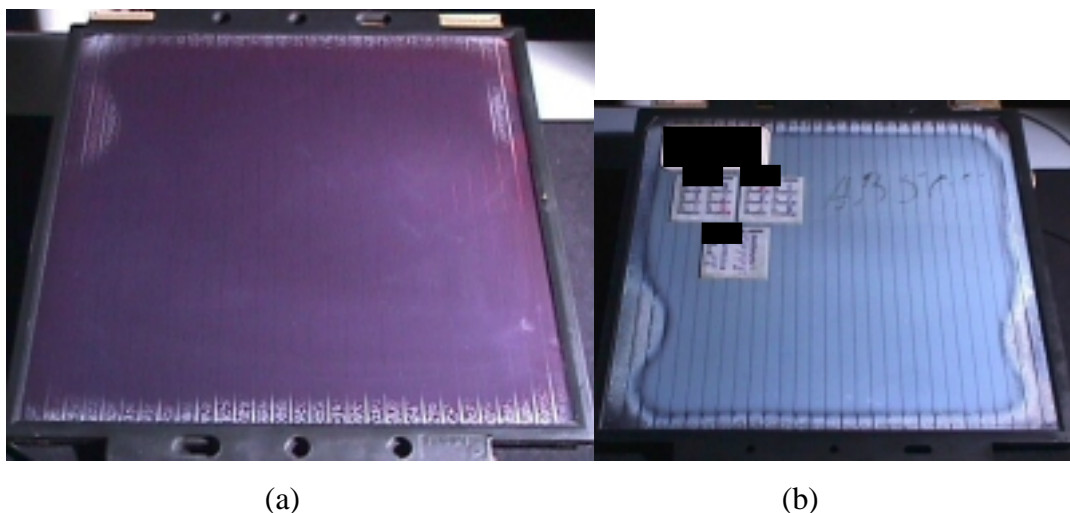
Figure 4.17 *Photographs illustrating the visual defects in the (a) front and (b) back of the a-Si module AB505 after 2000 hours of damp heat testing. The other module AB504 had similar visual defects after 2000 hours of damp heat testing.*

Electrical Performance

The normalized average results in electrical performance for 1 x 1 ft^2 a-Si modules in the first series of damp heat testing are shown in Figure 4.18 below. No degradation in short circuit current or in open circuit voltage was observed. In maximum power the a-Si modules experienced a degradation of 10 % and in fill factor a degradation of 9 %. The degradation patterns are similar for both modules and thus the average describes the degradation of a-Si modules well.

The normalized degradation of the one CIGS prototype module included in the first series of damp heat testing is shown in Figure 4.19 below. The degradation in the short circuit current, fill factor and maximum power started after 100 test hours. After 485 hours of damp heat testing no current could be measured anymore. The module degraded mostly in I_{sc} and P_{max}. Also the fill factor degraded in the beginning of the test but stabilized around 300 hours of testing. The open circuit voltage had degraded after 285 hours of damp heat by 7 % which is significantly less than the degradation values of 77 % in I_{sc} and 89 % in P_{max} at the same point of testing.

The normalized average degradation in the CdTe modules in the first series of damp heat is shown in Figure 4.20 below. In the end of the test the short circuit current had experienced a degradation of 17 % and the open circuit voltage and fill factor a degradation of 53 %. The degradation in the maximum power was 82 %. Most of the degradation in all IV-parameters occurred between 200 and 600 hours of testing after which the values nearly stabilized until the end of the testing. Both CdTe modules included in the first series of damp heat testing degraded the same way and thus the average describes their degradation patterns well.
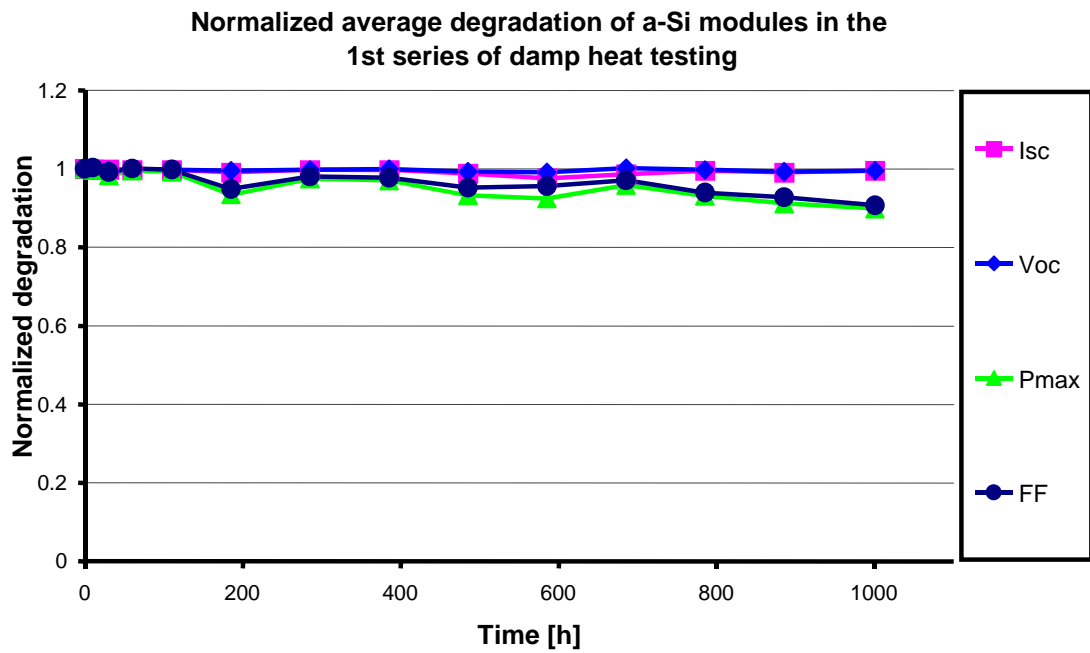
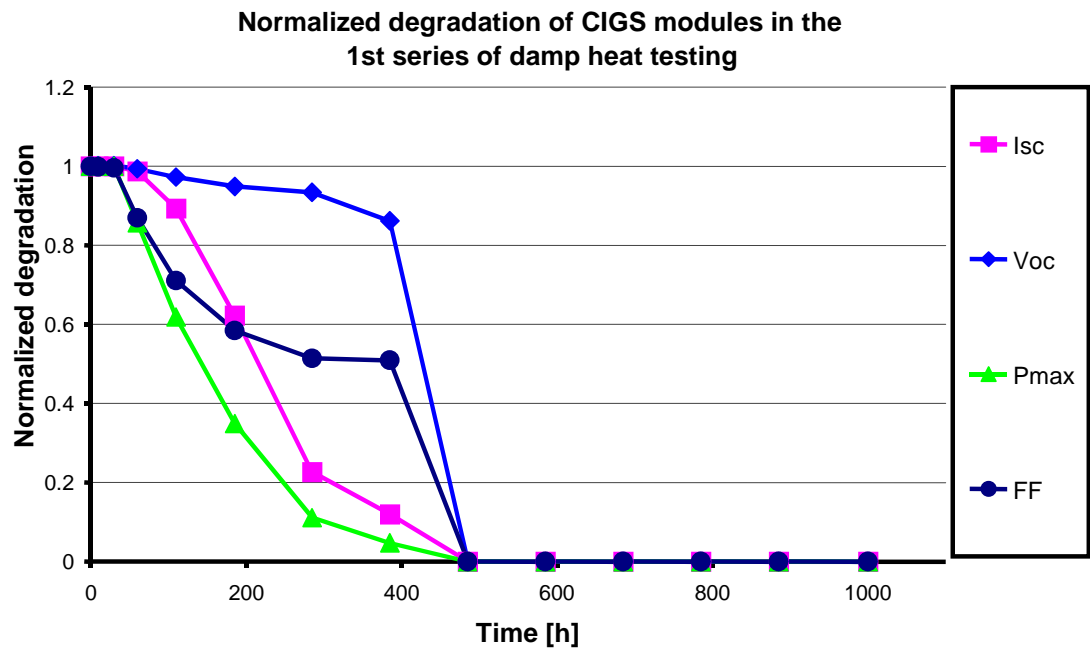**Figure 4.18** *Normalized average degradation of 1 x 1 ft² a-Si modules in the first series of damp heat testing.*

Figure 4.19 *Normalized degradation of the CIGS prototype mini-module in the first series of damp heat testing.*

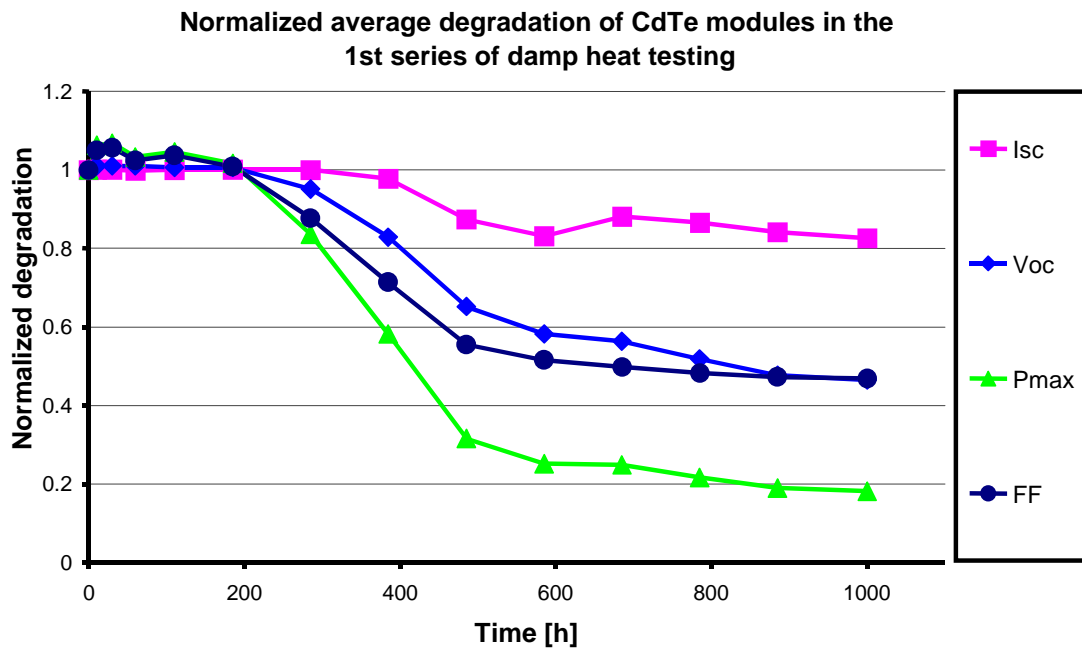**Normalized average degradation of CdTe modules in the 1st series of damp heat testing**

Figure 4.20 *Normalized average degradation of the CdTe modules in the first series of damp heat testing.*

The average normalized degradation of 1 x 3 ft^2 a-Si modules in the second set of damp heat testing is illustrated in Figure 4.21 below. The modules did not degrade in electrical performance in any of the IV-parameters. Both of the modules behaved the same way in the test so that the average describes their behavior well.

The normalized average degradation of CIGS prototype mini-modules in the second set of damp heat testing is presented in Figure 4.22 below. The modules experienced only minor degradation especially in maximum power and fill factor until 500 hours of testing. After 500 test hours the short circuit current, maximum power and fill factor started to decrease rapidly. In the end of the test the I_{sc} had degraded 51 %, V_{oc} 12 %, P_{max} 81 % and fill factor 56 %. In general the V_{oc} had a stable degradation of 4 % throughout the entire testing period and degraded to its final degradation value only between 900 and 1000 hours of damp heat exposure. Both modules degraded the same way and thus the average describes the CIGS module behavior well.

The normalized average degradation of CdTe prototype modules in the second set of damp heat testing is shown in Figure 4.23 below. The modules degraded on average in I_{sc} 9 %, in V_{oc} 29 %, in P_{max} 58 % and in fill factor 36 %. In the open circuit voltage, maximum power and fill factor the degradation started to rapidly increase after 300 hours of damp heat exposure. In the short circuit current no degradation was observed until after 700 testing hours. However the two modules behaved somewhat differently during the damp heat test. Thus the electrical performance is plotted separately for the two modules ZB510 and ZB511 in Figure 4.24 below. The CdTe module ZB510 degraded in

I_{sc} 13 %, in V_{oc} 37 %, in P_{max} 70 % and in fill factor 45 %. The CdTe module ZB511 degraded in I_{sc} 5 %, in V_{oc} 20 %, in P_{max} 45 % and in fill factor 28 %. Thus the other module ZB511 performed slightly better than the module ZB510 but the general degradation trends were the same for both modules and the average describes them well.

The normalized average degradation of 1 x 1 ft^2 a-Si modules in the second set of damp heat testing are shown in Figure 4.25 below. These modules were exposed already in the first set of damp heat testing for 1000 hours of damp heat and thus after the second set of testing had been through 2000 hours of damp heat exposure. The starting point in Figure 4.25 is the electrical performance after 1000 hours of damp heat. By the end of 2000 hours of damp heat exposure the modules had degraded on average in I_{sc} 11 %, in V_{oc} 4 %, in P_{max} 45 % and in fill factor 35 %. The short circuit current and open circuit voltage were very stable throughout the entire second damp heat exposure. In maximum power and fill factor a constant degradation towards the 200 test hours was observed. Both modules degraded with the same degradation pattern between 1000 and 2000 hours of damp heat exposure.
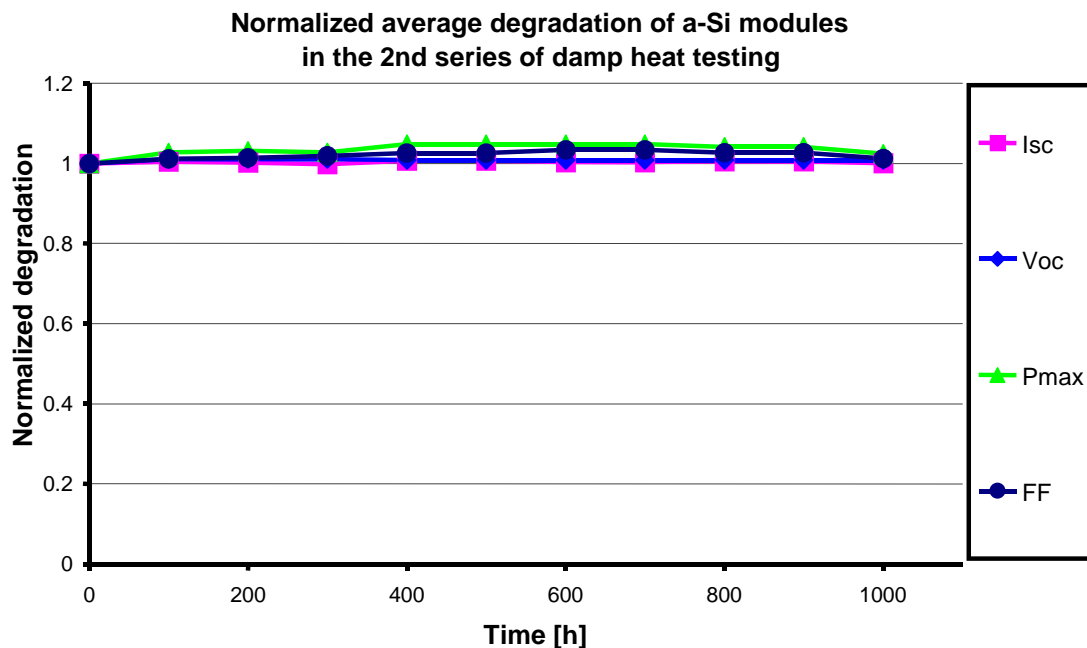
Figure 4.21 *Normalized average degradation of 1 x 3 ft^2 a-Si modules in the second set of damp heat testing.*
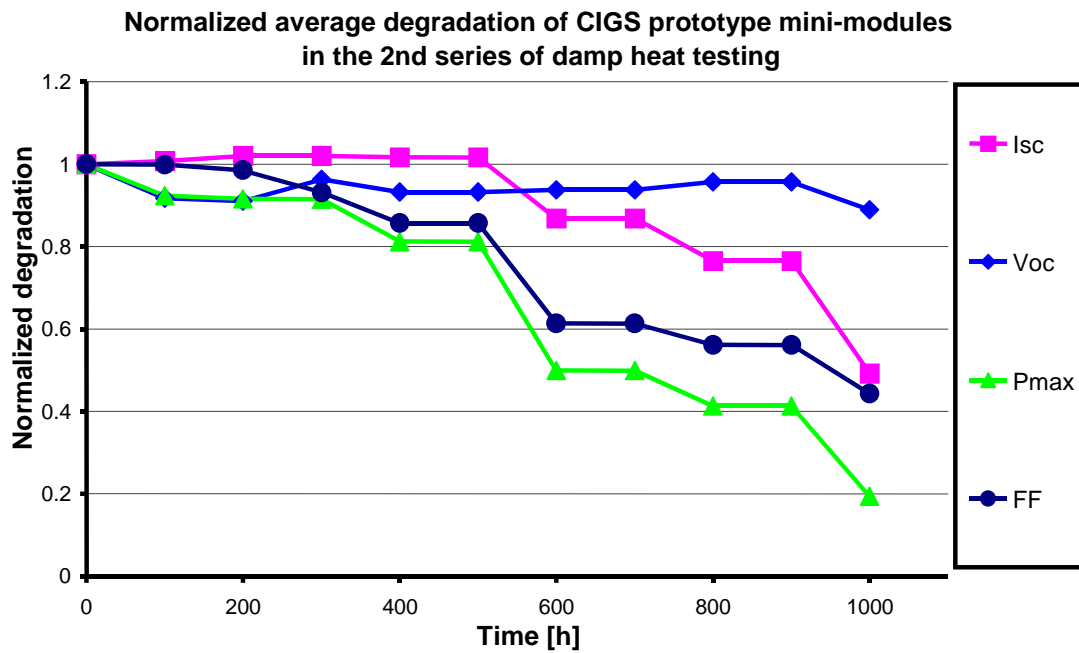
Figure 4.22 *Normalized average degradation of CIGS prototype mini-modules in the second set of damp heat testing.*
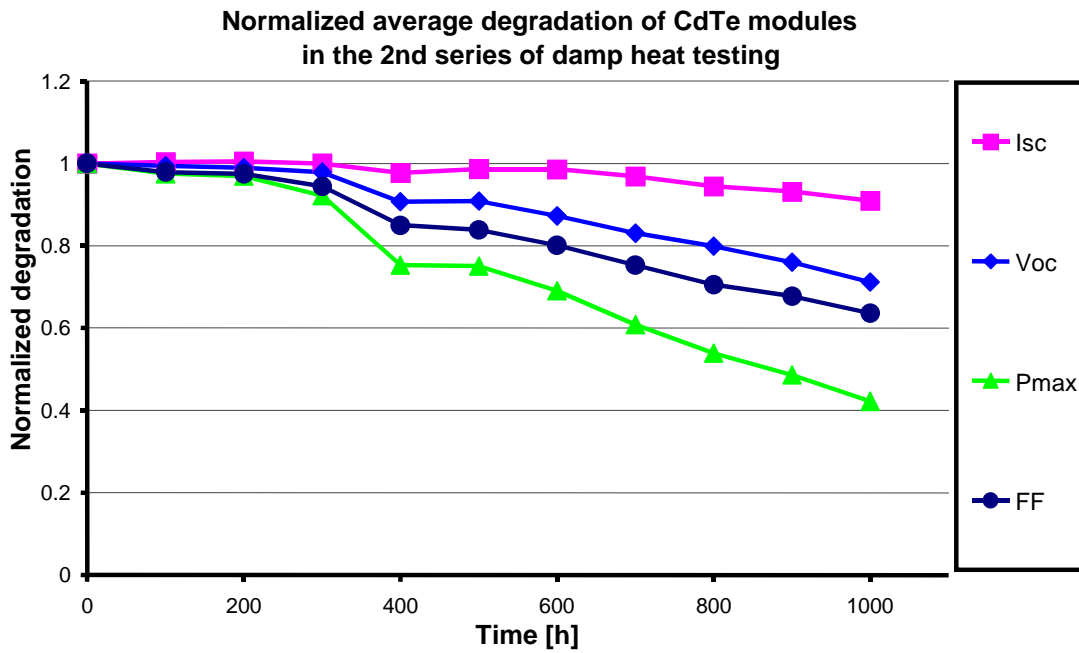
Figure 4.23 *Normalized average degradation of CdTe prototype modules in the second set of damp heat testing.*
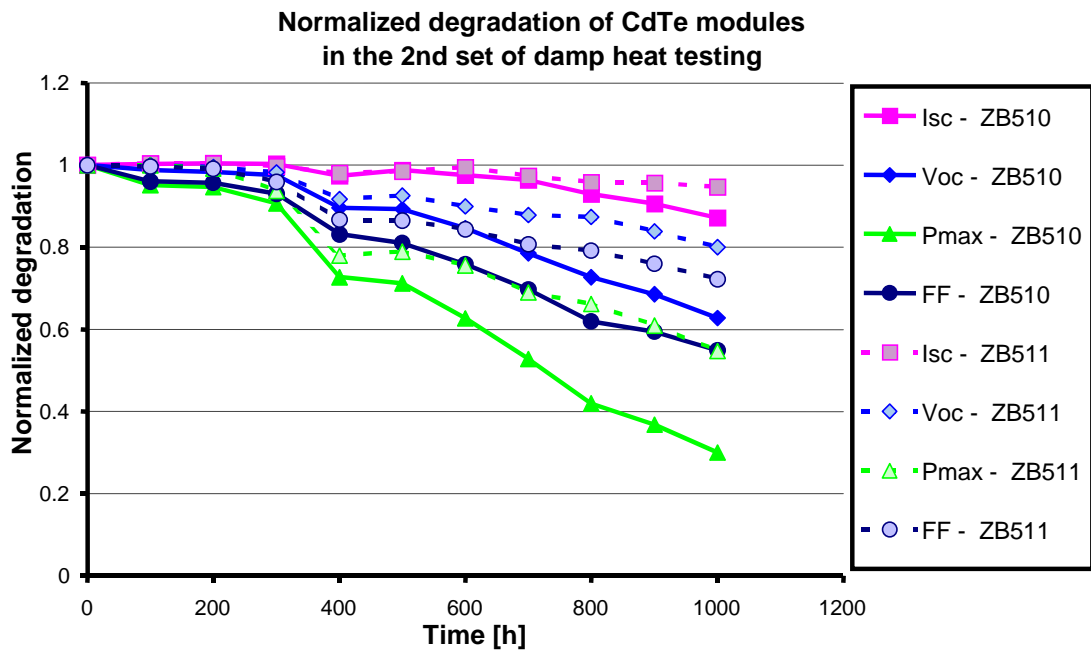
Figure 4.24 *Normalized degradation of CdTe prototype modules in the 2nd set of damp heat test. The IV-parameters are plotted separately for each of the two modules, ZB510 and ZB511, included in the testing sequence.*
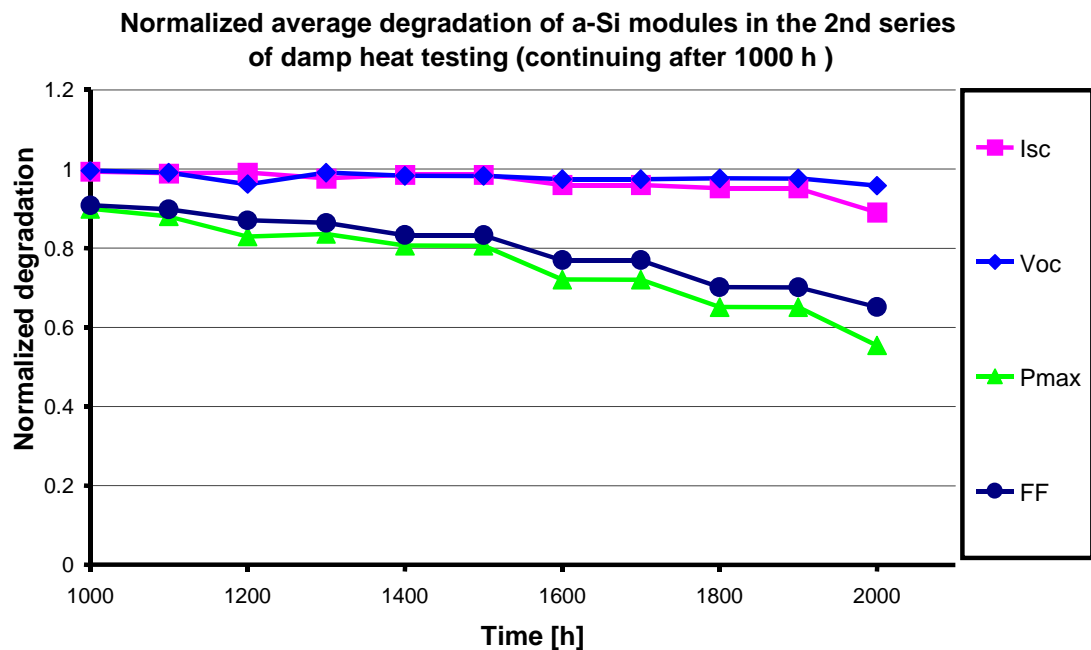

Figure 4.25 *Normalized average degradation of 1x1 ft² a-Si modules in the 2nd set of damp heat test that continued from the 1stt set of testing and had thus been exposed to 2000 h of damp heat.*

4.4   Dry heat test

4.4.1   Test sequence and sample description

The dry heat test was executed for one CdTe prototype module. The test was performed in a dark heating oven with normal air atmosphere. The module was kept in the oven at +85 °C totally for 1000 hours. During the test the module was electrically measured and visually inspected before and after the test and after every 100 test hours. Before each measurement during the testing the oven was switched off and the module was left to cool in the oven for several hours. The performance measurements were made with SpectroLab LAPSS large area pulsed solar simulator and crystalline silicon reference device was used as reference.

The module tested, ZB507, was a 30 x 30 cm^2 glass-glass CdTe prototype module. It was laminated with EVA and framed with aluminum frame.

4.4.2   Results

Visual inspection

A few visual defects were detected in the CdTe prototype module during the dry heat testing. Some bubbles and delamination around the piece of tedlar in the back of the module appeared (Figure 4.26(b)). This piece of tedlar is located in the center of the back contact and is underneath the junction box. The color of the front film changed from dark green towards yellow. On the back side some whitening or oxidation appeared on the busbars (Figure 4.26(a)) even though no extra humidity was present in the oven atmosphere. Also some slight back contact peeling was visible nearby these oxidation spots. Some silicon came out from the frame after 200 hours of testing and the junction box deformed with holes looking like craters after 700 hours of testing. Photographs of some of the visual defects can be seen in Figure 4.26 below.
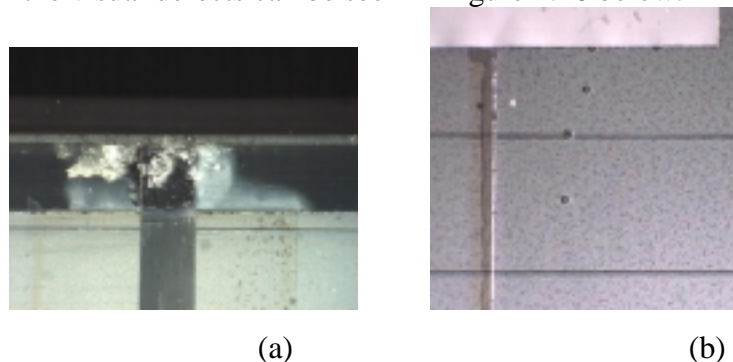

(a)   (b)

Figure 4.26 *Visual defects observed in CdTe prototype module during dry heat exposure. (a) Oxidation of busbars after 200 hours of testing. (b) Bubbles and delamination around the piece of tedlar in the back of the module.*

Electrical performance

The normalized degradation in the electrical performance of the CdTe module during the dry heat test is shown in Figure 4.27 below. During the first 100 hours the maximum power increased by 10 % and the fill factor by 7 %. However by 200 testing hours both P_{max} and fill factor started to degrade. After 1000 hours of dry heat the P_{max} had degraded 11 % and the fill factor 9 %. In short circuit current a small increase of 3 % was observed. In open circuit voltage a small decrease of 5 % was seen.

Normalized degradation of CdTe module during dry heat exposure
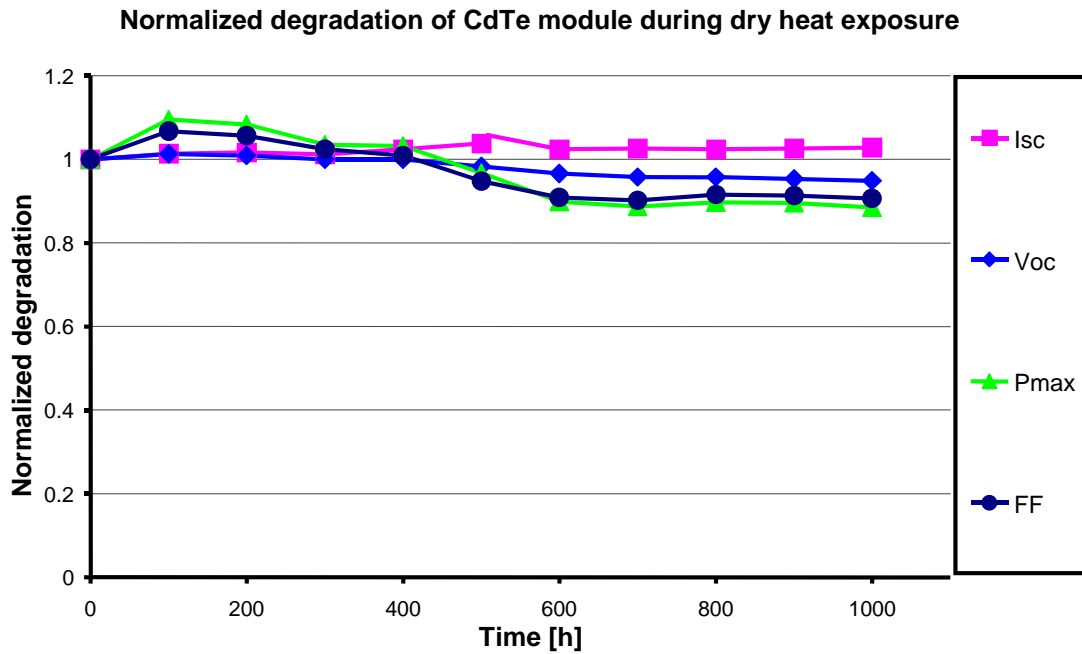
Figure 4.27 *Normalized degradation of CdTe prototype module during dry heat exposure.*

4.5   Discussion of cyclic lifetime tests, and damp and dry heat tests

a-Si

Two sets of a-Si modules with different sizes were included in the thermal cycling and humidity freeze test cycles. After the tests no major visual defects were observed in the modules. Also no particular degradation in the electrical performance was observed in the modules after either thermal cycling or humidity freeze tests.

A-Si modules of two different sizes were included in the damp heat tests. Two modules were altogether tested for 2000 hours in damp heat. After 1000 hours of testing the major visual defects observed were some corrosion of back contact and front film as well as some delamination, all around the edges of the modules. In the modules that continued through 2000 hours of testing, the same visual defects that were observed after 1000 hours of testing continued to grow. Also in these modules the plastic material in the electrical wires cracked. The smaller sized a-Si modules degraded after 1000 hours of damp heat exposure around 10 % in maximum power and in fill factor. When these modules had been through 2000 hours in damp heat the degradation in maximum power and fill factor had significantly grown to reach 45 % and 35 % respectively. In short circuit current the degradation was 11 % and in open circuit voltage no significant degradation was observed after 2000 hours of testing. In the larger sized a-Si modules no significant degradation in electrical performance was observed after 1000 hours of damp heat testing.

In literature not many results are reported on the accelerated lifetime testing of a-Si modules. Most concern has been given to the instability of a-Si material under light, which is discussed in detail in section 4.6. Some groups have reported on outdoor testing of a-Si modules [55], [54], [148], [149], but all degradation in electrical performance reported has been due to light induced degradation. In [148] the authors mention that in in-situ testing of advanced thin film PV systems no module failures have been reported although some changes in visual appearance of a-Si have been observed [148]. Some groups even consider accelerated testing or aging of a-Si modules to be a synonym of testing light induced defects for which they suggest new fast stability testing methods [150].

In this study in the first set of damp heat testing the a-Si modules exposed to damp heat developed many visual defects but the electrical performance was not much affected. The fill factor and maximum power degradation suggests that the module series resistance has increased, which can also be identified by comparing the IV-curves of the modules before and after the damp heat test. The change in the IV-curve shape can be seen in Figure 4.28 below showing the IV-curves of one of the two modules tested before and after the exposure.
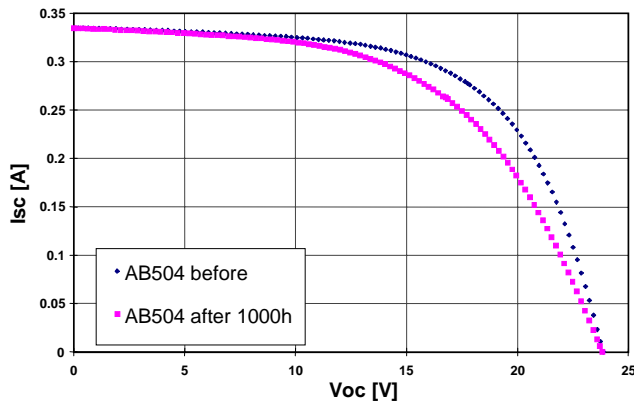
Figure 4.28 *IV-curves of module AB504 before and after damp heat test.*

When these modules continued through another 1000 hours of damp heat testing, the same trend continued but the modules still gave half of their initial maximum power. However the visual appearance of the modules after 2000 hours of damp heat would have suggested a much more drastic degradation in electrical performance than it actually was. The larger sized modules had some visual defects after 1000 hours of damp heat testing but no change in the electrical performance.

It is thus suggested that slight corrosion of thin films in a-Si modules, seen in the visual appearance of the modules, does not affect the electrical performance of the modules. Only when corrosion is advanced to a point where for example no back contact aluminum is left, the lack of active film cause degradation in electrical performance and especially in short circuit current accordingly. This was the case for module corner areas after 2000 hours of damp heat exposure. The correlation between the short circuit current degradation and lack of back contact aluminum was confirmed in the laser scanning measurements discussed in Chapter 5. The degradation in maximum power and fill factor noticed in the smaller sized modules was probably due to the degradation of contact wire material causing humidity penetration to the copper leads of the wires and thus increasing the series resistance of the modules.

It is also suggested that the main cause for the degradation is humidity penetration to the photovoltaic module encapsulation during the long humidity exposure in the test. In thermal cycling and humidity freeze tests no degradation was noticed since either there was no other than atmospheric humidity present or the modules were under humidity exposure only for a comparably short time. These tests could have caused breakage of glass plates if for example the polyurethan frame material would have been too hard or too soft. In these cases the frame material would not have conformed to the temperature expansion of the glass plates or would not have given the support needed especially in the case of large sized modules. Thus the effort needed had been given to the design of proper encapsulation of these a-Si modules and their service lifetime has

increased accordingly.

CdTe

Two CdTe prototype modules were tested in thermal cycling and humidity freeze tests. One major visual defect observed in both of the modules was melting and deformation of junction box. In one of the modules the some color change in the back contact color was observed after humidity freeze test. In that module also some delamination was present after humidity freeze test. In the electrical performance some degradation was observed after both test cycles. The other module degraded little less than 10 % in maximum power and in fill factor after thermal cycling. In this module the degradation was little more than 10 % in these parameters after humidity freeze test. The other module did not significantly degrade in any of the electrical performance parameters measured after thermal cycling. However, significant degradation of around 30 % was observed in this module in maximum power and fill factor after humidity freeze test. In this module change in back contact color was observed visually after humidity freeze test.

In the first set of CdTe modules tested in 1000 hours of damp heat the major visual defects observed were deformation of junction boxes and back contact color change radially around the corner areas (Figure 4.12). In the second set of CdTe modules included in the damp heat test for 1000 hours (Figure 4.16), also deformation of junction boxes was observed. The back contact color changed but for these modules in a peeling like pattern. In the front some delamination patterns were detected and in the other module the front glass was broken. These modules differed from the first set of CdTe modules in that the humidity tightness had been enhanced using resin between the back contact and the EVA. In electrical performance the first set of CdTe modules degraded after 1000 hours of damp heat exposure around 20 % in short circuit current, around 50 % in open circuit voltage and fill factor and around 80 % in maximum power. The electrical performance of the second set of CdTe modules after 1000 hours of damp heat exposure degraded somewhat less than the first set of modules but the degradation trend was the same for both sets. Again the maximum power degraded most, on average around 60 %.   The open circuit voltage and fill factor degraded on average around 30 % and the short circuit current on average around 10 %. In this second set of modules, the other module degraded somewhat less than the other module, but the degradation patterns were similar for both modules.

One CdTe module was exposed to 1000 hours of dry heat test. The major visual defects observed after this test were some delamination and slight oxidation or corrosion patterns on the busbars, even though only atmospheric humidity was present in the oven. In the electrical performance of the CdTe module an increase of about 10 % was first observed in maximum power and fill factor but by the end of the test these parameters had degraded by about 10 %. No major changes were observed in short circuit current or open circuit voltage.

In literature many groups report that the back contact is causing most of the

stability problems detected in CdTe devices [151], [152], [153], [154], [155], [156], [26], [99], [7], [107]. Most widely used back contacts in laboratory scale devices are gold and copper compounds, mainly Cu/Au, Cu/graphite, Cu doped ZnTe with Au or Ni metallization, Cu/Mo or just Au [151], [90], [92]. The stability problems occur when devices are stressed in increased temperature and/or reverse biased conditions [153], [156]. In [156] the authors have noticed that the stress effects are generally larger at open circuit [156].

Back contact problems primarily increase series resistance, and hence decrease fill-factor [155]. In [153] the authors report that some CdTe devices subjected to stress testing or life time testing displayed high series resistance and/or evidence of a reverse diode – both characteristics which could be attributed to the back contact. In CdTe devices that have been subjected to stresses beyond normal operating conditions there appears to be changes that are associated with stress temperature and electrical bias. The degradation in short circuit current, open circuit voltage and fill factor, and subsequently the increase in series resistance, is larger for devices held at reverse bias than for those held in forward bias. Keeping samples under open circuit conditions during testing creates a strong electrical field that may enhance the electromigration of impurities. All the changes noted were either accelerated or increased in magnitude when the temperature was increased [153], [107], [151].

Presence of Cu in the back contact appears to be an important factor in determining stability in CdTe solar cells [156], [151]. Cu-based contacts give high efficiency but Cu diffuses along the grain boundaries and across the junction [151]. In [26] the authors report to have abandoned development of an electrode based on tellurium, as a result of stability problem. The primary mode of degradation in such cells was a loss of open circuit voltage. The rate of degradation was strongly dependent on temperature. Similar results were obtained using gold or nickel electrodes. A graphite electrode indicates good stability when adequately encapsulated. The principle mode of degradation which an unencapsulated cell using this improved electrode can exhibit is an increase in series resistance due to an overexposure to humidity [26]. Most recently some groups have used Sb_2Te_3 successfully as their back contact material [157], [151], [152].

Apart from temperature and bias conditions causing instability in CdTe devices, CdTe/CdS modules are known to be sensitive to moisture induced degradation [99], [106]. Thus the reliability of CdTe photovoltaic modules depends markedly on the structure of the module, especially on the humidity tightness of the encapsulation [158], [7]. This was also concluded in [143] in which cheaper encapsulation schemed than glass/EVA/glass were investigated. However, the CdTe modules did not last in damp heat when various conformal polymer coatings and organic varnishes were used, materials that are frequently used in automotive and electronics industries [143].

However, in [106] the authors report that after designing a humidity tight encapsulation the module still degraded significantly in hot and humid conditions. They

concluded that the degradation was due to decrease in oxygen concentration inside the encapsulation space. When oxygen in a sealed module decreased down to 2 vol.%, photovoltaic properties of the module degraded, but they recovered nearly completely at room temperature after five days when sealing of the module was broken and sufficient oxygen (air) was supplied. This recovery phenomenon may be the same as increase in p-type characteristics in high resistivity CdTe by heat treatment in air in other fabrication processes [106], [158].

In this study the CdTe modules degraded significantly in electrical performance in humidity freeze and damp heat tests, in other words in all the tests in which humidity was present. After these tests the major visual defect observed was the back contact color change. After humidity freeze test the degradation in the CdTe modules resembled the degradation after damp heat testing with the only difference that both the degradation in electrical performance and the back contact color change were less in quantity after humidity freeze test. This is probably due to that in humidity freeze test the modules were exposed to humidity for a shorter time than in the damp heat test. Thus it can be suggested that the major cause for degradation in electrical performance is instability in back contact due to humidity penetration.

When the modules were laser scanned after damp heat test, the results of which are reported in detail in Chapter 5, no short circuit current could be detected on areas where the back contact color change was visible. Additionally Auger electron spectroscopy measurements made on the back contact material composition after damp heat test detected changes in the back contact material composition on the areas were the color had changed. When comparing the percentage of decrease in short circuit current in the modules and the relative area of visual back contact color change, the values correlate well. Also no degradation in short circuit current was observed in the dry heat test. Thus it can be concluded that the short circuit current degradation in the CdTe modules after humidity freeze and damp heat tests can be attributed to the humidity penetration into the encapsulation causing instability or total loss electrical activity in some areas of the back contact.

In the second set of damp heat testing the degradation in electrical performance was less than in the first set of testing. This can be due to the enhanced humidity tightness of the module encapsulant with resin between the glass and the back contact. However, the glass breakage in one of the modules and the delamination patterns suggest that the resin glues the glass plate too tight to the thin films and the expansions due to increased temperature cause other kinds of problems to the module package. These stresses are also reported in [93]. The increased humidity tightness does seem to anyway decrease the degradation rate and thus increase the lifetime of the module.

When one CdTe module was tested in dry heat test, similar degradation pattern was observed than in the damp heat tests, only in a lot lesser extent and without any degradation in short circuit current present. No particular change in back contact color was detected but there was some oxidation on busbars inside the module laminate. In

this test some increase in the electrical performance was observed during the first hours of testing. This can be due to the possible additional curing of EVA lamination because of heat. The degradation in especially maximum power and fill factor and somewhat in open circuit voltage cannot be due to humidity penetration, since also the short circuit current was very stable throughout the whole testing period. One possibility is the suggestion of the authors in [106], that there would be lack of oxygen in the back contact, which causes this degradation. A theory could be that the oxygen contained in the back contact is removed because of heat and possibly causes the corrosion visible on the busbars. This would leave the back contact in deficit of oxygen, which could then be detected as degradation in the electrical performance of the CdTe module. However, further investigations on this matter are needed for proof. It is also possible that the module simply degrades due to temperature induced instability in the back contact. All the tests were executed in short circuit conditions and thus no additional stress was caused by electrical bias.

There are references that some CdTe modules have been stable in outdoor exposure for 2-3 years [106], [7]. No evidence exists that CdTe-based devices would be intrinsically unstable [7]. It can be said that CdTe photovoltaic thin film material seems to be very sensitive to humidity. Thus the only way to achieve increase in the service lifetime of CdTe modules is to design an as humidity tight encapsulation as possible.

CIGS

Two CIGS prototype, unframed mini-modules were included in the thermal cycling and humidity freeze tests. After thermal cycling test no major visual defects were observed in these modules. The only major visual defect that was observed in both of the modules after humidity freeze test was that the EVA turned white or foggy starting from the edges of the modules. No changes were observed in the electrical performance of either of the samples after thermal cycling test. After humidity freeze test both samples degraded around 10 % in maximum power and in fill factor.

There was one CIGS prototype mini-module included in the first set of damp heat testing and two in the second set. The modules in the second set came from a different batch and were better protected from humidity as the module in the first set. The major visual defect observed after the first set of damp heat exposure was that the cell separation lines became transparent starting from the edges of the module. Also in the CIGS samples included in the second set of damp heat testing cell lines turning transparent was observed. In these samples the EVA turned white or foggy around the edges of the module. The samples included in the second set of damp heat test came from the same batch as modules that were tested in thermal cycling and humidity freeze tests. The electrical performance of the CIGS sample in the first set of damp heat testing degraded to zero by the end of the test. Most degradation was observed in short circuit current and maximum power. In the second set of damp heat testing the samples degraded on average about 50 % in short circuit current and fill factor, about 10 % in open circuit voltage and about 80 % in maximum power.

In literature some reports on testing of CIGS against degradation can be found. In most of these reports the lifetime testing has be effectuated to bare, unencapsulated CIGS solar cells [29], [159], [30] and thus suggestions of phenomena causing possible CIGS material instability and environmental degradation are available. In [160] also CIGS modules have been exposed to damp heat testing. Long-term stability is a fundamental requirement in order for polycrystalline CIGS thin film solar cells to be a future industrial success. In CIGS solar cells humidity increased device degradation is believed to originate from ZnO window layer degradation [29], [30], [161], [10] and from Mo back contact corrosion [29], [10], or from corrosion of cell interconnect area connecting the front contact ZnO and back contact Mo [160]. Also oxidation and especially oxidation together with Na passivation has been investigated by several groups [159], [162], [163].

When testing bare CIGS solar cells in damp heat conditions, the authors in [29] and [160] as well as in [30] and [161] observed that the short circuit current remained essentially unchanged while the open circuit voltage and fill factor decreased in parallel. A likely explanation for the degradation in fill factor and increase in series resistance is the degeneration of the ZnO/CdS window layer after extended humidity exposure [29], [30], [161]. However, increasing series resistance of the ZnO window should normally not affect the open circuit voltage of the device. The correlation between the defect density and the open circuit voltage leads to the conclusion that changes in the bulk or at the grain boundaries are responsible for losses in the open circuit voltage. Such an effect is conceivably caused by in-diffusion of water and/or oxygen [29], [30].

In [164] it is concluded that long-term oxidation at room temperature in the presence of humidity takes place in the bulk of the semiconducting film, preferably at the grain boundaries. Visual oxidation of the Mo back contact in the humidity exposed cell isolation scribes is detected. After a few hundred hours in damp heat conditions, this led to decreased Mo conductivity and to a major loss in fill factor [29]. In [160] the authors have further investigated the cell interconnect corrosion and conclude that the major cause for fill factor loss would not be Mo corrosion nor degradation of ZnO but rather corrosion of the front contact ZnO and back contact Mo connection at cell interconnect area [160].

In [10] the authors state that accelerated lifetime testing of CIGS modules with EVA/glass encapsulation has shown that the module performance is susceptible to water vapor. Also in this case the main reason found was the increasing electrical resistance of the ZnO. In [10] it is claimed that Mo has a minor influence on the decrease of the performance. Only if the Mo is totally destroyed in the interconnected region the efficiency is nearly zero. From this the authors conclude that ZnO degradation in combination with the heterojunction is the major degradation effect initiated by the water vapor [10].

A large improvement in solar cell efficiency has been achieved by utilizing the positive influence of Na incorporated into the CIGS absorber on both, the film

morphology and electronic structure [159]. Empirically, Na treatments have invariably been found to increase the open circuit voltage of ZnO/CdS/CIGS solar cells. On the chemical side Na is primarily associated with grain boundaries, and the oxidation of CIGS is accelerated in the presence of sodium [163]. On the electrical side, Na was found to induce elimination of gap states acting as recombination centers, and induce an increase in the free hole density [162].

Since adequate encapsulation of the solar cell cannot completely suppress humidity influences, the contribution of Na to the solar cell performance focuses new attention on the influence of impinging or adsorbed H_2O and in particular on its interaction with Na [159], [83]. Reducing the amount of Na from the CIGS surface and from internal surfaces and grain boundaries due to humid conditions is expected to negatively influence the electronic properties of CIGS. However this is partly reversible due to self-stabilization of the Na-CIGS system [159]. Irreversible reactions play a crucial role for the long-term electrical performance of solar cell devices. The formation of a Na-O-CIGS complex is irreversible and leads to a surface oxidation, which is stable against annealing up to 550 K [159]. The Na-O correlation appears as soon as O_2 is introduced. If Na is used, its catalytic properties cause the oxygenation of the CIGS surface to be achieved in-situ [162]. The finding of irreversible reactions demonstrates the importance of adequate encapsulation of CIGS solar cell absorbers and the optimization of preparation processes with respect to dry ambient conditions [159].

The third phenomenon suggested in literature to cause instability in CIGS material is Cu migration.[165], [162], [166], [167]. Cu can diffuse across the space charge region of the CIGS absorber in a few minutes to several days at most. Such a rapidly migrating species potentially could raise serious concerns to the long-term stability of CIGS-based devices. However, it is suggested in [167] and in [166] that CIGS is a material that posses a degree of flexibility that is essential for accommodating externally imposed changes, in other words it functions according to a "soft lattice" model. Parallel to the CIGS ability to accommodate intrinsic defects, the electronic properties of the material appear less sensitive to impurities than is usually found in other semiconductors. Specifically in case of Cu migration, it is proposed in that as Cu atoms are the most weakly bound ones in the CIGS lattice, they are most likely to be liberated from their sites due to external perturbation. The resulting Cu interstitials are highly mobile, so that they can diffuse or migrate and eventually restore their equilibrium distribution. Furthermore, Cu-involving defect reactions, the product of which may be electrically neutral, accelerate the equilibrium restoration process and allow for the passivation of other defects as well. This minimizes any strong local variations in electrochemical potential of Cu-related species, thus providing a natural explanation for the self-healing capabilities of the CIGS material. Thus, the unusual stability of CIGS comes from its ability to accommodate chemically and electrically the defects created by stresses brought upon it rather than from the difficulty to actually have these stresses lead to the formation of defects.[166], [167].

In this study it is evident that the CIGS prototype minimodules are suffering from humidity based degradation after accelerated lifetime testing. In the first set of damp heat testing the prototype module encapsulation was not evolved enough to keep humidity out and thus the module lost its electrical performance before the end of test. In the second set of damp heat testing the prototype encapsulation design was more humidity tight than in the first module. However, some humidity penetration was observed also in these modules. In both sets of CIGS prototype minimodules tested in damp heat as well as after humidity freeze testing, same kind of degradation mechanisms were visible. Practically no degradation in open circuit voltage was detected in any of the samples and most degradation was seen in maximum power and fill factor. In the first set of damp heat, however, also short circuit current degraded rapidly.

The fill factor degradation can probably be addressed to the back contact Mo corrosion or corrosion of ZnO/Mo contact at cell interconnect area caused by humidity penetration. The corrosion at cell interconnect area could also be detected visually after damp heat testing. To verify whether the corrosion of the cell interconnect area is mainly caused by back contact Mo corrosion or corrosion of the front contact ZnO and back contact Mo connection require further investigations. Especially after the second set of damp heat testing and after the humidity freeze testing also some fogginess could be observed in the EVA of the samples. This could have caused at least partly the degradation in electrical performance observed in short circuit current after damp heat testing. Whether some degradation observed was caused by humidity related changes in the ZnO window layer have to be solved in further investigations.

In case of accelerated lifetime testing of CIGS prototype minimodules it can be concluded that humidity penetration causes degradation in electrical performance of the modules. However, in our case the minimodules were prototype ones and not properly protected from humidity penetration. Even then the second set of modules in the damp heat test resisted rather well the test conditions. At least in [161] the authors report their modules to have lasted 1000 hours of damp heat testing and in [148] CIGS modules are stable after being kept in outdoor conditions for more than six years. Thus, it can be concluded that after improving the humidity tightness of the CIGS encapsulation the CIGS technology based photovoltaic modules are be able to last well in various environmental conditions.

4.6 Light soaking

4.6.1 Test sequence description

The controlled light soaking was performed in a chamber equipped with xenon mercury vapor lamps. The UV part of the spectrum in the light was filtered out with plain glass sheet which cuts off the wavelengths below 330 nm. The sample temperatures were regulated using two air fans. The samples were kept at open circuit and continuously monitored for their V_{oc} and the temperature. The irradiance during the light soaking was approximately 1000 W/m^2 and the irradiance was continuously monitored with a pyranometer.

The electrical performance of the first set of samples was measured with SpectroLab Large Area Pulsed Solar Simulator (LAPSS) before the test and then after every 24 hours of testing for the first 72 hours and then after every 48 test hours until 216 test hours. After 216 test hours the samples were stored in dark for a couple of weeks and then remeasured for electrical performance. The controlled light soaking was continued and the modules were then left under light exposure for another 187 hours before measurement, then for a further 48, 72 and 48 hours. The total testing time was 571 hours for the CdTe and the CIGS samples of this set. The a-Si samples finished the test after 523 hours of light soaking.

The second set of samples was also measured with SpectroLab LAPSS before the test and then infrequently first after 24 hours of test, then after next 115, 48, 72 and 48 test hours. The total testing time for these samples was 307 hours.

4.6.2 Sample description

The samples tested are listed in Table 4.VI below. The CdTe samples in different series were by different manufacturers and they were prepared with different manufacturing technologies. The CIGS samples in both series came from the same source but the second series samples were of later, modified production.

Table 4.VI *Sample description for modules included in light soaking.*

Quantity	Type	Size	Description
1st series			
2	a-Si	1x1ft^2	Framed module
2	CdTe	30x30cm^2	Framed module
2	CIGS	10x10cm^2	No frame, prototype minimodule
2nd series			
1	CdTe	5x5cm^2	No frame, prototype minimodule
2	CIGS	10x10cm^2	No frame, prototype minimodule

4.6.3   Results

Amorphous silicon

The average degradation patterns for a-Si modules exposed to controlled light soaking are shown for short circuit current, open circuit voltage, maximum power and fill factor in Figure 4.29 below. In average by the end of the test the I_{sc} had degraded by 17 %, the V_{oc} by 4 %, the P_{max} by 35 % and the fill factor by 18 %. Most of the degradation, 25 % in P_{max}, occurred during the first 48 hour of light soaking after which the modules degraded slowly 10 % more. Towards the end of the test the module degradation approached stability.

The interruption after 216 test hours and storing in dark had practically no effect on the a-Si module degradation. The difference after light soaking of 216 hours and after being thereafter in dark is only 0.5 % increase in maximum power. Both a-Si modules tested showed the same degradation pattern.
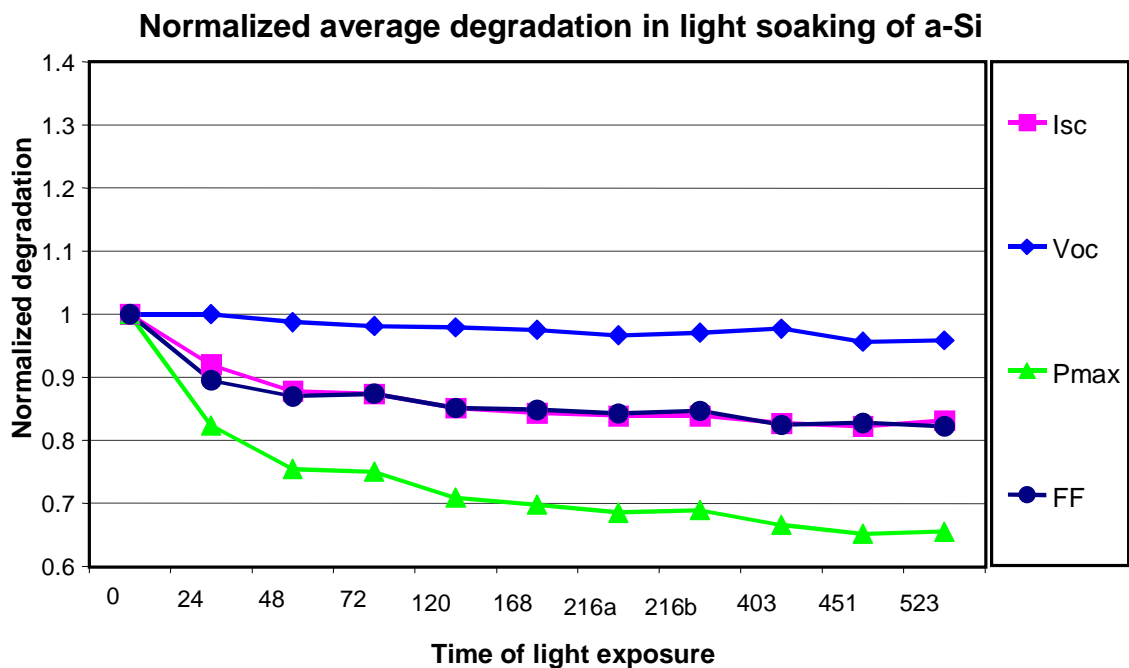
Figure 4.29   *Relative or normalized average degradation of a-Si samples in the first series of light soaking.*

CdTe

The average behavior of short circuit current, open circuit voltage, maximum power and fill factor during controlled light soaking of the first series CdTe modules is shown in Figure 4.30 below. The average changes in IV parameters for these modules at the end of test were 6 % degradation in I_{sc}, 3 % in V_{oc}, 10 % in P_{max} and 1 % in fill factor.

The two modules included in the controlled light soaking behaved very differently.

Thus the behavior in I_{sc}, P_{max} and fill factor is illustrated separately for the two modules tested ZB506 and ZB508 in Figure 4.31 below. The final decrease in P_{max} and in V_{oc} was about the same for both modules. However, in I_{sc} one module degraded 10 % and in fill factor no changes were observed. The other module degraded both in I_{sc} and fill factor 3 %. The average oscillating behavior of I_{sc} and P_{max} in Figure 4.30 for these CdTe modules is in fact due only to one of the modules, as seen in Figure 4.31, illustrating the different behavior of the samples.

The interruption in the light soaking after 216 hours affected only the module showing the oscillation pattern. This module was recovered during the time in dark almost to the original performance values. After continuing the light soaking, the module degraded quickly and stabilized there until the end of the test. The degradation pattern of damped oscillation was observed during this part of the test in I_{sc} and P_{max} for this module. The interruption did not seem to affect the other CdTe module exposed.

The degradation pattern of the CdTe sample in the second set of light soaking is shown for short circuit current, open circuit voltage, maximum power and fill factor in Figure 4.32 below. The sample degraded in I_{sc} 4 %, in V_{oc} 4 %, in P_{max} 11 % and in fill factor 5 %.
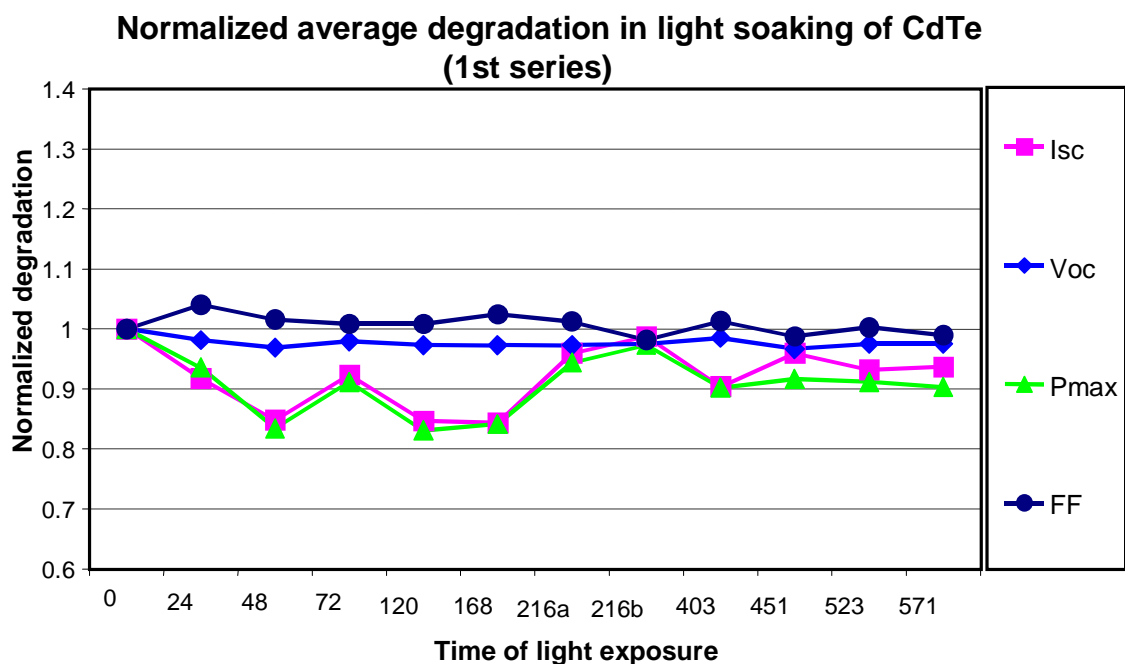
Figure 4.30 *Relative or normalized average degradation of CdTe first series of samples in light soaking.*
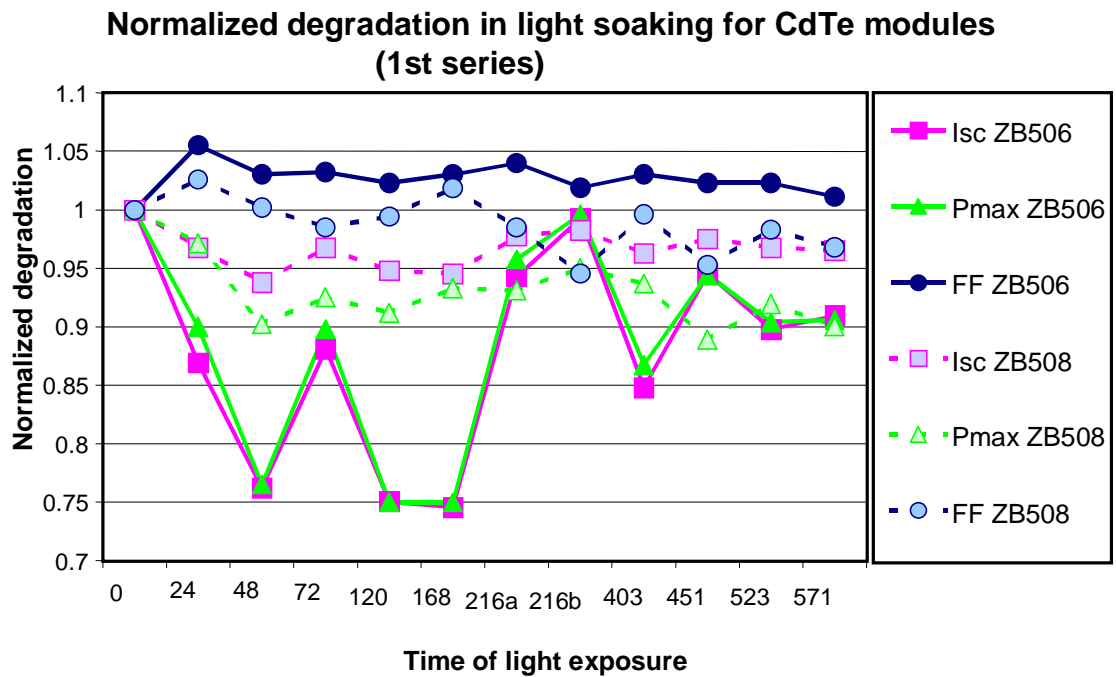
Figure 4.31 *Relative or normalized degradation of first series CdTe samples in light soaking. Degradation in I_{sc}, P_{max} and fill factor are shown separately for the two samples ZB506 and ZB508.*
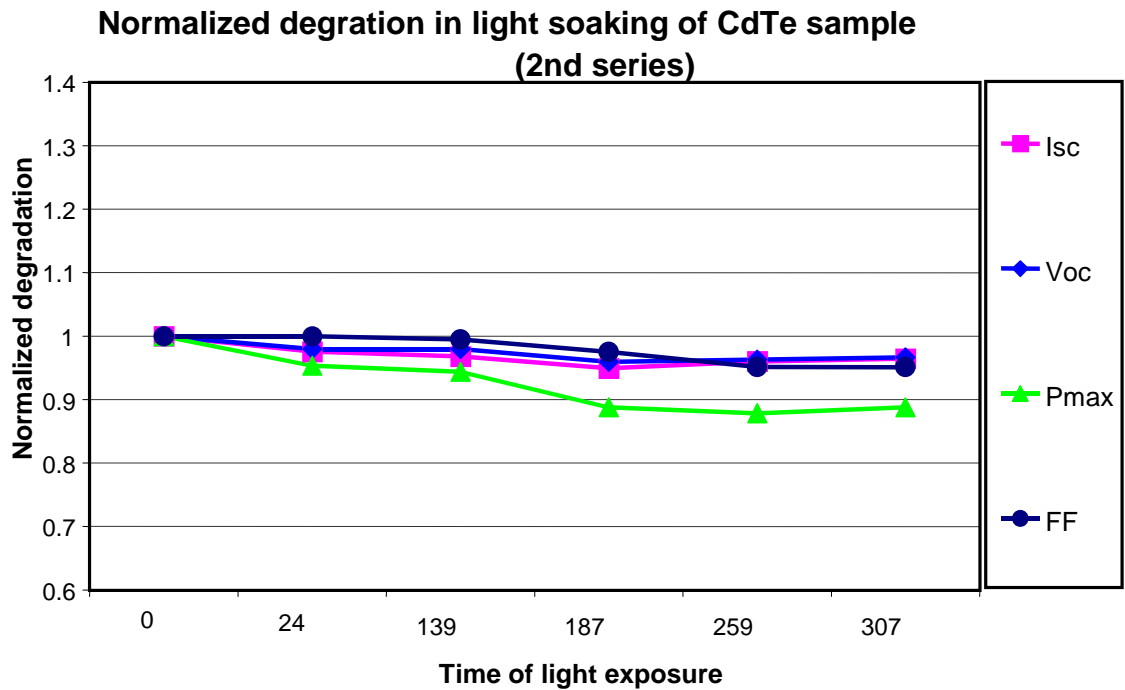
Figure 4.32 *Relative or normalized degradation for the one CdTe sample in the second series of light soaking.*

CIGS

The average behavior for CIGS samples in the first set of testing in short circuit current, open circuit voltage, maximum power and fill factor are shown in Figure 4.33 below. On average the CIGS samples degraded in I_{sc} 1 % and increased in V_{oc} 3 %, in P_{max} 25 % and in fill factor 23 %.

The behavior of the two modules exposed to controlled light soaking was the same. As a general pattern the maximum power and fill factor increased mainly during the first 24 hours of testing after which only slight changes were observed. During the interruption in the testing after 216 hour of light exposure, the fill factor and P_{max} dropped sharply from an increase of 23 % and 25 % to 12 % when compared with the original values. No significant changes in I_{sc} or in V_{oc} where observed over the whole testing period.

The average degradation for the CIGS samples of the second set of light soaking is shown for short circuit current, open circuit voltage, maximum power and fill factor in Figure 4.34 below. On average the CIGS samples degraded in I_{sc} 3 %, in V_{oc} 1%, in P_{max} 1 % and increased in fill factor 3 %.

The two samples behaved very differently from one another during the second set of testing. Thus the behavior in P_{max} and fill factor is illustrated separately for the two samples CB515 and CB516 in Figure 4.35 below. The first sample had increased by 11 % in P_{max} and fill factor after 139 testing hours but then dropped sharply after 187 testing hours. The sample then increased again by 8% in P_{max} and 11 % in fill factor after 259 hours of testing but for the final measurement dropped to an overall increase of 4 % in P_{max} and 7 % in fill factor with respect to the initial values.

In the other sample P_{max} decreased after 187 testing hours 6 % having been stable around the initial value for the beginning of the test. In this sample the fill factor increased first by 2 % but dropped after 187 test hours to a degradation of 2 % and oscillated around that degradation value throughout the rest of the testing time. The I_{sc} and V_{oc} values of both CIGS samples had the same degradation patterns.
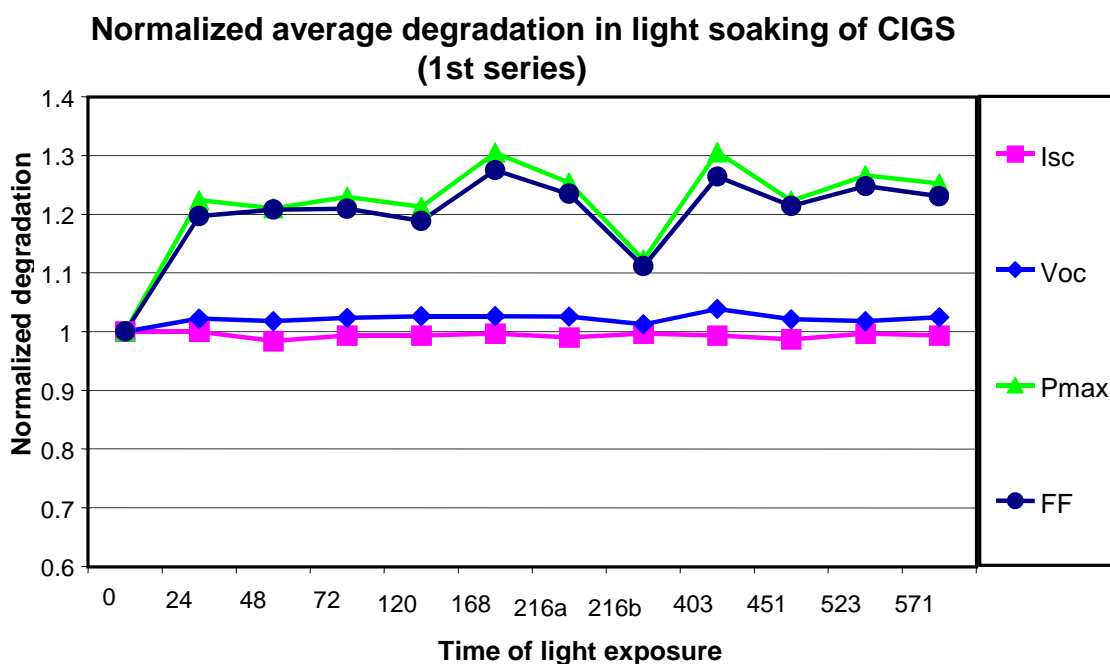
Figure 4.33 *Relative or normalized average degradation of CIGS samples in the first series of light soaking.*
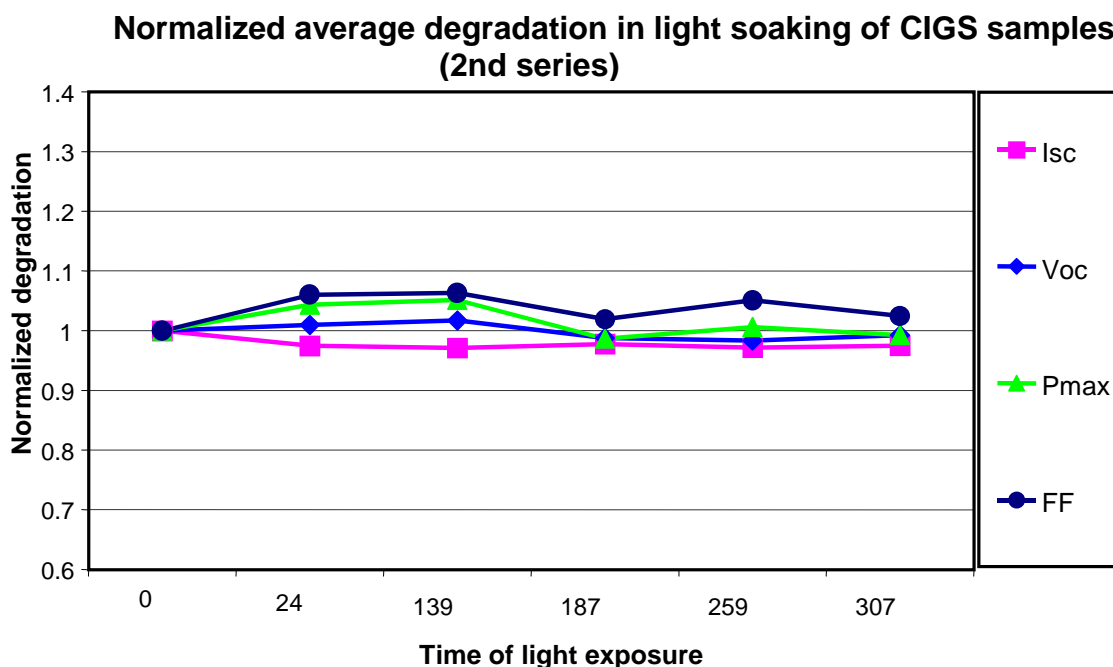

Figure 4.34 *Relative or normalized average degradation of CIGS samples in the second series of light soaking.*
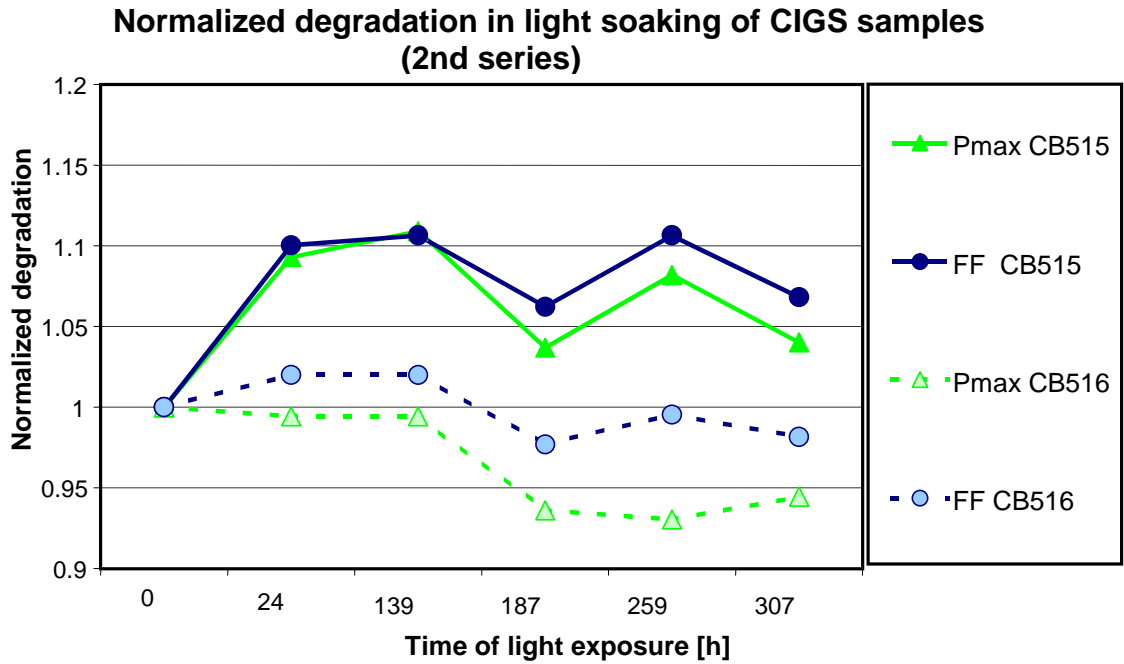
Normalized degradation in light soaking of CIGS samples (2nd series)

Figure 4.35 *Relative or normalized degradation of the second series CIGS samples in light soaking. Degradation in P_{max} and fill factor are shown separately for the two samples CB515 and CB516.*

4.6.4 Discussion on light soaking

Amorphous silicon

The behavior of amorphous silicon thin film solar cell material under light is used as basis for the IEC thin film qualification testing standard 61646 [140] which recommends light soaking to be used as preconditioning of the modules before the actual qualification testing. The amorphous silicon solar cell degradation behavior under light soaking or the so-called Staebler-Wronski effect was first described in 1977 [50]. There are several recent references describing this behavior when both single junction and multi-junction amorphous silicon solar cells and modules have been tested in controlled indoor and uncontrolled outdoor light soaking conditions (e.g.[56], [48], [57], [55], [54], [53]). A possible cause for the degradation behavior of a-Si under light was first suggested already in [50] and is discussed in more detail in [168], i.e. the compensation of dangling bonds by hydrogen atoms is playing an important role in the photoinduced metastability of a-Si material.

In our controlled light soaking study light induced degradation was observed mainly in short circuit current and maximum power and somewhat in fill factor. These results agree well with the experiences described in the various references listed above. Also as expected, the degradation stabilized towards the end of the test time. Thus the known light soaking behavior for amorphous silicon photovoltaic material was

confirmed.

CdTe

The CdTe samples did show some degradation especially in the maximum power when exposed to light soaking. However all the three samples tested in two series behaved very differently. One sample in the first series showed a strange oscillation pattern in maximum power and in short circuit current that however dampened towards the end of the test time. The interruption of the test and keeping the module in dark for some time affected this module such that the in light degraded parameters recovered nearly to their original values. The other CdTe sample in this series had a relatively stable behavior of slight degradation throughout the entire testing period. The degraded parameter values recovered slightly during the interruption but in this module the changes were minor. The CdTe sample of the second series of testing showed in the end of the testing quite similar degradation values than the modules in the first series of testing. However, the degradation for this sample was smooth without any oscillation behavior. The most common feature for all the CdTe samples was the about 10 % degradation in maximum power. However, it is difficult to give any general behavior pattern for CdTe photovoltaic material under controlled light soaking based on the results of our study.

There are only few references previously describing the light soaking effects of CdTe photovoltaic modules [169], [154]. In [169] as a final result of 1500 hours of light soaking of CdTe modules no degradation was observed. However the figures in [169] show slight changes in IV parameters during the testing. In [154] it is argued that the stability behavior of CdTe devices subjected to light soaking depends on the bias state. In their study the devices tested under resistive load were quite stable relative to devices tested at open circuit. They also suggest that increased temperature during light soaking does lead to increased rate of degradation. According to these findings the test method we used, as described in the qualification testing standard, that the samples are kept in open circuit under light soaking preconditioning step, maybe has enhanced the instability of the samples in our test. The temperature was around 50 °C all the time for all the samples so that should not have affected the degradation patterns. In future work further investigation of the effect of controlled light soaking with a resistive load would be useful.

CIGS

In the controlled light soaking study for the first series of CIGS samples there was no degradation observed but on the contrary large increases in maximum power and fill factor were noticed. The open circuit voltage and short circuit current were very stable throughout the entire testing period. The two CIGS samples in the first series behaved identically. For the second series of CIGS samples, which were delivered from the same source as the first series of samples but were of modified production, the changes in the light soaking were totally different compared with the first series. Also the two samples

within the second series behaved differently from one another. In both of them the open circuit voltage and short circuit current were quite stable throughout the entire testing period. In one sample of this second series of testing the fill factor was also stable but the maximum power decreased slightly. For the other sample increases in maximum power and fill factor were observed but not to such an extent as in the first series. The decrease after 187 testing hours might be due to measurement done not straight after cooling of the samples but after a somewhat longer waiting period.

For CIGS material photovoltaic modules there are several references describing the material light induced behavior and its possible causes, e.g. [170], [171], [165]. These references all observe increase in open circuit voltage and fill factor due to light exposure and the effect relaxes when kept in dark again. The same effect was observed when keeping the cells in dark with forward bias applied. In [165] it was claimed however that only the forward bias voltage is increasing the V_{oc}, illumination in short circuit did not have effect on the open circuit voltage. The opposite is claimed in [171] and [170].

The results of our light soaking study correlate well with the findings in literature when considering the increase in fill factor and relaxation of the effect when kept in dark again. The effect of increase in open circuit voltage (mentioned in the above references) was not however observed in this study. In [170] it is stated that the poorer quality devices show largest increases in V_{oc} and fill factor when illuminated. This is also consistent to our study since the second series samples, which showed fewer changes in fill factor and maximum power under illumination than the first series of samples, were of later and improved production.

For single junction amorphous silicon solar cell material the results of this controlled light soaking study confirmed what has previously been stated in the literature. That is, the a-Si photovoltaic modules degraded in light soaking mostly in short circuit current and in maximum power and somewhat in fill factor. Also as expected the degradation stabilized towards the end of the light exposure. In the CdTe a decrease in maximum power independent of the sample or manufacturer was observed. For other parameters no clear behavior pattern could be observed during the light exposure. The dependence of bias state during the exposure to CdTe module behavior should further be investigated. All the CIGS samples except one showed increase in maximum power and fill factor. However, the result differs between the first and second series samples tested, supporting the claim that the observed behavior may be material quality dependent.

As a general conclusion, even though no clear general trend for CdTe and CIGS material behavior under light exposure was observed, the behavior differed significantly from that of a-Si. Since the qualification standard demanding controlled light soaking preconditioning step is based on the behavior of a-Si material, revisions have to be considered for other thin film materials in order to meet their specific needs.

4.7   Conclusion on accelerated lifetime testing

In this study single junction amorphous silicon photovoltaic modules and CdTe and CIGS prototype modules were exposed to accelerated lifetime testing. Thermal cycling and humidity freeze tests were executed according to the standard procedures. During the damp heat tests the test was interrupted after every certain time periods and the modules were visually inspected and measured for their electrical performance. Otherwise the test methods for damp heat test were according to the IEC qualification standard 61646 [140]. Additionally dry heat test, which is not listed in the qualification test sequence, was executed for one CdTe prototype module. Light soaking was done for a-Si modules, CdTe prototype modules from two different manufacturers and for CIGS modules from two different batches. Light soaking was not considered in this study as a pre-conditioning step according to the standard, but rather a study of the light behavior of the different thin film technologies. The purpose of this study was not to qualify the modules officially and thus the tests have to be considered rather as reliability tests to find out potential failure mechanisms in the thin film modules than qualification tests.

The general conclusion for all the thin film photovoltaic technology modules included in this study is that the major cause for failure in accelerated lifetime tests is humidity penetration into the module encapsulation. In amorphous silicon modules humidity penetration caused major visual defects but the electrical performance was only affected in the first set of samples in P_{max} and FF by 10 %. In CdTe prototype modules humidity penetration caused changes in the back contact composition which could be visually detected and which lead to significant degradation in electrical performance especially in P_{max} in the first set of samples by 82 % and in the second set of samples by 58 % on average. In CIGS prototype minimodules humidity penetration corroded back contact Mo or the front contact ZnO and back contact Mo connection at the relatively unprotected cell interconnect areas. This could be observed both visually and as degradation in the electrical performance in which in the second set of samples most significant degradation was observed in P_{max} by 81 % on average. The first set of samples stopped working after 485 hours of testing. However, even if all these failures were caused by humidity penetration, there were differences between the technologies on how sensitive they were to humidity. The amorphous silicon modules were quite insensitive to humidity penetration. Even though the a-Si modules were visually badly corroded and delaminated after 2000 hours in damp heat test, the modules had still half of the initial maximum power left. In the case of CdTe modules even small amounts of humidity penetration causes changes in the back contact composition, which seems to be the major cause for electrical degradation. The prototype CdTe modules were at least equally tightly encapsulated as the a-Si modules were and in the second set of damp heat testing the humidity tightness was even enhanced with resin between the films and EVA. Even so, the modules in the second set of testing lost half of their maximum power after 1000 hours of testing. The CIGS prototype mini-modules were not as humidity tightly encapsulated as the a-Si and CdTe modules were. Thus they had only fifth of their initial

maximum power left after the damp heat test in the second set of testing. However, the technology does not seem to be as sensitive to humidity penetration as CdTe technology appears to be and thus slight development towards more humidity tight encapsulation design might give significant rise for the module service lifetime expectations. This is in accordance with the findings in [143] in which it is concluded that new, cheaper encapsulation methods and materials frequently used in the automotive and electronics industries can be successfully used for CIGS thin film photovoltaic modules encapsulation. For CdTe modules the results in [143] were not equally positive.

In light soaking the three thin film photovoltaic technologies behaved quite differently. For single junction amorphous silicon solar cell material the results confirmed what has previously been stated in the literature. That is, the a-Si photovoltaic modules degraded in light soaking mostly in short circuit current, by 17 %, and in maximum power, by 35 %, and somewhat in fill factor, by 18 %. Also as expected the degradation stabilized towards the end of the light exposure. In the CdTe a decrease in maximum power, on average 10 % in the first series and 11 % in the second series, independent of the sample or manufacturer was observed. For other parameters no clear behavior pattern could be observed during the light exposure. The dependence of bias state during the exposure to CdTe module behavior should further be investigated. All the CIGS samples except one showed increase in maximum power and in fill factor. In the first series of samples the P_{max} increased by 25 % and the FF by 23 %. In the second series of samples in average there was a decrease in P_{max} by 1 % and an increase in FF by 3 % but the samples behaved very differently. This supports the claim that the observed behavior may be material quality dependent. As a conclusion because the behavior of CdTe and CIGS materials differs radically from that of a-Si under light exposure, the qualification standard demanding controlled light soaking preconditioning step requires some revision to meet the specific needs of different thin film materials.

The IEC qualification testing standard for thin film photovoltaic modules 16164 [140] has mainly been copied as such from the IEC qualification standard for crystalline silicon photovoltaic modules 61215 [122]. For amorphous silicon modules this does not cause major problems since their major issue is light stabilization. Thus attaining qualification according to the current standard should not be too problematic for the a-Si modules since the humidity penetration caused mainly visual defects of cosmetic nature and high temperature or temperature cycling did not seem to affect the module performance. For CIGS and particularly for CdTe thin film photovoltaic technologies, humidity penetration into encapsulation is detrimental. Partly this problem has to be solved by enhancing the humidity tightness of the encapsulant to increase the service lifetime of these modules. However, partly it has to also be questioned whether the current qualification standard is adequate for these technologies or not.

In general the most important test in the current qualification standard for thin film photovoltaic technologies seems to be the damp heat test. It can be said that the thin film modules corrode as well as c-Si modules do but in much shorter time period since there

is much less material to corrode away than in c-Si modules. When new information is gained from the outdoor exposure or real time testing it should be reconsidered whether the long test cycles based on c-Si module performance are adequate for thin film modules and subsequently define a proper service lifetime for these technologies based on their own character. There are also some tests in the standard that can be questioned whether they give any necessary information on thin film module performance when executed, such as the hot spot test and the wet hi-pot test. However, the significance of these other tests was not considered in this study. Also the fact that the thin film qualification standard is mainly developed for a-Si technology does not necessarily imply that it is suitable for qualifying other thin film technologies. For example the light exposure procedures are adequate for a-Si technology but CdTe and especially CIGS had very different behavior under light. As a matter of fact it might even be necessary to consider the CIGS behavior in light soaking when assigning passing criteria for the modules in the tests. The passing criteria are based on absolute electrical performance or power rating values defined by the manufacturer instead of relative before and after test measurement values. With thin film photovoltaic technologies it might be difficult to attain measurement results comparable to the power rating values defined by the manufacturer as was discussed in Chapter 3 above, and some modules might even fail the qualification unnecessarily because of this.

When the third generation photovoltaic technologies are maturing for commercialization in the future some new problems might again have to be encountered in order to qualify the technologies. Thus as a conclusion it can be pointed out that certain basics in the accelerated lifetime testing remain in order to provide adequate service lifetimes for photovoltaic modules. However, some changes shall have to be considered in the method of determining the qualification tests such that the particular module characteristics are better foreseen and that the service lifetimes can better be estimated than today is possible.

5. LASER SCANNING

5.1 Introduction to laser scanning and its applications

In thin film photovoltaic modules it is sometimes necessary to gain information on the performance of individual cells in the series connected module. The IV characteristics might show degradation in efficiency and thus information is needed whether that is due to a global change in the module behavior or a partial failure of an individual cell. It is also difficult to determine from IV measurements whether a visual defect for example after accelerated lifetime testing is affecting the cell and module behavior or if the defect is merely cosmetic. Laser scanning is a nondestructive method, which gives answers to these questions. It can also be used to determine if the cell-to-cell uniformity has improved for example due to a change in manufacturing process. Laser scanning is used to learn about the characteristics of and variations over a single cell in the module, and to gain information about cell-to-cell comparisons in the module and thus it also gives information on the current uniformity of the module. To gain this information with the laser scanning method it is not necessary to disassemble or gain individual cell access to the module. However, comparison of individual cell parameters is complicated by the fact that the dependence of the data on individual cell parameters is often not intuitive. But when properly interpreted the scanning results can reveal photocurrent defects and shunt resistance of the modules.

The basic light spot scanning system was originally designed for analysis of integrated circuits and discrete transistor-like device.[172]. In [172] the authors introduce first laser scanning method for photovoltaic solar cells and modules developed at the National Bureau of Standards. The first laser scanning studies were done for c-Si solar cells. The method is based on scanning the cell with a spot of light while the cell is forward biased. The authors in [172] claim that the resulting response maps may be interpreted to provide information about the efficacy of cell design and construction and also be interpreted to reveal locations of cell conduction defects such as cracks and regions having ineffective ohmic contacts. The method should also be useful for pinpointing cell degradation mechanisms.[172]. Further proof for these claims are given in [173] where the authors derive theoretical foundation for interpretation of laser scanning results.

The basic principle of a laser scanner has been described in several references [32], [35], [36], [172]. A more detailed description of the measurement set-up in this study can be found below in the next section. In a large-scale laser scanner a laser beam is moved over the module and current is measured as a function of laser spot position, resulting in a two-dimensional map of the module. Laser illumination is chopped so that laser beam induced current (LBIC) can be measured even when background voltage biases or bias illumination are applied. The resulting two-dimensional map is a combined charge generation and collection efficiency map of the module where any variation in the generation or collection efficiency of the module appears as a change in

the corresponding current. The detected current is a function of the local photocurrent generated by the laser, the current generated over the entire sample by any light bias, and the external voltage of the sample. In principle, the measured current can be modeled in terms of the current generated in the spot being scanned by the laser, the dark current of the cell being scanned, the cell and module series resistance, and the cell and module light bias current.

One advantage of large scale laser scanning is that only variations important to electrical behavior are evident. The largest disadvantage is that the laser scanner does not supply direct identification of the physical origin of signal variations. Apparent non-uniformity is occasionally artificially introduced by measurement conditions. Thus, interpretation of laser scanning data often requires careful analysis and frequently must be supplemented with data from other characterization techniques.

Several groups have reported on work made with their laser scanning systems, which differ from each other slightly [32], [174], [175], [176], [177], [64]. The laser scanning system described in [32] consists of 633 nm laser beam which, after going through a beam expander, a beam chopper, a selectable lens, and a variable neutral density filter, strikes two computer controlled orthogonal scanning mirrors, which then scan the laser beam over the selected area of the sample. The neutral density filter is used for adjusting the amplitude of the laser generated signal and to bring the 2mW, 0.1 mm diameter laser beam from ~200 suns intensity down to ~1 sun intensity. For light or voltage biasing, beam chopping and lock-in detection are used [32].

In [175] the authors are using the laser scanning method that involves illumination of a small area of the cell with light sufficiently intense to make the internal resistance easily observable. They claim the technique to be especially valuable for spotting small changes in back contact resistance during accelerated stress testing and in identifying the source of any increased series resistance [175].

The first laser scanning set up at ESTI [174] was used for the identification of structural and electrical defects in photovoltaic devices. Two systems were built a high precision one for small devices and a large area one for any device up to module size. Both systems used three different laser wavelengths, 442 nm (blue), 543.5 nm (green) and 632.8 (red). In the high precision system, an interchangeable microscope lens was fixed over the center of the table to allow the focusing of the laser beam. The spot size could be chosen to be 50, 20 or 10 μm. The large area system had a pre-objective scanning configuration. An f-theta lens and an exactly defined negative distortion ensured proportionality between the deflection angle and the beam position on the scanning surface. The laser beam was transmitted to the two scanning systems through optical fibers.[174].

In [176] a scanning optical microscope (SOM) is used where a 4-mW He-Ne laser beam is focused to a small probe. In OBIC carrier injection takes place in a manner analogous to normal operating conditions. The transmitted laser power was reduced using filters. The collection efficiency of the cells and the variations therein (the image

contrast) in the higher intensity regimes were found to be a strong function of the laser intensity. The laser beam power was reduced to a low intensity regime where the collection efficiency and image contrast were measured to be the same as when using typical solar intensity.[176].

In [177] the authors report on work done with an optical double beam microscope with double frequency modulation for LBIC and reflected light measurements. The technical solution consists of using single or double beam configuration of a laser scanning microscope, each beam with its own frequency shift. Reflected light signals interfere on a photodetector and produce a signal equal to the frequency difference of the two laser beams. A lens configures angular parameters of the two laser beams, providing beam focusing and perpendicularity to the sample surface under investigation. The lens also maintains a constant distance between the beam spots on the specimen in the course of scanning. The LBIC experiment in standard amplitude mode at short circuit conditions detects photocurrent inhomogenities that depend on grain boundaries, diffusion length distribution, reflection losses, etc. When applying forward bias voltage the same inhomogenities are detected but the factor caused by the sheet resistance appears. Spatial resolution of the sheet resistance map is determined by the diameter of the focused laser beam spot in case of high absorbed incident light and by diffusion length in case of low absorption.[177].

The set-up in [64] consisted of two He-Ne lasers of wavelengths 632.8 nm (red) and 1152 nm (infrared), an optical focusing channel, a specular deflecting system, and an electronic amplifying circuit intended for detecting a phase modulated or constant optical signal. The red and infrared laser excited regions in the solar cells at different depths and therefore gave information about the surface layer and about layers far from the CdS/CIS (CIGS) heterojunction. The photoactive defects detected with the red laser beam are distributed in the upper layer of the absorber film. The infrared beam, however, does not see these defects since it carries information about bulk properties of the absorber film.[64].

The laser scanning measurements are normally done either in short circuit or forward bias conditions. The forward bias conditions can be provided by background illumination or by introducing an external forward bias source. Several references claim that forward bias conditions are essential in laser scanning measurement to reveal useful information of the sample [172], [32], [36]. In [172] the authors report that without significant internal shunting, i.e., for cells scanned while operating near zero bias, optical scanning does not reliably detect cell defects such as cracks, regions of poor contacting, regions of excessive emitter sheet resistance, etc., which may seriously influence cell reliability and conversion efficiency. Varying the diode forward bias can vary the values of the shunt resistance. Application of forward bias increases internal shunting to a degree sufficient to observe defects.[172]. Also in [36] it is reported that the forward voltage biased laser scans yield information about spatial variations in forward current characteristics, which is not available from short circuit scans. According to [32]

measuring the OBIC in the dark is sufficient if the superposition principle is valid. Measurements in the dark at zero volts bias yield an OBIC signal related to the photoresponse and "shunting current" of the individual cells in the module under test. The superposition principle is not valid for most thin film photovoltaic devices, thereby complicating the interpretation of OBIC maps without the addition of light biasing. With light bias it is also possible to extract information from the OBIC measurements about series resistance and recombination under operating conditions.[32].

However, there are some points to be noted when choosing between light bias and an external current source as a method to forward bias the sample. In the case when external current source is used the emitter is no longer an equipotential surface as it is in the case when bias illumination is used. In this case the cell conductance per unit area will vary with distance from the metallization stripes when c-Si solar cells are scanned, and the results obtained by laser scanning cells will differ quantitatively from those predicted when light bias is used. However, it is found that the qualitative features remain the same and thus also an external electrical current source can be used to provide forward bias to the photovoltaic sample being investigated.[172]. According to [36] a white light bias with only a few percent nonuniformity can act as a potential error source on the laser scan signal. More brightly illuminated cells are pushed further into forward bias, decreasing their signal. Less brightly illuminated cells show increased signals. As a result, white light biased laser scans with nonuniform light source may essentially yield an intensity map of the light bias source, rather than giving new information about cell performance.[36]. It is also noted that resistance that is not associated with the cell on a per area basis, such as TCO or lead resistance, has very little effect on the forward biased laser scan [36].

Red laser is most commonly used in laser scanning studies. However, in certain cases it might be useful to use lasers with other wavelengths for probing the different layers of device structures. For example, in CdS/CIS, 442 nm for the CdS, 633 nm for the CIS depletion layer and 1.06 μm for the bulk CIS. Combining multiple wavelength lasers with white light and voltage biasing techniques enables characterization of collection losses versus nongeneration losses and varying types of defects.[32]. In the studies of two special applications the blue laser scanning has been reported to reveal new information. These applications are the studies of red light distortion in CIS photovoltaic solar cells [34], [36] and the effect of EVA browning on the photovoltaic cell efficiency in a module construction [179], [36].

The red light curve of CIS photovoltaic solar cells exhibit a significant distortion that disappears under illumination by photons with energy greater than the CdS bandgap. It has been observed that the existence of this distortion is related to the type of chemical bath process used for the CdS buffer layer formation in CIS solar cells. Within experimental error, the boundary between short wavelength or blue and long wavelength or red response is the bandgap of CdS.[34]. In [34] the authors conducted studies on some CIS samples. They found that the red scan before white light bias shows

nonuniformities and low current areas in the short circuit current map. After white light biasing the short circuit current map shows high signal response throughout the sample. For blue laser scan the resulting short circuit current map shows high signal response both before and after white light biasing.[34], [36]. Thus using blue laser light to complement the red laser light laser scanning studies revealed new information on the red light distortion phenomenon in CIS solar cells.

The optical effect of EVA browning on photovoltaic cell efficiency loss can be resolved spatially by using scanning laser OBIC analysis [179]. In [179] the authors used an Ar blue laser of 488 nm and a He-Ne red laser of 633 nm. As a result the short circuit current map shows a higher response on the browned EVA parts with the red laser scan than with the blue laser scan [179]. In [36] it was reported that the discolored EVA absorbs 35 % of the originally transmitted blue photons but only 5 % of the originally transmitted red photons.

One major application of laser scanning results is the extraction of solar cell photocurrent and shunt resistance from the resulting data. The distributed character of the series and the shunt resistance should be taken into account particularly for the large area and thin film solar cells. Shunting results from current flow through paths other than the p-n junction, such as electrically active grain boundaries or localized defects. Series resistance can be due to bulk semiconductor resistance, TCO resistance, and resistance between the semiconductor layers and the contacts. Shunts can deteriorate the dark IV characteristics. While the series resistance inhomogenity decreases the short circuit current, the shunts can drastically influence the open circuit voltage and fill factor.[180], [36]. A number of methods other than laser scanning exist to examine shunt resistance and photocurrents, or some combination of both, in encapsulated modules. One of these methods is based on selective illumination and application of DC and AC voltages. This method can accurately extract shunt resistance of all cells in the module, and yields values that represent actual current flow through the module, independent of the position of spot illumination. However, it requires time-consuming shading of each cell and a very short stable and uniform background illumination. Another method scans light over each cell at short circuit. This method provides an estimate of the shunt resistance of good cells, but even moderately shunted cells may produce orders of magnitude less signal than the good cells, and therefore often no estimate can be made regarding the cells of particular interest. A third method chops selective illumination at varying frequencies to extract photocurrents and shunt resistance of individual cells. However this method is applicable to only single junction cells, and very high chopping frequencies – often beyond those attainable by mechanical chopping – are required to obtain information about severely shunted cells.[35].

The actual laser scanning signal obtained is proportional to both the cell's photocurrent and its shunting resistance. Shunting defects exhibit different signatures than defects that merely prevent production of photocurrent. Laser scan signal rolls off into a shunting defect, since photocurrent generated away from the defect can flow into

the defect. Photocurrent defects, on the other hand, do not affect the laser scan signal until the laser is incident on the defect. Therefore, laser scan signal does not roll off into a photocurrent defect, but drops off as sharply as the beam size allows. Photocurrent and shunting defects may occur in tandem, in which case the photocurrent defect may mask much of the shunting defect signal roll off.[36].

The principle of extracting the shunt resistance from the laser scanning data is given in [36]. With only the short-circuit DC signal, one cannot determine whether a relatively small signal from one cell is due to it having a small shunting resistance, a small photocurrent or some combination of both.[31], [36]. Shunting may be expressed as the forward diode conductance which is dependent on the forward bias of the cell, and thus on the level of cell illumination or forward current bias of the cell.[181]. Thus it is possible to extract qualitatively the shunted cells in the module by comparing the photocurrent maps from laser scanning done in short circuit DC conditions and in forward bias conditions. In case of severely shunted cells do not give any OBIC signal at short circuit regardless of frequency. At short circuit, the impedance of the good cells is larger than the impedance of the leaky cells. The good cells therefore give a much larger OBIC signal. As forward current increases, however, and the current of the good cells increases exponentially, and the impedance of the leaky cells, dominated by shunting, stays the same. At some forward currents, then, the impedance of the leaky cells may be larger than that of the good cells. The leaky cells therefore give a larger relative OBIC signal at these currents.[31], [36].

Another method to with which it is possible to approximate the shunt resistance values of the shunted cells is described in [31] and [36]. One can measure the total module impedance and the signal from all cells at two frequencies, with high and low frequencies. Equations presented in [31] and [36], and which are out of the scope of this work, then allow extraction of individual cell shunt resistance, photocurrents, and capacitance from these two-terminal measurements, assuming all cell capacitance are equal. The characteristic frequency that determines whether a measurement is in the high or low frequency regime is 1 kHz.[31], [36]. The theory of the above-described methods involves a number of approximations, making the extracted value of the shunt resistance an approximate value.[35]. First, it is assumed that the voltage shift in the laser-illuminated cell caused by turning on the laser is small enough to approximate the current-voltage (I-V) curve as linear over that region. For I-V curves with an approximately exponential shape, this requires that at the voltage bias of interest, the module impedance times the LBIC signal from any cell is less than the thermal voltage AkT/q, about 50 mV. Second, capacitive effects from chopping the laser have been ignored. Third, in identifying the slope of the I-V curve of the shunted cell as its shunt resistance, it is assumed that all the forward current through the shunted cell at the analysis voltage bias is shunted current. Fourth, variations in photocurrent from cell to cell have been ignored, as it is assumed that variations in shunt resistance from cell to cell are orders of magnitude greater when both faulty and efficient cells exist in the same

module. Fifth, the signal from the shunted cell will depend on the proximity of the laser beam to the shunt. The signal from the shunted cell is assumed to be the average signal collected from the cell near operating voltage. This assumption also ignores the effect on the average signal conduction paths from the laser spot to the shunt that involve current flow through the interconnect and neighboring cells.[35].

The authors in [33] have identified several issues that are important to the accuracy and reproducibility of OBIC or laser scanning data. These include laser beam power, size, intensity, and chopping frequency, optical alignment, correct amplifier calibration, and accurate measurement of voltage bias. Laser beam power and intensity are important when interpreting the laser scanning results properly. For polycrystalline cells the diode junction parameters may vary with beam intensity. In short circuit module measurements, the illuminated cell in a module is forward biased and all the remaining cells reverse biased. Forward biased cells produce a smaller OBIC signal than reverse biased cells. Therefore, at high beam powers, adjacent cells to the laser illuminated cell collect much more efficiently. There can also be an artificial increase in response near cell edges due to this adjacent cell collection. The beam power at which this effect becomes significant depends on the characteristics of the module being measured.[33]. The authors in [182] report that in the CdTe cells they had investigated, the collection efficiency and image contrast were found to depend strongly on the power of the incident beam, particularly at high powers. The image taken with low laser intensity has very low image contrast, which indicates very uniform collection efficiency. Images, in which some dark areas, indicating poor carrier collection efficiency, were only observed at high injection density levels.[182]. Beam size is important for resolution. Accurate amplifier calibration is important if conversion of OBIC signal to absolute collection efficiency is desired. OBIC signal depends strongly on voltage bias, so it is important to know the exact voltage bias of a measurement for reproducible results. When using white light bias as forward voltage bias, it must be noted that even small nonuniformities in white light bias change the distribution of voltage biases in the module enough to significantly affect the OBIC output. More brightly illuminated cells are more forward biased, and therefore produce a smaller OBIC signal. If care is not taken to have a uniform bias light source, relative signal heights of short circuit OBIC measurements may yield basically an intensity map of the light source. The effect of intensity nonuniformities is more severe at higher intensities. In module measurements there are some requirements for chopping frequency if lock-in amplifier is used. A typical requirement is that chopping frequency should less than 100 Hz to operate in the DC limit, although the exact requirement must be determined by the characteristics of the module being tested. If the module is measured above this frequency, the signal from leaky cells is enhanced and the signal from the good cells is diminished.[33].

In this chapter the technique of laser scanning used for the investigations of thin film photovoltaic modules was studied. In the first section the behavior patterns of amorphous silicon, CdTe and CIGS modules in laser scanning were investigated. The

modules were laser scanned with red laser in three different bias conditions or in short circuit, under light bias and exposed to externally supplied forward current bias. Also the technique found in literature to use laser scanning to reveal shunted cells in thin film photovoltaic modules was verified. In the second section laser scanning of a-Si, CdTe and CIGS modules with blue laser was investigated. With blue laser different active thin film layers in the modules can be probed. In literature blue laser scanning has been used mainly to study the red light distortion in CIGS modules. Use of blue laser was not found to give any further information in the scope of this work when compared to the information given by the use of red laser. In the third section a-Si, CdTe and CIGS modules were investigated by laser scanning them after 1000 hours (2000 hours in case of a-Si module) of damp heat testing. Three different bias conditions or short circuit, light bias and externally applied forward current bias conditions were used. The resulting photocurrent maps were compared with the visual defects observed after damp heat test. Laser scanning technique gives information on the short circuit current generation of the thin film photovoltaic modules. Therefore by laser scanning, the short circuit current degradation after accelerated lifetime testing could be correlated with the visual defects detected in the modules.

5.2   Laser scanning measurement set-up

The laser scanning equipment is very similar to that described by Matson and Emery [32]. The set up is illustrated in Figure 5.1 below. A collimated 632.8 nm He-Ne chopped laser beam passes through a focusing system and a scan head, which is a computer controlled couple of galvanometric mirrors steering the beam over the test device. An Iwatsu double PSD lock-in amplifier detects the signal generated by the laser. The chopping frequency was 1.2 kHz in all measurements described here. Such a frequency guarantees both speed up for the measurement and detection of the shunting effects [31]. The He-Ne laser after passing a neutral density filter and a diaphragm had an effective area of 4 mm^2 and an irradiance of 10 W/m^2.

The bias light was provided by a circular lamp system with 24 halogen lamps. The light intensity of the lamps can be regulated in four lamps at a time individually. Since its circular shape around the module being measured this lamp system provides a very uniform bias light over the module. A Kepco type BOP50/4 bipolar operational amplifier provided the forward current bias. It was used in the voltage mode in all the biased measurements.

The photocurrent of all the modules was measured via a resistance of 1 Ω. The first measurement was done in the dark and thus the module was kept in short circuit. In the second measurement the module was measured with full intensity light bias of 200 W/m^2. However, since halogen lamps were used, from their intensity 120 W/m^2 fall to crystalline silicon region and in the a-Si and CdTe regions the intensity is less. For the CIGS material region the intensity is the same as for the c-Si material.   The third measurement was done with half intensity light bias of 100 W/m^2. For this measurement the lamp system caused some disturbances in the measurements seen as noise in the results. This noise was probably due to high frequency harmonic of the lamp, which was not filtered by the chosen chopping frequency.

The measurements with forward current bias were done with 100 mA and 50 mA currents for the a-Si module and additionally also with 30 mA bias for the CdTe modules. The CIGS samples were measured with forward current bias values of 30 mA and 10 mA. During the forward current bias measurements no light bias was used and the measurement was done in dark ambient conditions. The time constant for the lock-in amplifier was kept in all the measurements at either 12.5 ms or 40 ms and before each subsequent measurement point there was a waiting time of 100 ms. The full scale sensitivity of the lock-in amplifier was set to 30 µV, 100 µV or 300 µV. The signal read from the analog output of the lock-in amplifier constantly ranged from 0 V to 10 V regardless of the settings. The resolution used for a-Si and CdTe module scans was 40x40 pixels and for CIGS 20x20 pixels.
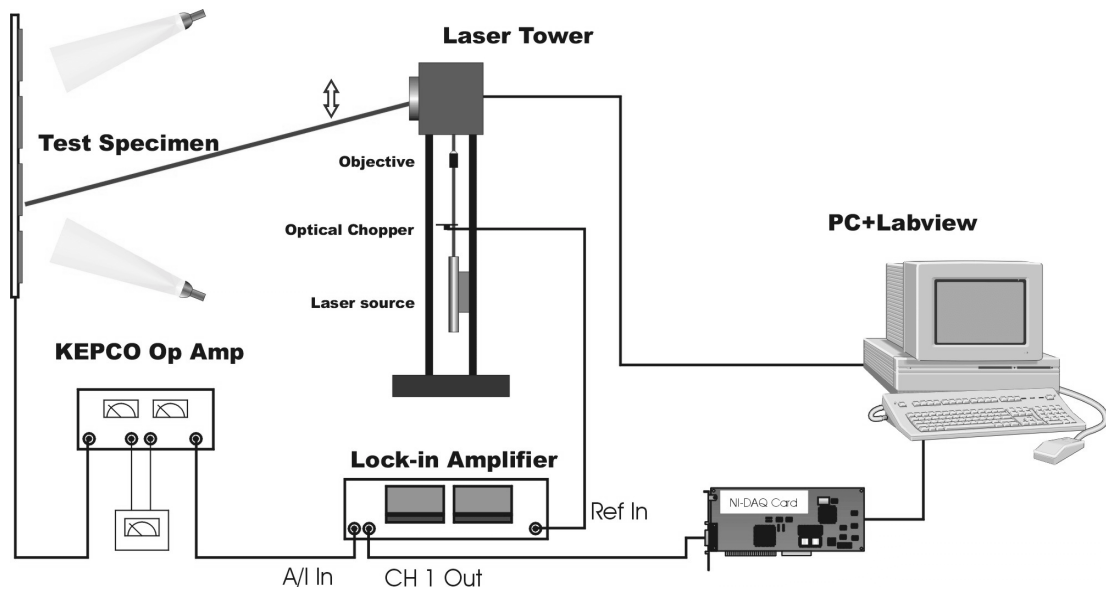
Figure 5.1 *The set up of laser scanning measurement system.*

5.3 Laser scanning used to investigate bias dependency

5.3.1 Sample description

One a-Si and two CdTe modules were laser scanned as well as two CIGS samples. The description of the samples can be found in Table 5.I below. Both CIGS samples came from the same manufacturer and were prepared in the same batch. Both CdTe modules were produced by same manufacturer but came from two different batches.

Table 5.I *Sample description of modules and samples that were laser scanned with different bias conditions.*

ESTI ID	Thin film material	Module size	Module description
AB510	a-Si	1x1 ft^2	Framed glass-glass module
CB515	CIGS	10x10 cm^2	Unframed glass-glass prototype mini-module
CB518	CIGS	10x10 cm^2	Unframed glass-glass prototype mini-module
ZB503	CdTe	30x30 cm^2	Framed glass-glass prototype module
ZB509	CdTe	30x30 cm^2	Framed glass-glass prototype module

5.3.2 Results

a-Si

The resulting photocurrent maps of the laser scanning with different bias conditions of amorphous silicon module AB510 are presented on Figure 5.2 below. The amorphous silicon module was first laser scanned in the dark in short circuit (Figure 5.2(a)). The response is quite even throughout all the cells, only some cells show somewhat higher response than the others have but the difference is not significant. With full intensity bias light (Figure 5.2(b)) the ninth and the last cells in the module stand out with much higher response than in the other cells. For the other cells the response is extremely even. With half intensity bias light (Figure 5.2(c)) the photocurrent map is very similar to that measured in short circuit. Only the overall response is shifted up and thus on the vertical scale 10 corresponds to a sensitivity of 100 μV when it in the short circuit measurement result corresponded to 30 μV. Unfortunately a lot of noise is included in the measurement result measured with half intensity bias light. The

photocurrent map measured with 100mA forward current bias in dark (Figure 5.2(d)) is again very similar to that measured with full intensity bias light. In this case the overall response is shifted down compared to the results measured in full intensity light bias. In the side view on the vertical scale 10 corresponds to 30 μV when it in the resulting photocurrent map after measurement in full intensity light bias corresponded to 100 μV. The two cells that had higher response when measured with full intensity light and high forward current biases have, in the photocurrent map measured with 50 mA forward current bias in dark (Figure 5.2(e)), only a slightly higher response compared to the other cells. Also in the result of this measurement some noise in included.
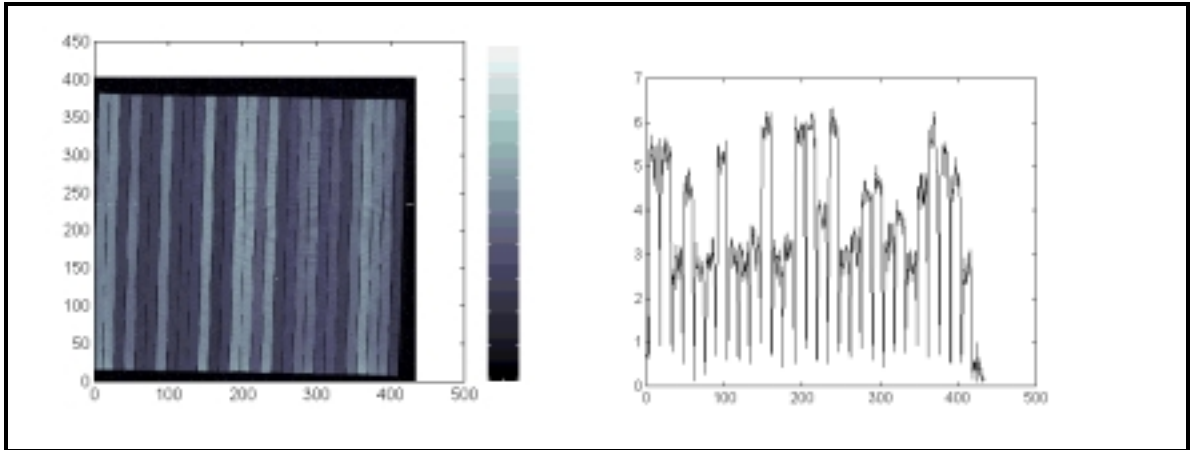
(a)
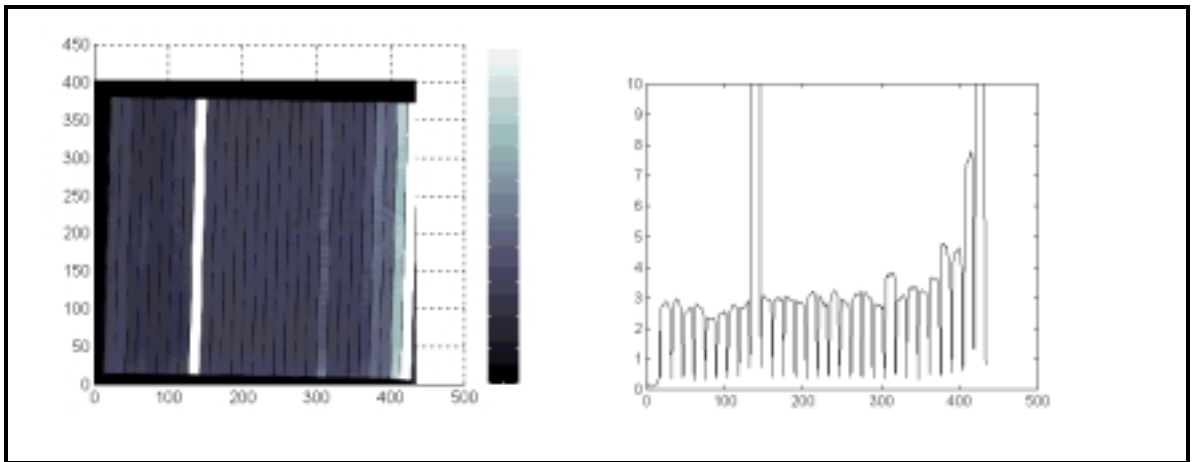
(b)
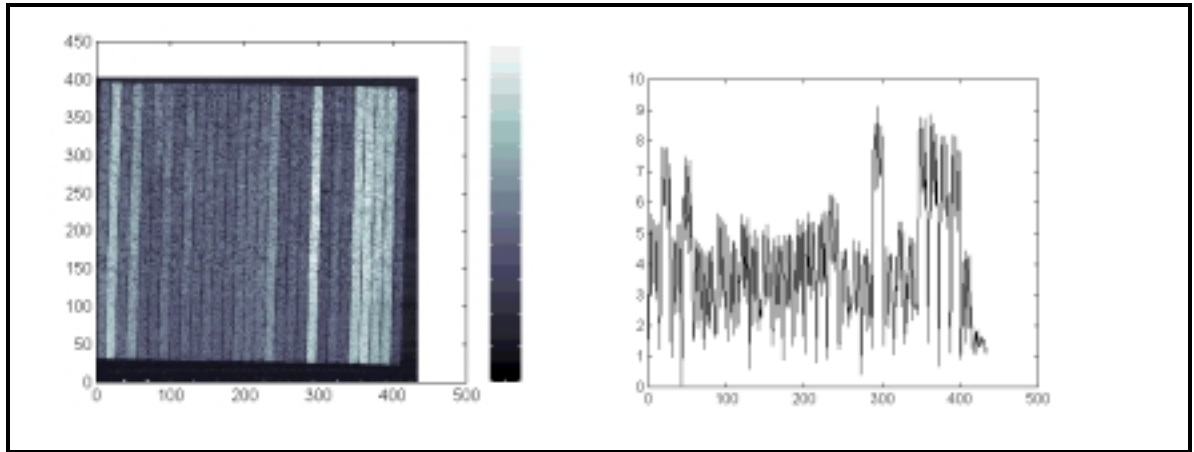
(c)
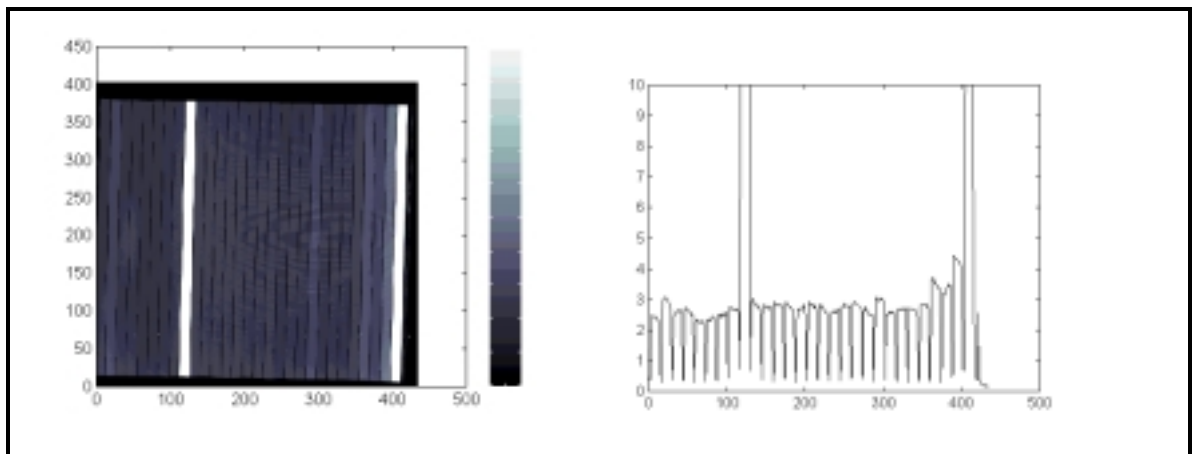
(d)
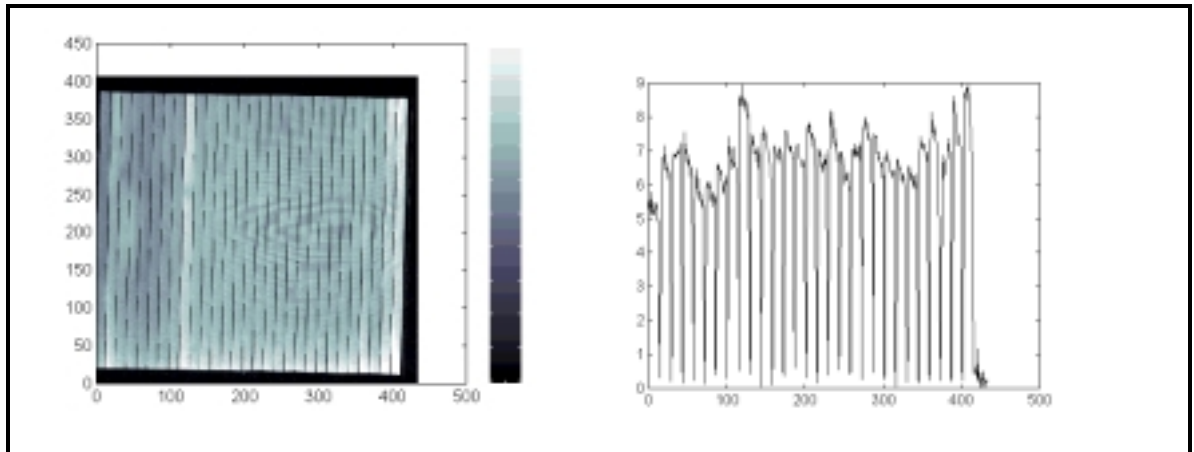
(e)

Figure 5.2 *Laser scanning of amorphous silicon module AB510 with different bias conditions. (a) Measurement without any bias in dark in short circuit. In the side view on the vertical scale 10 corresponds to 30 µV. (b) Measurement with full intensity light bias. In the side view on the vertical scale 10 corresponds to 100 µV. (c) Measurement with half intensity of the bias light. In the side view on the vertical scale 10 corresponds to 100 µV. (d) Measurement with forward current bias of 100 mA (corresponding*

voltage bias 22 V) in dark. In the side view on the vertical scale 10 corresponds to 30
µV. (e) Measurement with forward current bias of 50 mA (corresponding voltage bias
20 V) in dark. In side view on the vertical scale 10 corresponds to 30 µV.

CdTe

The results of laser scanning of two CdTe prototype modules ZB503 and ZB509 when scanned at different bias conditions are presented in Figures 5.3 and 5.4 below. In the photocurrent maps for ZB503 scanned in short circuit (Figure 5.3(a)), with full intensity light bias (Figure 5.3(b)) and with half intensity light bias (Figure 5.3(c)) the first half of the module starting from the left gives significantly lower response than the right half of the module. Especially in the laser scanning response in short circuit there are two cells, the second and the 14th cell from the left, that give a very low response. When the module is scanned with very high forward current biases of 100 mA (Figure 5.3(d)) and 50 mA (Figure 5.3(e)) the overall response is very even but also of lower intensity since the sensitivity is in these measurement 30 µV instead of 100 µV as in the other measurements for this module. There is also quite a lot of noise present with high forward current bias measurements. However when measured with 30 mA forward current bias (Figure 5.3(f)) the response is less noisy, has more intensity in the response signal than for higher forward current bias values and is also very even. Only two cells have somewhat higher response than the others, that is the second and the 14th cell from the left. These were exactly the same cells having especially low signal values when measured in short circuit and with light biases.

For the second CdTe module ZB509 the laser scanning photocurrent maps in Figure 5.4 below show a varying response from cell to cell. When measured in short circuit basically every other cell has a high and every other cell a low response (Figure 5.4(a)). The highest response area seems to be within the last cells on the right and after them towards left seem to be the lowest response cells. When using full intensity light (Figure 5.4(b)) and half intensity light biases (Figure 5.4(c)) the differences seem to even out even though they are still clearly notable. With 100 mA forward current bias (Figure 5.4(d)) the signal is quite even but also very low since the vertical scale of 10 corresponds in that photocurrent map to 30 µV when it in the other maps for ZB509 correspond to 100 µV. When using 50 mA (Figure 5.4(e)) and 30 mA (Figure 5.4(f)) forward current biases the photocurrent map has again very uneven signal response values. However when looked closely it can be noticed that the signal now shows a high value in cells that showed low values when scanned in short circuit or light biases and vice versa. The lowest signal values area is now within the last cells on the right and the highest value cells on their left. Also the first cells on the left showed very high response values in short circuit and with light bias measurements but with 50 mA and 30 mA forward current bias measurement they show very low responses.
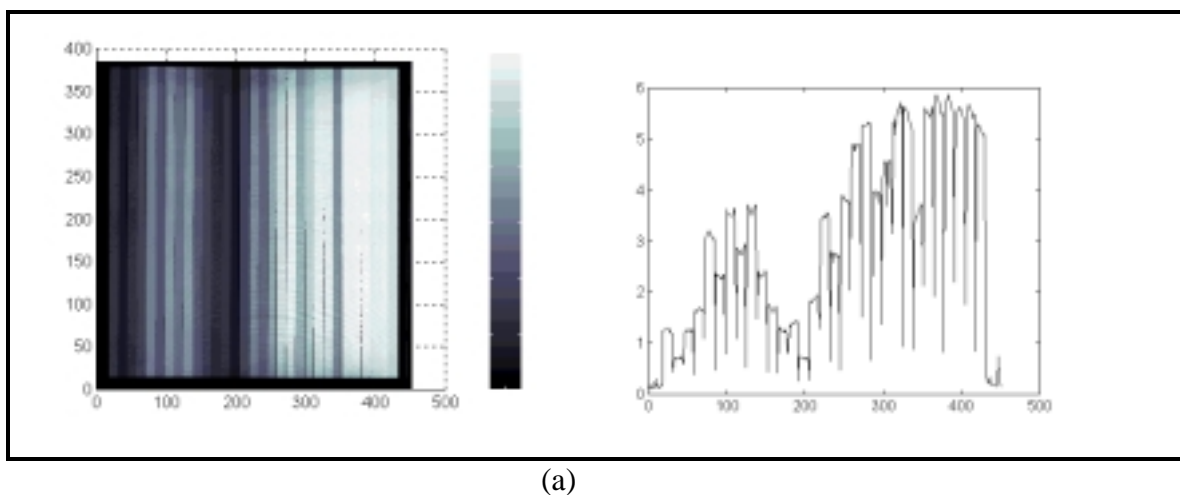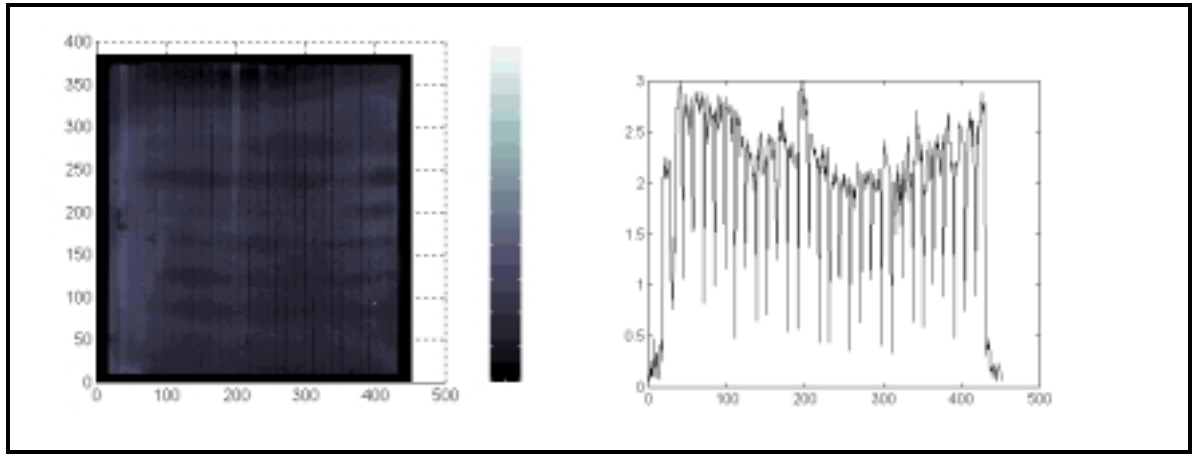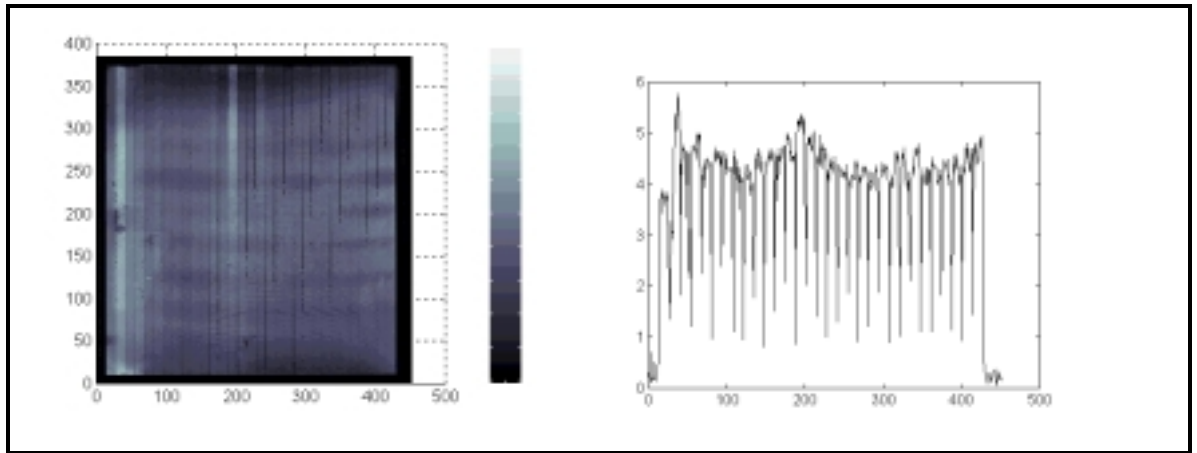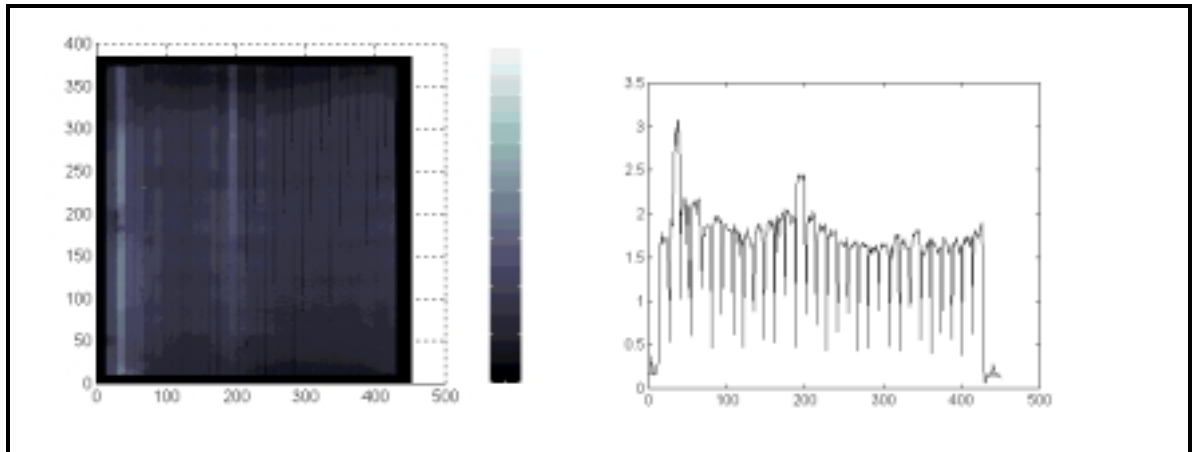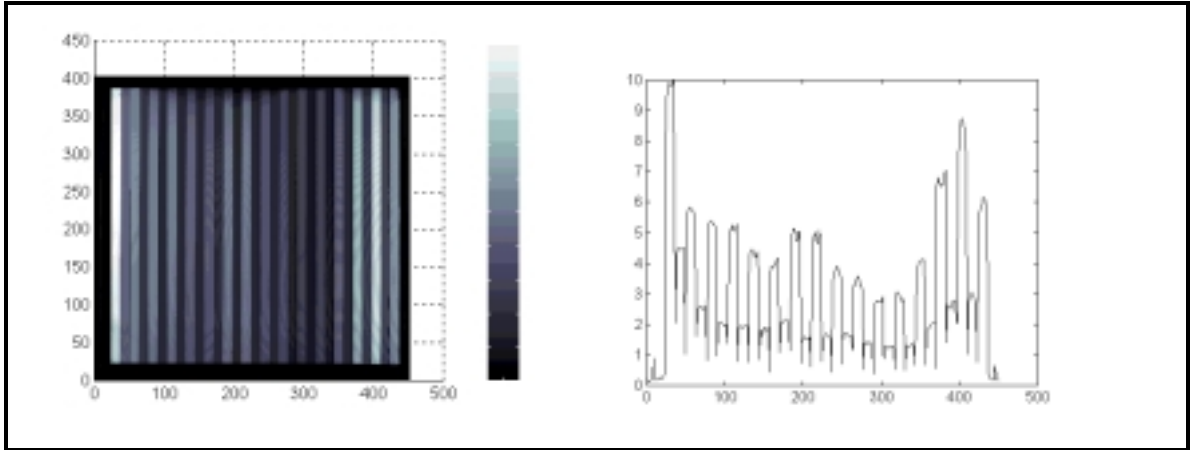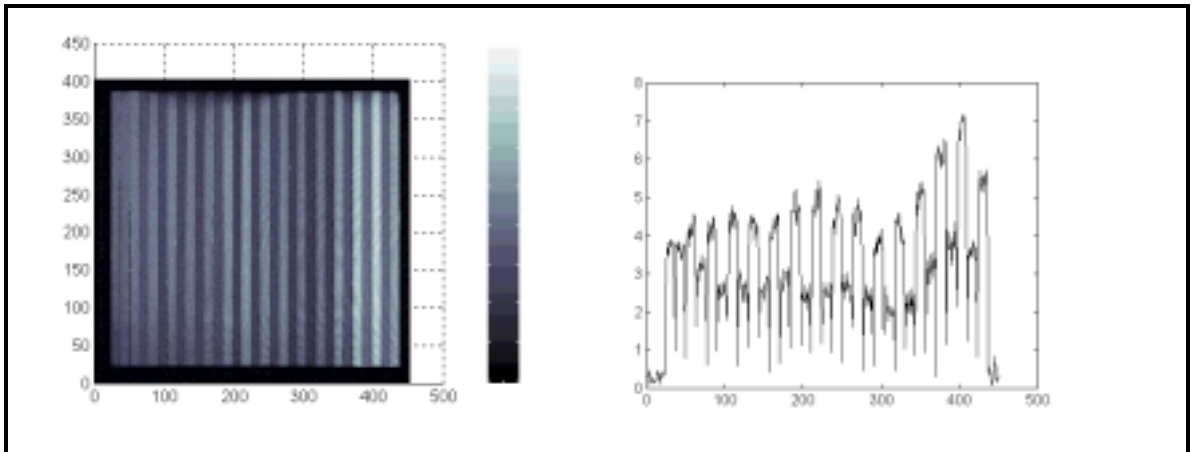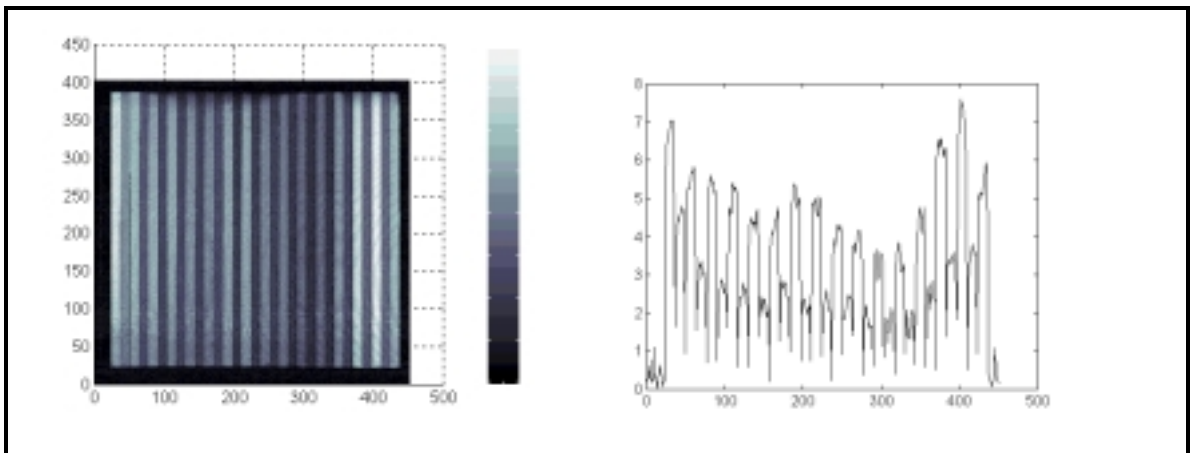
(a)
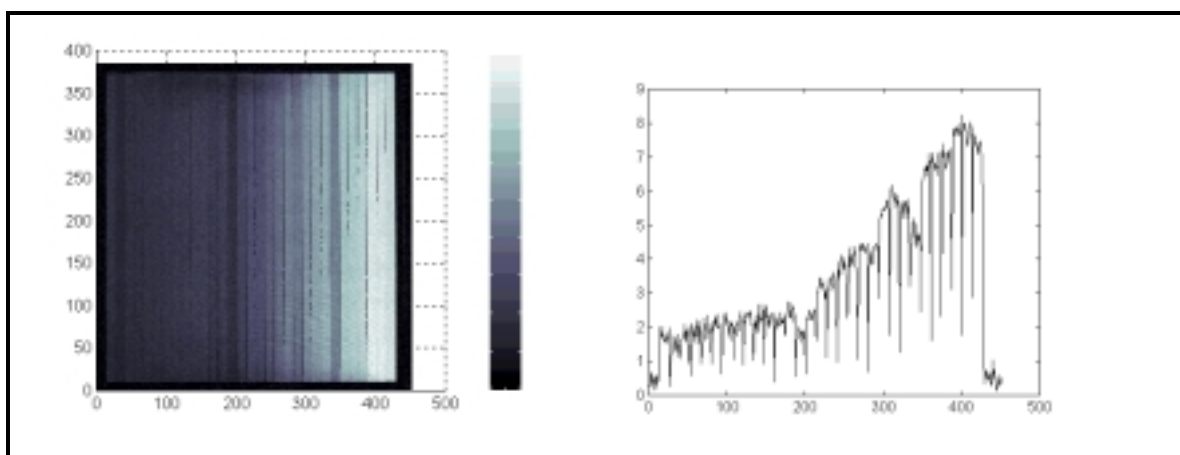
(b)
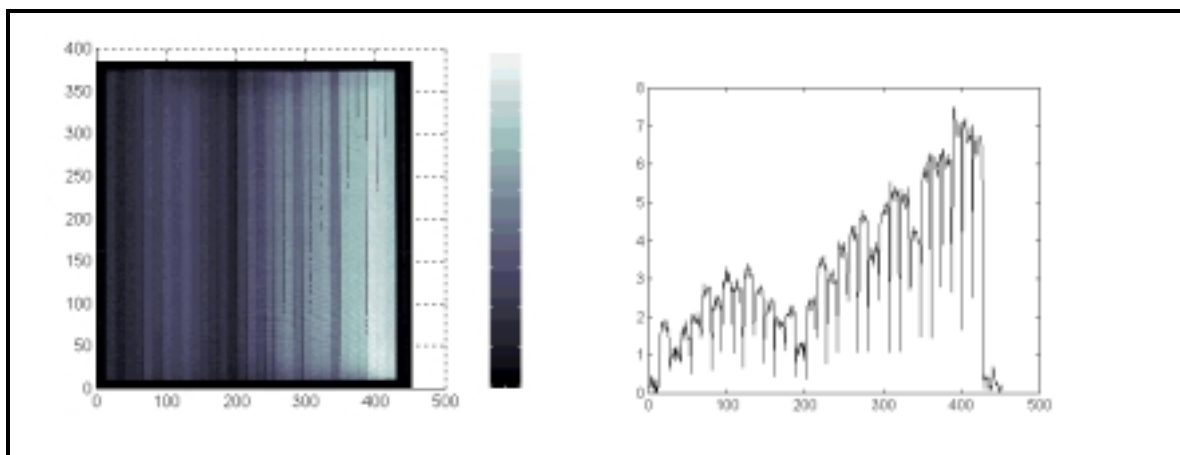
(c)

(d)

(e)

(f)

Figure 5.3 *Laser scanning results for the CdTe prototype module ZB503 with different bias conditions. (a) Measurement without any bias in dark in short circuit. In the side view on the vertical scale 10 corresponds to 100 µV. (b) Measurement with full intensity light bias. In the side view on the vertical scale 10 corresponds to 100 µV. (c) Measurement with half intensity light bias. In the side view on the vertical scale 10 corresponds to 100 µV. (d) Measurement with a forward current bias of 100 mA*

(corresponding voltage bias 21 V). In the side view on the vertical scale 10 corresponds to 30 μV. (e) Measurement with a forward current bias of 50 mA (corresponding voltage bias 19 V). In the side view on the vertical scale 10 corresponds to 30 μV. (f) Measurement with a forward current bias of 30 mA (corresponding bias voltage 18 V). In the side view on the vertical scale 10 corresponds to 100 μV.
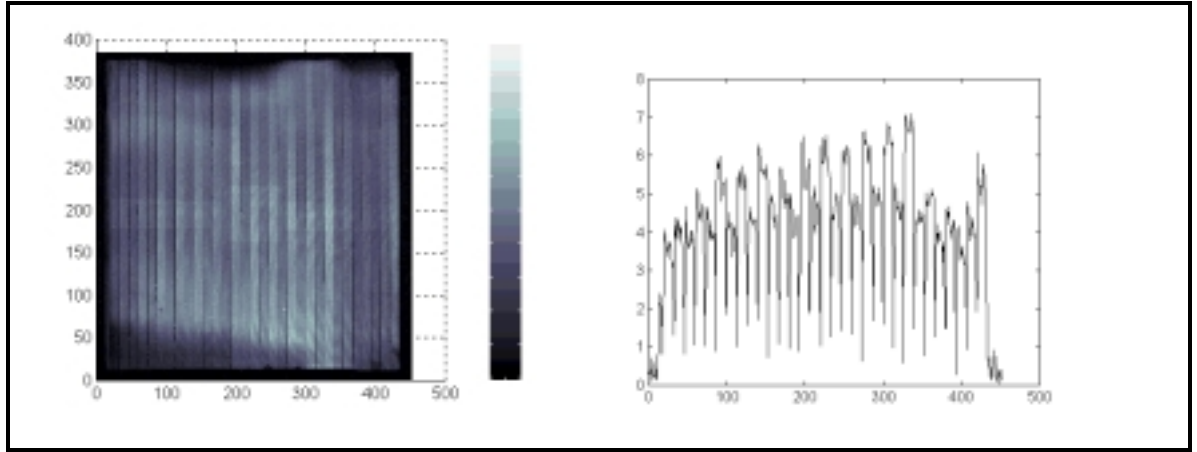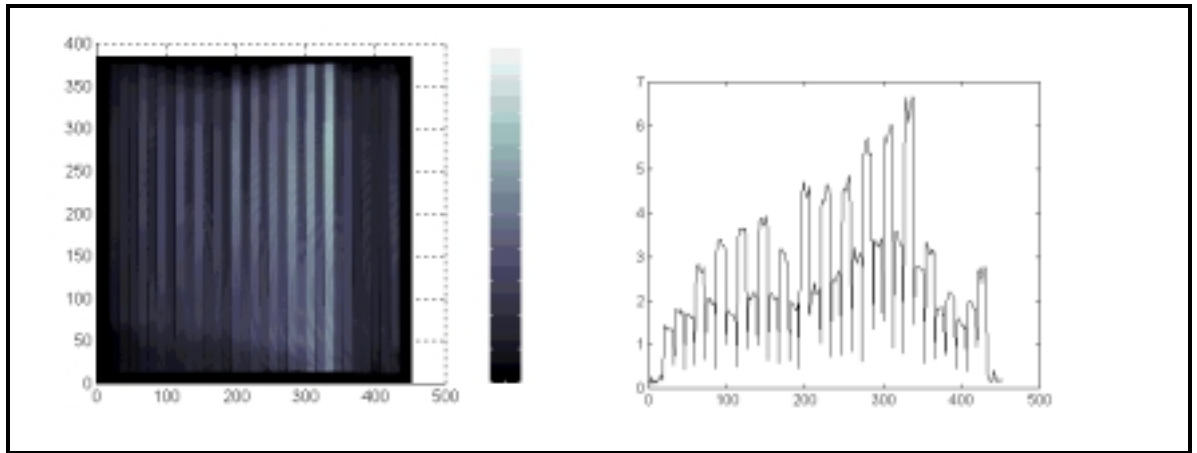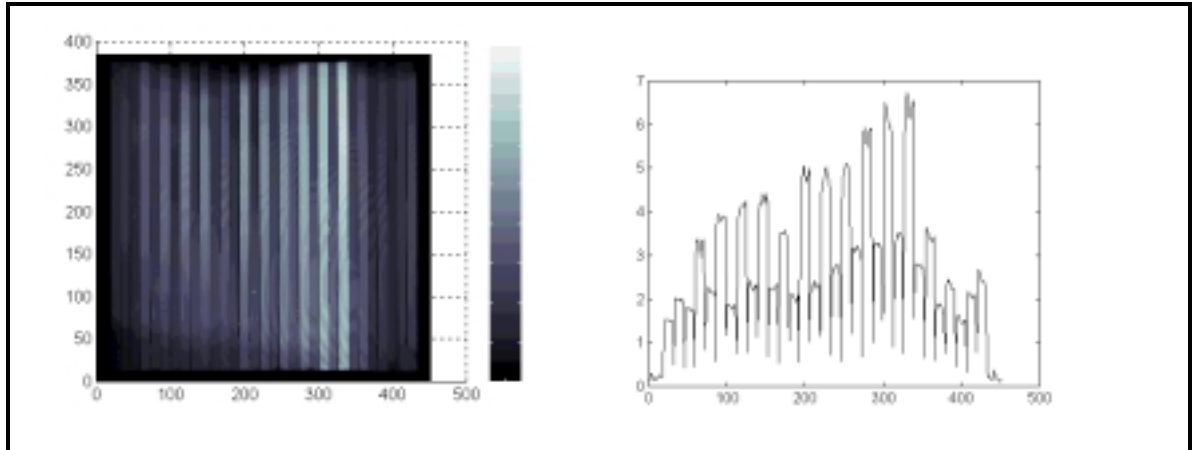

(a)

(b)

(c)

(d)

(e)

(f)

Figure 5.4 *Laser scanning results for the CdTe prototype module ZB509 in different bias conditions. (a) Measurement without any bias in dark in short circuit. In the side view on the vertical scale 10 corresponds to 100 μV. (b) Measurement with full intensity light bias. In the side view on the vertical scale 10 corresponds to 100 μV. (c) Measurement with half intensity light bias. In the side view on the vertical scale 10 corresponds to 100 μV. (d) Measurement with a forward current bias of 100 mA*
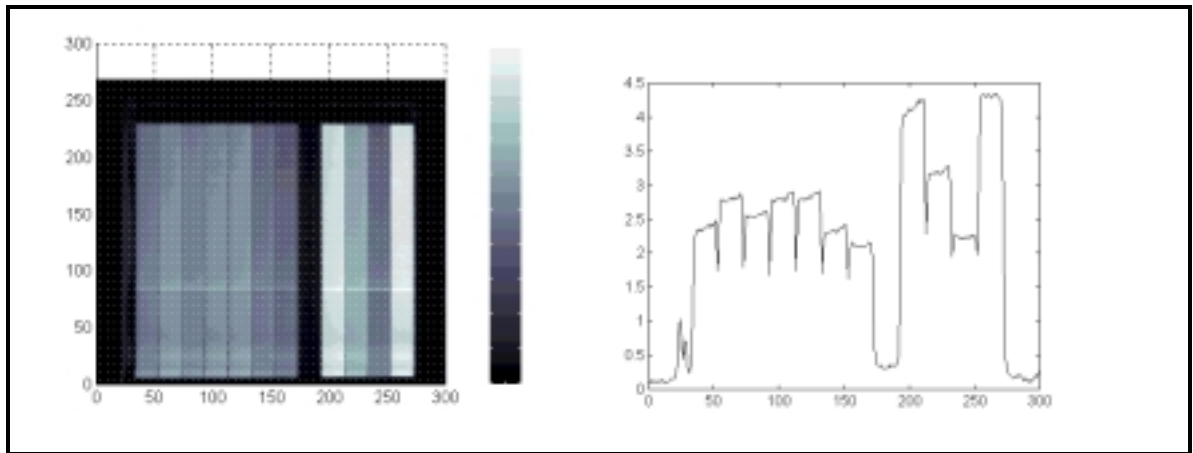
(corresponding bias voltage 20 V). In the side view on the vertical scale 10 corresponds to 30 µV. (e) Measurement with a forward current bias of 50 mA (corresponding bias voltage 16V). In the side view on the vertical scale 10 corresponds to 100 µV. (f) Measurement with a forward current bias of 30 mA (corresponding bias voltage 16 V). In the side view on the vertical scale 10 corresponds to 100 µV.
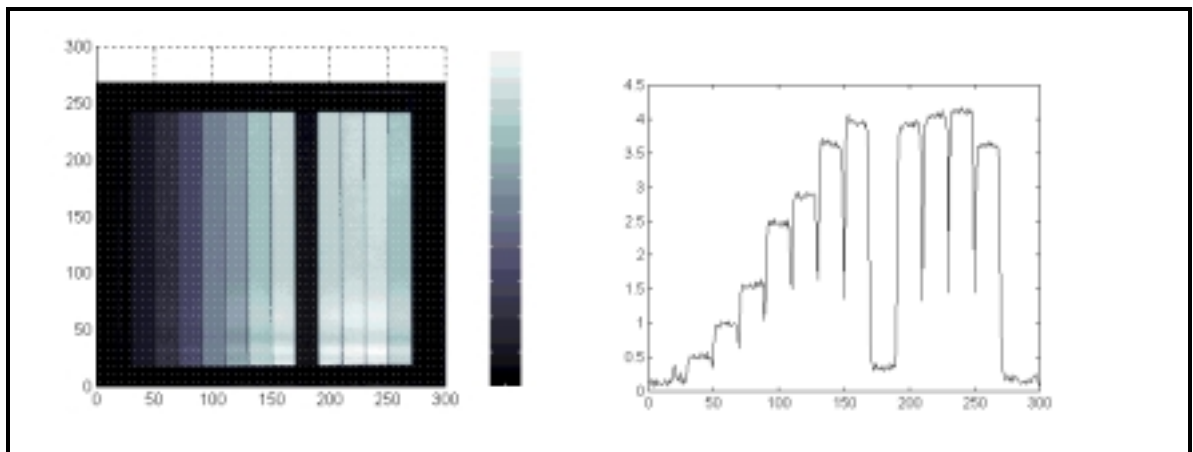
CIGS

The results of laser scanning of two CIGS prototype mini-modules CB515 and CB518 are presented in Figures 5.5 and 5.6 below. When the other sample CB515 was measured in short circuit (Figure 5.5(a)) the photocurrent map is quite even especially beginning from the left of the module. However the 5th cell from the right shows very low value. The last cells on the right have an uneven response. Overall the response is lower than when bias was used since the sensitivity was 100 µV instead of 300 µV as in the photocurrent maps measured with bias. When the sample was scanned with full intensity light bias (Figure 5.5(b)) and with half intensity light bias (Figure 5.5(c)) the 5th cell from the right still has a very low response. However for the first cells from the left the response has become uneven growing steadily from left to right. The last cells on the right have now a very even, high response for both light bias measurements. The photocurrent maps for measurements with 30 mA (Figure 5.5(d)) and 10 mA (Figure 5.5(e)) show a very high response to the 5th cell from the left, which had a very low response in short circuit and with light bias. For all the other cells the response is very even and much lower than for this one cell.

When the CIGS sample CB518 was measured in dark (Figure 5.6(a)) the 3rd and 4th cells from the left have a higher and the 6th cell from the right a lower response than the other cells that have quite even response. When measured with full intensity (Figure 5.6(b)) and half intensity (Figure 5.6(c)) light biases the 6th cell from the right still has a very low response. However the high response in dark for the 3rd and 4th cells has evened out. Their response has decreased and the neighboring cells' response has increased. Also the response for the first cells from the right have decreased. When using forward current bias of 30 mA (Figure 5.6(d)) the first cells from the left has a decreased response compared with the measurement results in dark and with light biases. The only cells that have a higher response in this measurement are especially the 6th cell from the right and somewhat the 4th cell from the right. When measured with 10 mA forward current bias the 4th and 6th cells from the right have a significantly higher response than the other cells. An especially low response is observed for the 2nd to 5th cells from the left. The 6th cell from the right had a in dark and with light biases a very low response but the 4th cell from the right has in all the other measurements had an average response when compared to the responses of the other cells in the sample. The overall response in this measurement was higher than in the other measurements with sensitivity of 300 µV when compared to 100 µV for the other laser scanning measurements for CB518 sample. The photocurrent maps in Figures 5.6 (b), (c) and (d) have a high noise level due to too low
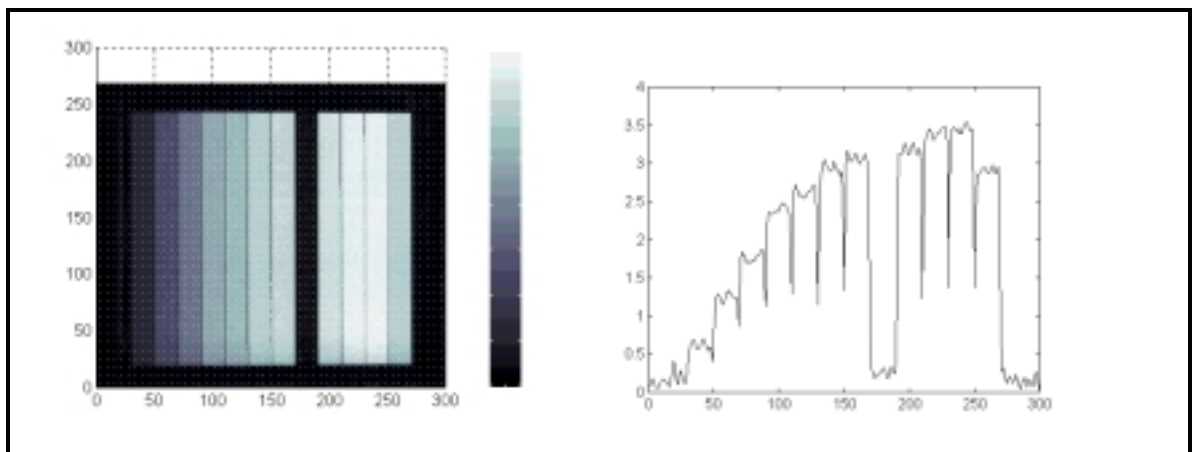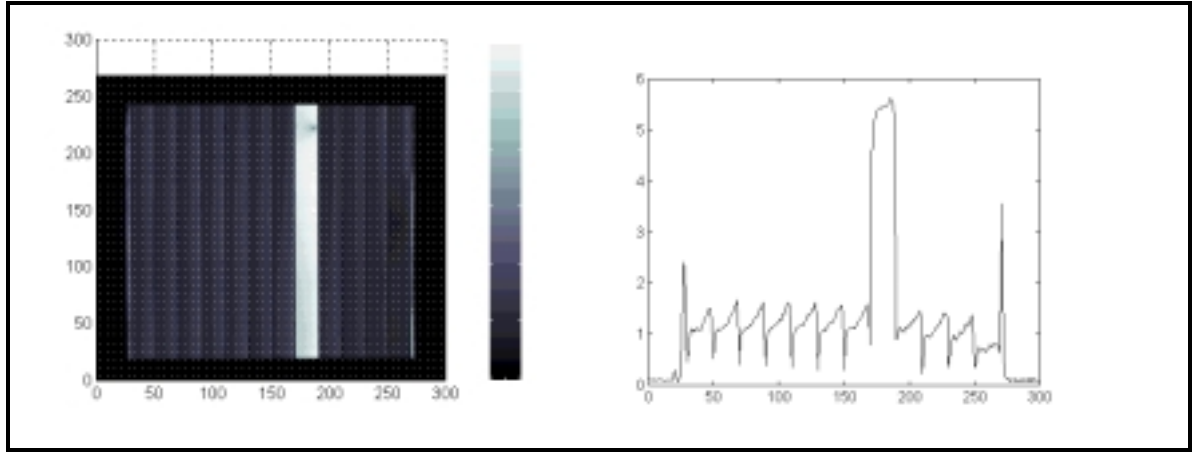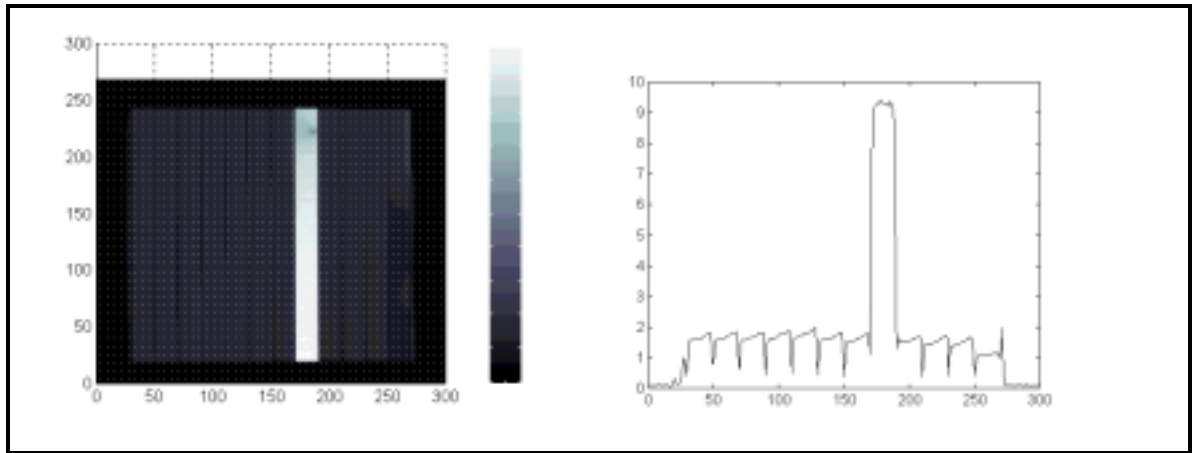
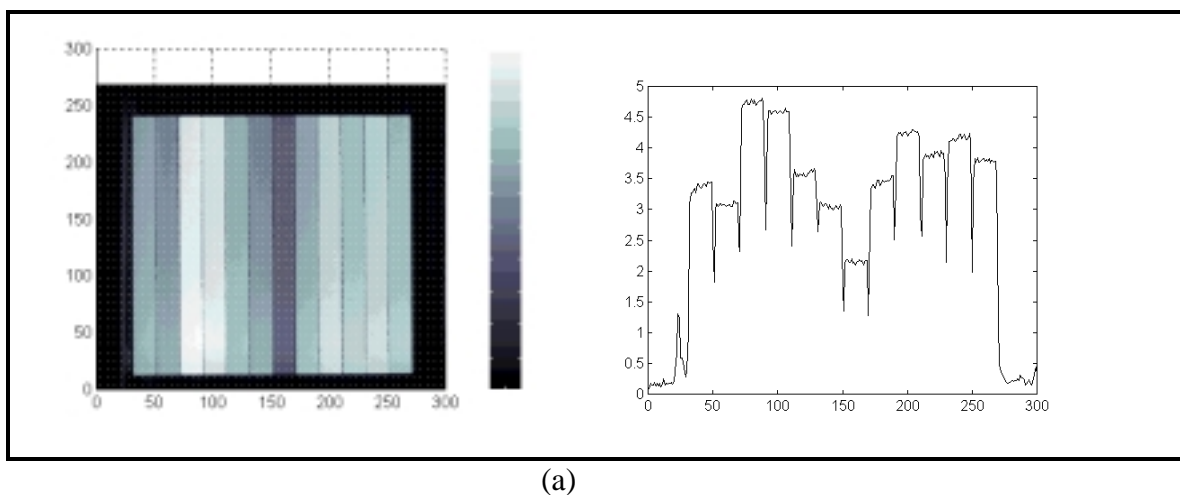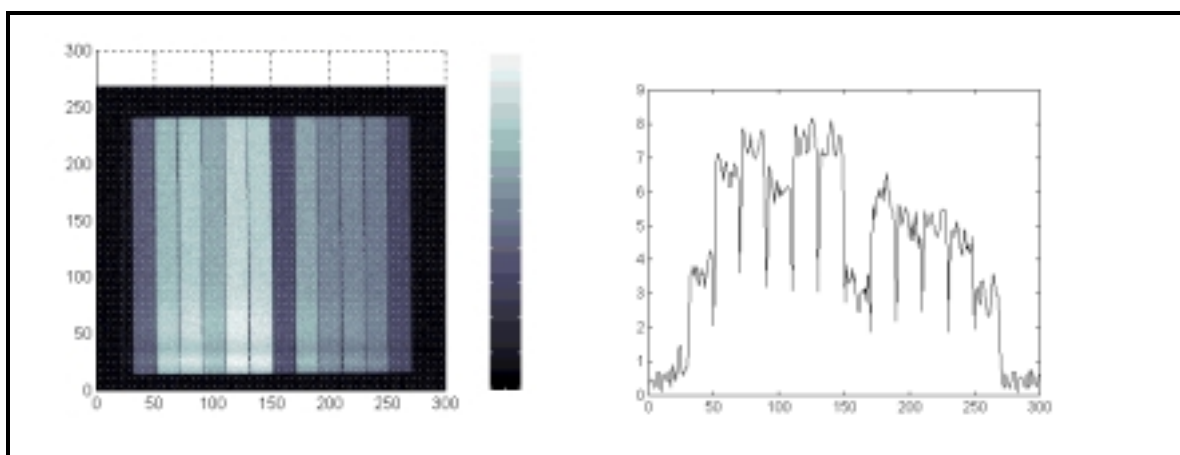time constant used.

(a)

(b)

(c)

(d)

(e)

Figure 5.5 *Laser scanning results for the CIGS prototype mini-module CB515 in different bias conditions. (a) Measurement without any bias in dark in short circuit. In the side view on the vertical scale 10 corresponds to 100 μV. (b) Measurement with full intensity light bias. In the side view on the vertical scale 10 corresponds to 300 μV. (c) Measurement with half intensity light bias. In the side view on the vertical scale 10 corresponds to 300 μV. (d) Measurement with a forward current bias of 30 mA (corresponding bias voltage 6 V). In the side view on the vertical scale 10 corresponds to 300 μV. (e) Measurement with a forward current bias of 10 mA (corresponding bias voltage 4 V). In the side view on the vertical scale 10 corresponds to 300 μV.*
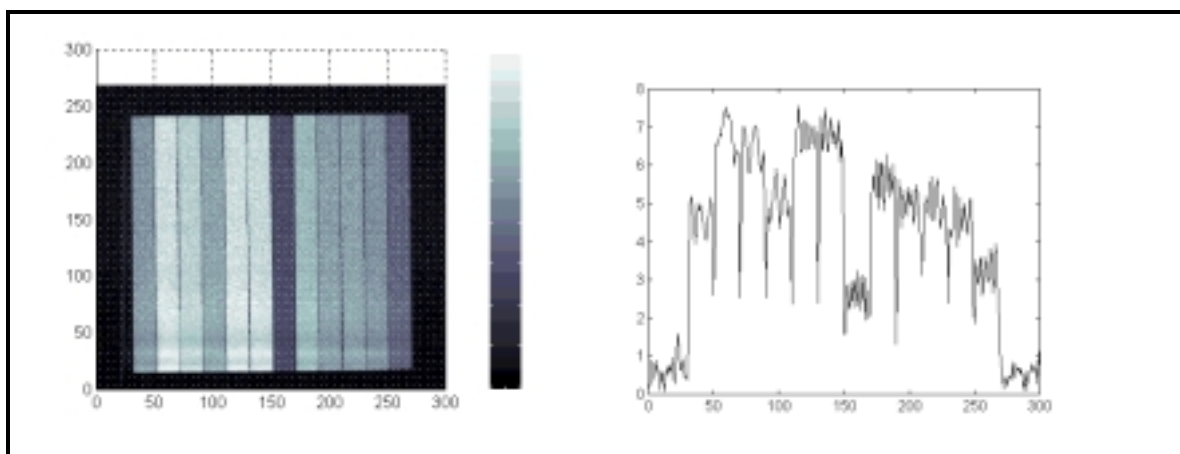
(a)

(b)

(c)

(d)

(e)

Figure 5.6 *Laser scanning results of CIGS prototype mini-module CB518 with different bias conditions. (a) Measurement without any bias in dark in short circuit. In the side view on the vertical scale 10 corresponds to 100 µV. (b) Measurement with full intensity light bias. In the side view on the vertical scale 10 corresponds to 100 µV. (c) Measurement with half intensity light bias. In the side view on the vertical scale 10 corresponds to 100 µV. (d) Measurement with a forward current bias of 30 mA (corresponding bias voltage 6 V). In the side view on the vertical scale 10 corresponds to 100 µV. (e) Measurement with a forward current bias of 10 mA (corresponding bias voltage 4 V). In t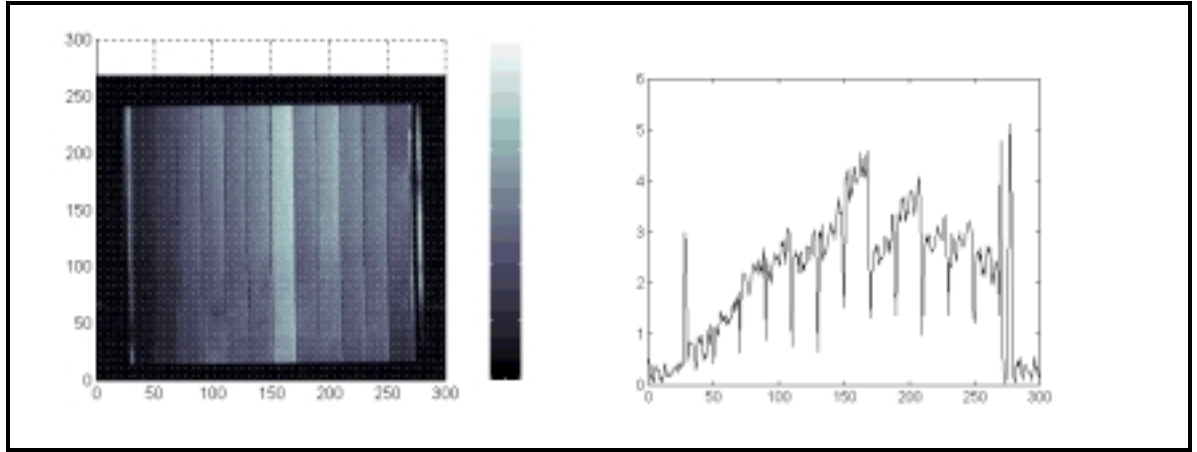he s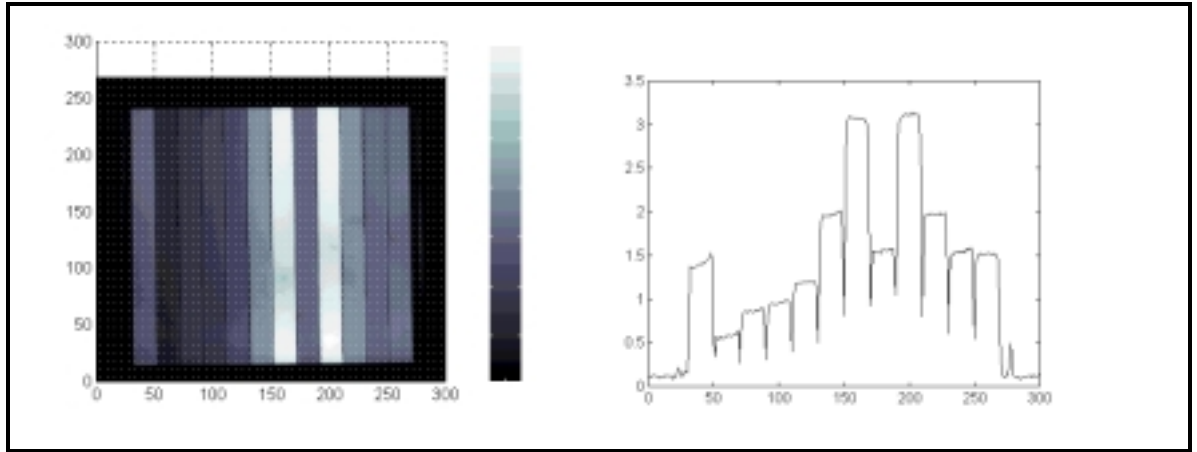ide view on the vertical scale 10 corresponds to 300 µV. Measurement results in (b), (c) and (d) show noise due to incorrect noise filtering when too low time constant was used.*

5.3.3 Discussion on bias dependency of laser scanning measurements

In the amorphous silicon module measured with laser scanning at different bias conditions, with low or no bias all the cells produce quite even photocurrent values. With full intensity bias light and with a high, 100 mA forward current bias in dark the

photocurrent map shows uniform values for most of the cells in the module. Only the ninth and the last cell in the module have much higher responses compared to the other cells. With low bias these cells have lower or about the same response as compared to the other cells in the module. When comparing the responses between high light intensity and high forward current or low light intensity and low forward current biases, the only difference observed is the photodiode behavior of the photovoltaic module shifting up the overall response level.

When the two CdTe modules were measured with laser scanning at different bias conditions, the results differ somewhat from those observed in the amorphous silicon module. In case of the CdTe modules at short circuit, the first module has two cells that show especially low response. The second module shows low response for every other cell in the module. With light bias there were no changes to these results, the same cells show low response than when measured in short circuit. Only when forward current bias is applied the response changes for both of the CdTe modules. In the forward current bias case the cells showing the lowest response at short circuit and with light bias, turn to show the highest responses in the modules. When applying different values of forward current biases, the first CdTe module shows quite noisy response at current values of 100 mA and 50 mA and also the overall signal response level was lower for these current values than observed with the other bias conditions. In case of the second CdTe module, the response was noisy for 100 mA forward current bias application and also in this case the overall response level was lower than for the other bias condition cases. Thus for CdTe modules the optimal forward current bias level was 30 mA.

The laser scanning results for the two CIGS modules at different bias conditions are similar to the CdTe module scanning results. In the first CIGS module there was one cell detected with especially low signal response in short circuit. This cell showed low response also with light bias conditions but with forward current bias its response was significantly higher than the response of the other cells in the module. A couple of other cells in this module showed medium level response in short circuit but high level response with light bias. However, this behavior was not consistent for all the cells showing medium level response in short circuit. A couple of cells showed medium response in short circuit but low responses in light bias conditions. In forward bias all the cells except one showed uniformly low response. The behavior of the second CIGS module in laser scanning under different bias conditions was even less consistent. However, also in this module there was one cell which showed low signal response in short circuit compared to the other cells in the module. The same cell showed low response with light bias conditions as well. With 30 mA forward current bias the cell response was somewhat higher and with 10 mA forward current bias significantly higher compared to the responses of the other cells in the module. With the application of 10 mA forward current bias there was also another cell, which showed higher response than the other cells in the module. However, this cell showed with other bias conditions average response compared to the other cells.

There are several references that discuss the results of laser scanning photovoltaic cells and modules with different bias conditions [35], [31], [36], [33], [177]. Under short circuit conditions, the laser scanning signal from each cell in the module is roughly proportional to the shunt resistance of that cell. The shunted cell IV curve has a much steeper slope and therefore much lower impedance than the other cells in the module. Therefore, severely shunted cells, and often moderately shunted ones, yield virtually no laser scanning signal in comparison with the good cells. However, the low or no laser scanning signal can also be due to a photocurrent defect in the cell instead of the cell being shunted. Thus it is difficult to draw a conclusion from laser scanning measurement results done in short circuit condition whether a low signal response in some cells in the module is due to low photocurrent or shunting.

When applying forward bias to the cells in the photovoltaic module it is possible to differentiate the shunted cells from the low photocurrent ones. Severely shunted cells show a laser scanning signal that increases in height relative to other cells in the module as forward bias increases, whereas a cell that produces no photocurrent would show no signal in either short circuit or forward bias.[31], [36]. This is explained as follows. At low forward current, the good and shunted cell IV curves have comparable slopes, and therefore comparable laser scanning responses. As forward current increases and the current of the good cells increases exponentially, the impedance of the leaky cells, dominated by shunting, stays the same. At some forward currents the impedance of the leaky cells may be larger than that of the good cells. Thus, at higher forward current, the good cell IV curve has a steeper slope and therefore the smaller laser scanning signal and the leaky cells give a larger relative laser scanning signal at these currents.[35], [31], [36].

As forward bias, either light bias or external forward current or voltage bias can be used. In this work light bias and external forward current bias were used. Laser scanning results should not depend on what kind of forward bias was used if only qualitative results are required such as in this work.[172]. However, care should be taken if light bias is used, that the bias illumination is spatially uniform over the module measured. Otherwise there is a risk that the laser scanning photocurrent map is representing the bias illumination uniformity rather than module performance.[32], [36]. Also, if external forward bias current or voltage is used, the bias voltage should be increased only until the signal from the cell under examination is comparable to the signal from good cells in the module. If the forward bias is increased too far, the current through the shunted cell will not be mostly shunted current.[35]. When measuring CdTe cells and modules it should be noted that CdTe cells show a significant dependence of shunt resistance on cell illumination history. For accurate results, measurements should be made in as short a period of time as possible, and no changes in position or illumination of the module should occur during the measurement.[31], [36].

For the modules measured in this work three different bias conditions were used. The results of the laser scanning measurements of the a-Si module correlate well with the

expectation from the literature [31]. When comparing photocurrent maps when measured in short circuit and forward bias conditions, the forward bias conditions of 100 mA bias current and light bias reveal two cells with exceptionally high response. The same cells had lower than average response in short circuit. Thus these two cells can be suspected to be shunted cells. A forward bias current of 50 mA or half intensity light bias do not show significant increase in the response of these two cells compared to the response in short circuit. Thus the forward bias level in these two bias conditions was not enough for the amorphous silicon module measured to reveal the two shunted cells. For the a-Si module there does not seem to be any difference in the results, whether light bias or external forward current bias was used. Also, since the photocurrent maps with light bias and forward current bias show similar phtocurrent values for all the cells in the module, it can be suspected that the illumination used for the light bias was spatially uniform.

In case of the CdTe modules laser scanned the results do not correlate with literature as well as in the case of a-Si module. In both of the two modules measured some shunted cells can be detected. However, the shunted cells are this time only detected when comparing the photocurrent maps after scans in short circuit and external forward current bias conditions. When light bias is used the resulting photocurrent maps are similar to the photocurrent map in short circuit. Thus the illumination does not seem to affect at all the laser scanning measurement results for CdTe modules. When 100 mA and 50 mA external forward current bias are used the response level is evened out for all the cells in the first CdTe module. For the second CdTe module the response evened out when 100 mA forward current bias was used. In those measurements a lot of noise was present. Thus for the first CdTe module 100 mA and 50 mA forward current bias seems to be too high and for the second CdTe module 100 mA forward current bias is too high to show the shunted current of those modules. Only when 30 mA forward current bias was used for the first CdTe module and 30 mA and 50 mA forward current bias was used for the second CdTe module, the cells showing low response in short circuit and with light bias, had an increased, above average signal responses. According to literature [31], these cells are suspected to be shunted.

The laser scanning results for CIGS modules are similar to the results for the CdTe modules. In the first CIGS measured there was one cell showing particularly low photocurrent response when measured in short circuit. In the second CIGS module there was also one cell showing lower than average response in short circuit when compared with the cells in the module. In both of these cases the application of light bias did not seem to affect the photocurrent responses of these cells. Only after application of forward current bias did the responses of these cells increase significantly when compared with the other cells in the modules and the cells could be concluded to be shunted cells. However, both of the CIGS modules contained cells that did not seem to behave according to this rule. In both modules there were some cells that showed average response in short circuit. In the first module these particular cells showed lower

than average responses when applying light bias. In the second module these cells showed lower than average responses when forward current bias was applied. Not all the average response cells behaved this way in either of the modules. Thus, there might be some unexplained differences in the cell behavior under different bias conditions probably depending on the material and manufacturing quality of the cell. Similar to the CdTe modules, the 30 mA forward current bias was too high for the second CIGS module. The response was evened out for all the cells in the module and the line scan was very noisy. For the first CIGS module this problem was not detected in any bias conditions. The first CIGS module, when measured in forward current bias, all the other cells in the module except the shunted cell, showed some signal increase towards the right cell edge. This effect is described in literature [33], [36] and it suggested to be due to too high beam power. According to [33] the beam power at which this effect becomes significant depends on the characteristics of the module being measured. In this work, however, this problem did not affect the qualitative results of the laser scanning.

As a conclusion it can be said that by comparing the laser scanning results done in short circuit with those done in forward bias conditions the shunted cells in thin film photovoltaic modules can be detected. For amorphous silicon module the shunted cells can be detected by using either illumination or external forward current bias as the source of forward bias. In case of CdTe and CIGS modules, light bias did not reveal the shunted cells but rather it was necessary to use forward current bias conditions. The modules were also quite sensitive to too high forward current bias and thus the proper level has to be experimentally verified before drawing conclusions of the results. The right forward current bias level also varied from one module to the other even if they were of the same thin film technology.

5.4   Laser scanning with blue laser

5.4.1   Measurement set-up and sample description

The laser scanning measurement set-up in the blue laser scan was otherwise the same as in the red laser scan (Figure 5.1) except that blue laser was used. The blue laser was a Helium-Cadmium laser with a wavelength of 442 nm. The laser light was taken via an optical fiber to the lens system and the chopper. The optical fiber however diverges the beam and thus it was converged with help of two lenses. The specified beam diameter was 0.290 mm but because of the divergence caused by the optical fiber the actual beam area on the specimen can be estimated to be about 6 – 8 mm^2. The specified typical output power of the beam was 23 mW but the actual power on specimen is much less because of the absorption of power by the optical fiber.   All the measurements were done in dark in short circuit. Also light bias and forward current bias was tried but the response was only noise and a proper photocurrent signal induced by the laser light could not be detected. The distance between the laser tower and the specimen was smaller than for the red laser light scans described in the previous chapters. Thus the resulting photocurrent maps have slightly different dimensions than the photocurrent maps resulting from the red laser scans. The resolution was kept the same as for the red laser scans. Due to alignment difficulties with the blue laser, the resulting photocurrent maps do not show the outlines of the modules for all the samples. However all the cells in the modules scanned should be present in the resulting photocurrent map. Thus the photocurrent maps scanned with the blue laser should be comparable with the photocurrent maps scanned with the red laser for the same modules.

One a-Si module AB510, two CdTe prototype modules ZB503 and ZB509, and two CIGS prototype mini-modules CB518 and CB515 were scanned. The modules were the same than those scanned with the red laser with different bias conditions of which the results were presented in Chapter 5.2 above. The module specifications were listed in Table 5.I above.

5.4.2   Results

a-Si

The laser scanning result of a-Si module AB510 when blue laser was used is shown in Figure 5.7 below. The scan was done in dark in short circuit. The resulting photocurrent map is very even, only for the 9th and the last cells from the left the signal response is low compared with the responses for the other cells in the module. When comparing these results with the red laser scanning results, the resulting photocurrent map with the blue laser in short circuit is much more even than the photocurrent map resulting from the scan with the red laser in short circuit. However, the 9th and last cells from the left that show low response when scanned with the blue laser are the same cells that showed high response when scanned with the red laser when compared with the responses of the other cells in the module. It should be noted that the response overall is lower when scanned with the blue laser than with the red laser. In the results on the vertical scale 10 for the scan in short circuit with red laser corresponds to 30 µV compared with the results with the blue laser in which on the vertical scale 10 corresponds to 10 µV.
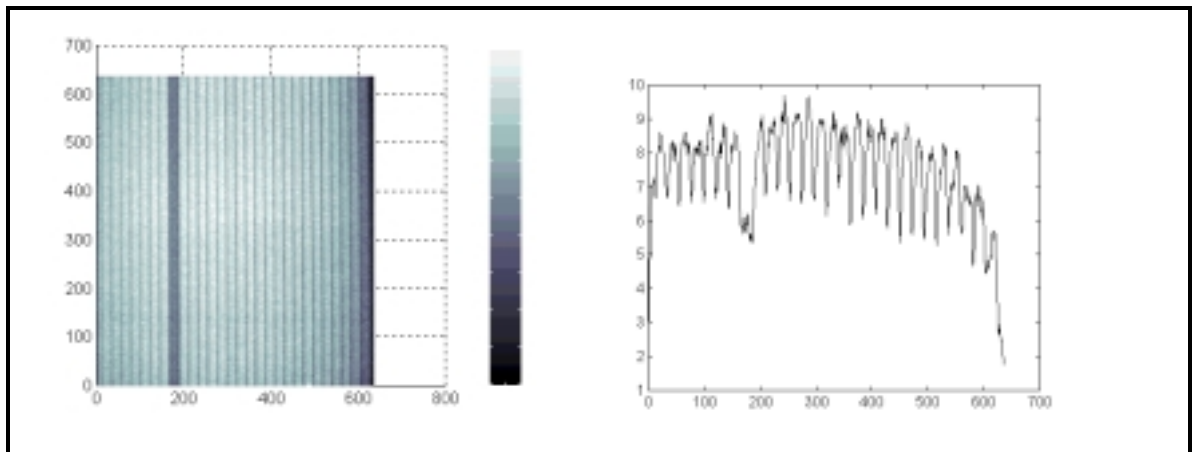

Figure 5.7   *Photocurrent map of a-Si module AB510 when laser scanned with blue laser in short circuit. In the side view on the vertical scale 10 corresponds to 10 µV. A time constant of 400 ms was used.*

CdTe

The laser scanning results for CdTe prototype modules ZB503 and ZB509 when scanned with blue laser are presented in Figures 5.8 and 5.9 below. Both scans were done in dark in short circuit only. In Figure 5.8 the photocurrent map for the module ZB503 is shown. The signal is not very clear and thus the cell lines are not well visible for all the cells in the module in the vertical view. However when both vertical and planar views are looked at there is a clear trend that the fist half of the module when starting from the left is performing less than the second half of the module. Especially low performance when compared with other cells in the module can be observed in the 2nd, 14th and 17th cells from the left and on the 7th and 11th cells from the right. When comparing these results with the results from the scan of the same module with red laser in dark in short circuit, it can be noticed that the photocurrent maps of the two scans look very alike. Also the cells with a low response when scanned with blue laser also have a low response when scanned with red laser compared with the responses of the other cells in the module. The only difference is that for the scan with the blue laser a lot more noise is present. Also the overall response is much lower with the blue laser than with the red laser. In the vertical scale photocurrent map for the blue laser 10 corresponds to 10 μV as compared with the photocurrent map scanned with red laser in short circuit on the vertical scale 10 corresponds to 100 μV.

The photocurrent map for CdTe prototype module ZB509 when scanned with blue laser in short circuit is shown in Figure 5.9 below. There is a lot of noise in the resulting photocurrent map. However it can be seen that every other cell is performing well and every other one has a low performance when compared with each other. The 1st cell from the left and 3rd and 5th cells from the right have the highest performances. All the low performance cells have equally low performances. This result is the same when compared with the scanning results with the red laser in short circuit when the same module was scanned. In the resulting photocurrent map from the measurements with red laser also every other cell is performing well and every other one has a low photocurrent response. Also exactly the same cells have the highest responses when compared with the results of blue laser scan. The results with the red laser scan are overall of higher photocurrent response. On the vertical scale in the results for the red laser scan 10 corresponds to 100 μV as it corresponds in the results for the blue laser scan 10 μV.
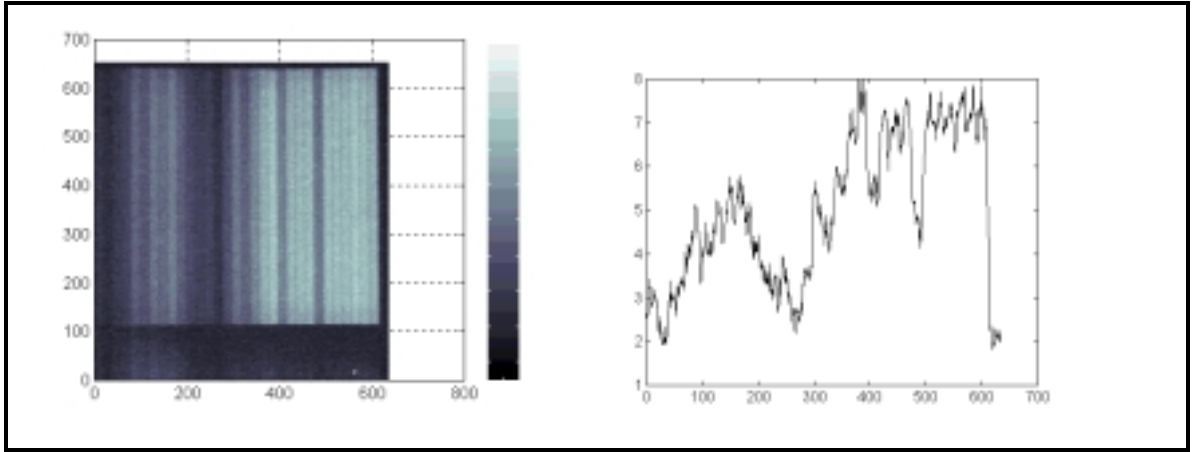
Figure 5.8 *Photocurrent map of CdTe prototype module ZB503 when laser scanned with blue laser in short circuit. In the side view on the vertical scale 10 corresponds to 10 μV. The photocurrent signal contained a lot of noise even if the time constant was as long as 400 ms.*
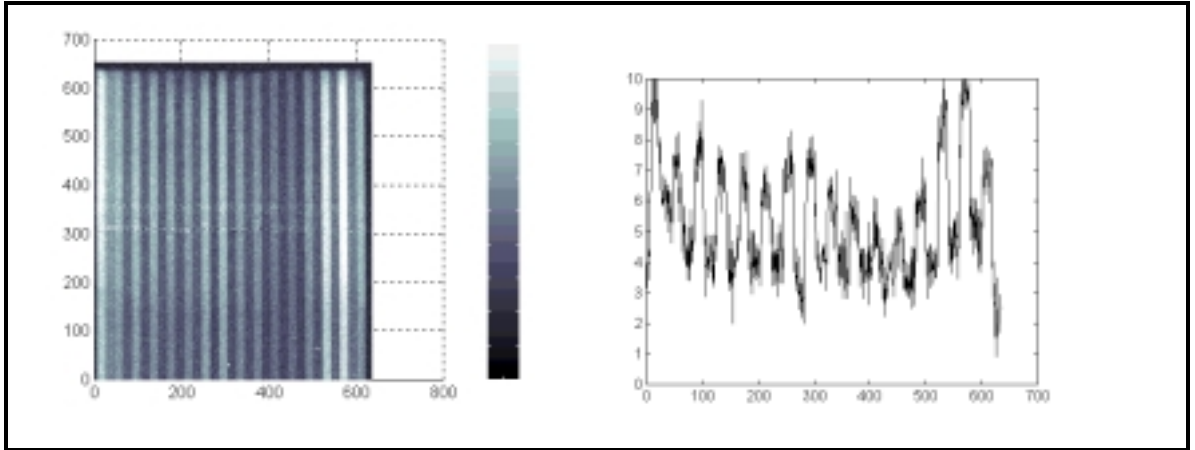

Figure 5.9 *Photocurrent map of CdTe prototype module ZB509 when laser scanned with blue laser in short circuit. In the side view on the vertical scale 10 corresponds to 10 μV. 125 ms time constant was used.*

CIGS

The laser scanning results for CIGS prototype mini-modules CB515 and CB518 when scanned with blue laser are presented in Figures 5.10 and 5.11 below. The resulting photocurrent map of CB515 when scanned with blue laser is shown in Figure 5.10 below. The cell lines are not very well visible in the vertical or side view because the signal contains a lot of noise but on the planar view they are well shown and thus can be estimated also for the side view. There are four clear performance peaks. The 1st and 3rd cells from the left and the 3rd and 7th cells from the right have clearly higher response when compared with the other cells in the module. The other cells are performing with a very low response in comparison. Unlike for a-Si and CdTe modules, when the performance of the CIGS module scanned with blue laser is compared with the

performance of the same module scanned with red laser the resulting photocurrent response maps look totally different. The only similarity is that the highest responses induced by blue and red laser lights are of about the same intensity since on the vertical scale in both cases 10 corresponds to 100 μV. All the peaks that show on the photocurrent map induced by the blue laser light do not exist as particular peaks on the photocurrent map resulting from the scan with red laser. Only the 5th cell from the right has in both cases a very low performance when compared to the other cells in the mini-module.

The photocurrent map of CB518 when scanned with the blue laser is shown in Figure 5.11 below. Like for CB515, the cell lines are not very well visible in the vertical or side view because the signal contains a lot of noise but on the planar view they are well shown and thus can be estimated also for the side view. There are four clear performance peaks situated at the responses from the 1st, 2nd, 3rd and 5th cells from the left and at the 3rd cell from the right when the performance is compared with the other cells in the mini-module. The other cells in the module have equally low performance. When the resulting photocurrent map from the blue laser scan is compared with the photocurrent map resulting from the red laser scan in short circuit for the same module, no similarities can be found. Only the 6th cell from the right has a low performance in both scans. Overall the signal is slightly lower in the scan with blue laser since on the vertical scale of the resulting photocurrent map 10 corresponds to 30 μV when it in the photocurrent map for the red laser scan corresponds to 100 μV.

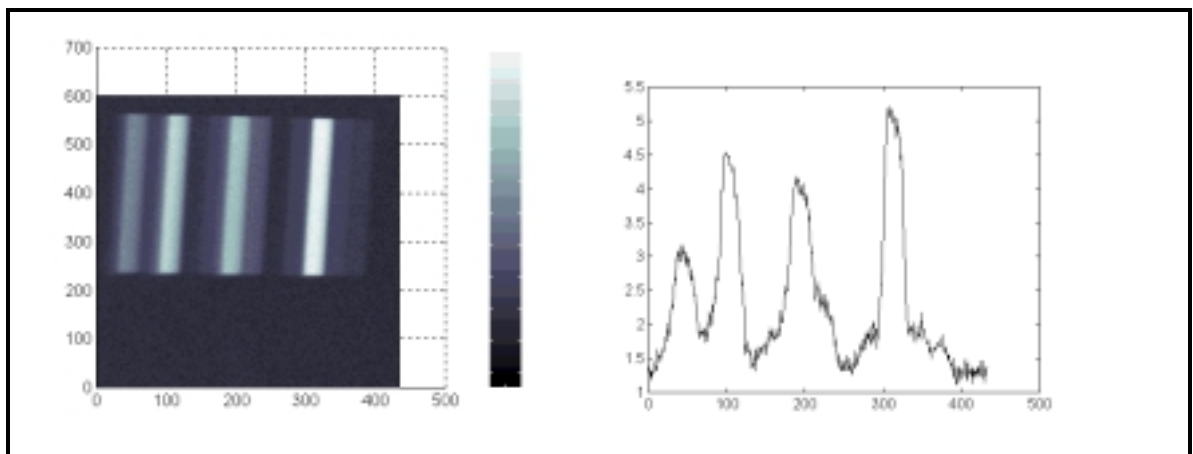

Figure 5.10 *Photocurrent map of CIGS prototype mini-module CB515 when laser scanned with blue laser in short circuit. In the side view on the vertical scale 10 corresponds to 100 μV. A time constant of 40 m was used.*

Figure 5.11 *Photocurrent map of CIGS prototype mini-module CB518 when laser scanned with blue laser in short circuit. In the side view on the vertical scale 10 corresponds to 30 μV. A time constant of 40 m was used.*
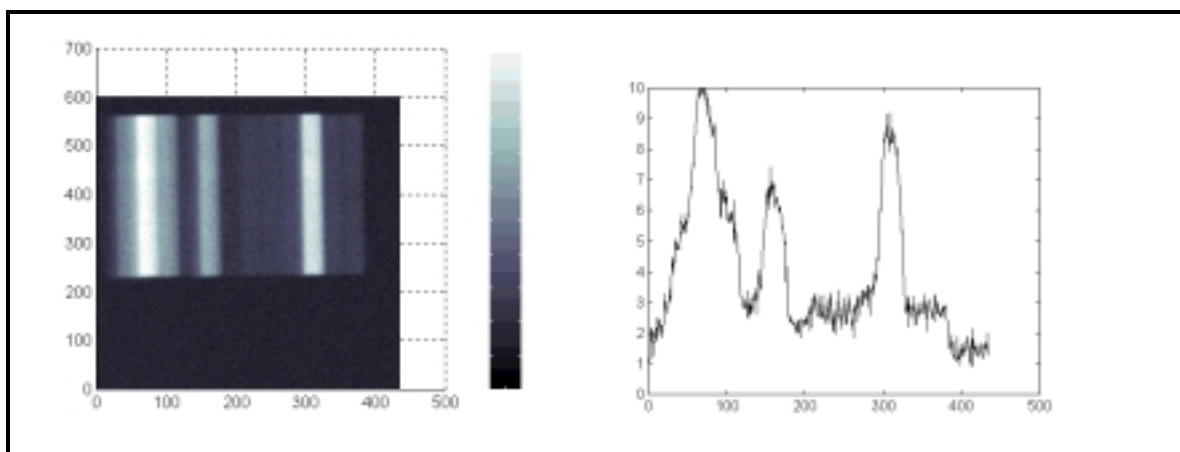
5.4.3 Discussion on blue laser scanning

The results of laser scanning with blue laser is in case of the amorphous silicon module in principle a negation when compared with the results after scanning with the red laser in forward bias conditions. There are two cells, which show lower than average response. These two cells are exactly the same cells, which showed higher than average response when scanned with red laser in forward bias conditions. When comparing the results for the CdTe modules, the photocurrent map measured with blue laser resembles those measured with red laser in short circuit and light bias conditions. For the first CdTe module, the left half of the module shows lower response than the right half of the module. There are also certain cells in the modules, which show especially low response. These cells are the same that showed low response when scanned with red laser in short circuit and with light bias. For the second CdTe module, the photocurrent map shows low response values for every other cell in the module. These cells are the same that showed low response when scanned with red laser in short circuit and with light bias conditions. In case of CIGS modules, the photocurrent maps measured with blue laser and those measured with red laser show very few similarities. For the first CIGS module, there are four cells that show high response while the other cells in the module show exceptionally low response. The only correlation with the red laser scanning results is, that the cell that showed very low response when scanned with red laser at short circuit and with light bias shows very low response also when scanned with blue laser in short circuit. The second CIGS module has five cells that show average or above average response when scanned with the blue laser while the other cells in the module show very low response. The one cell that showed in red laser scan in short circuit and with light bias lower than average response does also show low response when scanned with blue laser.

The different laser wavelengths excite different layers in the photovoltaic thin film

modules. For example in CIGS modules blue laser should probe the CdS layer of the device structure [32]. In literature there exist references of the use of blue laser in laser scanning experiments only for CIGS material thin film photovoltaic modules [32], [34], [36]. The blue laser measurements of CIGS samples have mainly served the research of the red light distortion phenomenon in CIGS material samples [34].

Since the penetration depth of the blue laser light is different than the penetration depth of red laser light, and in CIGS modules the blue laser light excites electrons mainly in the CdS layer, the photocurrent maps measured with blue laser can be said to represent the performance of the CdS layer in the modules. The same reasoning can be extended to the CdTe modules. However, on the contrary to the case of CIGS modules, the CdTe modules show approximately the same response when scanned with red and blue laser. Blue laser light affects the CdTe module thin film layers the same way as red laser light and thus no red light distortion or blue light enhanced improvements in the cell performance can be expected from the CdTe modules. Since the photocurrent response maps for the CIGS modules when scanned with red and blue laser differ so much from each other, some red light distortion effect can be expected to be present in the IV curves of these two modules. In the case of the amorphous silicon module, it is very interesting to note the contradictor behavior with red and blue laser scans. It might be concluded, that the blue laser scan in short circuit reveals the shunted cells as well as light or forward current biased red laser scans in a-Si modules. However, instead of increasing the photocurrent output of the shunted cells, when scanned with blue laser the shunted cells show lower than average photocurrent output. The phenomenon observed when scanning a-Si, CdTe and CIGS modules with blue laser are not however further investigated since it is out of the scope of this work. It is concluded that using the blue laser does not reveal any key information necessary for the conclusions within the scope of this work.

5.5 Laser scanning as a tool to investigate accelerated lifetime testing results

5.5.1 Measurement set-up and sample description

The measurement set-up for laser scanning of thin film photovoltaic modules after damp heat testing was the same as described in previous chapters. The set-ups shown if Figure 5.1 above. All the scans were done using red laser beam only.

The amorphous silicon, CdTe and CIGS samples that were laser scanned after damp heat testing are listed in Table 5.II below. As indicated in Table 5.II the a-Si module had participated both the first and second round of damp heat testing as thus gone through totally 2000 hours of damp heat. The CIGS sample has gone through 1000 hours in the second set of damp heat testing. The CdTe prototype module ZB502 participated the first round and the CdTe prototype module ZB511 the second round of damp heat testing both being tested totally for 1000 hours in the damp heat.

Table 5.II *List of modules and samples that were laser scanned in various bias conditions after damp heat testing.*

ESTI ID	Thin film material	Module size	Module description	Test description
AB505	a-Si	1x1 ft^2	Framed glass-glass module	2000 hours of damp heat (1st and 2nd sets of testing)
CB509	CIGS	10x10 cm^2	Unframed glass-glass prototype mini-module	1000 hours of damp heat (2nd set of testing)
ZB502	CdTe	30x30 cm^2	Framed glass-glass prototype module	1000 hours of damp heat (1st set of testing)
ZB511	CdTe	30x30 cm^2	Framed glass-glass prototype module	1000 hours of damp heat (2nd set of testing)

5.5.2   Results

a-Si

The laser scanning results of a-Si module AB505 after 2000 hours of damp heat testing can be seen in Figure 5.12 below. In the photocurrent map resulting from the measurement in dark (Figure 5.12(a)) the 7th and 12th cell from the left and especially the 7th and 11th cell from the right have lower response compared to the other cells which have quite even response. When scanned with full intensity light bias (Figure 5.12(b)) the response is lower from the 4th to the 15th cell starting from the left compared to the other cells in the module. The 11th cell from the right has a high response compared to the other cells but the 7th cell from the right has still very low response. The overall response is however higher when measured with light bias than when measured in dark since the sensitivity in the former was 30 µV and in the later 100 µV. When measured with 40 mA forward current bias (Figure 5.12(c)) the response is in general very even for all the cells with a couple of exceptions. That is, the 7th and 12th cells from the left stand out somewhat from the other cells. The 7th cell from the right has a much higher response than the other cells in the module when measured with forward current bias, which is contrary to the results in dark and with light bias. The overall response is however lower with forward current bias than in dark or with light bias since the sensitivity used was only 10 µV.

When looking at the plane view photocurrent map there are only minor areas around the corners and on the edge areas where the response intensity is significantly reduced. On each corner there is a small area of no photocurrent as well as a half circle area along the left edge. However this area is invisible when measured with forward current bias because along that corner the photocurrent map shows a larger area of reduced response signal. Some dots of no photocurrent area can be also seen on the lower edge of the module. These no photocurrent areas show similarly on all the photocurrent maps measured with different biases. No other damp heat induced defects are visible on the photocurrent maps.
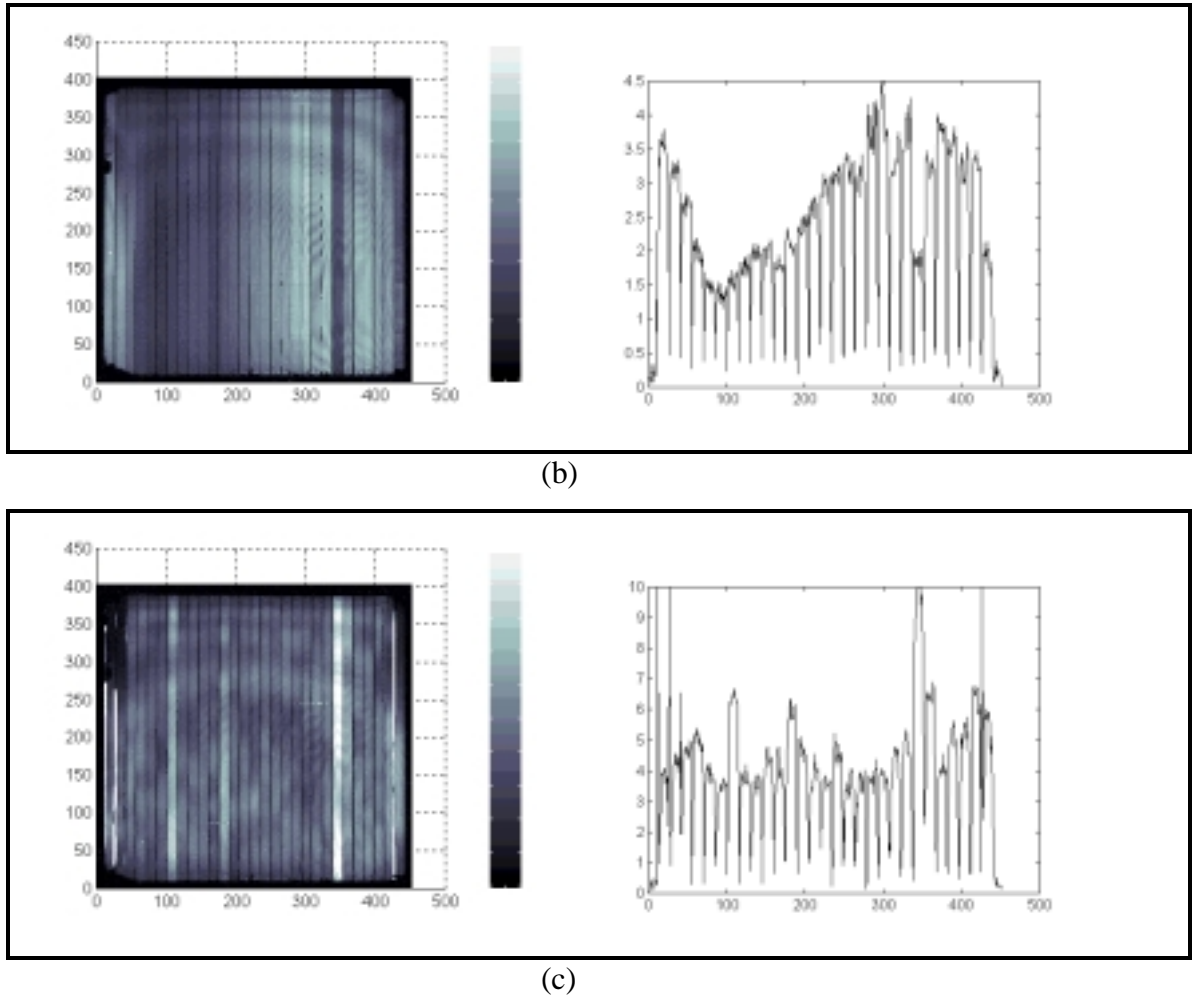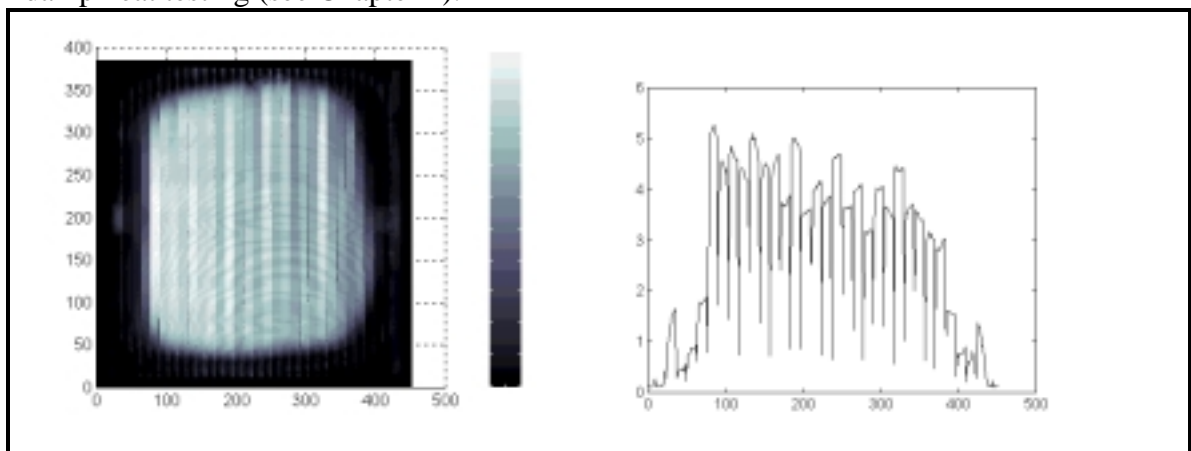

(a)

(b)

(c)
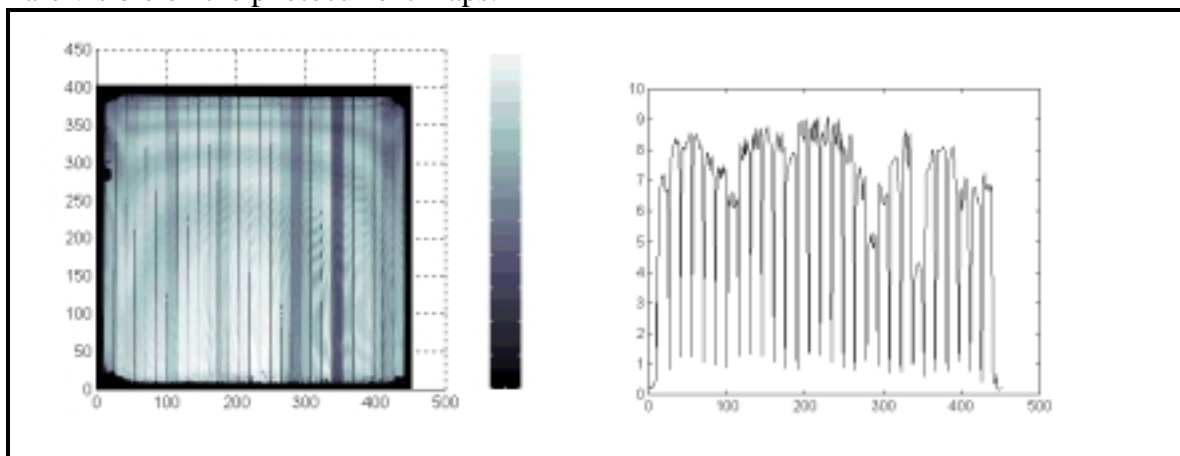
Figure 5.12 *Laser scanning results in various bias conditions of a-Si module AB505 after 2000 hours of damp heat testing. (a) Measurement in dark in short circuit. In the side view on the vertical scale 10 corresponds to 30 µV. (b) Measurement with full intensity light bias. In the side view on the vertical scale 10 corresponds to 100 µV. (c) Measurement with forward current bias of 40 mA (corresponding bias voltage 20 V). In the side view on the vertical scale 10 corresponds to 10 µV.*

CdTe

Laser scanning results for CdTe prototype module ZB502 and ZB511 after 1000 hours of damp heat exposure are presented in Figures 5.13 and 5.14 below when measured with different bias conditions. The measurement results for ZB502 in all the different bias conditions, that is in dark (Figure 5.13(a)), with full light intensity (Figure 5.13(b)) and with 150 mA forward current bias (Figure 5.13(c)), are very similar to each other. Overall the response is very even, only some minor signal height differences occur from cell to cell. Also all the tree measurement results are comparable since the sensitivity for all the measurements with different biases was 100 µV. As can be seen both from the plane and in the side views the module has in a circular pattern around the

edges no or very low photocurrent areas. These areas correspond with the visual defects areas observed after 1000 hours of damp heat testing in the module (see Chapter 4). The forward current bias had such a high value probably due to the low electrical performance of the module after damp heat testing.

The measurement results for ZB511 are very similar when scanned in dark (Figure 5.14(a)) and with full intensity light bias (Figure 5.14(b)). In both of these scans the resulting photocurrent map has quite varying signal responses. The photocurrent response is lowest towards both edges and the highest responses are around the middle of the module. The response is very low around the 7th cell, in the 18th cell and around 23rd cell as well as on the edges. When 40 mA forward current bias was used the overall response is somewhat evened out when compared with the results from the scans in dark and light bias but still some differences can be observed between the responses of the cells. Especially the cells that had low response in dark and with light bias have now higher responses but they still have lower responses compared with other cells in the module. The first and last cells continue to have the lowest responses. The results with all different bias conditions are comparable since they all had the same sensitivity value of 100 μV. The results in the plane view are also similar for all the different bias conditions used. Especially around the edge areas there are some low or no photocurrent areas. These areas correspond well with the visual defects observed in the module after damp heat testing (see Chapter 4).

(a)

(b)

(c)

Figure 5.13 *Laser scanning results in various bias conditions of CdTe prototype module ZB502 after 1000 h of damp heat testing. (a) Measurement in short circuit. In the side view on the vertical scale 10 corresponds to 100 μV. (b) Measurement with full intensity light bias. In the side view on the vertical scale 10 corresponds to 100 μV. (c) Measurement with forward current bias of 150 mA (corresponding bias voltage 7 V). In the side view on the vertical scale 10 corresponds to 100 μV.*
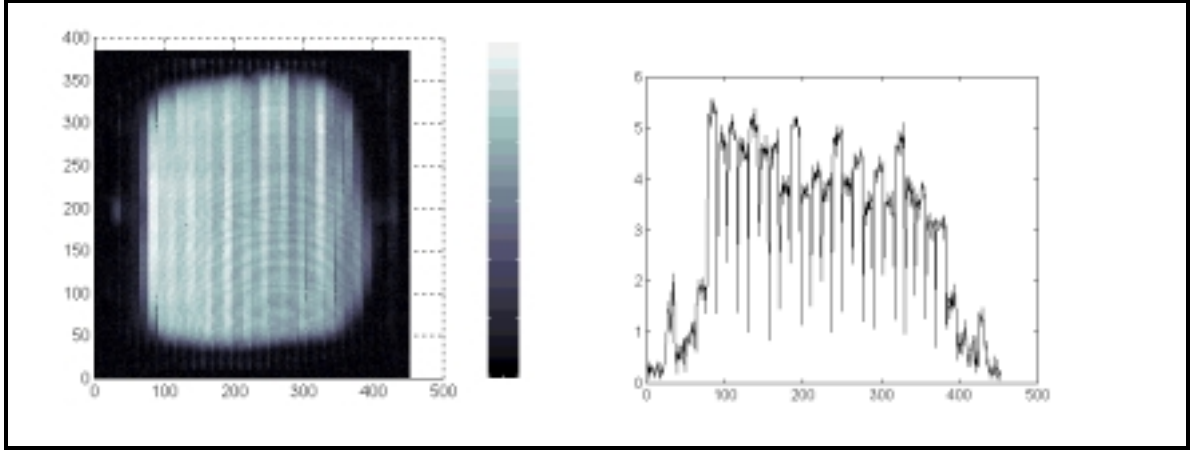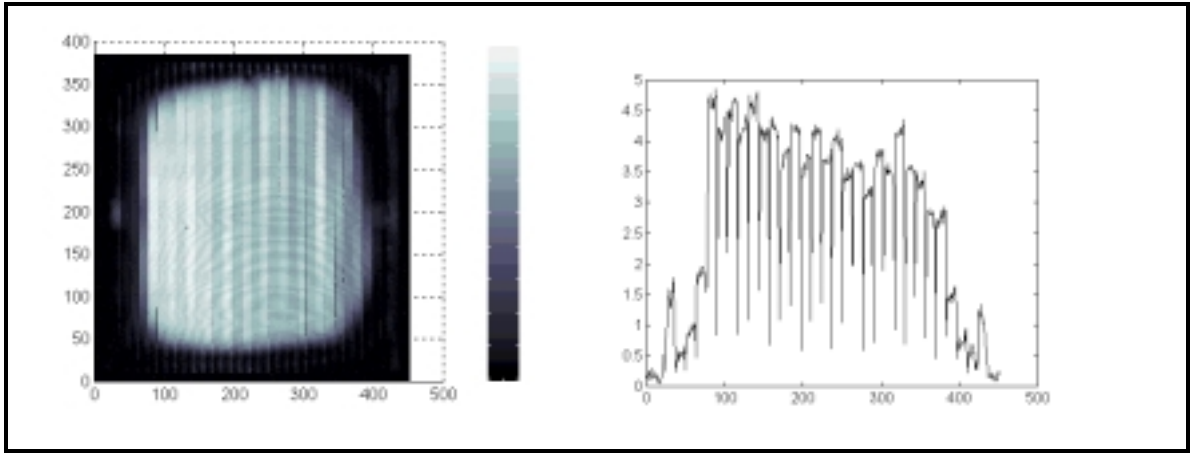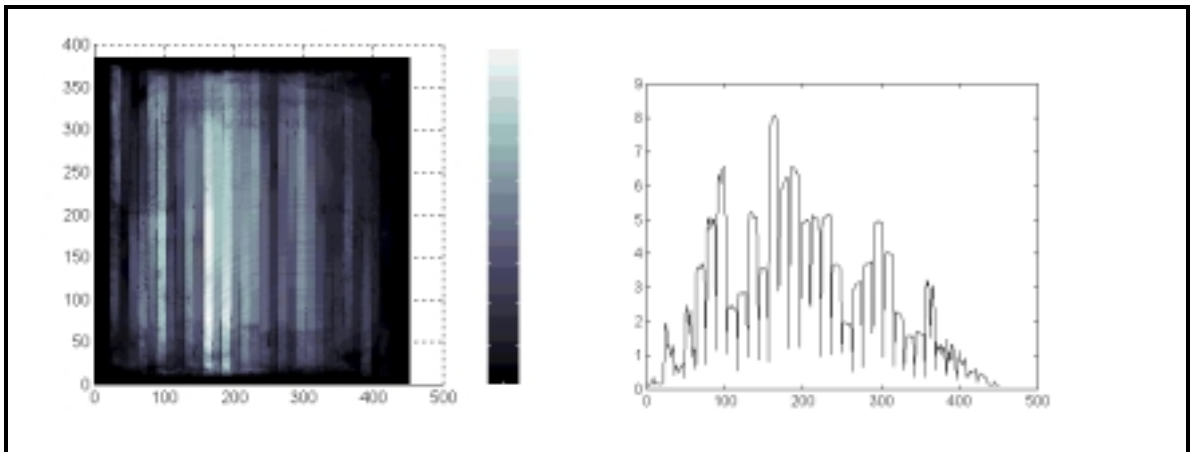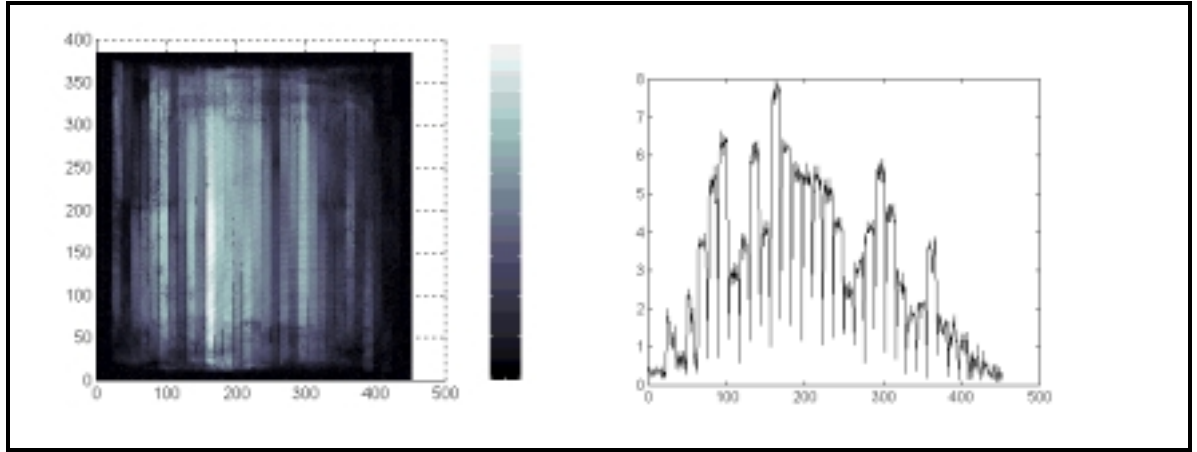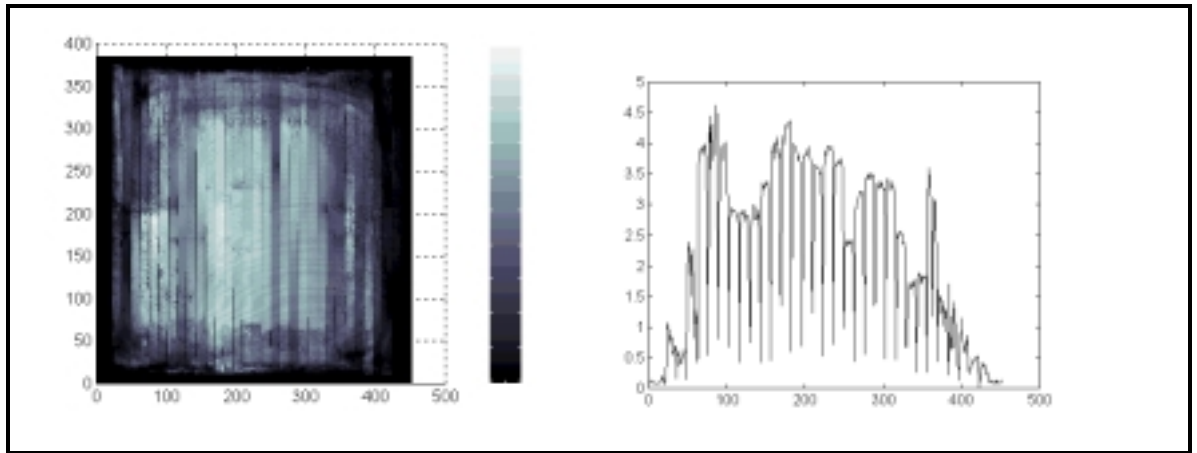

(a)

(b)

(c)

Figure 5.14 *Laser scanning results in various bias conditions of CdTe prototype module ZB511 after 1000 h of 2nd damp heat test. (a) Measurement in short circuit. In the side view on the vertical scale 10 corresponds to 100 µV. (b) Measurement with full intensity light bias. In the side view on the vertical scale 10 corresponds to 100 µV. (c) Measurement with a forward current bias of 40 mA (corresponding bias voltage 6 V). In the side view on the vertical scale 10 corresponds to 100 µV.*

CIGS

The laser scanning results for CIGS prototype mini-module CB509 after 1000 hours of damp heat testing are presented in Figure 5.15 below for various bias conditions. When measured in dark (Figure 5.15(a)) the cell lines for the two first and the two last cells in the sample are not well visible. The 3rd cell from the left has a low response and the 4th and the 6th cells from the left have somewhat higher response compared with the responses of the other cells. Otherwise the photocurrent responses seem quite even throughout the sample. When measured with full light bias (Figure 5.15(b)) the responses have evened out compared with the results of the scan in dark. Only the 1st and the 3rd cells from the left have low responses and the 2nd cell from the left have a

somewhat higher response when compared with the other cells. With light bias the cell lines are clearly visible between all the cells. The overall response is higher than when measured in dark since the sensitivity was 100 μV compared with 30 μV in the scan in dark. In the measurement result when scanned with 10 mA forward current bias (Figure 5.15(c)) the resulting photocurrent map is significantly different when compared to the photocurrent maps resulting from measurements with other bias conditions. The only cells having any photocurrent response are the first and the last cells in the sample. All the cells in the middle of the sample show no response at all. The sensitivity in this measurement was again 30 μV.

On the plane view the results of the scans of CB509 in different bias conditions are also very different depending on the scanning conditions. When measured in dark the response in the plane view is very even (Figure 5.15(a)). The white stripe across the middle of the module is probably a measurement artifact. In the plane view, when measured with light bias, the middle area of the module appears to have a somewhat higher photocurrent response than the edge areas (Figure 5.15(b)). In the measurement with forward current bias (Figure 5.15(c)) the edge areas have a higher response and the middle appears to be a circle without any or with very low photocurrent response. This corresponds well with the visual defect observed after 1000 hours of damp heat testing for this CIGS sample (see Chapter 4).
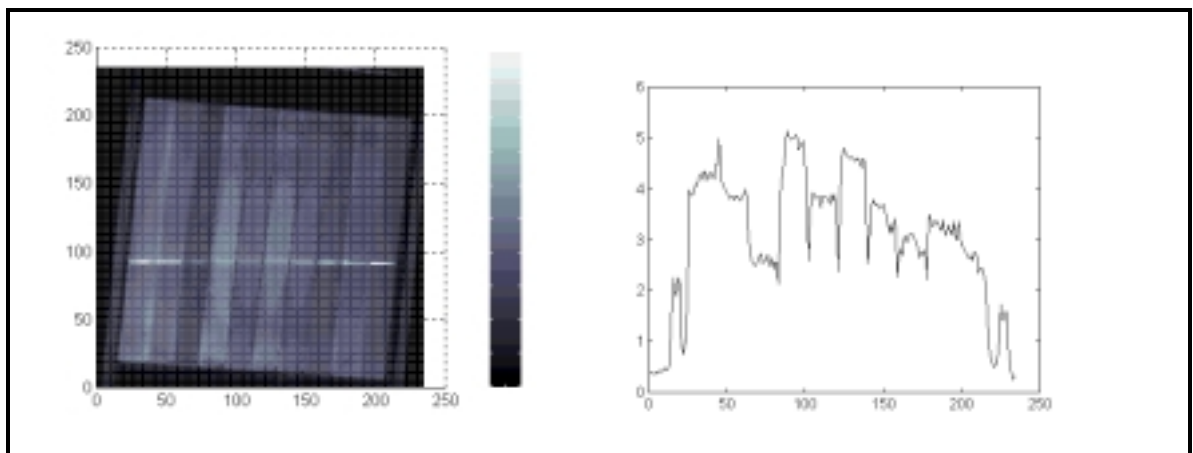

(a)
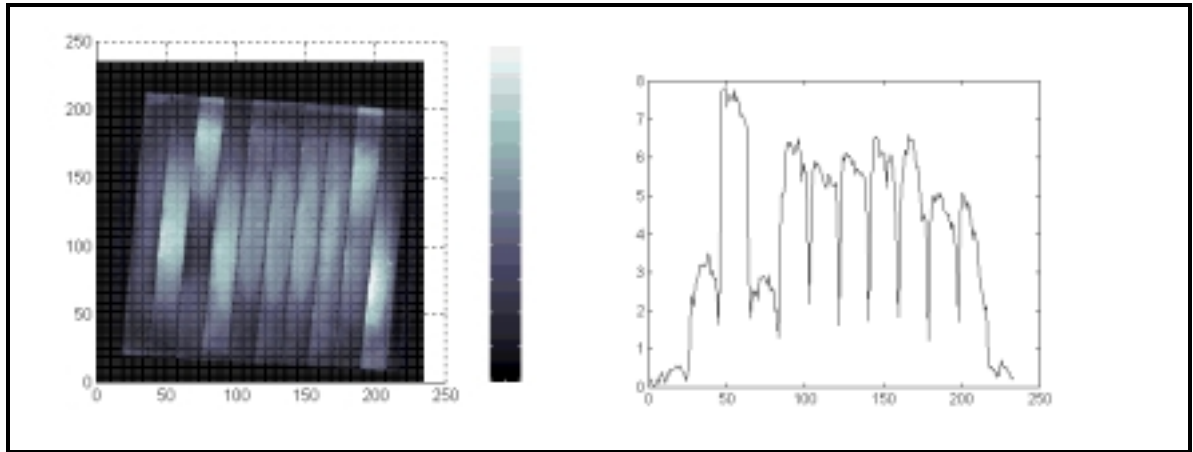
(b)
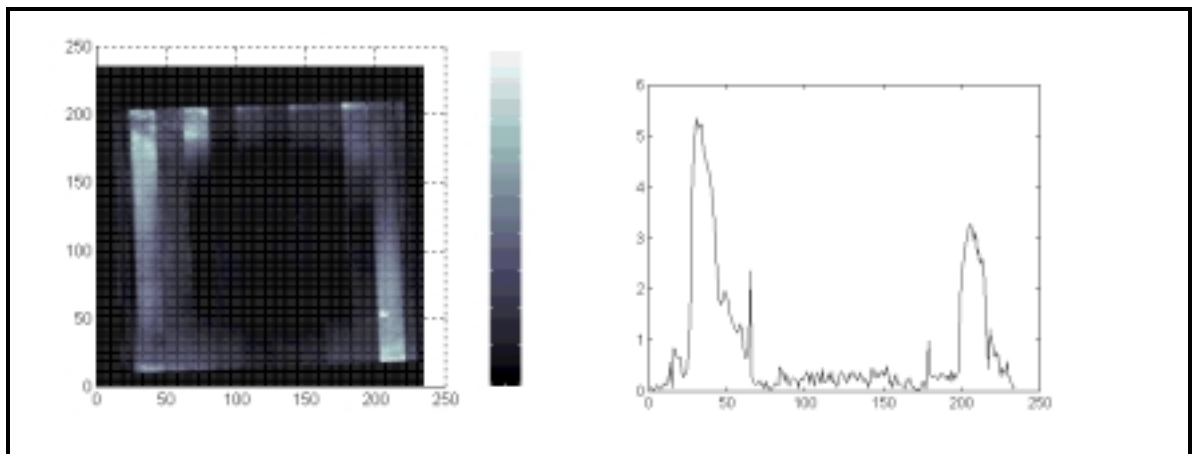
(c)

Figure 5.15 *Laser scanning results in various bias conditions of CIGS prototype mini-module CB509 after 1000 h of damp heat. (a) Measurement in short circuit. In the side view on the vertical scale 10 corresponds to 30μV. (b) Measurement with full intensity light bias.   In the side view on the vertical scale 10 corresponds to 100μV.   (c) Measurement with a forward current bias of 10mA (corresponding bias voltage 9V).   In the side view on the vertical scale 10 corresponds to 30μV.*

5.5.3   Discussion on laser scanning after accelerated lifetime testing

In the amorphous silicon module, when laser scanned with red laser after 2000 hours of damp heat testing, there was one cell in particular which showed lower than average response in short circuit and with light bias but high response in forward current bias. Two other cells in the module showed somewhat lower response in short circuit and with light bias and somewhat higher than average response with forward current bias when compared to the other cells in the module.   Another cell that had lower than average response in short circuit did not show any higher than average response in bias conditions. For the module scanned after damp heat it is especially interesting to note the plane view photocurrent map of the laser scanning results. In the plane view there are

dark or very low photocurrent areas visible around the corners of the module. Also some dark dots can be observed especially along the lower edge of the module. In the photocurrent map after scanning with forward current bias the dark area in the upper left corner has extended towards the middle of the module along the two first cells. Also some very high photocurrent areas are shown between the edge and the first and the first and the second cell as well as between the second last and the last cell.

In case of the CdTe modules, when laser scanned after 1000 hours of damp heat testing, the use of different bias conditions does not seem to give any differences in the resulting photocurrent maps in the first site. For the first CdTe module the line scan or side views of the photocurrent maps with different bias conditions do not show any changes when the bias conditions have been changed. Also the plane view photocurrent maps are very similar for the scans after different bias conditions. The side view showed very low response cells to be located on the sides of the module. The plane view shows that the very low response area is circularly shaped along the edges of the module. These very low photocurrent areas have low photocurrent response independent of the bias conditions used. It has to be noted that even though the edge area is of low photocurrent there are differences in the responses to be observed. There is practically no photocurrent in the upper left and in the two lower corners of the module. The other low photocurrent areas show some current. In the second CdTe module, when scanned after 1000 hours of damp heat testing, some minor changes can be observed when different bias conditions are used. In the line scan there are no major differences between the responses when different bias conditions are used. However, when in the plain view photocurrent map there are areas in some cells that show somewhat higher response when forward current bias is applied than in short circuit or when light bias is used on the lower half of these cells. In this CdTe module, even though there are cells and areas of low or very low photocurrent, most of the module shows some response. Only on very thin areas along the edges there are small areas of hardly any photocurrent.

When the CIGS module was laser scanned after 1000 hours of damp heat testing, significant differences in the photocurrent maps depending on the bias conditions could be observed. When scanned in short circuit a couple of cells show slightly below average response. For some reason the first and second cells as well as the second last and last cells do not show a clear cell separation in the line scan view. The plain view photocurrent map after scanning in short circuit shows quite even response throughout the module area. When laser scanned with light bias the CIGS module shows in the line scan all the cells with proper cell separations. The response is very even, only three first cells show lower and higher than average responses. In the plain view photocurrent map the response is quite even. There are some minor response changes within five individual cells but they do not form any pattern on the photocurrent map. On the contrary to the CIGS laser scanning photocurrent responses in short circuit and with light bias, the scanning with forward current bias shows very big differences in the response within the CIGS module. In the line scan there are only three cells showing proper signal

response, those being the first two cells and the last cells. The first two cells however, do not show properly the cell separation. The middle area of the module shows hardly any response at all. In the plain view photocurrent map in the middle of the module a circular shaped area of very low or no photocurrent is shown. Only the edge areas show some response.

The results of the laser scanning of thin film photovoltaic modules after damp heat testing are compared with the results of the damp heat test. In the first part of this chapter it was concluded that laser scanning with different bias conditions can reveal shunted cells and low photocurrent areas in the modules. The shunted cells show low photocurrent when scanned in short circuit. The photocurrent increases above the values seen in the other cells in the module when forward bias conditions are used. Depending on module characteristics and thin film technology, either bias illumination or externally applied forward current can be used as the forward bias source. If low photocurrent is due to a defect no or low photocurrent values are observed independent of bias conditions. Therefore it should be possible to verify with the laser scanning technique whether a visual defect after accelerated lifetime testing is causing shunting or a photocurrent defect in a thin film module. The technique also verifies if the visual defect is only cosmetic or if it is affecting the electrical performance of the module. It should be possible to correlate the possible decrease in short circuit current after accelerated lifetime testing with the area of low photocurrent values in the laser scanning results. Unfortunately however, the laser scanning technique can only be used to verify the current affected defects in the photovoltaic modules after accelerated testing. Because of the nature of the technique, it does not give any information to reveal the causes of possible decrease in open circuit voltage of the modules.

The amorphous silicon modules had degraded on average 11 % in short circuit current and 4 % in open circuit voltage. Visually large areas of delamination around the module edges and back contact aluminum corrosion in the corners were observed as well as humidity or oxidation dots especially on the upper and lower edges of the module. In the laser scanning results the one cell showing low photocurrent in short circuit and with light bias and high response in forward current bias is expected to be shunted. However, this is probably due to manufacturing defect rather than caused by accelerated lifetime testing since the damp heat results do not give any indication to have caused the shunting. The dark or very low photocurrent areas in the a-Si module mainly in the corners correlate well with the visually observed corrosion of aluminum back contact. Thus the corrosion of the back contact can be verified to have caused current decrease in module electrical performance. Also the shunted areas in between a couple of cells seen in the photocurrent map, when scanned in forward current bias, are suspected to be due to the back contact aluminum corrosion. This is because corrosion overlaps the areas of these cells. However, to verify this assumption some further investigations are needed which are out of the scope of this work. The oxidation of the front film seen visually as white dots is faintly visible especially in the photocurrent map after laser scanning with

forward current bias. This oxidation is mostly seen on the upper and lower edge of the module but there are two half-circle patterns of oxidation as well observed on the side edges on the upper half of the module. This oxidation might have caused the darkening seen on the left side in the plain view photocurrent map after scanning in forward current bias. Thus the oxidation can be verified to have somewhat affected the electrical behavior of the amorphous silicon module by contributing to the decrease in short circuit current of the module. The delamination of the module starting from the side edges can be verified not to have affected the electrical performance of the module and thus is only a severe cosmetic defect.

The first CdTe module had experienced a degradation of 17 % in short circuit current and 53 % in open circuit voltage (average of two CdTe modules tested) after 1000 hours of damp heat testing. Visually the back contact color had changed from light gray to nearly black radially around the corners and to dark gray in a circular pattern around the edges of the module. In the front film some minor color changes of areas turning yellow had appeared. A lot of bubbles were observed around the junction box area in the middle of the module. After laser scanning the first CdTe module after 1000 hours of damp heat testing, no shunted cells were detected. Since all the low photocurrent areas are shown on the photocurrent maps independent of the bias conditions, these areas have to have defects affecting the short circuit current in the module electrical performance. Even though the edges of the module show dark or low photocurrent areas in general, if looked closely, the corners do not practically show any response.

Therefore the correlation between the visual defects observed and the photocurrent map resulting from laser scanning verify that the color change in the back contact affects the electrical degradation of the module by contributing to the decrease in short circuit current.   The correlation also verifies that the stage of the color change is directly proportional to the short circuit current degradation. The low photocurrent area could be estimated to cover approximately the fifth of the module area thus roughly verifying that the major reason for short circuit current degradation after accelerated lifetime testing is the color change in the back contact. Neither the color changes in the front film nor the bubbles around the junction box seem to have affected to the short circuit degradation of the CdTe module after damp heat testing.   The second CdTe module that was laser scanned after 1000 hours of damp heat testing, had degraded in short circuit current 5 % and in open circuit voltage 20 % after the test. Visually some color changes in the back contact were observed, however this time the darkening of the back contact color occurred still around the edge areas but as dots or flakes and not necessarily starting from the very edge. There is also a faint circular pattern of slightly darker back contact color visible around the edges. In the front of the CdTe module, a circular pattern of faint color change could be observed the middle of the module being of lighter color than the edges. Some delamination patterns were detected especially around the corners. The figures shown of the visual defects in Chapter 4 only show the other CdTe module that

participated in the same damp heat test round than the laser scanned CdTe module. However, the visual defects were so similar after the test in these two modules that the figures of the other module well represent the visual defects observed in the CdTe module being laser scanned.

In the photocurrent map no major changes are observed dependent on the bias conditions. Thus no shunted cells can be identified in the CdTe module. The one area on the plain view on the left side on the lower half of the module shows somewhat lighter color or higher photocurrent values when scanned in forward current bias than the same area in other bias conditions. However, the change is so small that further investigations would be necessary to confirm the area being shunted. On the plain view photocurrent map there are dark or low photocurrent areas around the edges observed. These areas appear the same independent on the bias conditions. These areas correlate well with the color changes observed as visual defects in the CdTe module after damp heat testing. When looked closely, the middle area on the photocurrent map appears of lighter or higher photocurrent area and there is a circular shaped lower photocurrent area around the edge. The color changes in the back contact of the CdTe module appear exactly the same. Thus it can be verified for the second CdTe module laser scanned after accelerated lifetime testing that the changes in back contact observed visually affect the electrical performance of the module by degrading the short circuit current.

The low photocurrent patterns on the laser scanning response map, correlating well with the back contact color change, can be well approximated to cause the 5 % short circuit current degradation in the CdTe module after damp heat test. The kind of delamination patterns seen on the front of the module as well as the color difference in the front film are not visible in the photocurrent maps scanned in three different bias conditions. Therefore it is concluded that the visual defects on the front of the module are either only of cosmetic nature or at least they are not affecting the short circuit performance of the module. The laser scanning results verify the back contact color change to have caused mostly the short circuit current degradation of the CdTe module after accelerated lifetime testing. Unfortunately, the laser scanning does not give any information on the causes of the open circuit voltage degradation that was observed in all the CdTe modules tested in damp heat.

The CIGS module laser scanned after 1000 hours of damp heat testing experienced a degradation of 51 % in short circuit current and 12 % in open circuit voltage (average of two CIGS modules tested, but both behaved similarly). As visual defects, transparency and yellowness of cell separation lines in circular pattern around the edge was observed. Also on the front the middle of the active part of the module appeared to be of darker color than the edge areas of the module.

When the CIGS module was laser scanned after accelerated lifetime testing, the photocurrent response strongly depended on the forward bias conditions. No particular shunt areas were detected. When scanned in short circuit, the resulting photocurrent map in plain view no correlation to the visual defects were observed. On the contrary, in the

linescan the lack of cell separation lines between some cells can be correlated with the visual defect of the cell separation lines turning transparent and yellow. The transparency has been associated with the wear of the Mo back contact in the CIGS module. The wear has probably caused the cell separation cut lines to blur and the two cells show as one cell.

However, when light bias is used the cell separation lines appear again. Also when looked closely, the middle of the module in the plain view photocurrent map looks slightly to have higher photocurrent values than the edge areas. One possible explanation to the reappearance of the cell separation lines might be that the overall current is increased by application of illumination. The cell separation blurred in short circuit measurement response since the damp heat had deteriorated module short circuit current such a lot that the laser light by itself was not sufficient to invoke the proper function of the module.

In the third laser scan measurement when forward current bias was applied, the middle area of the CIGS module did not give any photocurrent response. The resulting plain view photocurrent map correlates well with the visual appearance of the module after damp heat test since the middle area of the module appeared of darker color than the edges. However, to explain the phenomenon that causes such a low photocurrent and that is such dependent on the laser scanning bias conditions is difficult without some further, more profound material investigations of the module which are out of the scope of this work.

It can be concluded that in principle with laser scanning it is possible to correlate the visual defects after accelerated lifetime testing of CIGS modules to the electrical performance of the module. However, for correct analysis of laser scanning results for CIGS modules it is necessary to conduct some further investigations to gain some principle correlation patterns which the analysis can be based on.

5.6   Conclusion on laser scanning

In this chapter the technique of laser scanning used for the investigations of thin film photovoltaic modules was studied. In the first section the behavior patterns of amorphous silicon, CdTe and CIGS modules in laser scanning were investigated. The modules were laser scanned with red laser in three different bias conditions or in short circuit, under light bias and exposed to externally supplied forward current bias. Also the technique found in literature to use laser scanning to reveal shunted cells in thin film photovoltaic modules was verified. In the second section laser scanning of a-Si, CdTe and CIGS modules with blue laser was investigated. With blue laser different active thin film layers in the modules can be probed. In literature blue laser scanning has been used mainly to study the red light distortion in CIGS modules. Use of blue laser was not found to give any further information in the scope of this work when compared to the information given by the use of red laser. In the third section a-Si, CdTe and CIGS modules were investigated by laser scanning them after 1000 hours (2000 hours in case of a-Si module) of damp heat testing. Three different bias conditions or short circuit, light bias and externally applied forward current bias conditions were used. The resulting photocurrent maps were compared with the visual defects observed after damp heat test. Laser scanning technique gives information on the short circuit current generation of the thin film photovoltaic modules. Therefore by laser scanning, the short circuit current degradation after accelerated lifetime testing could be correlated with the visual defects detected in the modules.

By comparing the laser scanning results done in short circuit with those done in forward bias conditions the shunted cells in thin film photovoltaic modules can be detected. For amorphous silicon module the shunted cells can be detected by using either illumination or external forward current bias as the source of forward bias. In case of CdTe and CIGS modules, light bias did not reveal the shunted cells but rather it was necessary to use forward current bias conditions. The modules were also quite sensitive to too high forward current bias and thus the proper level has to be experimentally verified before drawing conclusions of the results. The right forward current bias level also varied from one module to the other even if they were of the same thin film technology.

When using blue laser to scan the a-Si, CdTe and CIGS thin film photovoltaic modules the blue laser revealed the shunted cells in the a-Si module as well as the red laser did. However, with red laser the shunted cells could be detected by their increased response when forward bias was used when compared to the response when scanned in short circuit. In the blue laser scan, which was done only in short circuit conditions, the shunted cells showed lower photocurrent response than the other cell in the module. In blue laser response for the CdTe modules was the same as when scanned with the red laser in short circuit and light bias conditions. The response for the CIGS modules differed totally from the red laser scans. Therefore it was concluded that red light distortion could be expected from the CIGS modules but not from the CdTe modules.

However, using blue laser did not reveal any key information that would have not been available from the results of the red laser scans within the scope of this work.

Using the laser scanning technique to study thin film photovoltaic modules after accelerated lifetime testing was found to be helpful in correlating the visual defects observed to the short circuit current degradation of the modules. With laser scanning only current behavior of the photovoltaic module can be observed, it does not give any information on voltage behavior. In the a-Si module the visual defects of especially the back contact aluminum corrosion and somewhat the oxidation of the front film were verified to have contributed to the short circuit current degradation of the module after 2000 hours of damp heat testing. The delamination observed was found to be a visual defect of merely cosmetic nature. In the CdTe modules the visually observed color change in the back contact was verified to strongly correlate with the short circuit current degradations of the modules. Some front film color change and delamination patterns were found to be only cosmetic visual defects. In the CIGS modules the laser scanning response maps were found to strongly depend on the bias conditions. The cell separation line transparency, which was visually observed in the module, was visible in the short circuit measurement result but not in the light bias measurement result. In forward current bias there was very low photocurrent values observed in the middle of the module, which was visually found to be of darker color in the front film than the edge areas of the module. However, it was concluded that for correct analysis of laser scanning results for CIGS modules it is necessary to conduct some further investigations to gain some principle correlation patterns which the analysis can be based on.

In general it is concluded that laser scanned can be used as a tool to investigate the short circuit current performance of thin film photovoltaic modules. When comparing the resulting photocurrent maps scanned in short circuit and forward bias conditions shunted cells in the module can be verified. Use of blue laser was not found to give any further information in the scope of this work when compared to the information given by the use of red laser. Laser scanning is very helpful when trying to correlate the causes of short circuit current degradation after accelerated lifetime testing with the visual defects observed.

6. CONCLUSION

In this work single junction amorphous silicon modules, CdTe prototype modules and mini-modules, and CIGS prototype mini-modules were investigated to be reliably able to characterize the electrical performance and to find out potential failure mechanisms in accelerated lifetime testing. Amorphous silicon modules have been manufactured already for several years but the short lifetime of the first generation modules has given them a somewhat bad reputation. CdTe and CIGS modules are shortly entering the market. However, there is a lack of characterization and testing methods to reliably predict the power output and service lifetime of these technologies, which the current standard procedures do not totally fulfill. This may be a major obstacle if thin film modules are going to increase their share of the growing photovoltaic industry.

In this work firstly some physics, material and manufacturing issues related to amorphous silicon, CdTe and CIS thin film photovoltaic technologies were reviewed in order to understand possible failure mechanisms in accelerated lifetime testing. In the second part, the calibration measurement procedures and in particular the choice of the reference device for the thin film photovoltaic materials was investigated. The results enable to verify correctly if the modules have passed or failed the qualification tests and thus to predict the power output of the module during its lifetime. In the third part, the thin film photovoltaic modules, prototype modules and prototype mini-modules were exposed to accelerated lifetime testing. The potential failure mechanisms were investigated by testing them in thermal cycling and humidity freeze cycles, in damp heat, in dry heat and in light soaking. Only when failure mechanisms are known, the manufacturers can design proper improvements to the module constructions. In the last part, laser scanning was used to further investigate the observed failure mechanisms after accelerated lifetime testing. The method enables a non-destructive determination of the position dependent photocurrent throughout the module.

In the investigations of the calibration measurement procedures, it was found that the use of a c-Si reference device when characterizing CIGS modules gives reliable measurement results in the short circuit current calibration. In case of a-Si, the use of the filtered c-Si reference device the spectral response of which resembles that of a-Si gives more reliable results than the use of the c-Si reference device. In case of CdTe, a reference device made of a GaAs cell having a similar spectral response with CdTe, can be used. To obtain consistent I_{sc} values when measuring with the different simulators, a correction based on the difference in the slopes of the reference device and the sample in the normalized I_{sc} decay over the irradiance decay could be applied if the lamp spectrum was assumed to be constant at different irradiance levels. However, the lamp spectrum is not always constant and the response of the sample material is not necessarily linear at different irradiance levels. In this work it is suggested to use a reference device with a spectral response similar to that of the sample material. In that case a mismatch factor close to one is also obtained.

It was demonstrated that the major cause for failure in accelerated lifetime tests of a-Si, CdTe and CIGS modules and prototype modules and mini-modules is the humidity penetration into the module encapsulation. In amorphous silicon modules humidity penetration caused major visual defects but the electrical performance was only affected in the first set of samples in P_{max} and FF by 10 %. In CdTe prototype modules humidity penetration caused changes in the back contact composition which could be visually detected and which lead to significant degradation in electrical performance especially in P_{max} in the first set of samples by 82 % and in the second set of samples by 58 % on average. In CIGS prototype minimodules humidity penetration corroded back contact Mo or the front contact ZnO and back contact Mo connection at the relatively unprotected cell interconnect areas. This could be observed both visually and as degradation in the electrical performance in which in the second set of samples most significant degradation was observed in P_{max} by 81 % on average. The first set of samples stopped working after 485 hours of testing.

However, even if all these failures were caused by humidity penetration, there were differences between the technologies on how sensitive they were to humidity. The amorphous silicon modules were less insensitive to humidity penetration than the CdTe and CIGS devices. In the case of CdTe prototype modules even small amounts of humidity penetration caused changes in the back contact composition, which seemed to be the major cause for the electrical degradation. The CIGS prototype minimodules did not seem to be as sensitive to humidity penetration as the CdTe, even though significant degradation was caused by humidity penetration into module encapsulation also in these devices.

In light soaking the three thin film photovoltaic technologies behaved quite differently. The a-Si photovoltaic modules degraded in light soaking mostly in short circuit current, by 17 %, and in maximum power, by 35 %, and somewhat in fill factor, by 18 %. Also as expected the degradation stabilized towards the end of the light exposure. In the CdTe a decrease in maximum power, on average 10 % in the first series and 11 % in the second series, independent of the sample or manufacturer was observed. For other parameters no clear behavior pattern could be observed during the light exposure. The dependence of bias state during the exposure to CdTe module behavior should further be investigated. All the CIGS samples except one showed increase in maximum power and in fill factor. In the first series of samples the P_{max} increased by 25 % and the FF by 23 %. In the second series of samples in average there was a decrease in P_{max} by 1 % and an increase in FF by 3 % but the samples behaved very differently. This suggests that the observed behavior may depend on the material quality.

In the laser scanning it is concluded that the method can be used as a powerful non-destructive tool to investigate the short circuit current performance of thin film photovoltaic modules. When comparing the resulting photocurrent maps scanned in short circuit and forward bias conditions, shunted cells in the module can be identified. The use of blue laser was not found to give any further information in the scope of this

work compared to the use of the red laser. It was demonstrated that laser scanning can be used to correlate the causes of short circuit current degradation after accelerated lifetime testing with the visual defects observed.

In this work it has been shown that the current standards for measurement and testing photovoltaic devices may not necessarily be applied as such especially for the CdTe and CIGS thin film technologies. In calibration measurements, the calibration procedure is rather accurate when a reference device with similar spectral response to the measured material is used instead of the c-Si reference device. However, further investigations on the bias conditions during measurements and the dependence on light conditions before calibration measurements on the measurement results are still needed.

The qualification standard for thin film photovoltaic modules is mostly copied from the crystalline silicon module qualification standard. It is adapted especially for the a-Si module testing for which it is rather adequate. However, there are several points, which should be reconsidered in the thin film module testing. For example, when new information is gained from the outdoor exposure or real time testing it should be considered whether the long test cycles based on c-Si module performance are adequate for thin film modules and subsequently define a proper service lifetime for these technologies based on their own character. The light soaking procedures defined in the standard are adequate for a-Si but CdTe and especially CIGS had very different behavior under light. It may even be necessary to consider the CIGS behavior in light soaking when assigning passing criteria for the modules in qualification. The passing criteria are currently based on the absolute electrical performance or power rating values defined by the manufacturer instead of relative values before and after test. With thin film photovoltaic technologies it may be difficult to obtain measurement results comparable to the power rating values defined by the manufacturer. This depends on the reference device and accuracy of calibration measurement equipment and procedures in use. Thus some modules may even fail the qualification without any reason.

In defining the qualification standard, most important is to ensure adequate service lifetimes for the thin film modules on the market. Even if standards are redefined to take into account the special character of thin film photovoltaic modules, the modules have to be able to work in harsh and humid climates in real outdoor conditions. Thus, it is important to design proper and reliable encapsulation for the thin film modules. The manufacturers are constantly working on this matter and a lot of improvements will most likely be seen in the near future. In this task, the non-destructive laser scanning technique is of help since it can effectively be used to reveal specific spots of photocurrent degradation on the thin film modules. When using laser scanning the modules can be investigated as a final product and without breaking the module. It was demonstrated that this method provides good estimates for causes of degradation in the modules and enables correlation of observed visual defects with the degradation in the module photocurrent. This in turn helps to design thin film photovoltaic modules with longer service lifetimes than today's modules have.

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