ACTIVE MIXERS FOR DIRECT CONVERSION RECEIVERS WITH 0.35-µm BiCMOS

Kalle Kivekäs, Aarno Pärssinen, Kari Halonen

Helsinki University of Technology, Electronic Circuit Design Laboratory,
P.O. Box 3000, FIN-02015 HUT, Finland
tel:+358 9 451 2988, fax:+358 9 451 2269
E-mail: ***kks@ecdl.hut.fi***

Abstract

In this paper, the design requirements of different mixers for direct conversion receivers are discussed. Special attention has been paid into the detection of amplitude-modulated RF signal envelope. Three active mixers have been implemented to investigate the discussed requirements by using a 0.35-µm, 25-GHz BiCMOS technology. The same process allows an objective comparison between the different topologies. The mixers are designed for a single 2.7 V supply, and specified for low power consumption. Different topologies are compared by their Spurious Free Dynamic Ranges (SFDR) with respect to their individual power consumption. Also, their performance were measured at different LO power levels and supply voltages. The results show insignificant differences between the topologies in low voltage applications.

Key Words. Downconversion mixer, Direct Conversion Receiver, envelope distortion, BiCMOS

1 Introduction

Direct conversion receiver (DCR) is a prominent radio architecture to be used in wireless single-chip receivers due to its integrability. In addition to its evident benefits it has also well known limitations, that must be considered in the proper design [1, 2]. The strongest challenges in the DCR design are involved in reducing the effects of the even-order distortion and flicker noise especially in downconversion stage. Wide-band Code Division Multiple Access (WCDMA) has been selected as an air interface in the 3rd generation Universal Mobile Telecommunications Systems (UMTS). It uses Quadrature Phase Shift Keying (QPSK) as a modulation method between the mobile terminals and base stations. The QPSK modulated signal has a variable envelope which amplitude-modulated component may be detected in the mixer due to its improper second-order linearity performance.

The envelope distortion among the other low-frequency errors is more stringent to handle in the narrow-band systems. In CDMA systems, the information is spread over a wider band, and the low-frequency errors occupy a smaller portion of the total signal. Nevertheless, the signaling environment is not necessarily limited to the modulated in-band channels and their envelopes. Switching transients or modulated channels from other systems operating at the same band or close to it may also contribute significant envelope contents over the desired signal. The downconversion in the DCR is a part of the demodulation but the I/Q accuracy requirements are not so stringent as with image rejection architectures. On the other hand, the imperfect phase and amplitude balances in differential LO signal deteriorate both IIP2 and IIP3. Hence, the most substantial DCR design issues including flicker noise, DC-offsets, and even-order nonlinearity, as well as the LO signal isolation from the antenna are all strictly related to the downconversion mixers.

2 Mixers in Direct Conversion Receivers

In a direct conversion receiver (Fig. 1) an active mixer is preferred for several reasons. First, the RF front-end must provide at least 25-30 dB of voltage gain. Otherwise, the noise contribution of the baseband signal processing is not suppressed enough. Passive mixers exhibit always a loss of at least 3.9 dB. In that case the LNA must be able to provide not only all of the required RF gain but also additional gain to compensate the loss due to the passive mixer. Although that could be possible, it leads to even more unreasonable linearity requirements of a mixer. In addition, a single-stage LNA might not be sufficient for that due to it's own linearity and stability. However, if using a multi-stage LNA, the linearity and stability problems should be circumvented by trading-off with the current consumption. Another solution is to add an amplifying buffer stage with high linearity and low noise after the mixer, but again with the expense of power consumption. Typically the IIP3 requirements for receivers in cellular systems are between –20 and –10 dBm. The required third-order linearity of

the mixer can be found with respect to the linearity and gain of the LNA as

$$\frac{1}{iip_3} \approx \frac{1}{iip_{3,LNA}} + \frac{a_{V,LNA}^2}{iip_{3,MIX}}. \quad (1)$$

Here, $a_{V,LNA}$ is the voltage gain of the LNA, and iip_3, $iip_{3,LNA}$, and $iip_{3,MIX}$ are the third-order input intercept points of the front-end, LNA, and mixer, respectively. The front-end linearity according to Eq. (1) is shown in Fig. 2 with several mixer IIP3 values. The IIP3 of the LNA is assumed to be –5 dBm. Fig. 2 also illustrates the cascaded noise performance of the front-end in the right y-axis. The noise figures of the mixer and LNA are defined as 10 and 2.0 dB, respectively. The given 'gain-noise-linearity'-diagram is useful when optimizing the gain partitioning between the LNA and mixer to reach as linear and low noise performance as possible.

The topology of the direct conversion mixer should be balanced in order to cancel the even-order intermodulation properly. In the case of a perfect balance, the second-order intermodulation products are cancelled. However, even a small mismatch between the differential branches leads to the detection of the amplitude-modulated signals due to the second-order distortion. Also, double-balanced topologies are preferred to minimize the harmful LO signal leakage to the reverse direction of the receiver and improve IIP3. Still, all topologies are not very attractive candidates for DCRs. For example, the highly linear mixer topology presented in [3, 4] has typically too high noise figure due to the flicker noise of the buffering gain stage. The micromixer [5] is also rejected because of its asymmetrical RF signal routing, and thus potentially lower IIP2. The envelope distortion and RF self-mixing are more likely severe problems in wide-band CDMA receivers, because they occupy a bandwidth relative to the modulation. Hence, the proportional benefit of the wide radio channel is lost. On the other hand, the processing gain in CDMA systems efficiently reduces the effect of all interference, which falls over the desired channel.

3 Mixer Implementations

The BiCMOS process gives a freedom for the designer to select appropriate devices in the critical operations according to their special strengths. All implemented mixers are active double-balanced mixers, modified from the linear four-quadrant Gilbert multiplier [6]. The advantage of this type of an active mixer is its ability to provide conversion gain due to the current-mode output. The output current is converted back to voltage in the load resistors, which can provide considerably higher impedance level than the input $1/g_m$. Hence, the voltage conversion gain is proportional to the product

$(2/\pi)g_m R_L$. The term $2/\pi$ indicates the loss due to ideal brick-wall switching in the double-balanced case, g_m is the transconductance of the input stage, and R_L is the load resistance.

All implemented structures utilize the same commutating switch core. The commutating switch transistors are chosen to be bipolars due to the lower flicker noise than their MOS counterparts. The use of MOS transistors as the commutating switches in the direct downconverter is restricted because of their large flicker noise contribution to the output. The problem with a MOS transistor exists when the inherently higher flicker noise of a MOS device is stored into the parasitic drain-source capacitance after the upconversion. This charge is then self-downconverted by the LO signal during the next cycle [7]. In our simulations, the noise figure of a direct conversion mixer with MOS switches was increased by several decibels to an unacceptable level, and thus the choice of the bipolar switching devices was obvious. Flicker noise from the RF signal path is upconverted around the LO frequency, except of the leaked noise due to imperfect switching. This is however less important compared to the commutating switches and active baseband circuitry.

All mixers are loaded resistively and their outputs are buffered with the same on-chip emitter follower shown in Fig. 3(d). The buffer is designed to drive a 50 Ω load with an almost negligible degradation in noise or linearity performance of the mixer. The power consumption of the buffer is excluded from the given results because it is not necessary to match the output to a low impedance level in a complete DCR.

Three possible active mixer candidates are implemented to be used in an integrated DCR. The first mixer is fully bipolar. The second mixer has NMOS transistors in its input transconductance stage [8]. In the third mixer the signal is brought directly to the emitters of the commutating switches, and the long-channel NMOS transistors act only as current sources [9]. The topology is called a double-balanced switching pair mixer (DBSP) in this paper. The mixer topologies are shown in Figs. 3(a)-(c). Mixers are bonded directly on the PCB and measured using exactly the same measurement setup.

To achieve a high IIP2 the chip input must be assembled with an extreme care in order to avoid the extra imbalance in the RF and LO input stages because of asymmetrical bond wires or too large inductive load, which destroys the correct phasing in the desired input terminals. Hence, it is quite uncertain to determine unambiquously the IIP2 of a single direct conversion mixer without an LNA and on-chip LO buffers [10]. The reported mixers are optimized with respect of realistic interfaces in direct conversion receivers which are not matched to a typical 50 Ω impedance level of measurement equipment. The realistic interfaces provide significantly smaller parasitics that can be achieved by

using package or direct assembling on a PCB. The designed mixers are realized individually and therefore the IIP2 values in a complete system might be better than the reported ones [8]. However, several samples have been measured from all mixers in order to get more realistic investigation from their second-order characteristics. One important measure of the differential mixers is their immunity against common mode signals. Since the double-balanced structures have both differential input and output ports rather than common-mode rejection ratio (CMRR), this immunity is described by the common mode input to differential output ratio (CMDR), given as:

$$CMDR = 20 \cdot \log_{10}\left(\frac{A_{diff}}{A_{cmd}}\right), \tag{2}$$

where A_{diff} is the voltage conversion gain of the mixer for differential input signal to differential output, and A_{cmd} is the voltage conversion gain for the common mode input signal to differential output. In addition, *CMDR* gives also a good measure for the circuit imbalance. Therefore it is very useful parameter in the IIP2 analysis, as these two parameters together characterizes the second-order nonlinear performance of the balanced circuit. The input stages of bipolar and BiCMOS mixers are connected directly to ground. This results in improved linearity with the cost of increased sensitivity to supply noise and distortion [10].

3.1 Bipolar Mixer

The voltage conversion gain of the implemented bipolar mixer is 17.8 dB. That is considerably higher than the respective gains of the BiCMOS and DBSP mixers. The high conversion gain of the bipolar mixer is due to the fundamentally higher transconductance of bipolar transistor ($g_{m,BJT}$ = 47 mS) than the MOS transistors ($g_{m,MOS}$ = 17 mS) when appropriate device sizes are used. As the conversion gain is proportional to the product of the input g_m and output impedance, it cannot be decreased only by making the load resistor smaller. Otherwise the output DC voltage starts to rise which is undesired due to an intention to have equal output interfaces for each mixer. The branch current could not be scaled down either to reduce the input g_m and thus lower the gain. It would lead to the same DC problem. The equal gain with the BiCMOS and DBSP mixers could have been implemented by degenerating the bipolar mixer. Degenerated bipolar transistor consumes more current than the respective MOS device to achieve an equal transconductance and degeneration would have also led to device matching problems in differential input stage. Although, this topology is widely used, its linearity is only moderate due to the exponential transconductance characteristics of the input transistors.

3.2 BiCMOS Mixer

The BiCMOS mixer is similar than its bipolar counterpart, except of the NMOS input transconductors. By using the NMOS transistors in the input stage, an improvement in the mixer linearity is achieved. The maximum usable frequency of the input signal is restricted by the cut-off frequency of the input transistors. The measured operation range of the RF input was slightly below 2.5 GHz and is significantly lower than with bipolar devices. That is still sufficient for the current cellular applications.

3.3 DBSP Mixer

In the DBSP mixer the voltage-mode input signal is fed directly to the common emitter node of the commutating switches. This topology uses large, long-channel devices, M_1 and M_2, as current sources. Since, the DBSP topology does not have a g_m-stage as its input; it provides capability to be used also at higher frequencies. Its operating frequency is limited by the characteristics of the current source and the commutating switches, which have f_T over 20 GHz. The conversion gain depends on the source impedance of the driving stage preceding the mixer. The 50 Ω source used in measurements is probably not an appropriate choice for the load of the preceding LNA. The higher impedance level (200 Ω for example) gives a better optimum for the linearity of LNA with the same supply current. Then the gain of the mixer drops by 6 dB, with the same loading. Another drawback is the low LO-to-RF isolation that is due to the lack of the reverse isolation of the input transistors. Both issues can be avoided by attaching an extra AC-coupled stage between the LNA and mixer as in [11]. That should be however be considered as a part of the LNA or as a buffering stage which consumes extra current.

4 Layout Considerations

The layout symmetry is a key factor for double-balanced mixers in DCR. The LO- and RF signal routings have been drawn orthogonally to each other in order to minimize magnetic coupling between the conducting lines. Also different details have been realized as symmetrically as possible even though the double-balanced structures are complicate to implement with a perfect symmetry. The four metal layers relaxed the optimization. Critical units, as commutating switch core, have been shielded to reduce the substrate noise by surrounding wide guard bands. The most critical crossings were shielded with grounded metal layer between the wiring. The microphotograph of the chip is shown in Fig. 4. Each mixer core occupies less than 0.1 mm^2 active die area without bonding pads and output buffer.

5 Experimental Results and Comparison Between Topologies

All designed mixers establish sufficient performance to be used in a DCR. However, different amplifications and linearity properties require specific system partitioning. The designed mixers are all optimized according to their special strengths in topology. Measured performance of each mixer is given in Table I. To enable reliable comparison between the mixers, the biasing is arranged similarly. In addition, the same bonding pad pattern and test PCB have been used for each of them.

The reported noise figures are calculated cumulatively over the 2 MHz downconversion band, which takes the flicker noise contribution into account. However, the mixers have (within the measurement tolerances) almost similar 1/f-noise performances. This indicates that the flicker noise is dominated by the commutating switch core and the output buffer rather than input stages, which is as desired. Flicker noise performance of the mixers is illustrated in Fig. 5.

The mixers entail very different LO-to-RF isolation characteristics. The bipolar mixer provides better reverse isolation than BiCMOS mixer. The LO-to-RF isolation to the single-ended RF input is better than 60 dB. The superior isolation of the bipolar mixer is due to the smaller parasitic capacitances between the terminals of the input transistors than in the larger fingered MOS devices in the BiCMOS mixer. However, the precise determination of the LO-to-RF isolation is complicate, since the isolation between the differential LO and single-ended RF connectors of the test board is only 63 dB. As expected the DBSP mixer provides rather poor LO-to-RF isolation due to the lack of the input stage. The measurement from a single-ended input gives only a fair method to compare the differential topologies. The differential leakage to a balanced RF input would be significantly smaller and therefore difficult to measure confidentially.

In Figs. 6 and 7, the voltage conversion gain and IIP3 as a function of the LO signal power are presented for the mixers. All mixers provide rather stable conversion gain with respect to the LO power variations. Instead, their linearities depend strongly on the variations in the LO power. That is probably due to the improper setup in the measurement as discussed before. The variations were less abrupt in earlier BiCMOS mixer with buffered LO [12]. The bipolar mixer can be operated with a slightly lower LO but its linearity drops dramatically if driven too hard. This is however a matter of appropriate buffering. The smallest constant gain region of the DBSP indicates clearly the sensitiviness of operating conditions compared to the other topologies.

The voltage conversion gain and IIP3 as a function of supply voltage for the mixers are shown in Figs. 8 and 9, respectively. The BiCMOS mixer exhibits the best low voltage performance by

providing stable operation above supply voltage of 1.6 V. Although the DBSP mixer provides quite good performance under the design specifications, it is sensitive to the changes also in the supply voltage. It reaches stable conversion gain like bipolar and BiCMOS mixers but the IIP3 is more susceptible to supply variations. However, this is also excepted characteristics since the commutating core is not bufferd by the transconductance stage.

The measured IIP2 results show that the second-order characteristics of the mixers depend only vaguely on the supply-voltage or LO signal power. IIP2 describes the second-order distortion characteristics, but also the amount of imbalance that enables its detection. The impact of the imperfect cancellation of the second-order intermodulation has been investigated with simulations. In Fig. 10 three different mismatches of the BiCMOS mixer are illustrated. The mismatches in the load resistances and in the emitter resistances of the BJT commutating pairs degrade the even-order performance more than the variations in the threshold voltages in the NMOS input stages. Absolute imbalance due to the normal process variations is rather small for the threshold voltage, but for buried vias, resistors, and wire sheet resistances it may be significant. However, the V_T variations illustrate well the possible g_m mismatch due to input pair imbalance or biasing error, and its effects. The given IIP2 values are measured from the best samples. The worst values were about 10 dB lower but conclusions of statistical properties would require significantly larger number of tested circuits. The differences however reflect the sensitivity to degradation of performance between different topologies preferring the use of BiCMOS structure. Other parameters than IIP2 had only minor changes from sample to sample. The imbalance simulations have been performed only for BiCMOS structure.

The mixers can be compared using the spurious free dynamic range, as defined in [13]:

$$SFDR = \frac{2}{3}(IIP3[dBm] + 174[dBm/Hz] - NF[dB] - 10 \cdot \lg(BW)), \quad (3)$$

where BW is the noise bandwidth of the mixer output. However, this bandwidth factor disables to use of *SFDR* to compare mixers that are designed to systems having different bandwidths. Here, the comparison has been carried out for WCDMA having 2 MHz bandwidth at baseband. Therefore the plain SFDR is significantly smaller than in narrow-band conditions. Also, in CDMA systems prosessing gain, G_P, can be increased directly to *SFDR*. *SFDR* with respect to the power consumption is illustrated in the Fig. 11. Due to the large gain, the bipolar mixer is located far from the other two and therefore a direct comparison is not straightforward. Instead, the BiCMOS mixer has similar dynamic range to DBSP with slightly smaller power consumption.

6 Conclusion

In this paper, the requirements for the mixers in the integrated direct conversion receivers are discussed. Also, three slightly different active mixer topologies are implemented to meet the desired performance. It is shown that all realized mixers fulfill the typical requirements and could be used in modern wireless receiver. It is also noticed that the input and output interfaces must be properly designed for active mixers. For example, the DBSP mixer suffers from the lack of the buffering input transconductance stage. However, the BiCMOS topology with MOS transistors as input stages and bipolars in commutating switches is less sensitive to supply voltage and LO power variations than the other test structures. It also provides the best second-order linearity, and seems to be the promising topology for direct conversion receivers.

7 Acknowledgements

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8 References

[1] B. Razavi, "Design Considerations for Direct-Conversion Receivers", IEEE Transactions on Circuits and Systems-II, Vol. 44, pp. 428-435, Jun. 1997.

[2] A. Abidi, ”Direct-Conversion Radio Tranceivers for Digital Communications,” IEEE Journal of Solid-State Circuits, Vol. 30, pp. 1399-1410, Dec. 1995.

[3] B-S. Song, ”CMOS RF Circuits for Data Communications Applications,” IEEE Journal of Solid-State Circuits, Vol. 21, No. 2, pp. 310-317, Apr. 1986.

[4] J. Crols, M. Steyaert, ”A 1.5 GHz Highly Linear CMOS Downconversion Mixer,” IEEE Journal of Solid-State Circuits, Vol. 30, No. 7, pp. 736-742, Jul. 1995.

[5] B. Gilbert, ”The MICROMIXER: A Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage,” IEEE Journal of Solid-State Circuits, Vol. 32, No. 9, pp. 1412-1423, Sept. 1997.

[6] B. Gilbert, ”A Precise Four-Quadrant Multiplier with Subnanosecond Response,” IEEE Journal of Solid-State Circuits, Vol. 3, pp. 15-25, Dec. 1968.

[7] T.Melly, A.-S. Porret, C. Enz, M. Kayal,”A 1.3 V low-Power 430 MHz Front-End Using a Standard Digital CMOS Process,” IEEE Proceedings of CICC, pp. 503-506, 1998.

[8] A. Pärssinen, J. Jussila J. Ryynänen, L. Sumanen, K. Halonen, "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications", IEEE Journal of Solid-State Circuits, Vol. 34,

No. 12, pp. 1893-1903, Dec. 1999.

[9] C. Takahashi, R. Fujimoto, A. Satoshi, I. Tetsuro, U. Takashi, T. Hiroshi, T. Hiroshi, W. Shuji, H. Kenji, “ISSCC Digest of Technical Papers, pp. 138-139, Feb. 1995.

[10] S. Wu, B. Razavi, “A 900-MHz/1.8-GHz CMOS Receiver for Dual-Band Applications,” IEEE Journal of Solid-State Circuits, Vol. 33, pp. 2178-2185, Dec. 1998.

[11] B. Razavi, “A 1.5 V 900 MHz Downconversion Mixer,” in ISSCC Digest of Technical Papers, pp. 48-49, Feb. 1996.

[12] J. Ryynänen, A. Pärssinen, J. Jussila, K. Halonen, "An RF Front-End for the Direct Conversion WCDMA Receives”, in Proc. of the RFIC Symp., pp.21-24, Jun. 1999.

[13] A. Rofougaran, J. Chang, J. Rael, Y.-C. Chang, M. Rofougaran, P. Chang, M. Djafari, M.-K. Ku, J. Min, E. Roth, A. Abidi, H. Samueli, "A Single-Chip 900-MHz spread-spectrum wireless tranceiver in 1 μm CMOS---part I & II”, IEEE Journal of Solid-State Circuits, Vol. 33, pp. 515-547, Apr. 1998.

TABLE I.

MEASURED PERFORMANCE OF DIFFERENT TOPOLOGIES,

WITH V_{DD}=2.7 V @ 2 GHz.

		BiCMOS	BJT	DBSP
NF(DSB)	[dB]	9.6	10.7	12
Conv. gain	[dB]	7	17.8	8.5
IIP3	[dBm]	+3	-4	+5.3
OIP3	[dBm]	+10	+14.3	+13.8
IIP2	[dBm]	+53	+28	+41
ICP	[dBm]	-12	-20	-14
CMDR	[dB]	-26.9	-25.9	-28.9
LO-to-RF isol	[dB]	60	44	28
I_{DD}	[mA]	5	2.5	6
P(LO)	[dBm]	-9	-9	-9
SFDR	[dB]	69.5	64.4	69.3

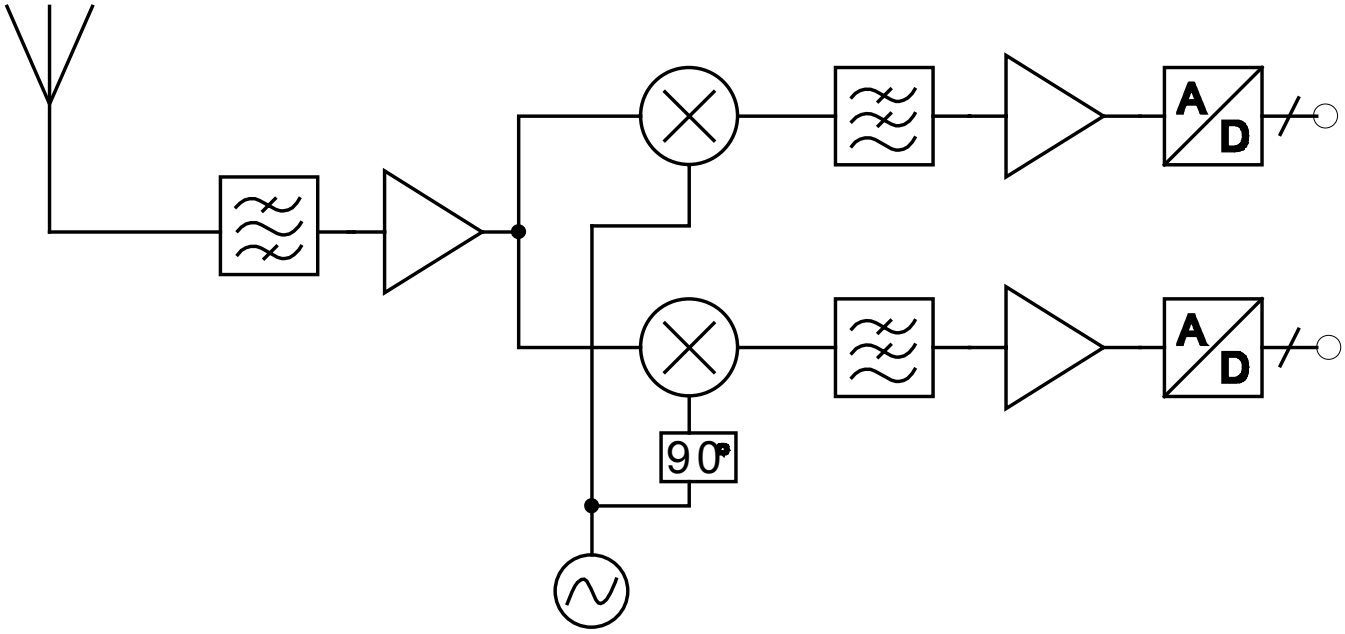

Fig. 1. Block diagram of direct conversion receiver.

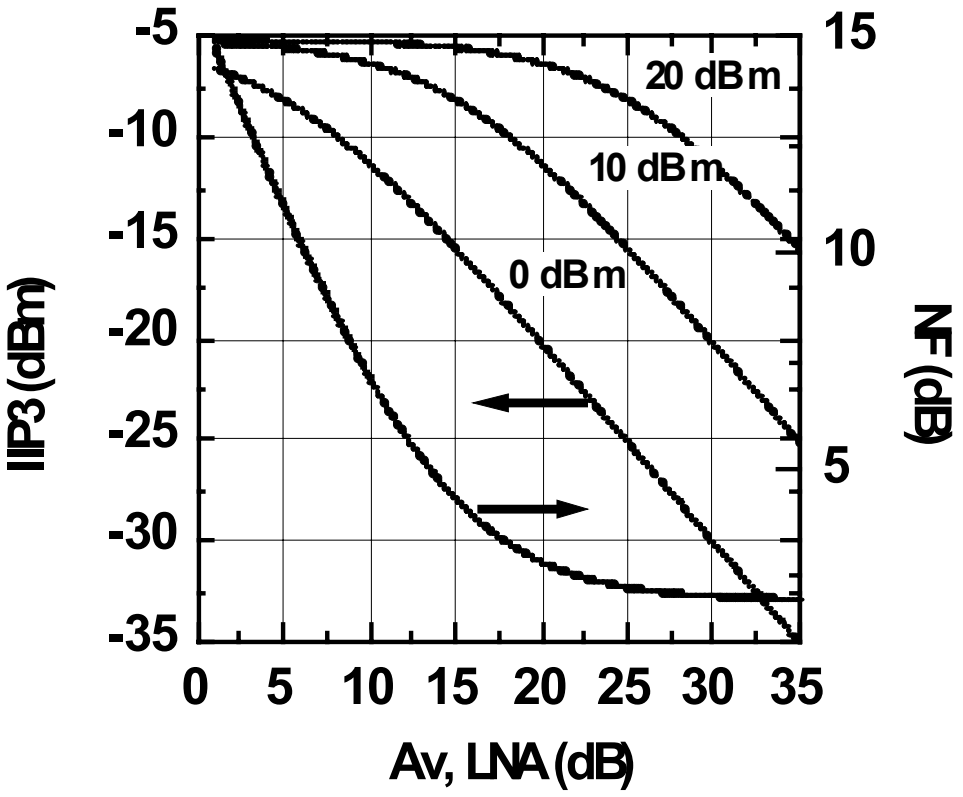

Fig. 2. IIP3 and NF of the front-end for three different mixer IIP3 values. The DSB noise figure of the mixer is assumed to be 10 dB and the IIP3 and NF of the LNA are –5 dBm and 2 dB, respectively.

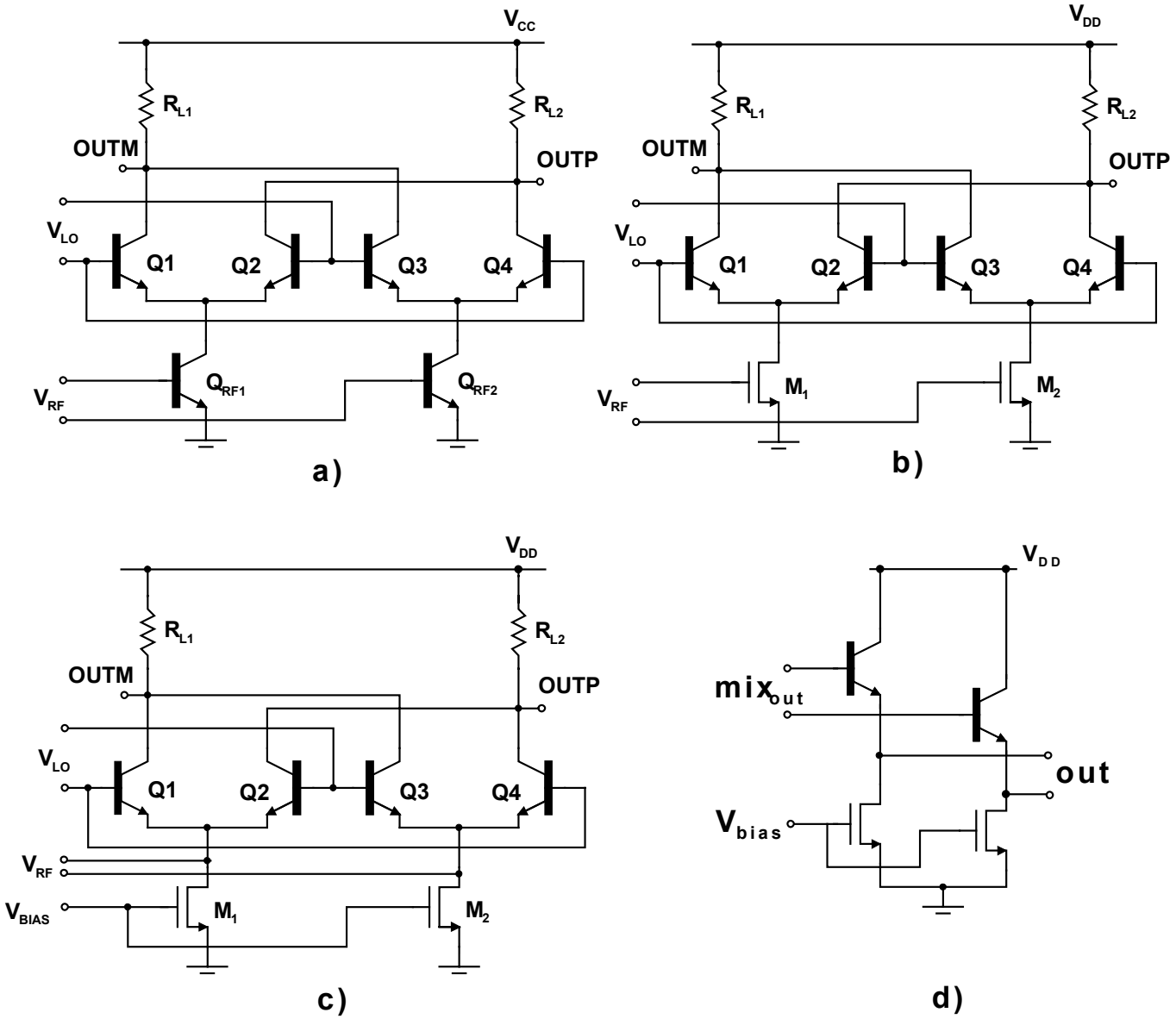

Fig. 3. Implemented a) bipolar, b) BiCMOS, c) DBSP mixer, d) output buffer.

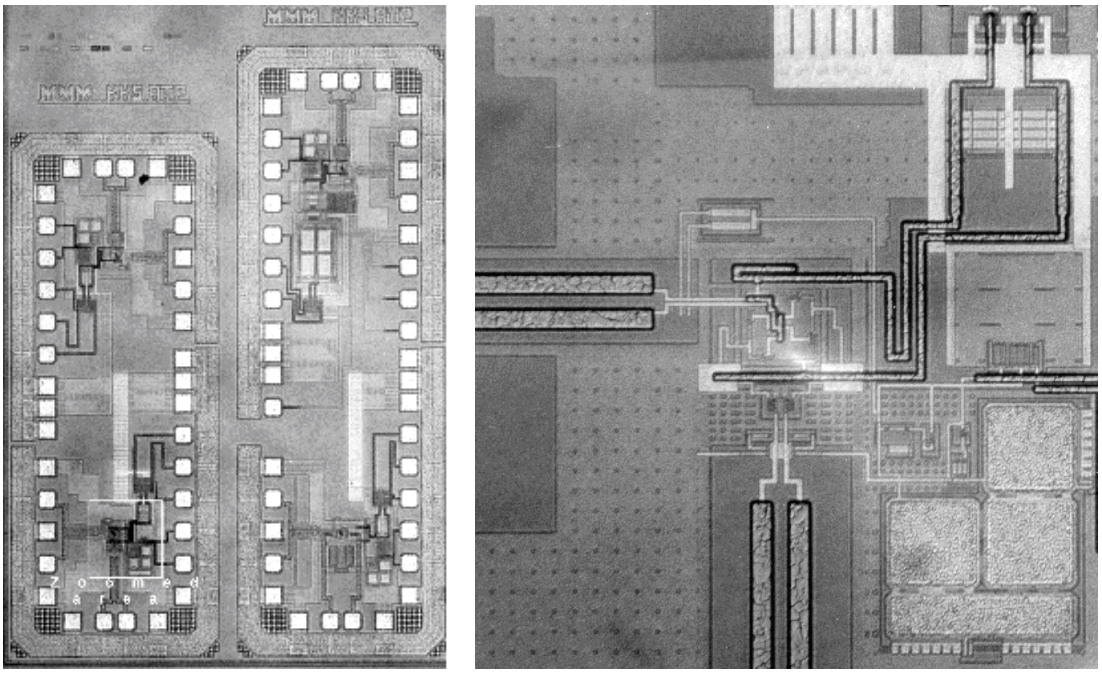

Fig. 4. Microphotograph of the test chip and bipolar mixer core.

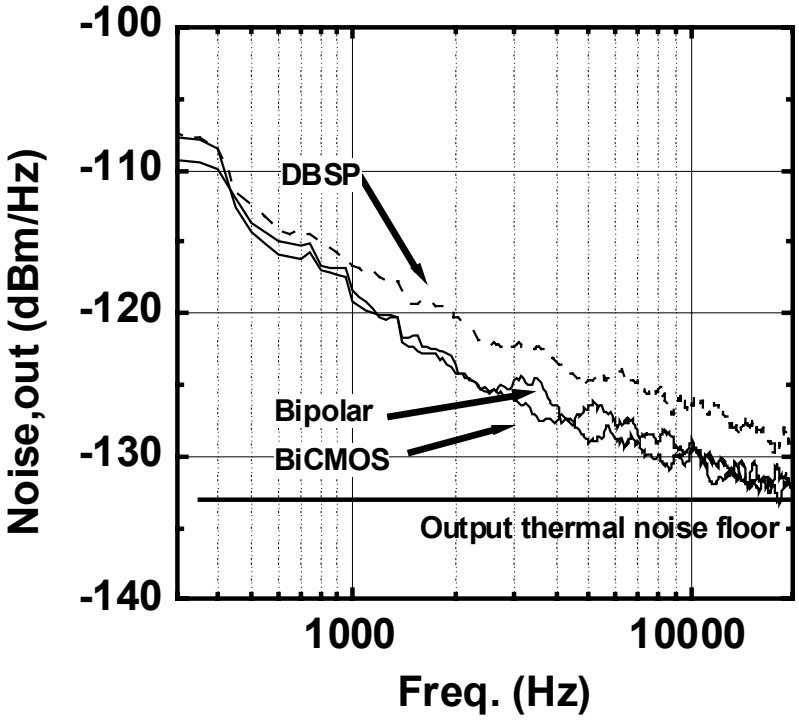

Fig. 5. Measured flicker noise performances of different mixers.

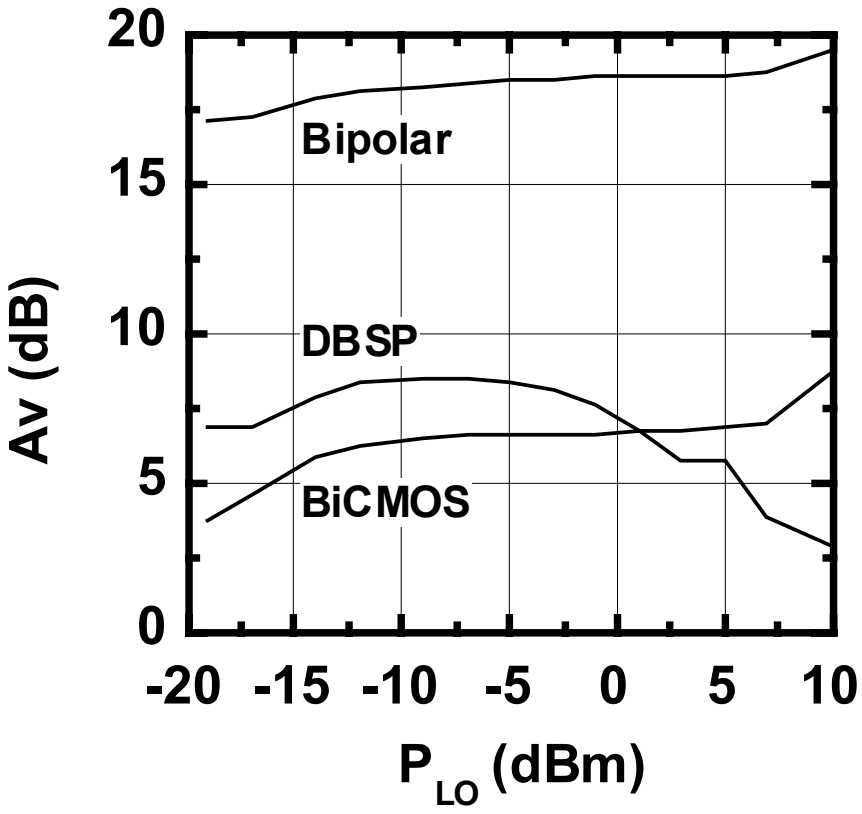

Fig. 6. Voltage gain vs. LO power for different mixers.

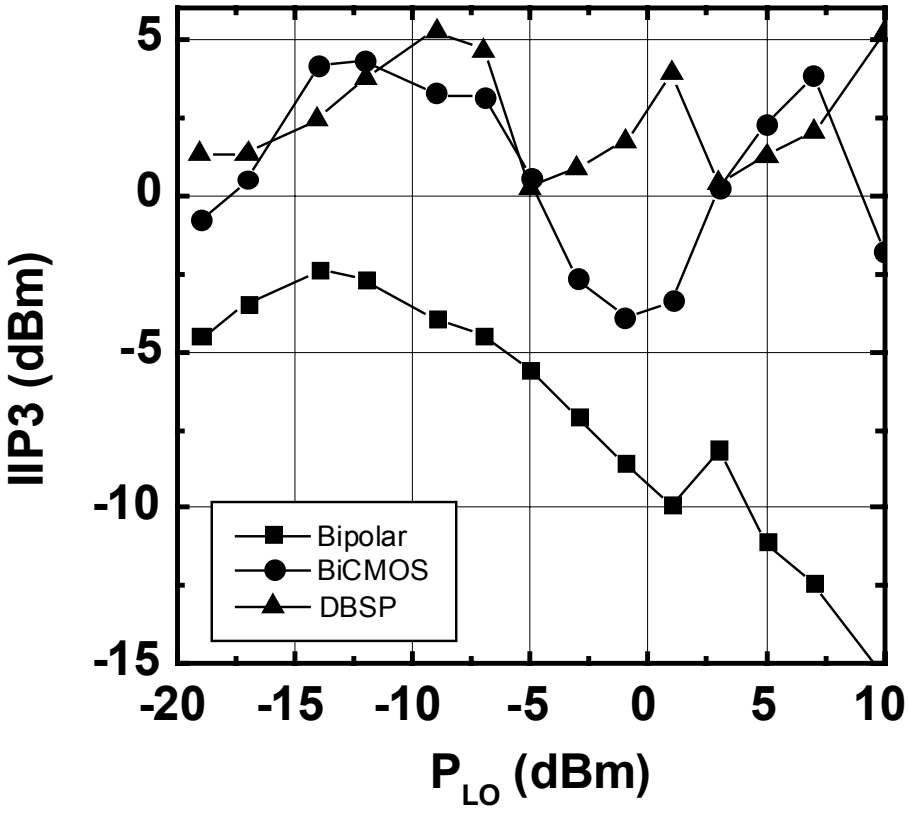

Fig. 7. Measured IIP3 vs. LO power.

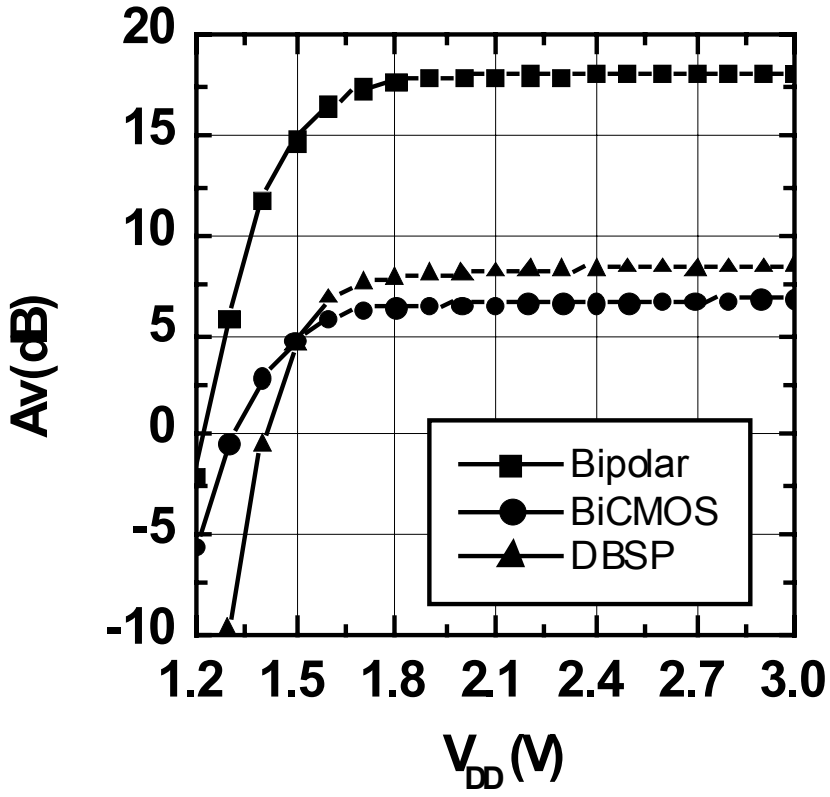

Fig. 8. Conversion gain vs. supply voltage for different mixers.

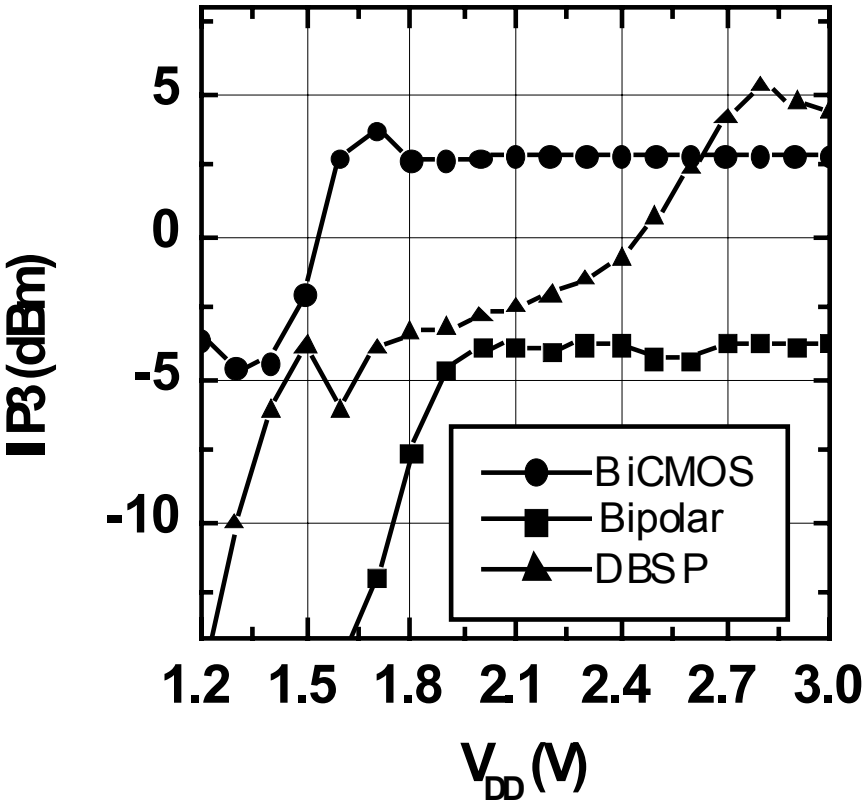

Fig. 9. IIP3 vs. supply voltage for different mixers.

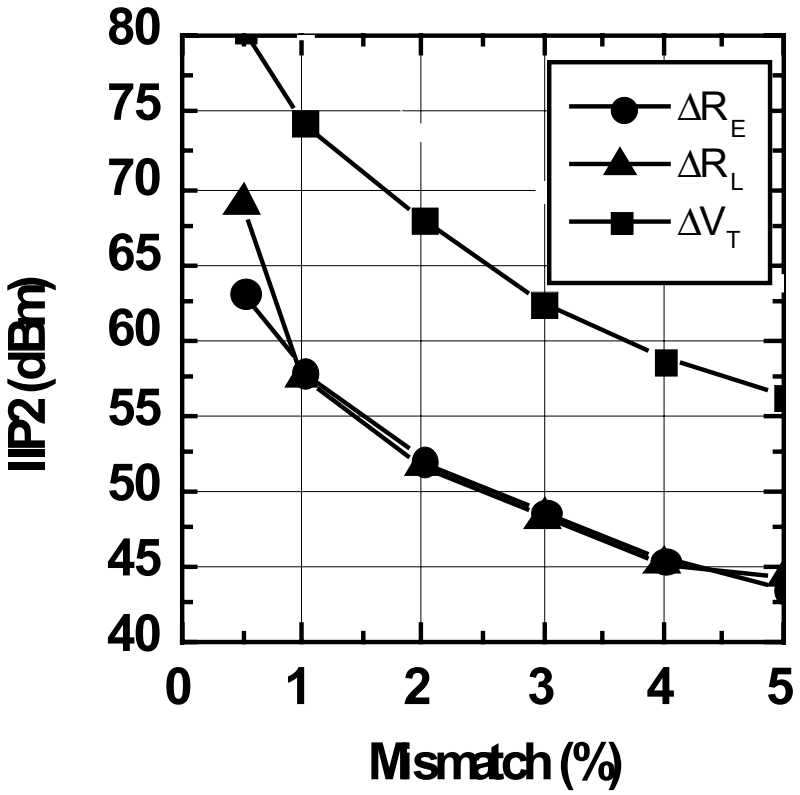

Fig. 10. IIP2 vs. three different mismatches in BiCMOS mixer.

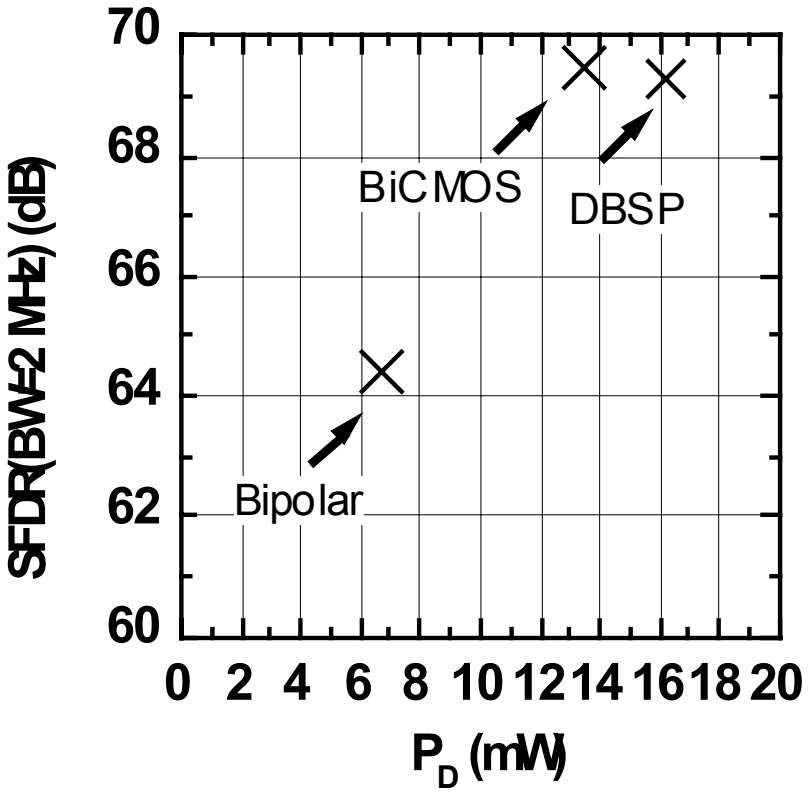

Fig. 11. Spurious free dynamic range of each mixer for 2 MHz bandwidth vs. power dissipation.