DESIGN OF LOW-VOLTAGE ACTIVE MIXER FOR DIRECT CONVERSION RECEIVERS

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ABSTRACT

Evolution and design trade-offs of a high performance, low-voltage downconversion mixer for wireless direct conversion receivers (DCR) are studied in this paper. As a first step, a mixer with active loads and adjustable conversion gain is presented. Then a different mixer topology that provides high conversion gain without deteriorating the linearity and noise performance is discussed. Finally, this topology is found to be well suitable for very low-voltage applications and thus its design and voltage scalability is depicted. The presented mixers are designed using a 0.35-μm BiCMOS process and characterized at 2 GHz frequency.

1. INTRODUCTION

As number of wireless communications subscribers is growing, the demands for wireless services and capacity increase as well. To establish that growth the new third-generation (3G) communications systems will be launched. The current networks will coexist many years during the transition phase with 3G networks. Due to several coexisting cellular systems the demand for multimode user terminals is justified.

The recent evolution in integrated circuit (IC) technologies has been rapid and advanced processes are nowadays capable of providing integrated transceivers for wireless communications [1],[2]. Furthermore, the analog and RF circuitry are following the development of decreasing the supply voltage of the digital circuitry. This voltage downscaling is due to the evolution of CMOS technologies and the reduced breakdown voltages. The direct conversion architecture (Fig. 1) has shown its capability for multimode receivers due to its advantages in adjustability and integrability.

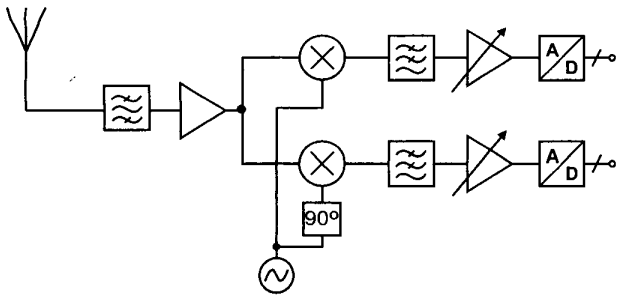

Figure 1. Block diagram of direct conversion receiver.

2. SYSTEM CONSIDERATIONS FOR DOWNCONVERTERS

All receiver building blocks pass through a huge development process before they provide enough modularity and adjustability to be used in a multimode receiver. Not only the bandwidths and radio transmission frequencies but also the modulation schemes, noise, and intermodulation characteristics differ a lot between the cellular standards. Usually the downconversion does not limit the flexibility of the direct conversion receiver for multimode applications. Generally, the only factors affecting that are the frequency handling capabilities of active devices and ac coupling either at the input or output. The specific modulation as well as the multiple access method is very important to take into account in the proper direct downconverter design. The amplitude variations in the modulation as well as the time varying envelope in the TDMA reception can cause a widespread envelope beat around dc as a consequence of the second-order nonlinearity. Usually the mixer dominates the linearity performance of the receiver. The envelope distortion is maybe the most essential individual unwanted phenomena in the direct conversion receivers. Therefore, not only every single building block but also the interfaces between the blocks must be considered properly in the design. The interface between the LNA and mixer must be ac coupled. Thus, the possible second-order distortion due to the LNA is rejected to pass to the mixer input and leak through the whole mixing path. In addition, the RF front-end should provide quite high gain (25-40 dB) in DCR. That is required to suppress the flicker noise contribution of active baseband filters, which is typically quite high. To provide this gain an active mixer is preferred in order to relax the gain requirements of the LNA.

Primarily, the mixer's function in a DCR is to perform direct demodulation from RF down to baseband. Nevertheless, it is practical to implement to the mixer also other functionality in so far as these can be fulfilled without trading off the quality of the downconversion itself. Functionality can be increased by proper interface design to neighboring blocks. High integration level reduces the need of interstage buffering between the blocks. The interface between the mixer and the baseband can be realized without buffering. The first lowpass pole is also practical to execute at the output of the mixer. Thus the out-of-band blocking signals are attenuated before passing to the baseband input. This first filtering should be adjustable in the terminals where both wide- and narrow-band signals are processed. In the filtering of very narrow-band signals, some restrictions apply due to reasonable component values (i.e., large capacitors). Furthermore, to implement a large gain control range the first gain control steps

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can be done already at RF. If the voltage gain of both LNA and mixer can be adjusted the linearity and noise specifications of several different cellular standards can be fulfilled easier.

3. CIRCUIT DESIGN

The conventional low-voltage modification of Gilbert cell mixer is shown in Fig. 2. It is modified from the four-quadrant linear multiplier [3] by removing the tail current source underneath the transconductors. This leads to the lost of the common mode rejection ratio (CMRR). The input devices (Q_{RF1} and Q_{RF2}) perform the VI-conversion. Then the current mode signal is commutated by the LO switching quad (Q_1-Q_4), and changed back to voltage again in the output. Here, different solutions to perform all required signal-processing functions are compared. The first step towards more advanced mixer topology is to replace the bipolar transconductors by NMOS transistors. The MOS devices establish more linear transconductance than the bipolars. Degenerated bipolar transistors could achieve same linearity with same current. However, this is impractical due to the matching problems in the DCR mixer input stage that is the main contributor of the second-order nonlinearity. A drawback is that the intrinsic MOS transconductance is lower but typically sufficient for mixer applications with appropriate sizing. Another drawback is in their more limited frequency handling capabilities. However, the used technology allows the input frequency range of 2-3 GHz.

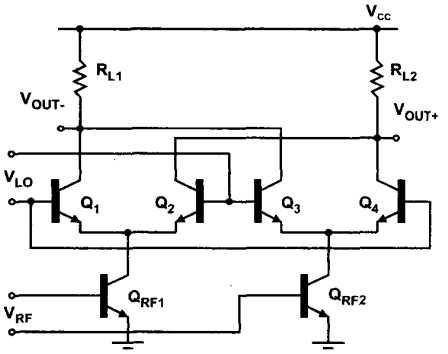

Figure 2. Conventional low-voltage modification of Gilbert cell mixer.

3.1 Variable Gain Mixer

More modularity is achieved by adopting gain control at the output stage of the mixer. The implemented adjustable variable gain mixer (VG mixer) is shown in Fig. 3. The major modifications are in the different input transistors and in the different loading. Another difference is that the mixer has a common-mode feedback (CMFB) circuitry to set the output dc-level to the desired value. The simplified schematic of the CMFB is shown in Fig. 4. As an option, the output dc-level can be set also manually without the CMFB by controlling the gate voltage of the load transistors. This option is established to analyze the effect of the CMFB to the linearity of the mixer.

Selection of bipolar transistors as a switching quad in the direct downconverter is obvious due to the lower 1/f-noise characteristic of the bipolars compared to MOS devices. In addition, the MOS switches typically require larger LO signal swing to exhibit complete switching compared to bipolars.

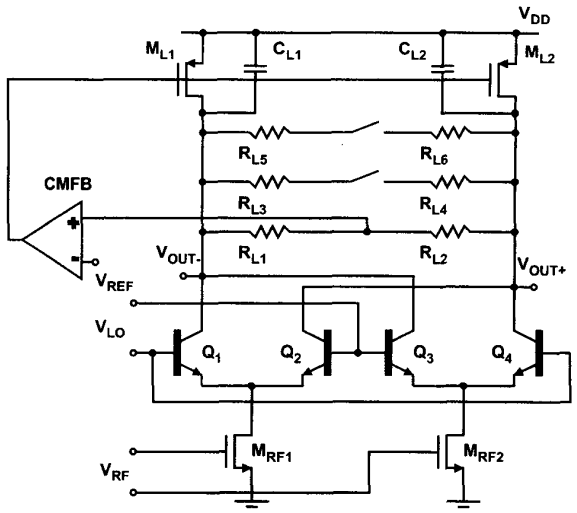

Figure 3. Realized variable gain mixer with common-mode feedback.

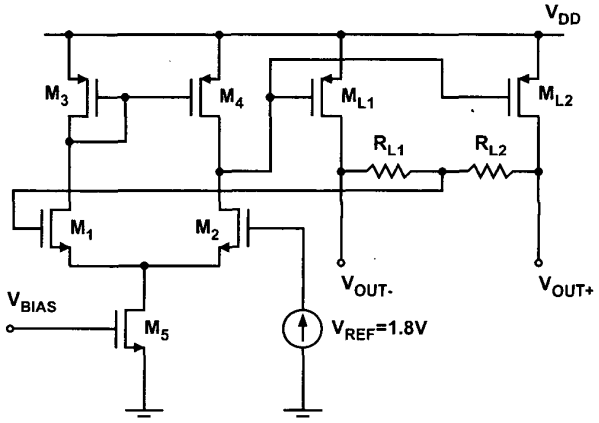

Figure 4. Realized CMFB-circuit.

Active loading compensates the lower transconductance of the NMOS transistor as an input device. The implemented mixer utilizes large long channel PMOS transistors. They are biased into the saturation region acting as current sources thus providing the bias current for the mixer core with negligible effect on the total noise performance. Hence, the use of high impedance load is enabled. In the conventional mixer structure of Fig. 2, the maximal voltage conversion gain is restricted by the usable supply voltage and biasing, and is $(2/\pi)g_mR_L$. As the conversion gain is directly proportional to the load resistance and the transconductance of the input transistors, the increase in the conversion gain easily affects the biasing of the mixer. Instead, in VG mixer, the switched resistors are connected between the differential mixer output in the implementation. They are independent from the biasing yielding a high adjustable conversion gain without significantly deteriorating the linearity. The gain control is realized by switching the parallel resistor pairs between the mixer output nodes. The best linearity is

achieved when the gain control switches are placed between the resistor pairs. The gain and the linearity depend on the value of the load resistance. Thus the load resistance is optimized according to the maximum linearity. In the simulations, the maximum OIP3 can be achieved through the total gain tuning range. Dependence of linearity, and gain from the load is illustrated in Fig. 5. The optimal load in this case is about 1 kΩ, which gives a voltage gain of 18 dB without deteriorating the input intercept point.

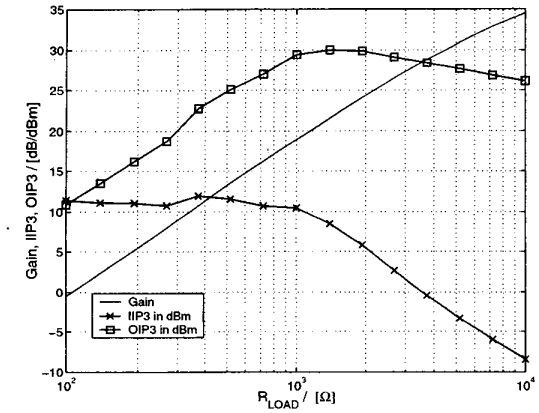

Figure 5. Simulated IIP3, OIP3 and conversion gain vs. total load resistance between the mixer arms.

It can be noticed that the gain curve in Fig. 5 is not straight. The reason for that is that the g_{ds} of the load transistors (M_{L1}, M_{L2}) is not infinitely small. The load transistors have been optimized to be large, in order to have a very small g_{ds}, low 1/f-noise performance, accurate matching, and very low $V_{d,sat}$ to enable maximal linear output voltage swing.

3.2 Current Boosted Mixer

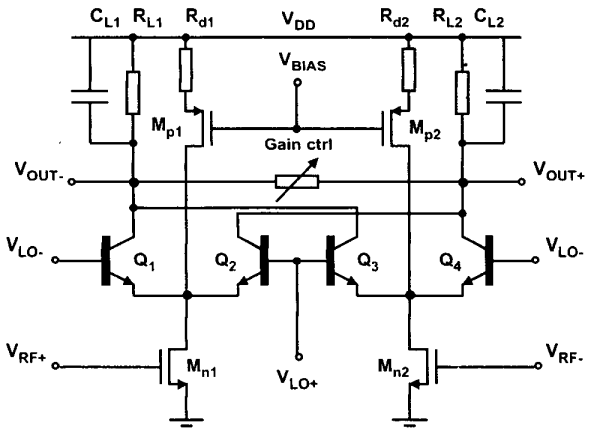

Figure 6. Current boosted mixer.

Fig. 6 illustrates a different double-balanced mixer topology [4],[5]. The mixer is current boosted to better relax the low supply voltage conditions. The additional dc current is fed through the current sources that are long-channel PMOS transistors (M_{p1}, M_{p2}). By current boosting, a lower mixer noise figure is achieved without deteriorating the linearity. In addition, boosting enables increased mixer conversion gain by allowing the higher impedance loading at the mixer output without changing the optimum quiescent point of active devices. Similarly as in the variable gain mixer the conversion gain is adjusted by connecting switched resistive loading between the outputs. The mixer provides three 4 dB gain steps with a maximum gain of 14 dB. The mixer has an RC low-pass pole at the output to relax the out-of-band linearity requirements of the following baseband stages. In addition, the larger resistive loading facilitates the implementation of on-chip RC low-pass pole. Therefore, smaller capacitors can be used. The mixer is designed to drive directly the first baseband stage and is thus unbuffered [6].

3.3 Current Boosted Mixer for Low-Voltage Applications

The current boosted basic mixer topology provides excellent potential to be utilized in very low-voltage circuits. Except of the gain control between the outputs, in which the required gate voltages of the switches easily become a problem. The current boost enables the sufficient conditions for active devices to operate under low-voltage conditions without deteriorating the performance. In Fig. 7, the simulated voltage conversion gain and IIP3 are illustrated. With a proper sizing the mixer provides almost constant performance starting above a 1.5 V supply.

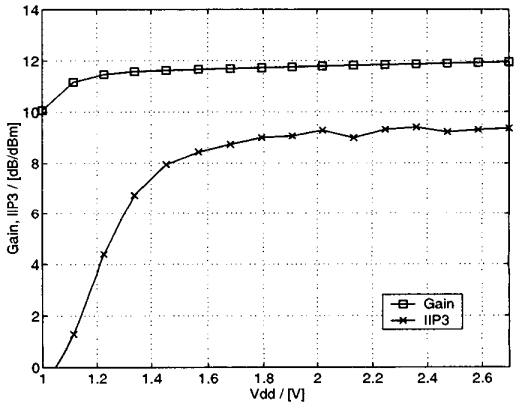

Figure 7. Simulated performance of mixer 3.2 vs. supply voltage.

The minimum supply voltage is set by the threshold voltage of the LO switching devices (Q_1-Q_4) and $V_{d,sat}$ of the input devices (M_{n1}, M_{n2}). Significant modifications must be done to arrange a proper biasing at low supply voltages. High performance operation is achieved, at a very low supply voltage, by biasing the bases of the LO switches to the supply voltage using inductors. Hence, even a 1.0 V supply can be utilized. Using on-chip V_{BE} voltage reference and one external reference current to bias the whole downconverter, as for mixer 3.2, the minimum usable supply voltage is limited to 1.2 V.

The device selection of the additional current sources is one of the most specious design steps in this topology. These current sources are significant noise contributors. Ensuring that the current sources exhibit as small g_m as possible the amount of additional noise is minimized as their thermal noise floor is suppressed. Large source

degenerated PMOS transistors can be used as current sources as in Fig. 6. However, the resistor degeneration is noisy by itself and does not decrease the g_m of the current source devices enough. Better performance can be achieved using small long-channel PMOS devices as the current sources. The simulated difference in mixer noise figure between these two implementations is about 0.5 dB.

4. MEASUREMENTS

The comparison between the different mixer topologies is fair since all mixers have been processed using the same 0.35-µm BiCMOS process. The low-voltage version of the current boosted mixer has not been processed yet and thus its performance is given as simulated values. The reported performance of the mixers 3.1 and 3.2 are based on the measurements. Throughout the mixer design the measurements and simulations have matched very well together. The variable gain mixer has been realized as a stand-alone mixer test structure. However, it is a bit uncertain to characterize its intermodulation performance without proper interfaces to LNA and LO [7]. The first version of the current boosted mixer is implemented together with an LNA [5], and the reported performance is extracted from the RF front-end measurement results and simulations. Another differences in the designs are the different supply voltages. The VG mixer uses a 2.7 V supply, whereas the basic current boosted mixer uses only 1.8 V. The low-voltage version of the current boosted mixer is characterized in Table 1 with 1.2 V supply.

Fig. 8 illustrates the measured downconversion responses of variable gain mixer. The shift in the lowpass frequency corner can be noticed, since the capacitors at the output are fixed and do not change between the gain control steps.

The basic current boosted topology (Mixer 3.2) has been characterized both for 900 MHz and 2 GHz bands. The measured IIP2 is about +60 dBm after extracting the LNA gain from the front-end measurements.

Table 1. Measured performance of implemented mixers.

	Mixer 3.1 Max gain	Mixer 3.1 Min gain	Mixer 3.2 [5]	Mixer 3.3
V_{DD} / [V]	2.7	2.7	1.8	1.2
Gain / [dB]	25.6	15	14	11.4
IIP_3 / [dBm]	-5.3	-1.5	+10	+3.6
OIP_3 / [dBm]	+20.3	+13.5	+24	+15
IIP_2 / [dBm]	+34	+33	+60	-
NF_{DSB} / [dB]	8.3	8.5	9.5	9.2
$L_{LO,RF}$ / [dB]	>50	>50	>58*	-
I_d / [mA]	3	3	6.7	1.8
P_d / [mW]	8.1	8.1	6.03	2.16

*Measured to LNA input @2GHz. Isolation @900MHz is >68 dB.

5. SUMMARY

Up to the present, the emphasis in this research has been placed on the optimization of an integrated direct conversion mixer. After verifying the performance satisfactory for applications the design target was placed in the performance restoring for low-power applications. The selected current boosted mixer fulfills well the strict linearity and noise performance requirements even at very low supply voltages. A specific biasing technique is adopted to guarantee the very low-voltage operation. It is obvious that the downconversion is not limiting the flexibility of the direct conversion receiver for multimode applications. The linearity and noise performance of the mixer can be optimized to provide sufficient operation in most cellular systems.

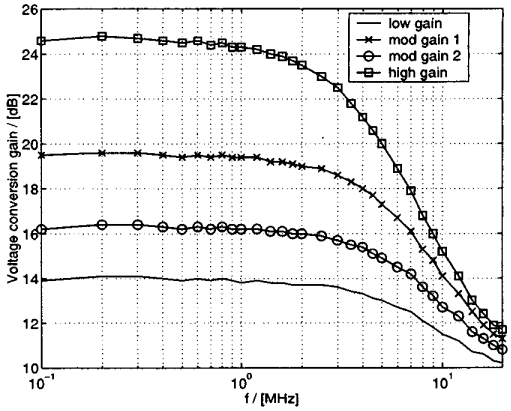

Figure 8. Measured downconversion channel responses at different gain settings of VG mixer.

6. ACKNOWLEDGEMENTS

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