Brief Papers

A 22-mA 3.0-dB NF Direct Conversion Receiver for 3G WCDMA

Jarkko Jussila, *Student Member, IEEE,* Jussi Ryynänen, *Student Member, IEEE,* Kalle Kivekäs, *Student Member, IEEE,* Lauri Sumanen, *Student Member, IEEE,* Aarno Pärssinen, *Member, IEEE,* and Kari A. I. Halonen

***Abstract*—A 2-GHz single-chip direct conversion receiver achieves a 3.0-dB double-sideband noise figure, −14-dBm IIP3 and +17-dBm IIP2 with 60-mW power consumption from a 2.7-V supply. The receiver is targeted for the third generation UTRA/FDD WCDMA system. The low power consumption has been achieved with a proper partitioning and by avoiding buffering between blocks. In the differential RF front end, current boosted quadrature mixers follow the variable-gain low-noise amplifier. At the baseband, on-chip ac-coupled highpass filters are utilized to implement amplification with variable gain having small transients related to gain steps. The outputs of the analog channel selection filters are sampled directly by the two single-amplifier 6-bit pipeline A/D converters. The spurious tones due to the feedthrough of clock harmonics to the RF input increase the noise figure less than 0.1 dB. The receiver has been fabricated with a 0.35-μm 45-GHz f_T SiGe BiCMOS process.**

***Index Terms*—Active filters, analog-to-digital conversion, BiCMOS analog integrated circuits, direct conversion, gain control, low-noise amplifiers, mixers, radio receivers.**

I. Introduction

A SINGLE-CHIP direct conversion receiver, which achieves a low noise figure (NF) and low power consumption together with a reasonable linearity, is presented for the third-generation (3G) WCDMA. The receiver has been designed according to the UTRA/FDD specification proposal [1]. The low NF and power consumption in this receiver are achieved with a careful partitioning between blocks and with unbuffered interfaces between blocks at the signal path. The receiver, in Fig. 1, includes a variable-gain low-noise amplifier (LNA), quadrature mixers, analog channel selection filters, variable-gain amplifiers (VGAs) and 6-bit A/D converters (ADCs).

When an RF input signal is converted to digital form on the same chip, the feedthrough of the clock harmonics to the RF input creates spurious tones, which can fall into the band of the wanted channel, decreasing the signal-to-noise ratio (SNR) [2]. Although wide-band CDMA systems are less sensitive to the downconverted clock harmonics, high isolation is still required. Spurious tones of only a few millivolts can be allowed at the output of a WCDMA receiver having a voltage gain of almost 100 dB.

Manuscript received May 3, 2001; revised July 30, 2001. This work was supported by Nokia Networks, Nokia Mobile Phones, Nokia Foundation, and the Finnish National Technology Agency.

J. Jussila, J. Ryynänen, K. Kivekäs, L. Sumanen, and K. A. I. Halonen are with the Electronic Circuit Design Laboratory, Helsinki University of Technology, FIN-02150 Espoo, Finland (e-mail: jaj@ecdl.hut.fi).

A. Pärssinen is with the Nokia Research Center, Helsinki, Finland.

Publisher Item Identifier S 0018-9200(01)09330-1.

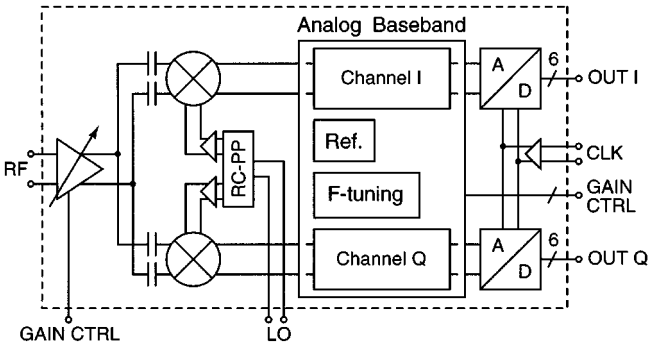

Fig. 1. Receiver block diagram.

The amount of variable gain depends on the receiver input signal range, and the accuracy and sampling rate in the A/D conversion. Most of the variable gain must be implemented in the analog baseband if an ADC with medium or low resolution is used. This requires that sufficient analog channel selection filtering precedes the ADC. The reception in the UTRA/FDD WCDMA system is continuous without idle times. When the gain is changed in discrete steps, large and slowly decaying transients can be generated due to the changes in the offsets of the system. These transients can seriously degrade the signal quality. Thus, VGAs, which do not generate significant transients, are required. Solutions to mitigate this problem will be presented later in this paper.

II. RF Front End

A differential LNA was used to decrease the crosstalk between RF and digital circuits. The bipolar LNA has two modes with a 21-dB difference in the gain. A single branch of the LNA switched into the high gain mode is shown in Fig. 2. In this mode, transistors Q_1 and Q_2 operate as a cascoded common-emitter LNA. In the low gain mode, Q_1 is turned off and Q_3 is operating in a common-base configuration [3]. With a resistive degeneration, the linearity is improved by 17 dB compared to the high gain mode with an equal supply current. In the high gain mode, the base inductance is reduced to a realizable value using the capacitor C_1. The resonator load is damped with parallel resistors. Hence, a sufficient bandwidth and tolerance against device parameter deviations are achieved without a significant increase in the NF. The base inductors of the LNA are implemented with bond wires while the other LNA components are placed on the chip, including all biases and switches. The ac-coupled interface to the quadrature mixers filters out the widespread envelope beat around dc, which is generated in the LNA.

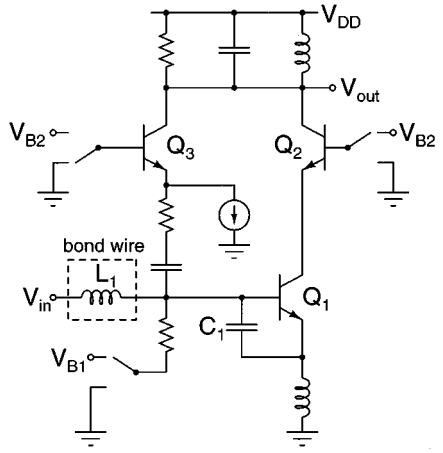

Fig. 2. Single branch of the LNA in high gain mode.

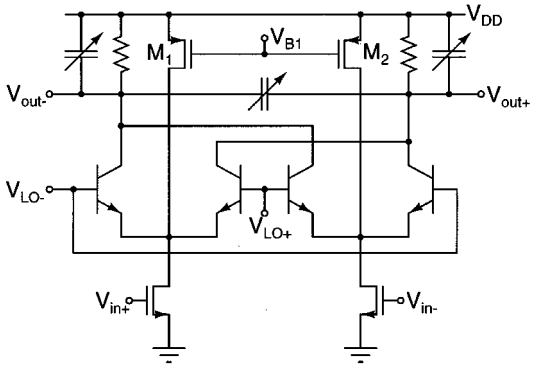

Fig. 3. Downconversion mixer.

The downconversion mixer, in Fig. 3, uses a modified Gilbert-cell topology with current boosting transistors M_1 and M_2 [4]. An external local oscillator (LO) signal is brought through a two-stage *RC*-polyphase filter. The loss of the filter is compensated with limiting LO-driving buffers, which are resistively degenerated bipolar differential pairs with resistor loads. The acceptable LO input power range is from -10 to 0 dBm. The mixer load is an on-chip *RC* structure forming the real pole of the odd-order lowpass filter used for channel selection [5]. Since the resistor values are in the order of 1 kΩ, the capacitor is implemented mostly as capacitors connected between the mixer outputs to minimize the silicon area.

III. Analog Baseband Circuit

The analog baseband circuit consists of two similar signal channels, a frequency tuning circuit and voltage and current references. One signal channel, in Fig. 4, includes an analog channel selection filter, amplification with variable gain, and three on-chip highpass filters (HPFs), which filter out dc offsets.

The channel selection filter is a fifth-order Chebyshev lowpass filter with a 0.01-dB passband ripple and -3-dB frequency of 1.92 MHz. The filter approximates the root raised cosine filter with a 0.22 rolloff, thus realizing the channel selection filtering and chip shaping in the analog domain. Ideally, the adjacent channel attenuation of the channel selection filter is slightly over 36 dB with a 3.84-Mcps chip rate and 5-MHz channel spacing.

The real pole at the mixer output, which in this case is located at 1.2 MHz, increases the linearity considerably by attenuating the out-of-band signals before the signal processing with active devices. A low input-referred noise with a low current dissipation can be achieved by amplifying the signals after the real pole before the other filter sections [5]. Here, the pole is followed by a pMOS differential pair (A1) loaded with the first opamp-*RC* biquad. A differential pair is used instead of a more linear common-source stage to attain common-mode rejection, which is needed to block the in-band common-mode second-order distortion components generated in the mixer. The high-pass filter (HPF1) between the mixer output and differential pair prevents the offset at the mixer output from deteriorating the balance of the differential pair and significantly decreasing the IIP2 of the analog baseband circuit. Two differential opamp-*RC* Tow–Thomas biquads form the complex poles of the filter.

A digitally controllable gain is desireable since the gain can be varied simply with switchable devices according to the adjustment codes calculated in the DSP. However, gain tuning in discrete steps at the baseband can cause problems in systems, which have continuous reception without idle times. When baseband gain is changed, large steps at the output can be generated due to changes in the offsets in the VGA. They degrade the signal quality and can even temporalily compress the receiver. These steps can be filtered out with HPFs but in spectrally efficient modulation schemes the time constants of these filters are usually made large to maintain the high signal quality. The steps are attenuated slowly, which increases the bit-error rate (BER). The solution leading to the maximum achievable signal quality is to use circuit structures, which do not generate these transients. In these structures, the internal offsets are not changed along with the gain steps. In addition, the offsets of the preceding stages are not amplified with a variable gain.

In this design, the adjustable gain is implemented with interstage transconductors A1 and A2, shown in Fig. 4. A1 is a parallel combination of three pMOS differential pairs. Transconductance g_m is decreased in two large steps by disconnecting the inputs of a transconductor from the signal path with V_{G1} and V_{G2}. In order to minimize the transients, the transconductor bias currents are not switched off. The differential pairs implementing the two smaller g_m's are resistively degenerated. In order to have accurate gain steps, the g_m's of the pMOS transistors are forced to be inversely proportional to a resistor value using suitable bias currents.

In A2, the variable attenuation is implemented with a resistive voltage divider, controlled with $V_{G3} \ldots V_{GN}$ and followed by a resistively degenerated pMOS differential pair with a fixed g_m. The step in the attenuator is 3 dB. The stage A2 was placed between the two biquads instead of the output of the second biquad to avoid the need for an extra amplifier to drive the ADC sampling capacitors. In A2, the parasitic capacitance at the differential pair input and the resistor chain limit the bandwidth. To maximize the bandwidth small transistors are used in the differential pair, whose balance is improved by using resistive degeneration. All switches are minimum size and they are arranged into a three-level switch tree.

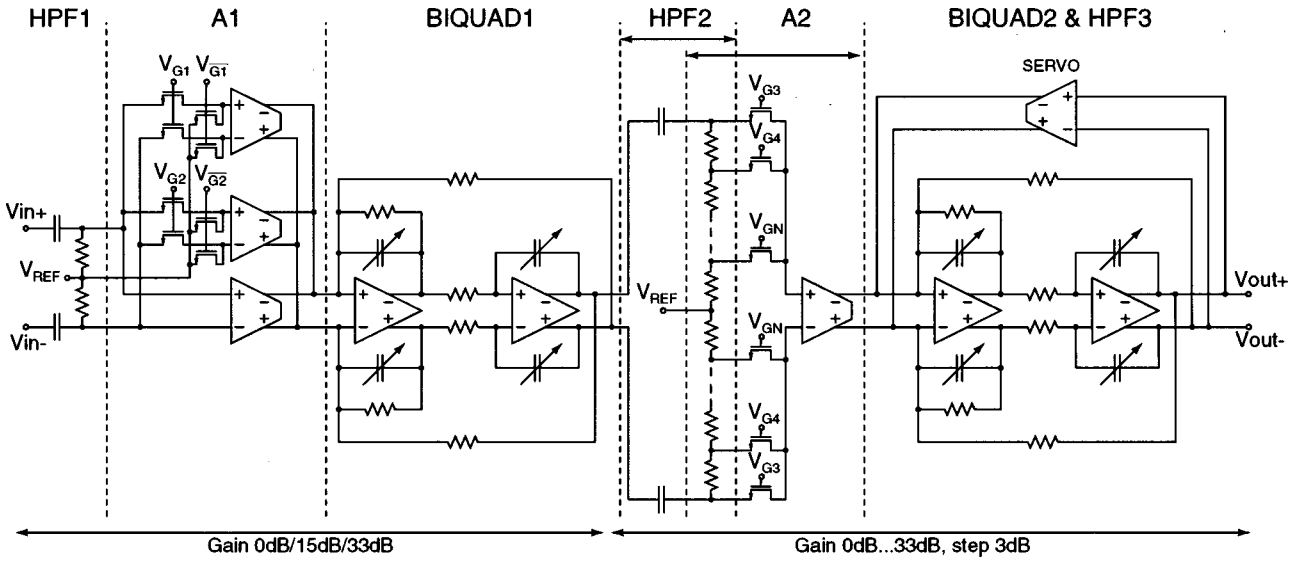

Fig. 4. One signal channel of the analog baseband circuit.

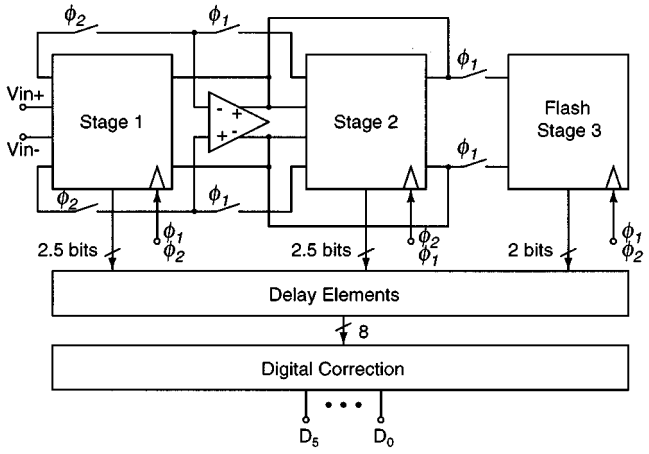

Fig. 5. A/D converter block diagram.

The parasitic capacitances at the input of A1 and at the input of the transconductor in A2 produce slowly decaying transients by temporarily altering the biasing at those locations. These transients become significant when large out-of-band blockers exist and the gain in A1 is changed. The magnitude of the transient depends on the parasitic capacitances and the voltage at the switching node at the switching instant. This problem is alleviated by attenuating the out-of-band signals before the switchable devices. Although the parasitic capacitances at the input of A1 should be minimized to mitigate the transients, large pMOS transistors are used in the differential pairs to maximize matching and IIP2. Large transients are avoided by lowering the gain at small wanted signal powers by increasing the attenuation in A2 and keeping the g_m in A1 constant. The baseband gain ranges from 0 to 66 dB in 3-dB steps.

IV. A/D Converters

The two 6-bit 15.36-MS/s pipeline ADCs sample directly the output of the continuous-time channel selection filter. The ADCs are implemented using two 2.5-bit stages followed by a 2-bit flash stage, as indicated in the block diagram of Fig. 5. Each 2.5-bit stage consists of a multiplying D/A converter (MDAC) and a six-level sub-ADC with a small decoding logic [6]. The properly delayed output bits of each stage are fed to a redundant sign digit (RSD) correction circuitry [7] and finally buffered out of the chip in parallel.

The partitioning of the resolution in the pipeline ADC is optimized for power in terms of the amplifier and comparator power dissipation. The current consumption is further reduced by alternating a single opamp between the two consecutive stages, exploiting the property of successive stages working in opposite clock phases. The shared opamp is a telescopic cascode amplifier with a switched capacitor common mode feedback. The low stage-resolution with RSD correction allows the use of dynamic comparators. The differential pair dynamic comparator, exploited in the design, is also very insensitive to mismatches [6]. The resistor string generating the reference voltages of A/D and D/A conversion is set as a part of the output stage of a Miller compensated amplifier, which adjusts the reference voltages under the variations of the common-mode reference and supply voltage. Only MOS transistors are used in the pipeline ADC building blocks.

Coupling of the clock signal into the sensitive RF input is a key issue in single-chip receiver designs [2]. High isolation is achieved by separating the digital parts into an isolated p-well in BiCMOS process. The contribution of the ADC clock to the substrate noise is reduced using a differential sinusoidal clock input with low amplitude, which is amplified on-chip into a sharp rail-to-rail clock signal. In addition, the output buffers are designed to have slow rise and fall times and on-chip decoupling capacitors are used in the supply voltage lines of ADCs and RF front-end.

V. Experimental Results

The receiver is fabricated with a 0.35-μm 45-GHz f_T SiGe BiCMOS process. The measured performance parameters of the

TABLE I
SUMMARIZED PERFORMANCE OF THE RECEIVER

Supply voltage	2.7 V
Current consumption	22 mA
Voltage gain	12 dB…99 dB
NF (DSB)	3.0 dB
Out-of-band IIP3	-14 dBm / +3 dBm *
Out-of-band IIP2	+17 dBm / +43 dBm *
-1dB compression	-27 dBm / -7 dBm *
LO-to-RF isolation	> 65 dB
S11	< -11 dB / -13 dB *
Filter bandwidth imbalance	< 0.5 %
Adjacent channel attenuation	36 dB

* High / low RF gain

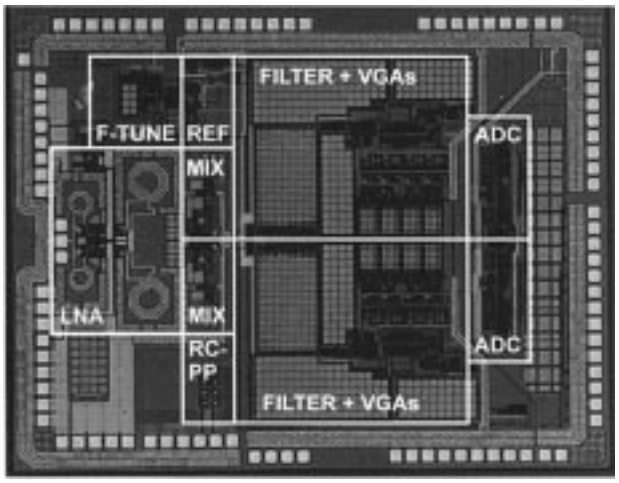

Fig. 6. Chip microphotograph.

receiver are given in Table I. The chip area is 10.3 mm^2 including the bonding pads, which are all electrostatic discharge (ESD) protected. The receiver is mounted and bonded directly on a printed circuit board (PCB). Although separate supplies are used on the chip, a single supply has been used on the PCB. The microphotograph of the receiver is shown in Fig. 6.

The maximum receiver voltage gain at 2.0 GHz is 99 dB and the RF gain step is 21 dB. The measured input matching of the LNA at the high and low RF gain values is better than -11 dB in both WCDMA bands.

The receiver NF is measured at the ADC output. The receiver NF as a function of the LNA quiescent current is shown in Fig. 7. The nominal LNA current used in the measurements is 3.0 mA. With a minor increase in the total current consumption the receiver NF can be decreased to 2.6 dB. The contribution of different building blocks to the noise power generated in the receiver at the maximum gain is approximately 50% in the LNA, 40% in the mixers, and 10% in the analog baseband circuit. The noise generated in the mixer load resistors and in ADC is included in the noise of the analog baseband circuit. The two mixers draw a supply current of 7.0 mA.

The IIP3 and IIP2 of the receiver are measured with 10 and 20.2 MHz and 10 and 10.2 MHz downconverted signals, respectively. The $+17$-dBm IIP2 with the high RF gain is the worst case out of several measured samples. The highest measured IIP2 value with the high RF gain is $+34$ dBm. The input power

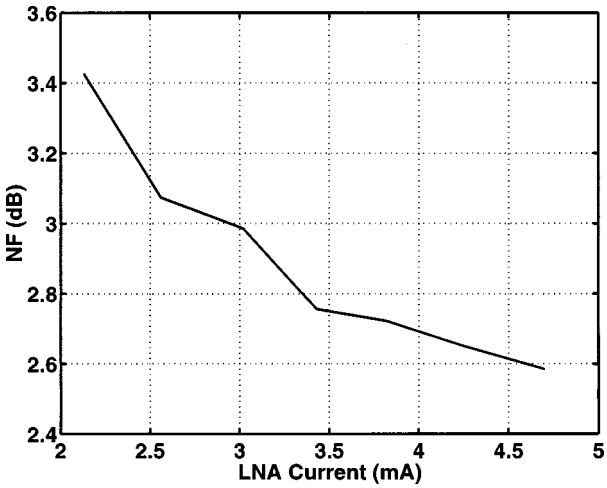

Fig. 7. Receiver NF as a function of the LNA quiescent current.

is referred to 100 Ω due to the differential input. The RF front end limits the IIP3 and IIP2 of the receiver. The blocking performance is defined using a blocker at a 15-MHz offset from LO and measuring the compression of a small in-band signal.

The adjacent channel attenuation has been measured using a modulated WCDMA channel at a 5-MHz offset from the LO. The attenuation compared to a WCDMA channel at the LO frequency is 36 dB when the -3-dB frequency of the filter is 1.92 MHz. The current consumption of the analog baseband circuit is 7.5 mA.

The differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC were found to be 0.27 and 0.18 LSB, respectively. The signal-to-noise plus distortion ratio (SNDR) is at least 35.6 dB, which corresponds to an ENOB of 5.6 bits (7.12-MHz input signal). The SFDR is limited by the third-order distortion and is more than 50 dB over the whole Nyquist band. The two ADCs draw a supply current of 4.5 mA including the twelve output buffers.

The spurious tone due to the feedthrough of clock harmonics to the RF input is measured using a 15.36-MS/s sample rate in the ADCs. The magnitude of the tone is measured as a function of the LO frequency over a 300-MHz band around 2 GHz. The worst clock spurious is smaller than 20 mV at the output, causing less than 0.1-dB degradation in the 3.0-dB total NF.

VI. CONCLUSION

A low-noise low-power single-chip direct-conversion receiver for the UTRA/FDD WCDMA cellular system has been described. A low current consumption of 22 mA has been achieved in a wide-band system, although the receiver includes on-chip ADCs. The transients related to variable baseband gain with discrete gain steps have been decreased using appropriate circuit topologies. The problems related to the clock feedthrough are mitigated in this design. The low NF verifies the appropriate partitioning and shows that the noise from the baseband circuits can be almost negligible even in direct conversion architecture together with a reasonable linearity and low power.

ACKNOWLEDGMENT

The authors would like to thank R. Ahola, M. Waltari, and M. Hirvonen for technical assistance.

REFERENCES

[1] *3rd Generation Partnership Project (3GPP) Technical Specification Group (TSG) RAN WG4 UE Radio Transmission and Reception (FDD)*, TS 25.101 V3.1.0, Dec. 1999.

[2] A. Pärssinen, J. Jussila, J. Ryynänen, L. Sumanen, K. Kivekäs, and K. Halonen, "A wide-band direct conversion receiver with on-chip A/D converters," in *Proc. IEEE VLSI Symp.*, June 2000, pp. 32–33.

[3] K. L. Fong, "Dual-band high-linearity variable-gain low-noise amplifiers for wireless applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 1999, pp. 224–225.

[4] J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, and K. Halonen, "A dual-band RF front-end for WCDMA and GSM applications," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 2000, pp. 175–178.

[5] T. Hanusch, F. Jehring, H.-J. Jentschel, and W. Kluge, "Analog baseband-IC for dual mode direct conversion receiver," in *Proc. ESSCIRC*, Sept. 1996, pp. 244–246.

[6] L. Sumanen and K. Halonen, "A single-amplifier 6-bit CMOS pipeline A/D converter for WCDMA receivers," in *Proc. IEEE ISCAS*, May 2001, pp. 613–616.

[7] S. H. Lewis and P. R. Gray, "A pipeline 5-M sample/s 9-bit analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 22, pp. 954–961, Dec. 1987.