Helsinki University of Technology Electronic Circuit Design Laboratory Publications

Teknillisen korkeakoulun Piiritekniikan laboratorion julkaisuja

Espoo, October, 2002 Report 34

DESIGN AND CHARACTERIZATION OF DOWNCONVERSION MIXERS AND THE ON-CHIP CALIBRATION TECHNIQUES FOR MONOLITHIC DIRECT CONVERSION RADIO RECEIVERS

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Dissertation for the degree of Doctor of Science in Technology to be presented with due permission for public examination and debate in Auditorium S4 at Helsinki University of Technology (Espoo, Finland) on the 18th of October, 2002, at 12 o'clock noon.

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Preface

The work for this thesis has been carried out in the Electronic Circuit Design Laboratory (ECDL) of Helsinki University of Technology between April 1999 and June 2002. The research has been a part of an industrial-academic co-operation project between the ECDL, Nokia Networks and Nokia Mobile Phones.

The partial funding of this research by the industrial partners Nokia Networks and Nokia Mobile Phones, as well as by the National Technology Agency (TEKES), is gratefully acknowledged. In addition, I thank the Foundation of Technology (TES), Emil Aaltonen Foundation, Nokia Foundation, and the Finnish Society of Electronics Engineers (EIS) for granting my post-graduate studies.

I am grateful to Prof. Kari Halonen for the opportunity to work with this challenging topic and for his guidance. Prof. Robert Weigel and Prof. Torben Larsen are acknowledged for reviewing my thesis. I wish to express my gratitude to Dr. Aarno Pärssinen for instructing me throughout my post-graduate studies, as well as his expert advice. In addition I would like to thank Dr. Barrie Gilbert for personal discussions.

During my thesis work I was lucky to belong to a powerful research team. I want to thank the team members, Jussi Ryynänen, Jarkko Jussila, and Lauri Sumanen, for creating a great working atmosphere and for fruitful collaboration. Thanks are also due to Timo Knuuttila, who originally proposed the research project on direct conversion receivers. In addition, thanks belong to all my colleagues in the ECDL, and particularly to our secretary Helena Yllö.

I wish to thank all my friends from the Athletic Club Toffee for various leisure time activities. My mother Kristiina deserves warm thanks for her continuous support during my studies. I also want to mention my father Heikki†, who taught me to read and to doubt everything. I am thankful to my parents-in-law, Airi and Heikki, for their encouraging support to my studies and decisions. My dearest thanks belong to my beloved wife Outi. Without your love and understanding this work would not have been completed.

Kalle Kivekäs

September 2002

Abstract

This thesis consists of eight publications and an overview of the research topic, which is also a summary of the work. The research described in this thesis is focused on the design of downconversion mixers and direct conversion radio receivers for UTRA/FDD WCDMA and GSM standards. The main interest of the work is in the 1-3 GHz frequency range and in the Silicon and Silicon-Germanium BiCMOS technologies. The RF front-end, and especially the mixer, limits the performance of direct conversion architecture. The most stringent problems are involved in the second-order distortion in mixers to which special attention has been given. The work introduces calibration techniques to overcome these problems. Some design considerations for front-end radio receivers are also given through a mixer-centric approach.

The work summarizes the design of several downconversion mixers. Three of the implemented mixers are integrated as the downconversion stages of larger direct conversion receiver chips. One is realized together with the LNA as an RF front-end. Also, some stand-alone structures have been characterized. Two of the mixers that are integrated together with whole analog receivers include calibration structures to improve the second-order intermodulation rejection. A theoretical mismatch analysis of the second-order distortion in the mixers is also presented in this thesis. It gives a comprehensive illustration of the second-order distortion in mixers. It also gives the relationships between the dc-offsets and high IIP2. In addition, circuit and layout techniques to improve the LO-to-RF isolation are discussed.

The presented work provides insight into how the mixer immunity against the second-order distortion can be improved. The implemented calibration structures show promising performance. On the basis of these results, several methods of detecting the distortion on-chip and the possibilities of integrating the automatic on-chip calibration procedures to produce a repeatable and well-predictable receiver IIP2 are presented.

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List of symbols and abbreviations

Symbols

α	Roll-off factor
η	LO duty-cycle factor
Δ	Difference
ω	Angular frequency
ϕ	Signal phase
Ω	Ohm
α'_n	Relative n^{th}-order nonlinearity factor
η_M	Negative gate function
η_P	Positive gate function
A_V	Voltage gain
C/I	Carrier-to-interferer ratio
C_{je}	Base-emitter junction capacitance
F	Noise factor
f_T	Unity current gain frequency
G	Power gain
g_m	Transconductance
G_m	Transconductance
ICP	Input compression point
$iip2$	Input referred intercept point of second-order
$IIP2$	Input referred intercept point of second-order
$iip2_{SE}$	Single-ended input referred intercept point of second-order
$iip3$	Input referred intercept point of third-order
$IIP3$	Input referred intercept point of third-order
$IMD2$	Intermodulation distortion product of second-order
$IMD3$	Intermodulation distortion product of third-order
$IP2$	Intercept point of second-order
$IP3$	Intercept point of third-order
K_P	Transconductance parameter
L	Loss
NF	Noise figure
$OIP2$	Output referred intermodulation product of second-order
$OIP3$	Output referred intermodulation product of third-order
P_{IMD2}	Second-order intermodulation product
$P_{IMD2,in}$	Input referred second-order intermodulation product
P_{IMD3}	Third-order intermodulation product
$P_{IMD3,in}$	Input referred third-order intermodulation product
P_{in}	Input power
P_{out}	Output power
r_b	Base resistance
R_E	Emitter resistor
R_L	Load resistor
S_{11}	Scattering parameter, reflection
V_{BE}	Base-emitter voltage
V_{CE}	Collector-emitter voltage

V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
v_{in}	Input voltage
v_{out}	Output voltage
v_{pp}	Voltage, peak-to-peak
V_T	Threshold voltage, Thermal voltage

Abbreviations

2G	2nd generation
3G	3rd generation
3GPP	3rd generation partnership project
A/D	Analog-to-digital
Ac	Alternating current
ADC	Analog-to-digital converter
AM	Amplitude modulation
ASIC	Application specific integrated circuit
AWGN	Additive white gaussian noise
BER	Bit-error-rate
BiCMOS	Bipolar complementary metal-oxide semiconductor
BJT	Bipolar junction transistor
BS	Base station
CCDF	Complementary cumulative distribution function
CDMA	Code division multiple access
CMDR	Common-mode to differential ratio
CMFB	Common-mode feedback
CMOS	Complementary metal oxide semiconductor
CMRR	Common-mode rejection ratio
CW	Continuous wave
DBSP	Double-balanced switching pair mixer
DPCH	Dedicated physical channel
D/A	Digital-to-analog
Dc	Direct current
DCR	Direct conversion receiver
DCS	Digital communications system
DNL	Differential nonlinearity
DS	Direct sequence
DSB	Double side band
DSBSC	Double sideband suppressed carrier
ECL	Emitter coupled logic
EDGE	Enhanced global system for mobile communications
ENOB	Effective number of bits
ESD	Electrostatic discharge
FDD	Frequency division duplex
FFT	Fast Fourier transform
FR4	Epoxy/glassfibre substrate material
GMSK	Gaussian minimum shift keying
GPRS	General packet radio service
GSM	Global system for mobile communications

HBT	Hetero junction bipolar transistor
HPF	Highpass filter
I	In-phase
IF	Intermediate frequency
INL	Integral nonlinearity
IP	Internet protocol
LNA	Low noise amplifier
LO	Local oscillator
LSB	Least significant bit
MDAC	Multiplying D/A converter
MOS	Metal oxide semiconductor
MS	Mobile station
NMOS	N-type metal-oxide semiconductor
PAR	Peak-to-average ratio
PCB	Printed circuit board
PCS	Personal communications system
PEP	Peak envelope power
PGA	Programmable gain
PM	Phase modulation
PMOS	P-type metal-oxide semiconductor
Q	Quadrature-phase, quality factor
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
RF	Radio frequency
RMS	Root mean square
RO4350®	Glass reinforced hydrocarbon/ceramic laminate material Rogers corp.
RRC	Root raised cosine
RSD	Redundant sign digit
Rx	Reception
SAW	Surface acoustic wave
SFDR	Spurious free dynamic range
Si	Silicon
SiGe	Silicon-Germanium
SNDR	Signal-to-noise plus distortion ratio
SNR	Signal-to-noise ratio
SSB	Single side band
TDD	Time division duplex
TDMA	Time division multiple access
Tx	Transmission
UMTS	Universal mobile telecommunications systems
UTRA	UMTS terrestrial radio access
VCC	Voltage common collector, positive supply-voltage
VCCS	Voltage controlled current source
VDD	Voltage, positive supply-voltage
WCDMA	Wideband code division multiple access
WLAN	Wireless local area network
VG	Variable gain
VGA	Variable gain amplifier

List of publications

P1 K. Kivekäs, A. Pärssinen, K. Halonen, "Active Mixers for Direct Conversion Receivers with 0.35-µm BiCMOS," *Analog Integrated Circuits and Signal Processing*, vol. 26, No. 1, pp. 17-26, Jan. 2001.

P2 K. Kivekäs, A. Pärssinen, J. Jussila, J. Ryynänen, K. Halonen, "Design of Low-Voltage Active Mixer for Direct Conversion Receivers," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. IV, pp. 382-385, Sydney, Australia, May 2001.

P3 J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, K. Halonen, "A Dual-Band RF Front-End for WCDMA and GSM Applications," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1198-1204, Aug. 2001.

P4 J. Jussila, J. Ryynänen, K. Kivekäs, L. Sumanen, A. Pärssinen, K. Halonen, "A 22mA, 3.0dB NF Direct Conversion Receiver for 3G WCDMA," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 2025-2029, Dec. 2001.

P5 K. Kivekäs, A. Pärssinen, K. Halonen, "Characterization of IIP2 and DC-Offsets in Transconductance Mixers," *IEEE Transactions on Circuits and Systems Part—II: Analog and Digital Signal Processing*, vol. 48, pp.1028-1038, Nov. 2001.

P6 K. Kivekäs, A. Pärssinen, J. Ryynänen, J. Jussila, K. Halonen, "Calibration Techniques of Active BiCMOS Mixers," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 766-769, June 2002.

P7 J. Ryynänen, K. Kivekäs, J. Jussila, L. Sumanen, A. Pärssinen, K. Halonen, "Single-Chip Multi-Mode Receiver for GSM900, DCS1800, PCS1900, and WCDMA," Accepted for publication in *IEEE Journal of Solid-State Circuits*.

P8 J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, K. Halonen, "RF Gain Control in Direct Conversion Receivers," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, vol. IV, pp. 117-120, Phoenix, USA, May 2002.

Contribution of the author

As a general guideline, the first author of each paper has the main responsibility for the manuscript.

In paper **P1,** I carried out the circuit design, analysis, and measurements. Aarno Pärssinen involved in the work as an instructor. The paper is an extension of a conference paper [K1], and was invited to the journal.

I was responsible for designing and analyzing the circuits presented in paper **P2**, except the common-mode feedback circuit, which was designed by Jarkko Jussila.

My contribution in paper **P3** is mixer design. The system partitioning and measurements were performed together with Jussi Ryynänen, who designed the LNA and single-ended to differential converter. He also had the main contribution to the multi-mode system considerations. In addition, I participated in the writing of the manuscript.

My contribution in paper **P4** was in the area of RF design. I designed the downconversion mixers and LO buffers. The device-level simulations for the whole RF front-end were made in co-operation with Jussi Ryynänen. I also participated in the measurements and writing of the manuscript.

In paper **P5**, I had the main responsibility for the theoretical analysis, simulations, and measurements. However, the work was carried out in co-operation with Aarno Pärssinen. He instructed me and also contributed to the theoretical work and analysis of the results.

I carried out the circuit design of downconverters, calibration circuitry, and LO generation of paper **P6**. I made the RF top-level simulations together with Jussi Ryynänen, who designed the LNA. Jarkko Jussila designed the baseband circuitry. The measurements were a co-operative effort.

In paper **P7**, I carried out the circuit design of downconverters, mixer calibration circuitry, and LO generation. I performed the RF top-level simulations together with Jussi Ryynänen. We also co-operated in the design of the interface between the LNA and mixer. Jussi Ryynänen designed the LNA, while Jarkko Jussila designed the analog baseband circuitry. Jussi Ryynänen and Jarkko Jussila carried out most of the measurements. I participated in the writing of the manuscript.

Jussi Ryynänen had the main responsibility for paper **P8**, although the analysis and manuscript writing were performed together with the co-authors. The contributions of the analyzed circuit implementations are described in connection with papers **P6** and **P7.**

Other related papers that I have authored or co-authored (not included in this thesis) are labeled as [KI-KV] in the reference list.

1 Introduction

1.1 Background

Current developments in mobile communications standards are directed towards the third-generation (3G). The launch of the third-generation networks in Europe has been delayed from the originally planned time of spring 2001, while initial 3G services will not be offered in most European countries until 2003. In the meantime, the development work with second-generation (2G and 2.5G) telecommunication standards continues. The advanced upgrades of the GSM standard, the general packet radio service (GPRS) and the enhanced data rates for GSM (EDGE) are already able to provide wireless Internet and other wireless applications requiring high-speed data connection for cellular users. The transition from second-generation mobile communications to third-generation has therefore already started. These 2.5G systems are making the shift from circuit-switched to packet-switched IP-based networks. In the course of writing this thesis, it was estimated that the adoption of 3G services will be slow in the early years and will have remained less than 30% of the worldwide mobile-subscribers by 2010 [1].

This means that there will not be a clear transition period in which the 3G systems replace the current systems. Even if there were, the operators would have to provide all the required services and network coverage for the 2G and 2.5G systems, as well for the 3G, for a lengthy period after the launching of the 3G networks. That is to say, the existing user terminals are being renewed relatively slowly, while the operators have to continue providing coverage and services, and will have to continue doing so even following the expiry of the production of older technology. The maintenance of several overlapping networks is expensive for operators because the current large investments do not bring in short term revenues. On the other hand, from the viewpoint of the cellular user, it is very advantageous to have different systems and services that they can use to meet their different needs.

For the hardware manufacturers, the transition phase is challenging because they have to deliver both user terminals and networks for a number of co-existing systems. Therefore, it would be of great practical help to have flexible hardware sub-units that could be reconfigured according to the system used, both in base stations and user equipment. For example, all wireless terminals need the analog radio receiver and transmitter to communicate through the air-interface at several different frequency bands. A lot of emphasis has already been placed on the work of miniaturizing these terminal sub-units from discrete electronic solutions to integrated circuits (IC) starting from the late 1980's. The achievements in reducing the production costs per unit have been significant, but the work is still under way. However, there is usually a particular receiver and transmitter for each application, specific to a certain cellular standard. If the same receiver or transmitter could withstand several different standards and applications, the IC production volumes could be increased, which would result in even lower unit production costs. In addition, the wireless local area networks (WLANs) are becoming mass-produced products in both homes and offices. In general, the same receiver ICs could be used in WLAN terminals also. This market drive and the developments in enabling integrated circuit technology have triggered research activities relating to direct conversion receivers (DCRs) [2]. Out of several different receiver architectures, a DCR can be integrated into the remaining analog and digital sections of the transceiver, thus having the potential to constitute a "single-chip" radio. Besides, the direct conversion receiver favors multi-mode, multi-standard applications and thereby constitutes another step towards the "software radio". A direct conversion receiver has special potential in low-cost, small size, applications due to its advantages in integration.

The superheterodyne receiver [3] has been the overhead receiver architecture since the early decades of the 20th century because of its superiority in terms of performance. However, it cannot be integrated on the single chip by current standard technological advances. Instead, the DCR[1] is a practical choice of receiver architecture for mobile terminals or small base stations. Its performance is competitive to the superheterodyne receiver in most current and future cellular standards. It is a common ambition among the hardware manufacturers to have a receiver chip that meets the specifications of the most commonly used cellular standards.

1.2 Objectives of the work

The research described in this thesis focuses on the design of downconversion mixers for direct conversion radio receivers. The RF front-end, especially the mixer, limits the performance of direct conversion architecture. The most stringent problems are those involved in the second-order distortion in mixers, to which special attention has been given in this thesis. Also, the calibration techniques to overcome these problems are presented and discussed. Their effective development establishes the integration of high performance direct conversion receivers and lower cost integrated RF solutions for wireless systems.

1.3 Contents of the thesis

This thesis is divided into two parts. In the first part, an overview of the monolithic mixer design issues for direct conversion receivers is given to summarize the technical work that has been carried out. In the system aspects, the overview is focused on the UTRA/FDD WCDMA and the GSM standards [5],[6],[7]. In Chapter 2, the direct conversion receiver architecture is discussed and fundamental concepts and definitions introduced to give perspective to mixer basics. A more detailed description of bipolar Gilbert-cell mixer design is given in Chapter 3. In Chapter 4, the envelope distortion in direct conversion receivers is introduced. Chapter 5 summarizes the different solutions to overcome the problems of improper even-order intermodulation rejection in the downconversion mixer of a DCR. In addition, the I/Q-amplitude balancing method introduced in paper **[P6]** is supplemented at the end of Chapter 5. The second part of this thesis contains the published papers.

[1] To avoid any confusion, it must be emphasized that the direct conversion receiver is definitely not a new receiver architecture. It was invented as long ago as 1924. Tucker published a historical overview of its early days in 1954 [4].

2 Direct conversion receiver and fundamental definitions

The design philosophy of the integrated direct-conversion receiver differs substantially from that of the traditional radio receiver. A dramatic difference is that the interfaces between different blocks do not need to be matched. The dimensions of the semiconductor chip are electrically very small compared to the signal wavelength in the range of 1-6 GHz. Therefore the signals, even at the RF interfaces on the chip, can be considered to preserve their phase. Thus, the components can be considered as lumped elements, instead of distributed ones, and signals as voltages instead of waves. Only the off-chip signal routings must be matched. The direct unmatched on-chip interfaces between the different blocks increase the design flexibility but, on the other hand, they complicate the use of traditional performance parameters familiar to radio engineers. As the impedance levels are quite arbitrary, it is preferable to consider signals as voltages and refer those to receiver input rather than use the power-defined quantities. The interfaces of the mixer between its neighboring blocks are discussed in detail in Section 3.2.

The block diagram of a direct conversion receiver is shown in Figure 2.1. The strengths of the architecture are that it does not suffer from the image problem, and it provides a possibility of a high degree of integration. Furthermore, the architecture is favored for multi-mode receivers due to its reconfigurability. The fundamental design aspects of DCRs have been presented, e.g., in [8],[9], and [10]. Many objections against the direct conversion architecture have been stated mainly on the grounds of its dc-offset problem and improper even-order intermodulation rejection. However, the dc-offsets can be handled successfully as presented, e.g., in [2] and [11]. Also, techniques to improve the even-order intermodulation rejection exist, as will be shown in Chapter 5. A proper comparison of the receiver architectures for WCDMA mobile terminals is given in [12].

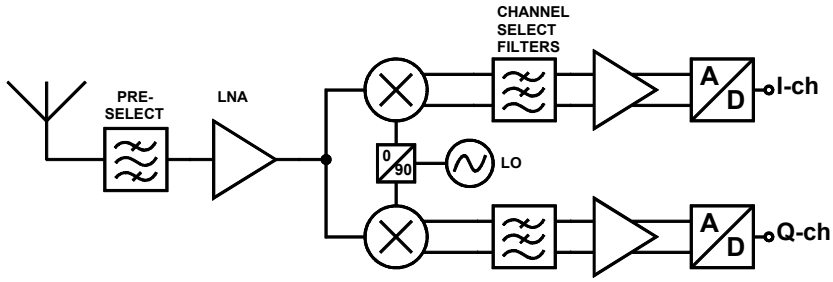


Figure 2.1 *Direct conversion receiver.*

2.1 RF front-end and mixer topologies

The partition of the RF front-end can be made in a number of different ways in a DCR. Different system issues, like the required sensitivity, duplex method, and modulation, set the requirements for the selection of the topology to be used. In addition, the RF front-end can be integrated or placed in proximity to many sources of interference, resulting in an increased common-mode rejection requirement. Furthermore, the RF and baseband interfaces, both on-chip and out-of-chip, can be of either a single-ended or differential form. Hence, it must be carefully considered whether a single-ended signal path or a balun should be used. One partition is always a trade-off with some parameter. The different RF block partition issues are discussed below.

The antenna, which is a single-ended structure, feeds the received signal to a bandpass filter that is used for the preselection of the received RF band. In FDD systems, the bandpass filter is also used for duplexing, i.e., to connect the separate reception and transmit branches to the same antenna. It also suppresses the transmitter signal leakage to the sensitive receiver port. In general, the antenna and the RF filters are off-chip components. The RF filter feeds the signal to the LNA, which is needed to amplify the RF signal in order to reduce the noise contribution of the following stages. The LNA can be connected directly or through a filter to the downconversion mixers. The lowpass channel selection filters follow the mixers.

The preselection filter is usually a surface acoustic wave (SAW) or ceramic filter and placed out-of-chip. These filters are mainly single-ended structures, although recently filters performing the single-ended to differential conversion have also become available. However, if a balanced LNA is used, then either an additional balun before it or a preselection filter providing a balanced output has to be used. Both of these configurations suffer from decreased sensitivity due to the increased insertion loss before the LNA. The fully differential signal path has greater immunity from certain interference mechanisms such as substrate noise, but typically at the expense of increased current consumption in the LNA. Furthermore, the single-ended LNAs usually require less die area than the differential LNAs, especially if they use tuned reactive load and inductive degeneration. The configuration in which the single-ended LNA feeds the signal to mixers that perform the single-ended to differential conversion is widely used in many commercial mixer and RF front-end ICs. Although this is a practical solution, the most used monolithic mixer topology, Gilbert-cell, unfortunately suffers from a few decibels lower linearity if driven single-endedly.

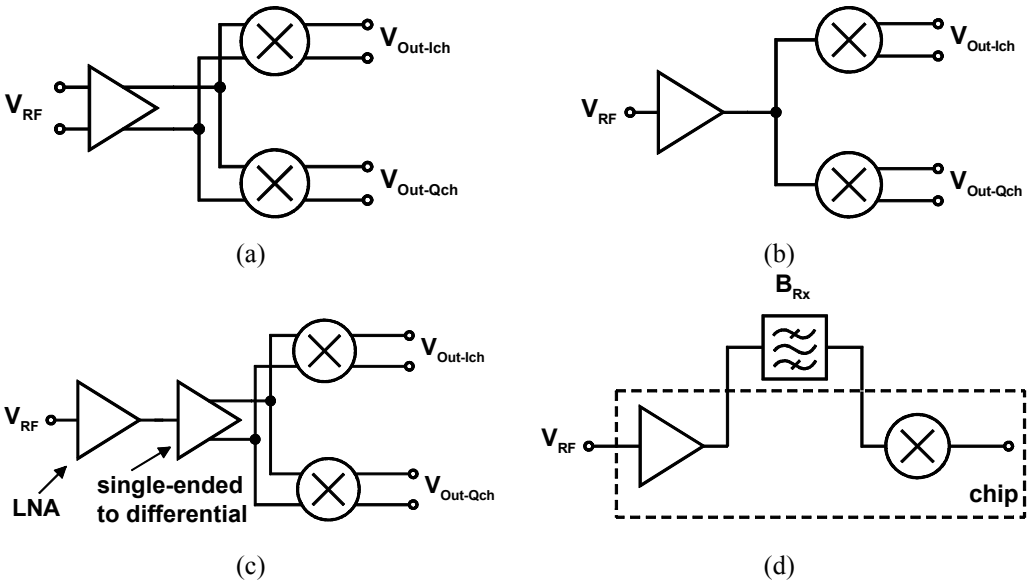


Figure 2.2 *Different direct conversion RF front-end configurations, a) fully differential, b) single-ended LNA driving balanced mixers, c) single-ended LNA, on-chip single-ended to differential conversion and fully differential mixers, and d) either single-ended or differential off-chip bandpass filtering between the LNA and mixers.*

The different LNA-mixer block partitions are shown in Figure 2.2. The LNA and mixers can be fully differential structures, as shown in Figure 2.2a. In this configuration, a double-balanced mixer topology is used. Figure 2.2b illustrates the LNA that is single-ended and drives mixer single-endedly. In this case the mixer is either single- or double-balanced. A single-balanced mixer topology is

preferred to achieve a better linearity if the mixer is driven single-endedly. It is also possible to integrate the single-ended to differential converter on chip as in Figure 2.2c. It can be implemented as an active stage between the LNA and mixers as in [K3] or by using monolithic transformers as presented, e.g., in [13],[14],[15]. Figure 2.2d shows a configuration in which an off-chip bandpass filter is placed between the LNA and mixers. The off-chip filter can be either fully single-ended or perform the single-ended to differential conversion as in [16] and [17]. This configuration is somewhat different compared to the others as both the output of the LNA and input of the mixers must be matched to the filter. However, filters also for higher than 50 Ω impedance levels are available. This configuration is sometimes preferred in FDD systems to provide better isolation between the transmitter and receiver.

2.2 Mixing phenomena

In principle, mixing in communications systems is considered as the frequency translation of the signal from one carrier to another or either attaching or removing the baseband signal to or away from the carrier. For the first time, the use of a mixer stage was utilized in the superheterodyne first reported by Armstrong [3]. He called mixer the "first detector" to convert the incoming RF signal to a lower intermediate frequency (IF). Mixing and frequency multiplication are nonlinear operations by nature. Although the nonlinear characteristic is essential to mixers, their signal handling capacity is limited due to their nonlinearity at large signal amplitudes. The mutual dependencies of the IF, RF, and local oscillator (LO) frequencies are given as

$$f_{IF} = \left| f_{RF} \pm f_{LO} \right| . \tag{2.1}$$

In a DCR, the mixer downconverts the signal from a particular radio carrier directly to the baseband. It provides either conversion gain or conversion loss to the signal. These are measures that compare signal strength before and after the frequency translation at different frequencies. If the interfaces are impedance matched, the power gain is typically used. Instead, if the interfaces are not matched, as is often the case with the mixers in DCRs, a voltage or current gain is given.

2.3 Linearity and nonlinearity

Primarily, all electronic circuits are nonlinear, even though most are only weakly nonlinear in their actual ranges of operation. The linear circuits are defined as those for which the superposition principle holds. If excitations x_1 and x_2 are applied separately to a circuit having responses y_1 and y_2, respectively, the response to the excitation $ax_1 + bx_2$ is $ay_1 + by_2$, where a and b are arbitrary constants [18]. Roughly, the effect of the nonlinearity is its ability to generate harmonics and spurious frequencies. It can happen if the response of a circuit is nonlinearly dependent on the excitation. One special case is the clipping. Although the response would be otherwise linear, it is distorted and spurious frequencies that are generated when the signal is clipped at particular high excitation levels. If the excitation of a nonlinear system consists of several frequency tones or a modulated channel, the separate frequency tones intermodulate each other, thus influencing linear combinations of all excitation frequencies and their harmonics producing a response as

$$f_{n,m,k} = nf_1 + mf_2 + kf_3, \qquad n,m,k \in \mathrm{Z} . \tag{2.2}$$

Mixers are very nonlinear time variant circuits. As mentioned in the previous sub-section, the nonlinearity is essential to enable the mixers to perform the frequency translation. Their operation is

based on either the switching of the signal path, or the modulation of a nonlinear component by a large signal tone, with the presence of the information-contenting signal to be converted in frequency. Despite the receiver architecture, the linearity performance of the receiver is most often limited by the first downconversion stage.

In radio receivers, in which nearby channels are also occupied, the nonlinearity leads to the aliasing of the power from the unwanted channels to the receiver passband. Therefore, the receivers and their building blocks, if they are to be used in applications that require large dynamics, must be sufficiently linear. Different methods of analyzing the linearity performance of circuits are discussed, e.g., in [18]. Two methods are suitable for hand calculations. Analysis using Volterra kernels is presented in references [19],[20],[21],[22],[23]. Another technique is to use memoryless power series analysis. The power series are often used because they are simple and illustrate the phenomenon quite intuitively. Here, the analysis using power series is used to illustrate the two-tone test that is often used to characterize the linearity performance of the receiver. In the two-tone test an input signal of

$$v_{in}(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)\,, \tag{2.3}$$

is applied to the circuit input. Here, A_1 and A_2 are the amplitudes of the test tones. The output voltage of a nonlinear circuit can then be given as

$$v_{out}(t) = \alpha_0 + \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t) + ,...,+ \alpha_n v_{in}^n(t)\,. \tag{2.4}$$

Here the α-terms are constants proportional to the order of the nonlinearity. The spectral representation of the two-tone test for a downconversion mixer is illustrated in Figure 2.3. Here the two test signals (f_{RF1}, f_{RF2}), which are downconverted to frequencies f_1 and f_2, intermodulate each other thus producing also spurious frequencies, namely intermodulation products. The f_{IMD2} is due to (f_{RF2}-f_{RF1}), $f_{IMD3,L}$ due to downconversion of ($2f_{RF1}$-f_{RF2}), $f_{IMD3,U}$ due to downconversion of ($2f_{RF2}$-f_{RF1}), and $f_{IMD5,L}$ due to downconversion of ($3f_{RF1}$-$2f_{RF2}$), etc. In practice, a similar phenomenon occurs in the downconversion of a weak desired signal in the presence of two large interfering adjacent channels. Hence, due to the intermodulation of the interfering signals, an unwanted product can overwhelm a weak desired signal preventing the detection. At lower power levels, the third-order products from the odd-order effects dominate the linearity of the mixer. However, as the input power increases, the fifth-order, and even higher, products may become significant.

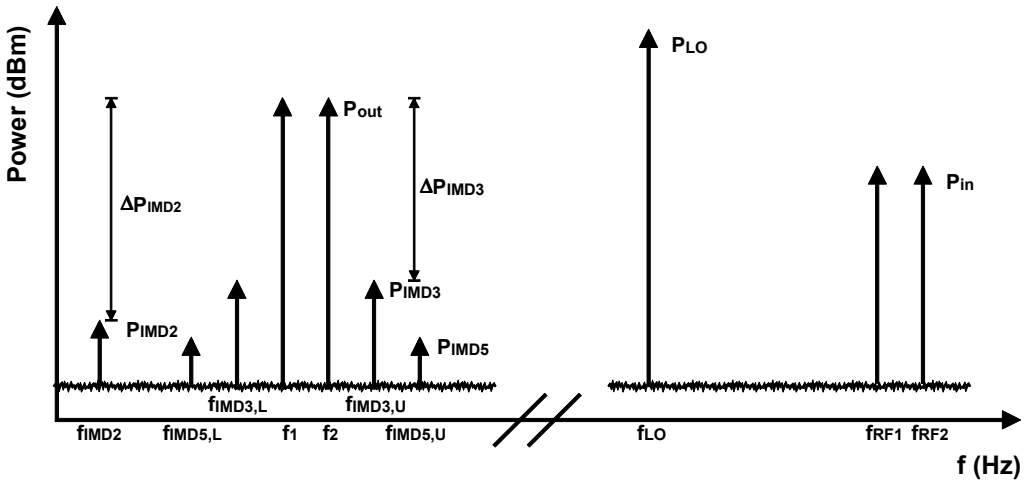


Figure 2.3 *Nonlinear downconversion spectrum.*

The nonlinear effects are divided into odd-order and even-order products that are caused by the odd- and even-order terms of Equation 2.4. The problems caused by the odd-order distortion are similar regardless of the receiver architecture. The even-order terms do not cause problems in heterodyne receivers because of the channel selection filtering at IF. Thus, the strong interfering signals do not pass to the input of the mixer stage that performs the final demodulation to the baseband. In direct conversion and receiver architectures using significantly low IF, the even-order distortion causes severe problems. The issues of even-order distortion are discussed in detail in Chapters 4 and 5.

Input referred intercept points are used as figures-of-merits to characterize the linearity performance of a receiver or separate blocks like a mixer. They are imaginary input amplitudes at which the desired signal becomes equal to the spectral component, which is generated by the respective intermodulating signals. The intercept points are determined by a two-tone test at small signal levels, when the nonlinear response is linearly dependent on the stimulus, as illustrated in Figure 2.4. At larger signal levels, the higher order nonlinearities, which also generate spectral responses to the same frequency, start to dominate, and the responses are no longer linear.

Another widely used performance parameter, which illustrates the linearity, is the input 1-dB compression point (ICP). It is used to describe the large signal handling capabilities of the circuit. The gain compression occurs either due to the odd-order nonlinearity or voltage clipping and current limiting. A strong signal can cause the compression. The ICP of the mixer must be sufficiently high to tolerate large blocking signals. A large blocker can desensitize the mixer in many ways. The different desensitization mechanisms are presented, e.g., in [23],[24],[25]. In general, a strong interferer blocks the mixer and reduces its small-signal conversion gain when the mixer is receiving a weak desired signal. It can also cause a rise in the noise level.

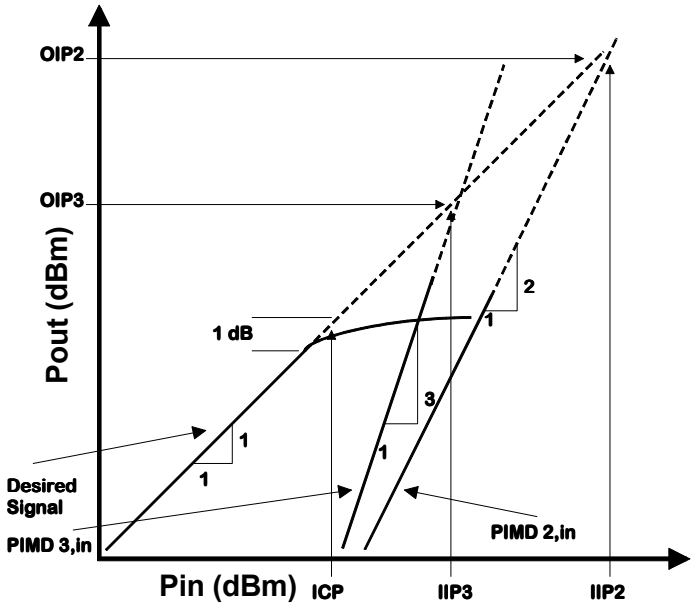


Figure 2.4 *Conceptions of intercept- and compression points.*

The second-order and third-order input-referred intercept points are defined by extrapolating (Figure 2.4.) Similarly they can be defined from the spectral lines using the linearity equations given below. These are valid for the signal levels at which the receiver is not driven into compression and the signal slopes are 2:1 and 3:1 for second-order and third-order nonlinear products, respectively. Hence the following relations for IIP2 and IIP3 can be given:

$$IIP2 = 2P_{out} - P_{IMD2} - G = 2P_{in} - P_{IMD2,in} = P_{in} + \Delta P_{IMD2} \tag{2.5}$$

$$IIP3 = \frac{3}{2}P_{out} - \frac{1}{2}P_{IMD3} - G = \frac{3}{2}P_{in} - \frac{1}{2}P_{IMD3,in} = P_{in} + \frac{\Delta P_{IMD3}}{2} \tag{2.6}$$

Here, P_{in} is the input power of a single excitation tone, P_{out} is the power of the linear output response of the input defined excitation, and G is the power gain. The intermodulation products are illustrated graphically in Figure 2.3 and Figure 2.4. The Equations (2.5) and (2.6) give IIP2 and IIP3 as power-quantities. However, they can also be rewritten for voltages [26] as:

$$IIP2\left[dBm/dBV\right] = 2V_{out} - V_{IMD2} - A_V \tag{2.7}$$

$$IIP3\left[dBm/dBV\right] = \frac{3}{2}V_{out} - \frac{1}{2}V_{IMD3} - A_V \tag{2.8}$$

One manifestation of nonlinearity is the AM-PM conversion. It is a nonlinear phenomenon in which the amplitude variations of the signal cause phase shift when applied to a nonlinear device, i.e., the unintentional amplitude variations cause unwanted phase modulation. In the downconversion process, the AM-PM conversion is a particular concern in the design of LO generation and its feeding circuitry to the mixers. The mismatches between the quadrature LO paths can contribute the phase deviation to the downconverted baseband signals due to the AM-PM conversion.

2.4 Noise in mixers

The noise performance of the mixer is expressed usually by the noise factor and noise figure. The noise factor is defined as a ratio of signal-to-noise ratios (SNR) at the input and output. The noise figure is the noise factor in decibel scale. Depending on the downconversion architecture, the mixer noise figure is defined accordingly for single-sideband (SSB) and double-sideband (DSB) signals [25]. Actually, there exist two conflicting definitions for the SSB noise figures and only one for DSB, which is the only well defined concept for mixers having significant image response, as explained by Maas in [27]. Nevertheless, the basic difference is that in SSB systems the LO downconverts noise from the image-band also, whereas, in DSB, the image consists of the signal by itself. Therefore, the downconversion of an SSB signal can be considered to have twice as many noise contributors as the downconversion of a DSB signal. In addition to the noise figure, which is very illustrative quantity, it is practical to use input-referred noise voltage in the mixer design of DCRs due to the unmatched interfaces. Power-defined quantities establish the easy use of a cascaded formula for noise figures given by Friis in [28]. In references [26] and [29], the Friis' equation is reformulated for unmatched interfaces and voltage gains.

The mixers contribute noise to the signal while performing the frequency conversion. If the signal-to-noise ratio is considered, the desired signal is either amplified or attenuated by the amount of mixer conversion gain or conversion loss, respectively. That is not the case with the noise. Noise present at the signal frequency in the mixer input goes through the similar process as the signal itself but is also incremented by the amount of additional noise generated in the solid-state devices and resistive components in the mixer. Generally mixers have quite poor noise performance. This is a consequence of the signal loss in the switching, but also of noise being transferred from multiple frequency bands to the output, as shown in Figure 2.5. The harmonics of the LO signal mix the noise from their sidebands directly to the IF or baseband. Ideally the loss in the switching elements of double-balanced switching

mixer is 3.9 dB, but can be easily several decibels higher, typically around 5-6 dB. This is an indirect effect of the gain degradation due to the non-ideal LO polarity switching [30]. However, the mixer is usually divided into three stages of noise contributors, input stage, time varying actual switching stage, and output stage. Each of these contributes noise from different frequencies to the band resulting from the frequency conversion. The analysis of the mixer noise is not straightforward due to its time varying characteristics. Different descriptions and analyses of noise for transistor mixers are presented, e.g., in [27],[31],[32],[33].

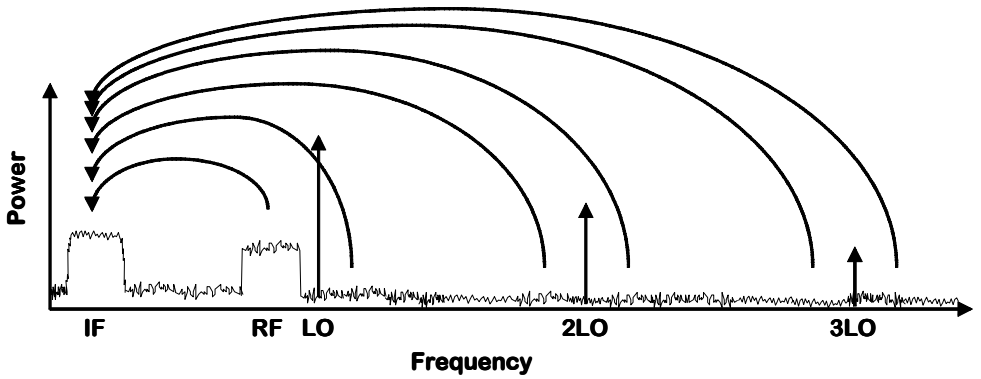


Figure 2.5 *Noise aliasing from harmonic LO sidebands.*

2.5 Mixer specification

Wideband RF front-end, and particularly the downconversion mixers, affect only the receiver own channel dynamics. Therefore, the most important specifications for the mixer are gain, noise, and linearity. In addition, the downconversion stage, including the LO signal generation in a DCR, is the main contributor of the imbalance between the in-phase (I)- and quadrature (Q)-channels. Special emphasis has to be paid also to the output dc-level in the DCR design. Furthermore, there are other application-specific requirements for the mixer, such as the power consumption, supply-voltage, and temperature stability.

2.5.1 Noise and third-order linearity

In practice, the RF front-end dominates the linearity and noise performance of the whole direct conversion receiver. As Friis' equation and Figure 2.6a illustrate, the LNA has to provide enough gain to suppress the noise of the mixer. On the other hand, the LNA gain should be designed according to the mixers' third-order linearity, as shown in Figure 2.6b and Equation 2.11, in which the IIP_3 of a cascaded system is shown. The LNA gain is not allowed to exceed the value

$$A_{V,LNA} = IIP_{3,MIX} - IIP_{3,SPEC} - N\ (\text{dB})\ . \tag{2.9}$$

Here $IIP_{3,\text{MIX}}$ is the mixer IIP3 and $IIP_{3,\text{SPEC}}$ is the required system third-order linearity. N is an additional 1-3 dB margin that ensures that the linearity is not totally limited by the downconverter. Practically, an active mixer is required in a DCR. It is important that the RF front-end is capable of providing a relatively high voltage gain (approx. 35 dB) [34]. The high front-end gain is needed to

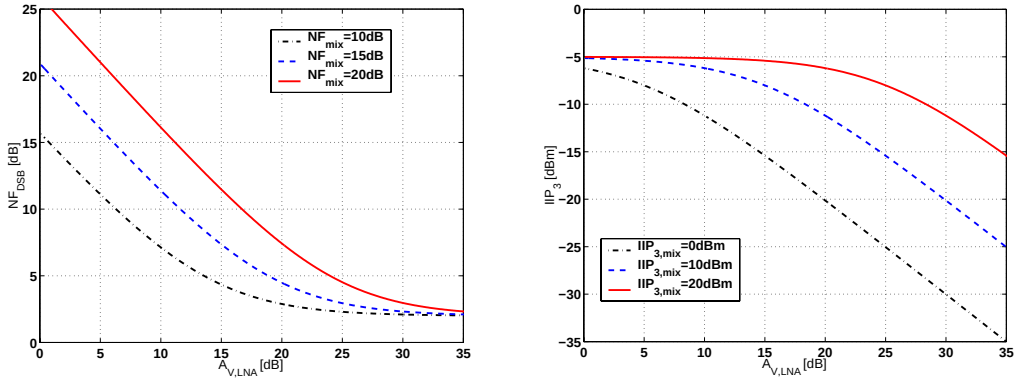
suppress the flicker noise contribution of active baseband filters. For this reason the passive mixers cannot be considered for a DCR. Hence, and paradoxically, a mixer with as low noise figure as possible is desirable to relax the LNA gain requirement, and therefore the needed mixer linearity.

$$F_{TOT} = F_{LNA} + \frac{F_{MIX} - 1}{a_{V,LNA}^2} + \frac{F_{BASEBAND} - 1}{a_{V,LNA}^2 \cdot a_{V,MIX}^2} + ,\ldots, . \tag{2.10}$$

Here F_{TOT}, F_{LNA}, F_{MIX}, and F_{BASEBAND} are the noise factors of the cascaded blocks, LNA, mixer, and following baseband circuitry, respectively. $a_{\mathrm{V,LNA}}$ and $a_{\mathrm{V,MIX}}$ are the voltage gains of LNA and mixer.

$$\frac{1}{iip3} = \frac{1}{iip3_{LNA}} + \frac{a_{V,LNA}^2}{iip3_{MIX}} + \frac{a_{V,LNA}^2 \cdot a_{V,MIX}^2}{iip3_{BASEBAND}} + ,\ldots, . \tag{2.11}$$

Here $iip3$, $iip3_{\mathrm{LNA}}$, $iip3_{\mathrm{MIX}}$, and $iip3_{\mathrm{BASEBAND}}$ are the iip3 values of the cascade system, LNA, mixer, and following baseband blocks in rms-voltages, respectively. $a_{\mathrm{V,LNA}}$ and $a_{\mathrm{V,MIX}}$ are the voltage gains of LNA and mixer.



(a) (b)

Figure 2.6 *(a) Front-end noise with three different mixer noise figures, and (b) IIP3 with three different mixer IIP3 values vs. LNA voltage gain. The NF and IIP3 of the LNA are 2 dB and -5 dBm, respectively.*

2.5.2 Gain compression

The conditions that specify the gain compression requirement for a downconversion mixer are the highest possible blocker together with the desired signal close to the sensitivity level, or the largest possible own band signal. The level of a large blocker is not allowed to reduce the mixer small-signal gain after amplified by the LNA. As an example, the largest blocking signal that receiver must tolerate is –44 dBm in 3GPP WCDMA specification [6]. This –44 dBm is the average power and does not take into account envelope variations of modulation. The margin of 5-10 dB has to be taken into account to take the peak-to-average ratio (PAR) into account. The blocker power of –44 dBm is measured from the antenna connector and a loss of about 1-2 dB can be assumed before the LNA. If the LNA has 20 dB of gain, the largest blocker signal level in the mixer input is about –24 dBm without the PAR margin. Hence the ICP requirement of the mixer is quite high. On the other hand, the maximum power

of the own signal at the antenna connector can be –25 dBm. Similarly, calculating a power of –5 dBm (assuming 50 Ω impedance level) at the mixer input must be tolerated with a system BER of at least 0.1%.

3 Mixer design

In principle, the mixer can be almost any nonlinear or multiplying component or device. Therefore several different circuits applied as mixers exist. The first division between the different topologies is to categorize them into active and passive structures. Passive mixer techniques, such as diode and passive FET mixers, are well documented in the literature, e.g., in [27]. Within the context of this thesis, the overview is limited to only active topologies applicable for use in DCRs and to those that can be fabricated in integrated circuit technologies without special processing techniques. Almost all such mixers originate somehow from the four-quadrant linear multiplier, familiar to most circuit designers as a Gilbert-cell [35]. However, it is sometimes also called a Bilotti's multiplier [36]. That topology originates in the 1968 Solid-State Circuits Conference where Gilbert and Bilotti both presented their works [37],[38]. They both utilized the similar multiplier topologies, and, probably because of this, there is a connection to Bilotti also. Nevertheless, at that time the topology was not novel for Gilbert, who had been developing the current-mode cells since 1967. Unfortunately, the multiplier-cell by itself had already been used before Gilbert's patent application [39], under another patent, by H. E. Jones [40], but only as a part of a particular system that was described. Although Jones' patent did not refer to the cell as a mixer, Gilbert could not have an issued patent for a multiplier-cell as a mixer, due to partial overlap of the claims. Nevertheless, it was Gilbert, not Bilotti or Jones, who first proposed the multiplier-cell as a mixer, modulator, and detector. Since that it has been used widely also as a mixer. The integrated monolithic systems often use that topology.

The basic structure of the Gilbert-cell is shown in Figure 3.1. It includes a tail current source (Q7), a differential transconductance stage (Q1, Q2), and a switching quad (Q3-Q6). The output can be driven to a resistive or reactive tuned load. Although the Gilbert-cell was initially designed with bipolar transistors, its operation principle is similar using CMOS technology [41].

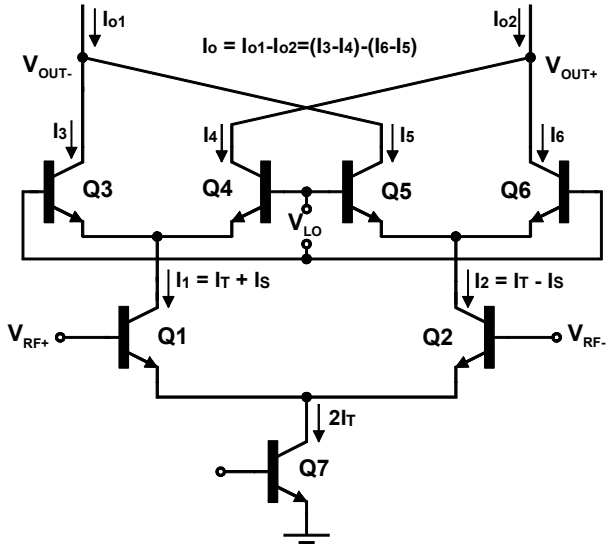


Figure 3.1 *Bipolar Gilbert-cell.*

The Gilbert-cell is a double-balanced topology. Principally, this means that if either the LO or RF signal is applied alone, the output is always zero. The double-balanced configuration offers high port-to-port isolation. The Gilbert-cell can be modified into a single-balanced configuration as well. Then it is a half of Gilbert-cell consisting of a grounded common emitter/source transconductance stage and a

switching pair. The design procedure is similar for both topologies. Both the double-balanced and single-balanced topologies can offer conversion gain. The single-balanced topology suffers from the strong LO port to IF port feedthrough. The Gilbert-cell mixer can also be driven by single-ended RF- and/or LO signals. In this case, the other side of the differential pair or switching quad is ac-grounded. Also, a single-ended IF output can be taken, although it is impractical in DCRs. The design and analysis of the Gilbert-cell and its modifications are widely reported, e.g., in [19],[21],[22],[23],[25],[42],[43],[44],[45],[46],[47]. References [19],[21], and [22] concentrate mainly on analyzing the nonlinearity, whereas in [42], the noise analysis of current commutating CMOS mixers is given. In [33], the noise analysis using state-equations for mixers is presented. In references [48] and [49], the predictive models for noise in RF CMOS mixers, which takes both the flicker noise and white noise into account are presented.

3.1 Design flow of active Gilbert-cell type mixer

In this sub-section, the behavior of a Gilbert-cell as a downconversion mixer is illustrated. The used simulation models are from a 0.35-µm RF SiGe BiCMOS process. The purpose is to show a downconverter for a direct conversion receiver with relatively constant performance over a wide band (1-6 GHz). In the given frequency range, both bipolar and MOS devices could be used. Figure 3.2 illustrates the mixer schematic presented here in detail. Even though the active devices are all BJTs, some specific issues considering the MOS devices are discussed. References [50] and [51] provide useful additional design considerations.

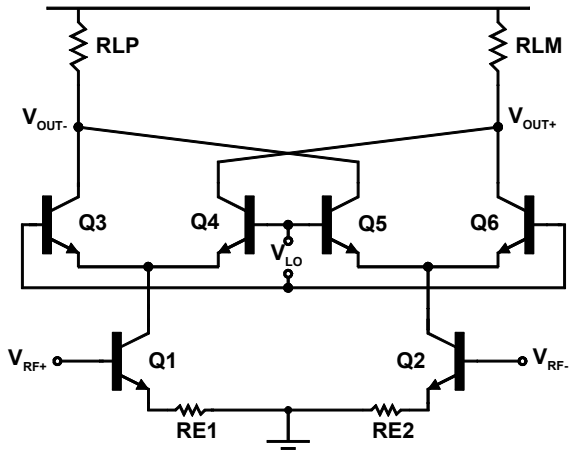


Figure 3.2 *Schematic of emitter degenerated bipolar Gilbert mixer. V_{LO} is 210 mV_{RMS}. V_{CC} is 2.7 V, and 1.3 mA current through the both devices Q1 and Q2 is drawn. The values for RL and RE are 500 Ω and 50 Ω, respectively.*

The RF front-end architecture used affects the selection between the single-balanced and double-balanced topologies. The single-balanced topology has a poor LO-to-IF isolation, but on the other hand, for a given supply-current, it exhibits less input noise than the double-balanced configuration [51]. It also provides better linearity with the same bias current and transconductance than the differential pair [22]. If the design target is a receiver with very low power consumption, e.g., for paging systems, the single-balanced topology has many advantages. However, the Gilbert-cell is often used as a mixer without the tail current source underneath the transconductance stage. Then the available voltage headroom is relaxed by the amount of one V_{CE} or V_{DS}. Instead of having a constant tail current, the input stage is a differential pair with grounded emitters/sources. By removing the tail

current source, the third-order linearity is also improved, but the common-mode rejection ratio (CMRR) requirements may come to have a significant role [52],[50]. Similarly, the linearity of the double-balanced topology is decreased a few decibels if it is driven by a single-ended RF signal, compared to a differentially driven mixer. In addition, it has lower conversion gain because only half of the available transconductance is used for signal amplification. Another consideration relates to the selection of LO switching devices. Typically the bipolar transistors are optimally driven with a LO signal of around 300 mV_{PP}, while the MOS devices require voltage swing at least twice as high to properly switch between the on and off states.

3.1.1 Mixer core

The active devices in the mixer determine the performance limits. For a given bias current, and when scaled to the same third-order linearity, a properly sized MOS transistor has higher transconductance than a degenerated BJT [50]. Although MOS devices are attractive owing to their linearity, they suffer from worse noise performance than bipolars. In particular, the flicker noise of bipolars is much lower. BJTs also have a higher f_T. Many advanced RF Silicon processes include SiGe HBT devices as bipolars. These, in addition to their higher f_T, also exhibit smaller base resistance r_b than the silicon bipolars, thus improving not only the noise performance, but also the linearity of the switching pair or quad [21]. In Figure 3.2, both the LO switches and transconductors are bipolars. A resistor degenerated common-emitter differential-pair transconductance stage is used as a driver. The degeneration linearizes the transistors forming a negative feedback. The degeneration could be implemented also reactively. Using inductive degeneration, the best linearity with the smallest drawback in noise figure could actually be achieved [22]. However, the four on-chip inductors needed for quadrature mixers, instead of requiring four small on-chip resistors, would require significantly more silicon area and thus should be avoided.

The mixer design optimization starts from the dc-analysis. The appropriate dc-quiescent points must be provided for active devices in order to optimize their performance. The degenerated differential pair transconductor (Q1, Q2) is biased at a fixed operating point. If MOS devices are used in the transconductance stage, the gate overdrive voltage is used to improve the linearity. The switches (Q3-Q6) are biased to conduct. These are then driven by a large LO signal to establish the paired on-off switching. Figure 3.3 illustrates the dc-transfer characteristics of an emitter-coupled pair. When the LO signal is applied to the circuit, one of the branches conducts at a time. It is seen that when the V_{LO} exceeds $|4V_T|$, one switch is closed and the current through the other is saturated. The dashed line in the figure presents a case where the emitter degeneration is used to linearize the pair. It is noticed that the degeneration increases the required LO voltage for proper on-off switching as the collector currents saturate later. The linear V-I range is $\pm 2V_T$ for the differential pair without emitter degeneration. Instead, if the emitter degeneration is used, the linear range is equal to a voltage twice that of $I_E R_E$, in which I_E is emitter current and R_E is degeneration resistance. The behavior of the MOS source-coupled pair is similar to the behavior of the BJT emitter-coupled pair, but requires an LO voltage swing of $\sqrt{2}V_{D,SAT}$. Thus, at higher overdrive voltages, a larger LO voltage is needed.

The branch current, together with the load resistors, determines the output dc-level. It is important to provide enough voltage headroom at the output, since the highest specified input signals must be prevented from clipping.

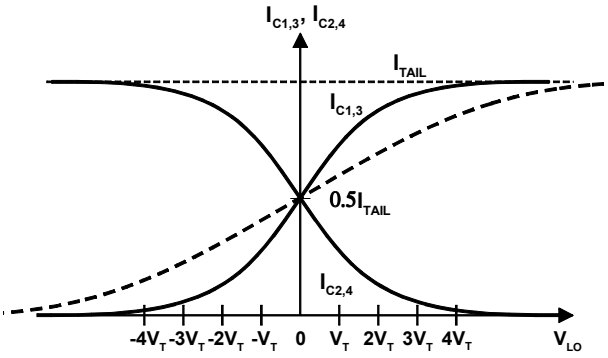
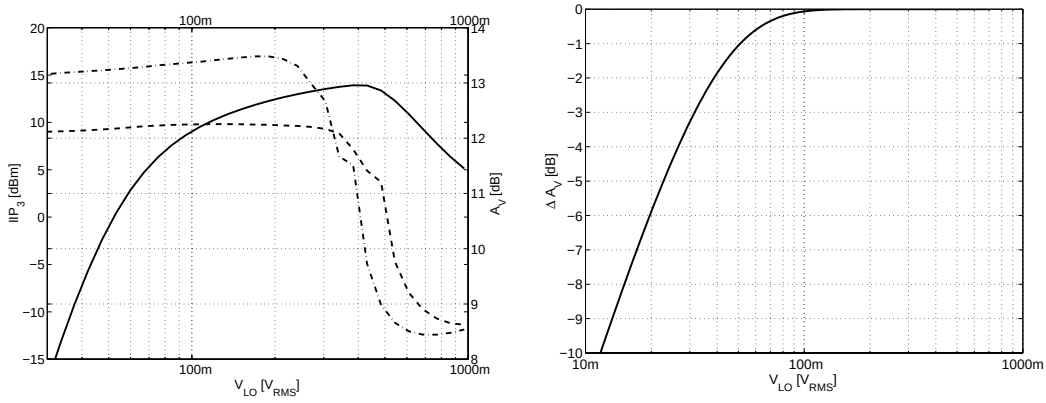


Figure 3.3 *Mixer LO pair collector currents vs. differential LO voltage.*

3.1.2 Optimization according to LO drive level (gain, linearity, noise)

As the active devices are selected and biased roughly to the appropriate dc-operating points, the steady-state analysis with three tones is needed to further optimize the mixer conversion gain, linearity, and noise as functions of LO signal amplitude. This must be performed regardless of the technology used. Together with the LO amplitude sweep, the gain, linearity, and noise must all be evaluated as functions of the emitter degeneration.

In most cases, the transconductance stage dominates the nonlinearity of the mixers when the f_T of the switching devices is high enough (more than 10 times the LO frequency) [23]. However, the contribution of the switching devices is not negligible in the total linearity performance. In general, the linearity of the switching stage is increased as the LO signal drive is increased up to a certain level. The optimization of the switching devices is a trade-off between the noise and linearity. The large LO signal reduces the duration time when both polarity branches of the switching stage are conducting simultaneously. When the switches do not conduct simultaneously, the active branch acts like a cascode amplifier for a short period, until it is switched to off-state and the other branch starts to conduct. Although the cascode transistors have only a small contribution to the linearity [23], the switching devices start to dominate the linearity at large LO amplitudes, as shown in Figure 3.4a. The drop in the IIP3 (>200 mV_{RMS}) is caused by the base-emitter junction capacitors (C_{je}) of the LO switches. The high amplitude switching leads to excessive current being pumped into the common-emitter points of the switching stage through the nonlinear C_{je} [21],[23]. The dash-dotted line in Figure 3.4a illustrates the IIP3 when the input transconductors are replaced by the ideal (linear) voltage-controlled current sources (VCCS) having an equal transconductance to the actual driver differential pair. Thus only the linearity of the switching stage is studied. The dashed-line represents the same phenomena with actual degenerated bipolar input devices. This proves that the linearity degradation at higher LO amplitudes is due to the switching stage [21].



(a) (b)

Figure 3.4 *(a) Simulated IIP3 and conversion gain vs. LO amplitude. The solid-line presents A_V. The dashed-line illustrates the real IIP3 and dash-dotted line the IIP3 when the input stage is replaced by two VCCSs. (b) Calculated A_V degradation vs. LO amplitude.*

The C_{je} increases when larger switching devices are used, and the linearity is decreased. On the other hand, small devices experience a large base resistance r_b. This results in increased noise and excessive voltage drop across the r_b, reducing the effective LO signal amplitude driving the switches [53]. Therefore, in addition to the benefits in the LNA design, the benefits of the SiGe HBT, compared to the Si bipolars, are remarkable in the optimization of the switching stage. The higher f_T and lower r_b establish smaller noise with the same device size. The linearity considerations discussed above are for BJT switches. The linearity issues of the current commutating MOS mixers are presented, e.g., in [19].

The low LO amplitude also contributes additional conversion loss in the mixing, as shown in Figure 3.4b, where the conversion loss as a function of LO amplitude for bipolar switching pair is plotted [54] according to

$$\Delta A_V = 20\log\left(\tanh\left(\frac{V_{LO}}{2V_T}\right)\right). \tag{3.1}$$

Here, ΔA_V is the degradation from the voltage conversion gain, V_{LO} is the voltage amplitude of the LO signal, and V_T is the thermal voltage. In Figure 3.5, current waveforms through the emitter-coupled switching transistors at two different LO amplitudes are shown. It is seen that the larger amplitude (solid-line) sharpens the transition between the on and off states. The dark-gray bands in the figure highlight the time periods when the transistors are clearly either conducting or in the off state, whereas the light-gray bands show up the transition periods. It is seen that the transition period is much shorter in larger LO amplitude, i.e., Δ is larger. The additional loss due to non-sharp switching directly worsens the noise figure by the amount of its loss. The gain degradation and its contribution to the mixers' noise are discussed, e.g., in [33],[42],[48]. In addition, for good gain matching between the I- and Q-channels, the switching devices should be driven with a relatively large LO amplitude. Figure 3.6a presents the simulated noise figure as a function of LO amplitude with 1 kHz and 100 kHz IFs. The flicker noise is dominating up to 10 kHz. The gain degradation clearly affects the noise performance at low LO amplitudes. In Figure 3.6b, the simulated operating band is shown.

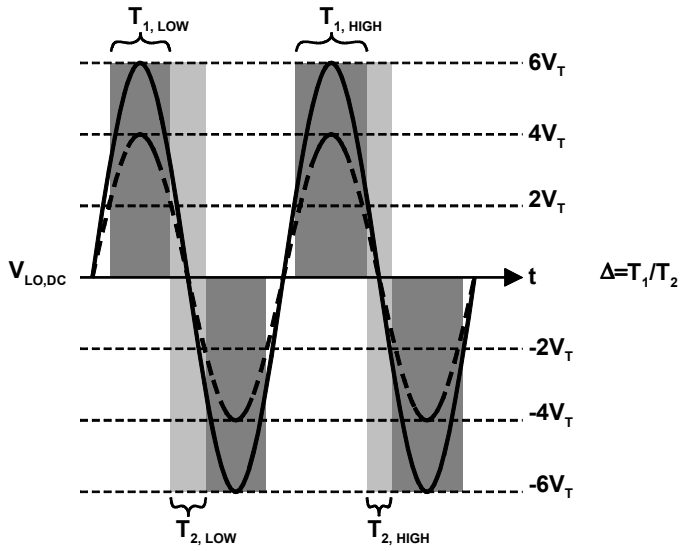
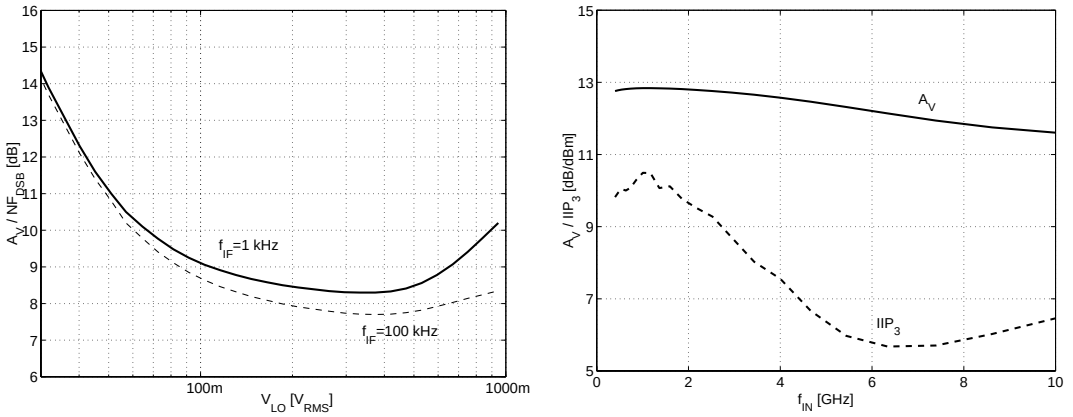


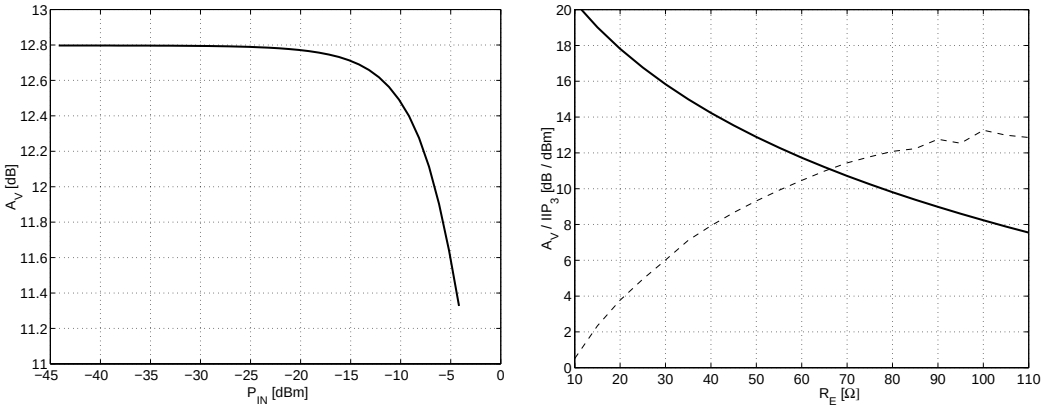
Figure 3.5 *Current waveforms of an emitter-coupled pair. The solid-line presents the switching with larger amplitude LO and the dashed-line that of smaller LO amplitude.*



(a) (b)

Figure 3.6 *(a) Simulated NF_{DSB} vs. LO amplitude. (b) Simulated A_V vs. frequency. In the two-tone simulation the excitations $f_{RF1}=f_{LO}+2.6$ MHz, and $f_{RF2}=f_{LO}+3.5$MHz.*

The signal handling capacity of the mixer must also be optimized, as was discussed in Section 2.5.2. The gain compression can originate from either clipping and current limiting, or the smooth desensitization of the input stage at high input powers. To affect the compression performance, the reason for the reduction must be investigated. If the gain reduction does not happen smoothly as the input power is increased, the compression is due to clipping. Then the output power remains constant even if the input power is increased. In Figure 3.7a the simulated gain compression of the mixer of Figure 3.2 is shown. Figure 3.7b shows the voltage conversion gain and IIP3 as functions of emitter degeneration.



(a) (b)

Figure 3.7 *(a) Simulated gain compression. (b) Simulated A_V (solid-line) and IIP3 (dashed-line) vs. emitter degeneration resistance.*

3.1.3 Other design nonidealities

IIP2 optimization is difficult as it is strongly interrelated to both the circuit linearity and the asymmetry. The IIP2 can be estimated by statistical simulations as will be shown in Chapter 4. However, the statistical simulations are not useful for fast optimization purposes. More practically, the second-order distortion component can be observed from the single-ended mixer output independent of circuit balance. Although it is only a conceptual parameter, it can be used to maximize the fundamental even-order linearity of the mixer during the design. It directly reflects the circuit nonlinearity, not asymmetry.

Another feature to be taken into account is the AM noise of the LO signal. If the LO signal is not properly filtered before feeding into the mixers, any AM noise superposed onto it is seen in the mixer output. In the double-balanced configuration, this common-mode LO noise cancels itself due to differential signal processing, as long as the circuit is well in balance. However, in single-balanced mixers, this noise exists differentially at the output, increasing the mixer noise significantly. Therefore, the single-balanced topology sets strict requirements for the LO feeding circuitry to filter out this noise. A typical value for the spectral noise density of the LO signal is between –130 to –120 dBm/Hz. An equivalent amount of noise should be added to the LO signal used in noise simulations in order to take this significant noise-coupling path into account. To the author's knowledge, the lowest published spectral noise density for a divider generating LO is –140 dBm/Hz by Tham in [55].

3.1.4 Current boost

Typically, quite a high gain is needed from the RF front-end, as already explained in Section 2.5. If an active Gilbert-cell mixer is used, the gain of the LNA cannot be increased over a certain limit without affecting the overall linearity. If the function is to suppress the baseband noise by increasing the RF front-end gain, it may be practical to increase the mixer gain. One technique for doing that is to boost the mixer input stage with a dc-current diverted from the switching core, presented for the first time for VGAs [56]. Thus the dc-current delivered to the transconductor, and thus the transconductor linearity, can be preserved while the current through the load resistors is decreased. This enables the enlargement of the load resistors without lowering the dc-voltage at the mixer output. Similarly, the

headroom problems can be avoided. The capacitance at the common-emitter node of the switching transistors can be also reduced resulting in faster switching. The advantage of the current boost is that almost the same IIP3 can be preserved without trading off with the noise. However, a small drop off in the linearity can be observed if high gain and high linearity are required from the mixer simultaneously. The boosting current sources also comprise an additional noise source and increase capacitance to the node of current injected. Both the increased noise and capacitance can be minimized using small long-channel PMOS transistors having large V_{DS}. In the mixer shown in Figure 3.2, a 2.9 dB increase in the voltage conversion gain is observed when the load resistors are enlarged from 500 Ω to 700 Ω and the boost current of 0.5 mA is diverted from the switching core. Theoretically, the gain increase equals to $20\log_{10}(700/500) = 2.9$ dB as long as the transconductance and the switching conditions remain unchanged. Similarly, the biasing conditions of the LO switching devices must be changed to correspond to the reduced I_C through the switches.

3.2 Interface considerations

As discussed in Chapter 2, the unmatched block interfaces require careful design in direct conversion receivers. Significant savings can be achieved in the power consumption if the interface buffering can be avoided. Consequently, the design becomes more complex when the analog RF circuitry has to be designed as an entity instead of separate blocks just to be cascaded. The dc and impedance levels at the interface must be sufficient both to the subsequent input stage and to the previous output stage. The possibility to use ac-coupling at the mixer output depends on the modulation and bandwidth because the ac-coupling filters will remove a part of the signal spectrum. The interface issues are crucial especially in low power circuits, in which special care must be given in the optimization to maintain sufficient performance with the lower power consumption. It is usually difficult to define an explicit border between the mixer and baseband, unless a particular buffering was used.

3.2.1 LNA-mixer

The input RF signal is usually fed ac-coupled to the mixer. The ac-coupling is used to partly filter out the second-order distortion generated in the preceding RF sections [57], but also because the dc-level of the LNA output, loaded with a parallel resonator connected to a positive supply-voltage, is usually incompatible to the mixer input stage. Depending on the LNA-mixer configuration used, the size of the dc-blocking capacitors must be optimized in order to not cause significant voltage division, and thus incremental signal loss. For example, in the work reported in [P4] the simulated loss is less than 0.2 dB over the 7-pF ac-coupling capacitors. The low frequency spurious signals generated in the LNA are also already attenuated at the resonator loaded LNA output, owing to the lower impedance level at low frequencies. If a bandpass filter is used between the LNA and mixer, it filters out the spurious signals at low frequencies. The mixer can use cascode transistors to separate the driver-stage and switching stage from each other, as shown in Figure 3.8. The cascode transistor provides more reverse isolation and thus reduces the LO-to-RF leakage. Besides, it establishes smaller capacitive loading to the drains of the transconductance stage, resulting in an increased operating bandwidth. In addition to the improved reverse isolation and bandwidth, these cascodes can be used as the additional band-select switches in multi-band applications [50]. In Figure 3.8, the multi-band LNA has two separate single-ended outputs, loaded with resonators (T1 and T2) tuned to different frequencies. The mixer has to be able to use the active LNA output while shunting the inactive input to ground. Simultaneously, the possible feedthrough from an inactive frequency band is minimized. Although the required number of mixer inputs is increased, and the dc-decoupling is needed for each band, the configuration does not considerably increase the required die-area.

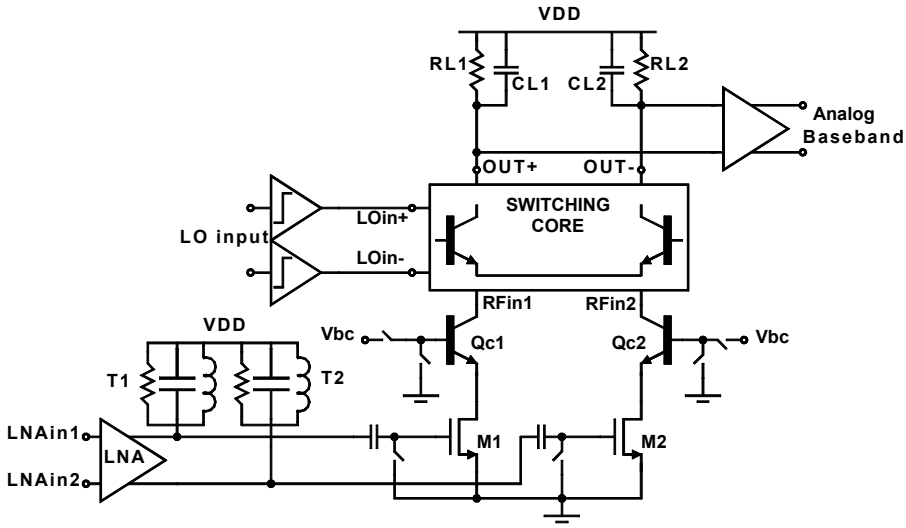


Figure 3.8 *Interfaces of the mixer.*

3.2.2 Mixer-baseband

The mixer and the first baseband stage are usually dc-coupled to each other although the ac-coupling is possible in wideband systems and in systems using modulations having a spectral null at the dc. The mixer load can also consists of an RC pole, as shown in Figure 3.8, which, either together with the analog baseband filtering, forms the first lowpass pole of the filter or independently suppresses high frequency signals. Alternatively, the mixer output can be considered to drive the current mode signal to the first stage of the channel selection filter. However, the most stringent requirements follow from the device matching and symmetry. As the first baseband stage is directly loading the mixer output, any imbalance in that or in the interface can deteriorate the second-order intermodulation rejection performance of the receiver. In addition, if some calibration takes place in the mixer, as will be presented in Chapter 5, the calibration should also perform the pole equalization. Furthermore, if the calibration changes the dc-offset at the mixer output, the first baseband stage must be insensitive to the offset.

3.2.3 LO-mixer

The interface between the LO and mixer easily dominates many unwanted effects if not carefully designed. Imbalances or mismatches in the differential branches easily deviate the LO duty-cycle from 50%. Consequently, the switching loss, and thus the mixer noise figure increases. In addition, the asymmetric LO duty-cycle causes an imbalance between the mixer polarity branches that lowers the even-order intermodulation rejection. A single-balanced mixer is inherently more sensitive to these errors. In the output of a single-balanced mixer the noise from the LO is differential, whereas common-mode in a double-balanced mixer. Therefore the LO signal should have as low noise power as possible at the IF or baseband. This can be taken into account in the LO buffer design [11]. Reactive bandpass or highpass loading in the LO buffers suppresses the noise at the IF or baseband [25]. As a disadvantage, the differential LO buffers with such loads for I/Q downconversion would need at least four on-chip inductors. To avoid the increase in the chip area, the double-balanced mixers are usually

preferred. The insensitivity of the mixer against the LO noise can be evaluated using a noisy LO signal, as was discussed in sub-Section 3.1.3.

Figure 3.9 illustrates the routes along which the LO signal can couple to the RF signal path in a DCR. The solid lines depict the coupling between the bond wires and the dashed lines the on-chip coupling. The figure also illustrates some conceptual floor planning issues to reduce the self-mixing. First, the LO buffers are placed as near the mixers as possible to minimize the length of on-chip routing of the strong LO signal. Even more benefit to the reduction of LO-to-RF coupling is achieved when the quadrature LO signals are generated on-chip from the double-frequency LO signal. Then the paths of the LO signal to couple to the sensitive RF input and bias lines are reduced to on-chip routes, while the package and bondwire coupling no longer occurs. In addition to the LO buffers, the quadrature signals also should be generated near the mixers to further reduce the length of the LO routing at the actual LO frequency. In reference [58], Singh has reviewed some floorplan and substrate coupling issues. Reference [59] includes illustrative analyses of substrate coupling and comparisons of different guard-bands and discusses the benefits of the differential signal path compared to single-ended.

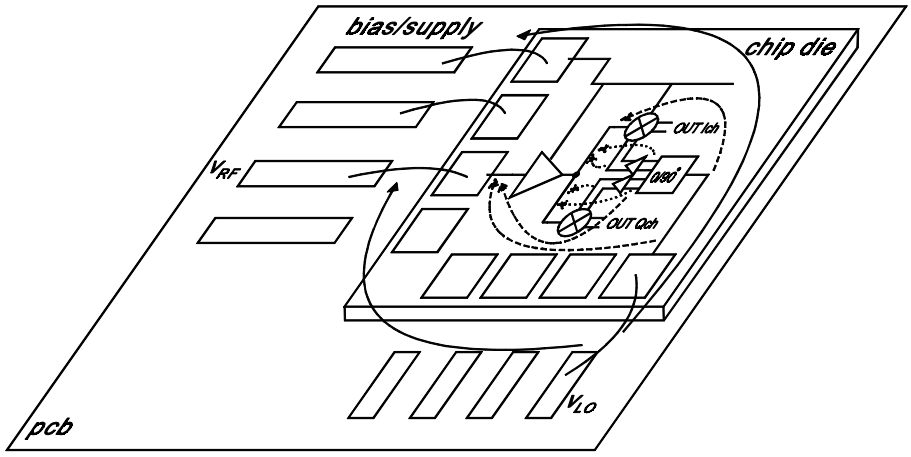


Figure 3.9 *LO couplings through substrate, package, bond wirings, and supplies to RF signal resulting self-mixing. The solid lines depict the coupling between the bond wires and the dashed lines the on-chip coupling.*

There are a number of particular circuit design and layout techniques that can be used to reduce the LO-to-RF leakage. The use of cascode transistors, as illustrated in Figure 3.8, between the driver and switching stages in the mixer, improve the reverse isolation inside the mixer. The improvement is roughly 10 dB. Another circuit design issue is the use of bipolar devices as LO switches. Among their many benefits [60], they require small voltage swing for complete on-off switching. Therefore, the LO signal leaking into the reverse direction or through the substrate is already quite small.

Although the static dc-offsets can be handled successfully in direct conversion receivers, the minimization of LO-to-RF leakage is essential. Publication [P8] discusses the phenomena and illustrates the problem of the strong dc-transient at the mixer output that occurs in the interrelation of LO self-mixing and gain control at RF stages before the mixer.

3.2.4 Quadrature generation

The required quadrature LO signals for downconversion are usually generated either by an RC-CR poly-phase network or by a divide-by-two circuit consisting of two cross-clocked d-latches. The RC-CR networks, shown in Figure 3.10, are discussed comprehensively, e.g., in references [61] and [62].

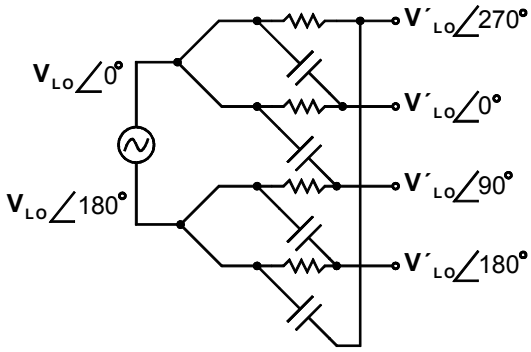


Figure 3.10 *I/Q-generation by a poly-phase RC-CR network.*

A schematic of an ECL divide-by-two circuit is shown in Figure 3.11. It can be implemented as two latches in a cross-connected loop. The shown current-steering topology achieves a high speed in both bipolar and CMOS technologies. The divider phase accuracy depends on the accuracy of the CLK signal (VLO). Hence, the phase accuracy is easily lost when driven single-endedly. The different topologies and details of divide-by-two circuits are discussed in [29].

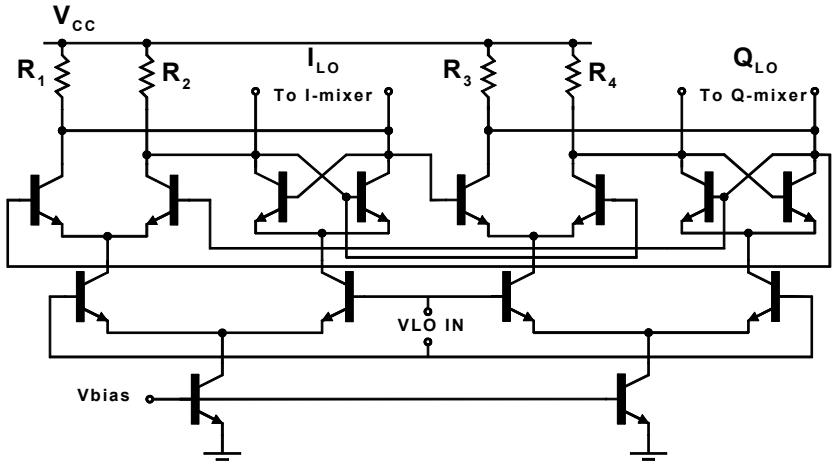


Figure 3.11 *I/Q-generation by an ECL divide-by-two circuit.*

Both I/Q-generation techniques have their own advantages and disadvantages. The benefit of the RC-CR technique is its simplicity. However, in multi-mode or multi-band applications a single poly-phase filter is insufficient. A poly-phase structure is frequency-selective and therefore every separate band requires an own filter. This is impractical for many reasons. First, the die area is increased. Then, the multi-band off-chip interface is difficult to realize for multiple RC-CR filters. Also, a relatively large LO signal has to be brought on-chip in order to compensate the theoretical loss of 3 dB per filter stage. Otherwise the LO signal has to be amplified on-chip to provide sufficient voltage swing for mixers. Instead, one divide-by-two circuit can be used to generate quadrature signals for several frequency

bands. Thus, the better way, from the multi-mode viewpoint, is to use an active frequency divider to generate quadrature LO signals. Also, as noted in sub-Section 3.2.3 it establishes the reduction of LO leakage. However, the off-chip interface impedance matching becomes complicated if multi-resonance or very wide impedance bandwidth is required. The needed impedance bandwidths are twice as wide with a double-frequency LO.

Practically the LO buffers are needed with both topologies to drive the mixers. The limiting LO buffers are needed in the poly-phase RC-CR generation to obtain necessary amplitude matching of the I and Q channels [51]. In the RC-CR filter, the amplitudes are equal only at the pole frequency. However, the smoothly limiting LO buffers are also needed with divide-by-two I/Q-generation. A characteristic feature of this topology is that the voltage swing in one branch is slightly smaller than in the other. Hence, limiting is required to minimize the amplitude imbalance between the I- and Q-branches for good channel matching [11].

3.2.5 Layout issues

Monolithic integration of analog circuits provides opportunities to good device matching and isothermal operation. Layout issues play an important role in these considerations. The device matching is critical particularly in the mixers used for direct downconversion, as the mixer dominates the receiver second-order distortion characteristics. Although there are techniques to improve the imperfect second-order intermodulation rejection in the receivers, as will be presented in Chapter 5, the design philosophy is still to minimize all possible mismatches. In addition, the matching of the quadrature downconversion channels is important. Typically downconversion mixers and LO signal generation are the largest individual contributors to the I/Q-imbalance due to the mismatching devices and parasitics. Furthermore, the different layout techniques have a significant affect on the receiver LO-to-RF isolation. The capacitive coupling to the substrate and resistive coupling through the substrate is the dominant on-chip effect of the LO-to-RF cross-coupling if the coupling between the bonding wires and packet leads are excluded. Nevertheless, the LO and RF signal routings should always be orthogonal to each other in order to prevent any on-chip magnetic coupling between the lines although the magnetic on-chip coupling can be considered almost insignificant at used frequencies. In addition, to further improve the LO-to-RF isolation, the LO switching devices should be placed into their own well surrounded by a grounded guard-ring, and the transistors of the driver stage into another. The on-chip LO signal routing should also be shielded from the substrate. This can be done in P$^-$substrate, for example, by placing an N-well or N-epitaxial layer underneath the LO wires. By connecting the N-well to the positive supply-voltage, the reverse biased PN-junction provides a proper shield, together with the dc-supply capacitors [P8].

The mixer core by itself can be divided into three different parts: load, LO switching quad or LO switching pair, and driver stage. From the second-order distortion point of view, the matching of the load is the most crucial. When approaching a precise matching (~±0.01%), special rules and carefulness in the layout must be used.

The matching load resistors can be realized from a large number of wide, cross-wired, interdigitized structures to make them as immune against the process, temperature, and stress variations as possible. The fingers should be placed in close proximity. If the IC process used provides several material options for resistors, the poly-resistors should be used instead of diffused ones. In addition, if high-ohmic poly-resistors are used, even wider resistors can be realized with a smaller number of unit squares. For precise matching, the dummies should also be used at both ends of the resistor array. The wide parallel structures increase the parasitic capacitance at the output nodes. If an RC pole is implemented at the baseband interface of a mixer as shown in Figure 3.8, the shift in the output poles can be taken into account in the design. An example of the resistor-pair layout is shown in Figure

3.12a. A lot of attention must also be paid to the symmetrical wiring and the number of contacts and vias, as they can have significant process variations.

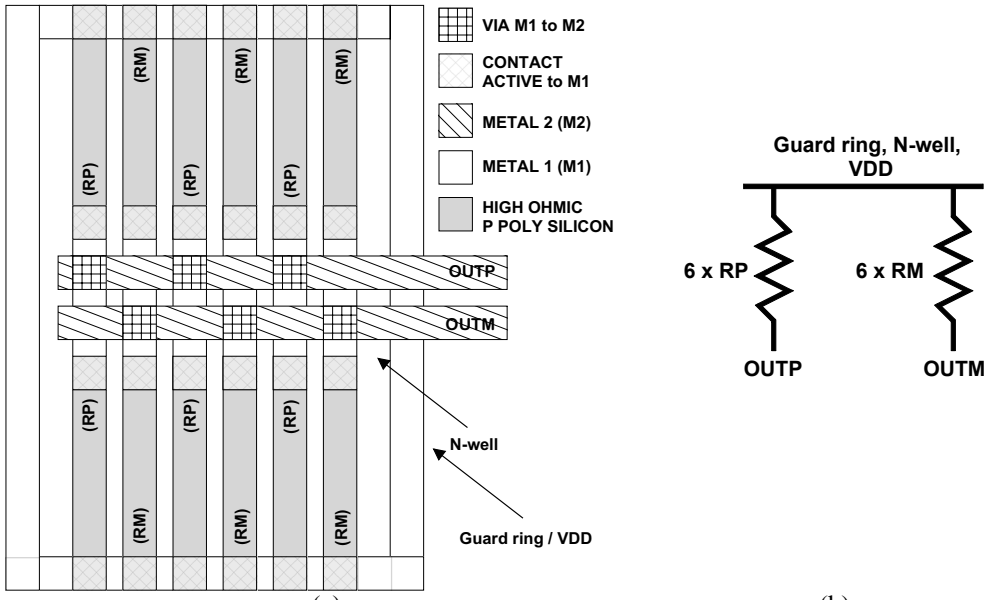


Figure 3.12 *(a) Layout of resistor pair for precise matching and (b) equivalent circuit.*

The matching of the LO switching core devices is also important from the second-order distortion point of view. The devices of the LO switching pair of the single-balanced mixer can be easily placed and oriented to match, but the switching quad of a double-balanced Gilbert-cell is much more complex. Different mismatch combinations of the bipolar switching quad transistors leading to different offsets are presented in [63]. The switching core devices can be arranged in many ways according to different matching requirements. They can be placed either in a star, ring, parallel, or in 2×2-matrix forms. A common problem with all these configurations is to feed both the LO and RF signals symmetrically to the switching devices and particularly with minimal number of overlappings. Other details to be taken into account are the current directions, and the differences in the horizontal and vertical diffusions. The device matching issues are overviewed in [64].

It is best to divide the driver stage of a Gilbert-cell into four unit devices and arrange them into a common-centroid layout. If bipolar transistors are used, particular attention should be paid to the matching of the emitter degeneration. The matching of the emitter degenerated bipolars can be dominated by the matching of the components composing the emitter degeneration. Hence, the emitter degeneration by inductors is not practical in a DCR, as typically the inductors suffer from poor matching. Instead, the resistors designed for precise matching would provide the best choice from the matching viewpoint.

4 Envelope distortion

4.1 Phenomena

The even-order spurious signals consist of sum and difference terms of the excitation frequencies. The receiver architectures with sufficiently high IF and bandpass IF filtering suppress the second-order products generated in the preceding stages. Therefore all other than the desired signal, or a relatively narrow band around it, are attenuated. Instead, the even-order intermodulation rejection is an important design issue in direct conversion and certain other receiver architectures employing a low IF or loose bandpass filtering before downconversion to baseband.

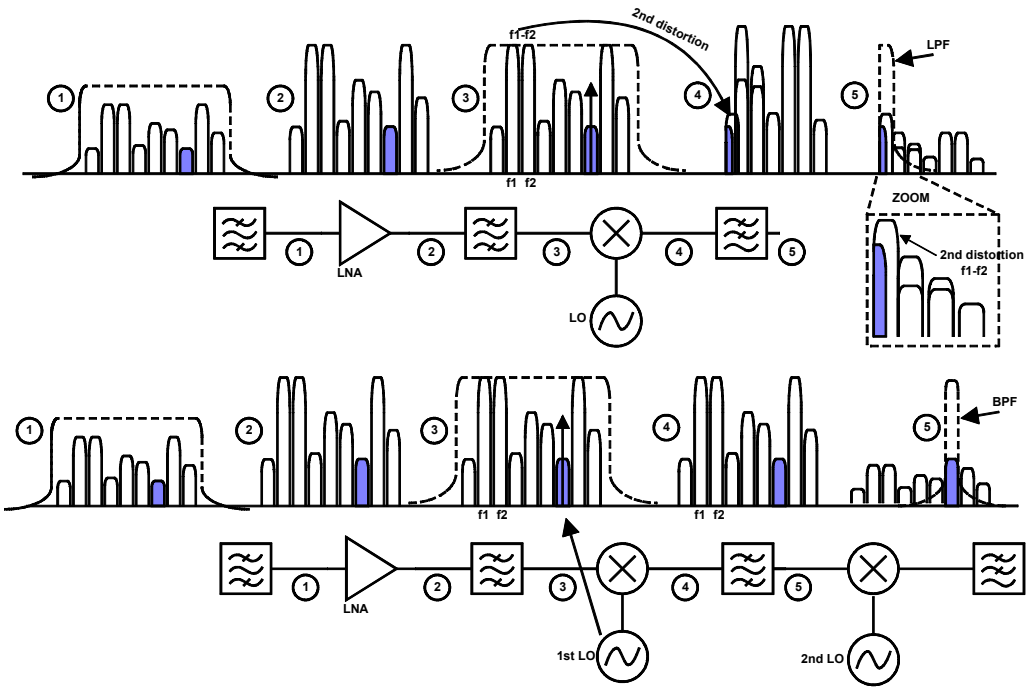


Figure 4.1 *Illustration of spectral aliasing in a DCR (above) and superheterodyne (below) when the system is noiseless and only the second-order nonlinearity of the first mixer stage is considered. The darkened band illustrates the desired channel. Quadrature path in downconversion to baseband is excluded.*

Figure 4.1 illustrates the imaginary spectral aliasing of a DCR (above) and superheterodyne receiver (below). The strong nearby signals f_1 and f_2 intermodulate each other due to the nonlinearity in the first mixer. In a superheterodyne receiver, in which a proper IF frequency and filtering are used, the resulting spurious signal is filtered out, but in a DCR it can be aliased over the desired downconversion band, depending on the frequency separation of the intermodulating tones. However, any strong in-band channel causes spectral re-growth due to second-order distortion.

Although the generation mechanism behind the envelope distortion is even-order nonlinearity, the discussion is limited only to the second-order nonlinearity. The effects of the higher even-order terms

cannot be separated from those of the second-order by the measurements, but the overall behavior of even-order distortion can be illustrated by second-order terms only. The second-order nonlinearity causes signal squaring, which removes the polarity information of the phase. Hence, the distortion is common-mode, which is not a problem as long as the differential signals do not suffer from any mismatch, i.e., imbalance. However, even a minor imbalance leads to the imperfect cancellation of common-mode distortion. Then, any amplitude modulation (signal envelope) in the signal is demodulated by the second-order nonlinearity and imbalance. Thus, the second-order distortion demodulates signal AM components. In addition to the envelope beat, squaring creates a dc-component. This dc-offset is totally different from the dc-offset caused by the self-mixing, although, in the literature, the self-mixing is sometimes confusingly considered to originate due to second-order nonlinearity.

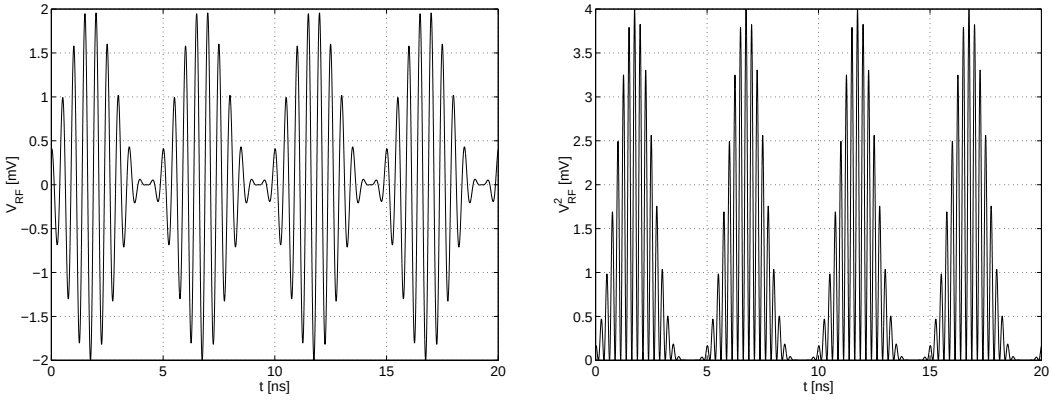
As already discussed in Section 2.3, the two strong nearby interfering tones (with appropriate frequency separation) produce a spurious baseband signal when exposed to a second-order nonlinearity. In addition, a single strong interfering tone produces a significant baseband distortion component. This kind of interferer is illustrated as $v_{in}(t)=a(t)\cos[2\pi f_C t+\theta(t)]$. It has an AM component $a(t)$, which can be considered as a non-constant envelope, and an arbitrary phase $\theta(t)$. When $v_{in}(t)$ is put into a nonlinear system, the squaring produces a spurious signal of the form

$$v_{in}^2(t) = \frac{1}{2}a^2(t)\left[1+\cos\left[4\pi f_C t + 2\theta(t)\right]\right]. \tag{4.1}$$

In general, it is important to notice that the $a(t)$ is not necessarily a periodic signal, as it was when described with a two-tone sinusoidal excitation. It is clear that the generated distortion component lies at dc if the interfering signal is either a single carrier only, or the $a(t)$ has a constant envelope. Such a dc-offset can be removed in many ways, as discussed, e.g., in [2],[10],[65]. In Figure 4.2a, a general amplitude modulated signal of the form

$$X_C(t) = A_C\left[1+\mu\cdot x(t)\right]\cos(\omega_C t) \tag{4.2}$$

is illustrated, in which A_C is the carrier amplitude, μ is the modulation index, $x(t)$ is a sinusoidal tone at 200 MHz, and $\cos(\omega_C t)$ is the 2 GHz carrier. In Figure 4.2b, the signal $X_C(t)$ is shown after squaring.



(a) (b)

Figure 4.2 *(a) AM modulated RF signal, and (b) its squared replica.*

To avoid the demodulation of the described amplitude envelopes, the DCR requires a high second-order intermodulation suppression performance. The performance parameter describing the ability of

the receiver to tolerate the envelope distortion is IIP2. IIP2 is a convenient figure-of-merit for describing the second-order intermodulation rejection performance, although the direct specification for IIP2 is not usually characterized for the DCR in association to the intermodulation tests. In addition, the IIP2 is easily characterized for receivers, together with the other intermodulation tests. However, the IIP2 specification is usually defined backwards from other specified receiver tests as will be discussed in sub-Section 4.2.4. In the following parts of this chapter, different radio system characteristics are discussed with a view to evaluate possible AM envelopes; the IIP2 requirements of direct conversion receivers in different systems are also discussed. To conclude the chapter, a mixer design to estimate the second-order intermodulation characteristics is described.

4.2 Envelopes in different systems

The different digital communications systems have different spectral amplitude envelopes depending on the modulation, pulse-shaping, duplexing method, etc. In this section, the main differences between the specific envelope generation mechanisms and different systems are discussed. Later in Chapter 5, it will be shown how some of the system characteristic issues can be adopted, e.g., to detect the receiver envelope distortion performance together with the on-chip calibration.

4.2.1 TDMA systems

In TDMA systems, the signal transmission (Tx) and reception (Rx) occurs in bursts. Therefore, the burst mode transmitter ramping mainly causes the envelope variations. The receiver band envelopes of the whole system band are quite different for base stations (BS) and mobile stations (MS). For example, in GSM the BS synchronizes the intra-cell mobile terminals, and hence the power ramping takes place mainly when the receiver is not active in the reception mode. However, neither the co-located cells of the other operators nor the other base stations of the own operator are no longer synchronized. An even worse situation arises for the MS receivers in EDGE/GPRS that can use multiple timeslots for reception. The reception is therefore more susceptible to the power ramping of other nearby transceivers regardless of the synchronization. The BS receiver is a subject of more AM-distortion because it has to receive during all time slots. Figure 4.3a illustrates how the basic GSM MS uses the TDMA timeslots to receive and transmit. Seven mobile stations in total can operate simultaneously in one frequency carrier. One time-slot is used for monitoring purposes (MON) and is common for all intra-cell mobile terminals and for those making a handover. Figure 4.3c shows how an interfering burst, which is not synchronized, overlaps the reception timeslots of another receiver, which are highlighted in Figure 4.3b. Although these two asynchronous transmissions are separated in frequency, the AM envelope is detected.

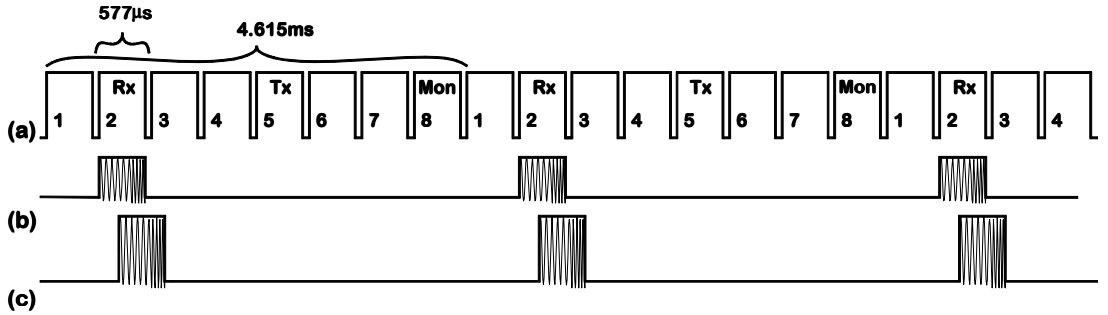
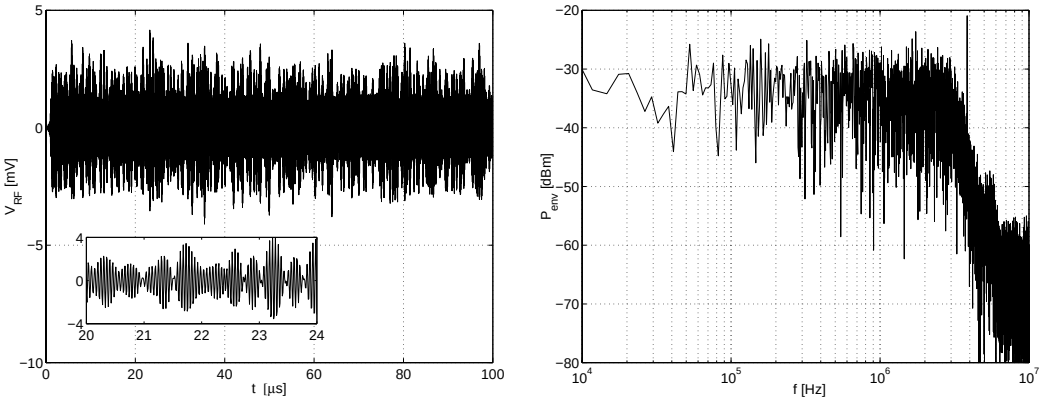


Figure 4.3 *MS operation in a GSM traffic channel.*

4.2.2 CDMA systems

The envelopes of DS-CDMA systems are different from those of TDMA systems. In Figure 4.4a, an RF waveform of a 3.84 Mchip/s QPSK modulated signal upconverted to a 10 MHz carrier is shown. A detail of the signal envelope is seen in the zoomed region. In Figure 4.4b, the spectrum of RF envelope after the squaring is shown. The figures illustrate that significant AM-components exist even in a single QPSK-channel. The envelope spectrum is interesting as the largest envelope component is located at the frequency of used symbol-rate. The observation that the largest envelope content is around the baud-rate or symbol-rate was first made by Tsurumi in [66]. The spectrum of the envelope power does not continue above that frequency if several code channels composing the physical frequency channel are spread synchronously.



(a) (b)

Figure 4.4 *(a) Waveform, and (b) envelope power of QPSK channel at 3.84Mchip/s with RRC-filtering of 0.22 roll-off.*

In WCDMA, the wideband downlink signals are composed of several code channels and can have a high crest factor (CF) resulting in very large variations in the signal envelope. This envelope is then demodulated by even-order nonlinearities causing envelope distortion. The CF is defined as the ratio of maximum instantaneous peak and average powers. The difference between the peak envelope power (PEP) and the average power, i.e., peak-to-average ratio (PAR), depends on the modulation type and the pulse-shape filtering. The distribution of modulated symbols also affects the PEP. Table 4.1 shows measured PAR-values for several different modulations and filterings.

Table 4.1 *Different PAR values measured for certain standards and digital modulations with different pulse shape filtering roll-offs.*

	PAR		
modulation	RRC α=0.5	RRC α=0.35	RRC α=0.22
π/4 DQPSK	2.7	3.1	4.3
8PSK EDGE	3.1	3.8	5
IS-95 OQPSK	2.8	3.3	4.1
BPSK	3.1	3.8	5
IS-95 QPSK	3.1	3.8	5

Figure 4.5 illustrates the complementary cumulative distribution function (CCDF) diagrams of several composed signal channels. Reading the curves from left to right, the corresponding code channel numbers and CFs are 1 DPCH, 4 DPCH, and 16 DPCH and 5.5 dB, 9.5 dB, and 11.0 dB, respectively.

For comparison, the CF of additive white Gaussian noise signal is about 10 dB. The CF of the WCDMA downlink channel saturates to about 10 dB when 16 or more code channels are used. The uplink of the WCDMA uses a more complicated hybrid-QPSK (HPSK) modulation. The uplink HPSK signal is basically similar but has slightly smaller crest factors than downlink.

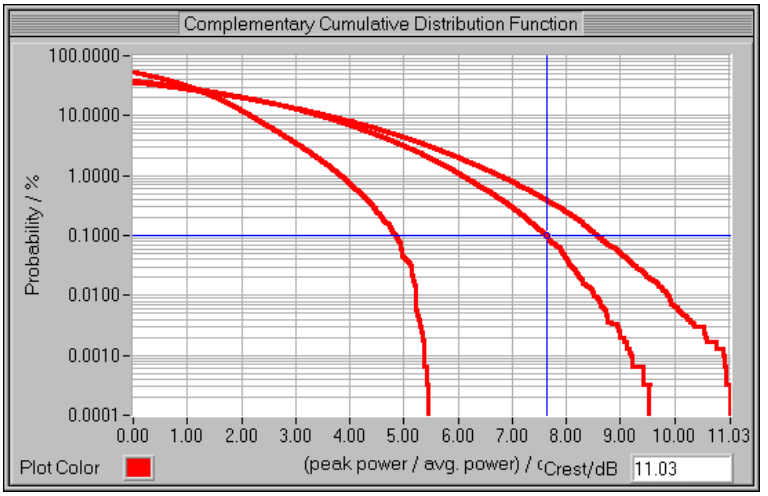


Figure 4.5 *CCDF diagram of several 3GPP WCDMA DPCHs.*

The digital systems use different diversity methods to suppress various signal degradations. The bit interleaving reduces the system susceptibility to fast errors like a possible bit error due to the envelope peak. However, the system performance can still be significantly degraded if the high peak powers occur frequently, i.e., if the CF is large. Hence, the probability of certain peak levels in the modulated channel should be considered rather than an average of the envelope. The CCDF diagram is a useful tool in receiver design also. Power amplifier designers use the CCDF diagram extensively for determining the amplifier back-off gain due to the spectrally linear modulations. To determine a PEP of a certain digital modulation, it is assumed that the modulation symbols are not uniformly distributed. Instead, the most unfavorable case is considered.

The envelope variations can be reduced by different spreading and data synchronization techniques. The complex spreading technique [67],[68],[69], for example, is typically used. Also, the data and pilot synchronization provides significant envelope reduction in multi-coded channels. However, the envelope variations can still be over 10 dB with several code-channels, as already shown.

4.2.3 OFDM systems

The envelope distortion can also be crucial in such systems that use orthogonal frequency division multiplexing (OFDM). In OFDM, the signal consists of a number of independent sub-carriers, which can cause a significant PAR, when added-up coherently. If N sub-carriers are added with the same phase, as unavoidably sometimes happens, they produce a peak power that is N times the average power. This does not directly mean a high IIP2 requirement, but may require high AM suppression performance from the receiver.

In OFDM, the PAR reduction can be accomplished by trading-off against the increase in the self-interference. Possible techniques are, e.g., clipping and peak-windowing [70]. However, the benefits in PAR are quite negligible from the receiver envelope distortion viewpoint.

4.2.4 IIP2 specifications

The requirement for the IIP2 depends on the system. For example, in GSM, the IIP2 specification for a DCR has to be extracted either from the blocking or AM sensitivity test [5], as shown by Laursen in [71]. It turns out that the AM sensitivity test sets stricter requirements and therefore is used to determine the IIP2. The carrier-to-interferer (*C/I*) ratio of at least 9 dB must be achieved for a signal 3 dB above the reference sensitivity level of -102 dBm, with the presence of a GMSK modulated interferer of –29 dBm. Hence, it can be calculated that the required

$$IIP_2 = \left(\frac{C}{I}\right) - (-99\,\text{dBm}) + 2(-29\,\text{dBm}) = \left(\frac{C}{I}\right) + 41\,\text{dBm}\,. \tag{4.3}$$

However, according to Laursen, the *C/I* can be slightly lower than 9 dB while still achieving the required BER in the AM sensitivity test. In [71], a *C/I* of 5 dB is reported and thus the IIP2 of at least +46 dBm is required for DCR in GSM.

The IIP2 specification for a DCR used in mobile equipment according to the UTRA/FDD WCDMA air-interface specification [6] is presented in [72]. However, the specification is not straightforward. In [72], Jensen et al. classify two groups of possible interferers that can cause spurious baseband signals when exposed to second-order nonlinearity. These are the unwanted in-band blocker in the downlink band and the transmitter leakage signal. The latter depends on the Tx-to-Rx isolation and thus mainly on the duplex filter performance.

The in-band blocker test is explained in detail in references [6] and [72]. The receiver must tolerate the blocking signal, P_{BLOCK} of –44 dBm with frequency offset at least 15 MHz, having BER below 10^{-3}. The generated intermodulation product and noise powers are not allowed to exceed the desired signal, which is defined as 3 dB over the reference sensitivity level of –117 dBm, inserted by the amount of processing gain (25 dB). According to [72] the IIP2 requirement by the in-band blocker test is +8 dBm.

The IIP2 specification according to the Tx signal leakage, also shown in [72], becomes more stringent for the receiver. The same conclusion is also presented, for example, in [16] and [17]. The transmitted signal power is attenuated by the amount of duplex filter isolation in the receiver input. The lowest transmitter power classes 3 and 4 for user equipment are +24 dBm and +21 dBm, respectively [6]. If the duplex filter provides 60-dB Tx-to-Rx isolation, the leakaged Tx power $P_{\text{TX,LEAK}}$ at the receiver input is between –31 and –34 dBm. In [72], Jensen et al. define the required IIP2 of +47 dBm due to the transmitter leakage. They increase an additional 10 dB margin to ensure that the second-order intermodulation products are sufficiently attenuated.

In [73], Bautista et al. present the IIP2 specification for a DCR and low-IF receivers, which takes the different modulation and pulse-shape filtering into account. The approach is to specify the IIP2 high enough to avoid any susceptibility to IMD2-related blocking when the blocking signal has a non-constant envelope. They found that the blocking of a single blocker with a non-constant envelope is slightly smaller in comparison to the classical IMD2 interference of two tones, i.e., double sideband suppressed carrier (DSBSC). Similarly as Laursen specifying the IIP2 for GSM the Equation (2.5) is re-arranged in [73] as

$$IIP_2 = 2\left(P_{BLOCK} - 3\,\text{dB}\right) - P_{SENS} + \left(\frac{C}{I}\right) + DIIP2\,(\text{dBm})\,. \tag{4.4}$$

Here, P_{BLOCK} is the total power of the two-tone DSBSC signal. Hence 3 dB is subtracted to equalize the DSBSC blocker power to the average power of single interferer with non-constant envelope. P_{SENS} is the defined sensitivity level and *(C/I)* is the defined carrier-to-interferer ratio. A new modulation and

pulse-shape filtering dependent parameter *DIIP2* is adopted. Determining the *DIIP2* with respect to the different system parameters requires simulations with an interferer that has similar power and envelope characteristics as the actual modulated carrier. Finally, the *DIIP2* is the difference between IMD2 products with a DSBSC and non-constant envelope contenting excitations. The relationships of the RF signal envelope characteristics and IIP2 are also presented in [65].

4.3 Envelope distortion in downconversion

In Section 3.1, the design and optimization of the downconversion mixer was discussed. The emphasis was placed only on the third-order linearity performance, neglecting the even-order linearity. Here, the mixer optimization according to the second-order distortion is discussed. It is noticed that an unbalanced mixer cannot be used in the DCR, because it does not provide any second-order intermodulation suppression. Instead, the second-order intermodulation distortion can be monitored in the simulations from the single-ended mixer output, as introduced in sub-Section 3.1.3. The benefit of this approach is that the fundamental second-order nonlinearity can be evaluated with the same reliability as the third-order products, e.g., IIP3 without any dependency on the circuit balance. Although the approach does not reduce the importance of device matching and balance, the circuit can be optimized for highest second-order linearity independently of the asymmetry. As a result, the mixer can finally achieve a higher IIP2 with the same imbalance, while the second-order nonlinear behavior is fundamentally better.

It is important to evaluate the expected IIP2 of the designed receiver. A statistical simulation in which the device parameters are independently distributed according to the possible IC process tolerances can be used. An estimate of the yield of the receiver samples that achieve the required performance is simulated simultaneously. Figure 4.6a illustrates a simulated histogram of receiver IIP2, described in [P4]. A thousand samples were analyzed with a Monte-Carlo simulation. All component values of the mixer, LO generation, and respective bias circuitry are independent and uniformly distributed, having ±1% tolerances.

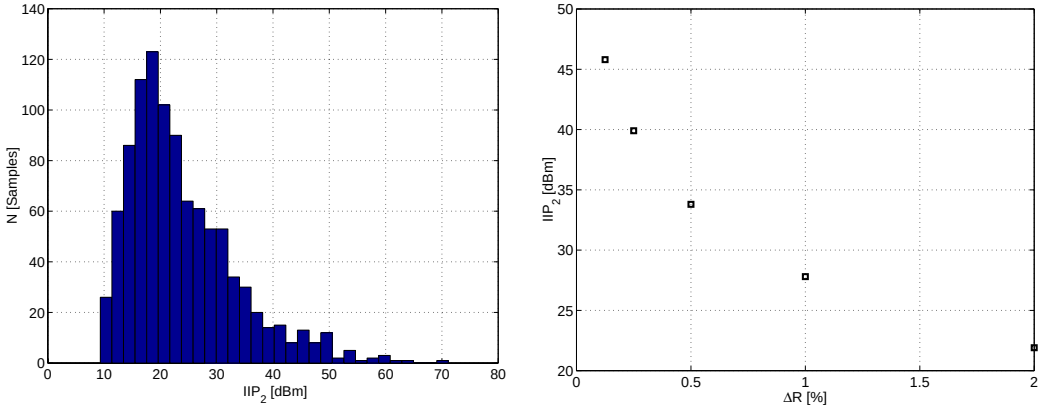
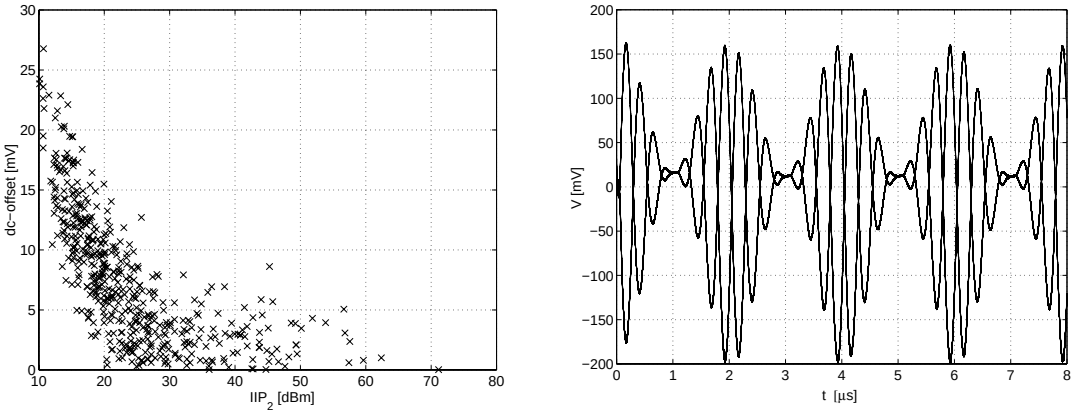


Figure 4.6 *(a) Simulated IIP2 histogram, and (b) simulated reference IIP2 with load resistance imbalance of the receiver RF front-end presented in [P4].*

Ten circuit samples in total were characterized in the measurements. The mean and standard deviation of the measured IIP2 values are +25 dBm and 7 dB, respectively, while the same numbers, according to the simulation in Figure 4.6a, are +24 dBm and 10 dB, respectively. As a reference, the simulated IIP2 of the same receiver, as a function of the imbalance between the load resistors as the only

mismatch, is shown in Figure 4.6b. The figures illustrate that the single 1% load resistor imbalance can be used to have a good first-order estimate for IIP2 in mixer simulations. The strong statistical characteristics of receiver IIP2 require that several receiver samples have to be characterized to determine the IIP2 reliably. It should always be given whether the given IIP2 is an average or worst measured value and how many samples were characterized.

The simulated dc-offset as a function of the corresponding receiver IIP2 is presented in Figure 4.7a. Statistical simulation similar to that in Figure 4.6a is carried out for 500 samples. It is seen that in the presence of various mismatches the high IIP2 does not necessarily guarantee a perfect dc-balance. As the distribution clearly illustrates, it is possible to achieve a high IIP2 simultaneously with significantly large dc-offset, although there is strong interrelation between the IIP2 and dc-offset. Figure 4.7b illustrates the simulated single-ended mixer output signals at 2-MHz IF in which the corresponding IIP2 is +27.8 dBm. In the simulation, two tones with equal amplitudes were used. Probably one of the worst-case conditions in WCDMA is the weak signal in the presence of a strong AM contenting interferer. The quadratic effect is seen as the signal AM content becomes asymmetric.



(a) (b)

Figure 4.7 *(a) Simulated statistical dc-offset vs. corresponding receiver IIP2. (b) Simulated down converted signal at 2-MHz IF with 1% load resistor mismatch.*

5 IIP2 improvement methods

Many different approaches to improve the receiver IIP2 and dc-offset have been published, as the improper even-order intermodulation rejection has been recognized as the most challenging problem limiting the effective use of direct conversion receivers. The linearization methods can be categorized mainly into two basic types. The first approach is to cancel the nonlinear response at the receiver backend by feedforwarding a compensation signal, which can be, for example, an inverted distortion signal, as presented, e.g., in [74],[75],[76]. Alternatively, the correction can be made already where the problems originate, i.e., in the mixer. In fact, it can be considered to lead to the best performance because a number of subsequent error sources can thus be eliminated. The problems related to the mixer in a DCR have been recognized, i.e., dc-offsets, self-mixing, and second-order distortion since the beginning of the 1990's. However, several scientific articles confuse the second-order distortion and self-mixing, which, in principle, originate from clearly different mechanisms. This may be the reason why many early approaches to overcoming the IIP2 problems have been based on the idea of minimizing the dc-offset. However, as shown in [P5], the dc-offset minimum is achieved simultaneously, as IIP2 is maximized only in the single-balanced mixer, not in the double-balanced mixer that is still the most used mixer topology. In practice, some improvement method must be utilized in a DCR to have a high IIP2. Only one published work, [15], overcomes the problem without any mention of calibration while still achieving +47/+49-dBm IIP2.

5.1 Overview of different methods to improve even-order intermodulation rejection in radio receivers

A mixer in which the transconductance stage is ac-coupled to the switching core to filter out the second-order beat generated in the preceding stages was first reported by Takahashi et al. in [57] and [77]. The configuration is shown in Figure 5.1. However, the achieved improvement is only moderate as they reported the mixer IIP2 of +32 dBm in static conditions, and +47-dBm IIP2 after external bias adjustment. A similar configuration for the LNA-mixer interface, and as a separation between downconverter input stage and switching stage, is also used in [10], [34], and [78].

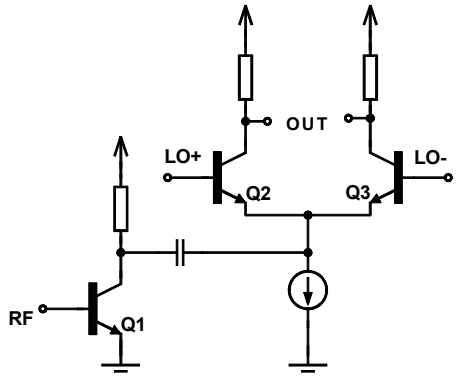


Figure 5.1 *Ac-coupled single-balanced mixer.*

In [79], Yamaji, et al. have made offset in the tail currents of the double-balanced harmonic mixer. The method aims better balance by adjusting the input signal amplitude balance and LO signal duty-cycle indirectly by way of making slight changes in the dc-operating points. They report an improvement of

approximately 10 dB in the IM2 rejection, and, a mixer IIP2 higher than +37 dBm. They show that the method used is not sensitive to the changes in the RF signal frequency. Although the method is fairly simple, its use is limited to double-balanced topologies, and the results show only moderate IM2 rejection. An enhanced concept of the method presented in [79] is illustrated in [80], in which the biasing of the LO switches can also be adjusted separately. Hence, it is applicable in single-balanced mixers also. In [73], Bautista et al. present a procedure called 'dynamic matching'. In that method, a periodic random signal is applied to modulate both the transconductors and the output of the Gilbert-cell mixer. This is actually a technique known as chopping. In their application, the even-order intermodulation rejection is improved by up to 20 dB. They report as high as +72-dBm IIP2 for a BiCMOS mixer and +66-dBm IIP2 for a CMOS implementation. This is fine method, as it simultaneously reduces the mixer 1/f-noise as well. As a disadvantage, the method is quite complex, requiring an additional clock signal to be applied. Therefore its use in, for example, handset applications, is questionable.

In [81], a direct conversion receiver for GSM, which achieves better than +65-dBm IIP2 after calibration, is presented. They make the calibration by a ramped blocker test, while monitoring the AM. However, the detailed mechanism of the calibration providing an improvement of 35 dB, is not given in the paper. The received signal is divided into quadrature components by a 2-stage poly-phase filter between the LNA and mixer, which uses a common-base stage as its input stage. The better linearity of the common-base driver stage and the loss of the poly-phase filter significantly affect the IIP2 at the receiver input.

As a summary, a number of techniques have been published how the mixer second-order intermodulation rejection can be improved. Instead, only a few of those give any insight how these techniques could be applied practically on-chip, and how the intermodulation characteristics of a chip sample could be detected without significant external measurement setups, thus constituting a practical on-chip calibration method. These issues are discussed later in this chapter.

5.2 IIP2 improvement methods based on balancing loads

As the improper even-order rejection results from the existence of both the nonlinearity and asymmetry, at least another of these must be adjusted to improve the even-order rejection. Although the fundamental linearity of the downconverter would have been designed as high as possible, the circuit always suffers from mismatching and, therefore, from second-order distortion. The circuit balance, especially at RF frequencies, depends on the device matching but also on the matching of parasitics (stray capacitances, wiring resistances, cross-couplings, and propagation delays) whose asymmetries are hardly controllable. However, the balance of the mixer can be adjusted by tunable load elements. As shown in [P5], a perfect dc-balance alone does not guarantee high mixer IIP2 because of the various circuit mismatches. In fact, the circuit can be balanced by means of controlling the circuit mismatches. The balancing methods presented in the following can be applied for both single- and double-balanced mixers.

5.2.1 Direct load tuning

The mixer loads can be made adjustable to control the mismatching. In practice, the balancing loads, which can consist of large resistive elements, are connected in parallel to both mixer outputs directly, as shown in Figure 5.2a. The implementation is straightforward, as it requires only the resistor finger banks (R_{TRIM}) in parallel to the actual mixer loads (R_L), shown in Figure 5.2b. The calibration procedure changes the dc-offset at the mixer output. Hence the first baseband stage has to tolerate the possible dc-offsets over the entire load tuning range. In the implementations described in [P6, P7], the

realized tuning range is ±10% of the fixed load resistance. The binary-weighted balancing resistor banks are placed in parallel to both differential outputs. The I- and Q-mixers must be trimmed separately. The banks are realized from high-ohmic polybase resistors, having a sheet resistance of 1 kΩ/□. The physical dimensions of one such 5-bit resistor matrix element are 105 μm×150 μm. In quadrature downconversion mixers, four of these are required in total. The binary-weighted parallel resistance is given as

$$R_{TRIM} = m \cdot R_L \cdot 2^{k-1} \cdot \frac{1}{n}, \qquad n = 1,...,2^k . \tag{5.1}$$

Here, m is a constant that is selected to determine the maximum tuning range, i.e., the ratio of the smallest parallel resistance to the R_L, k is the number of control bits, i.e., the number of parallel switchable branches, and n is an integer corresponding to the code word. However, the balancing elements are not necessarily limited to resistor banks; more generally they could be tunable load impedances. In resistor implementation, several factors such as switch nonlinearity, temperature characteristics, supply-voltage, and dc-levels must be carefully taken into account. The switch R_{ON} must be small compared to the resistance of the high-ohmic polybase resistor fingers. Moreover the resistance of the switchable resistor fingers must be significantly higher than that of the actual load resistors. Thus the switch nonlinearity becomes insignificant. The scaling also reduces the effect of the different temperature characteristics of MOS switches and poly resistors. Figure 5.3 illustrates the measured receiver IIP2 for several samples as a function of the load imbalance. The 5-bit tuning is implemented in a double-balanced mixer presented in [P7].

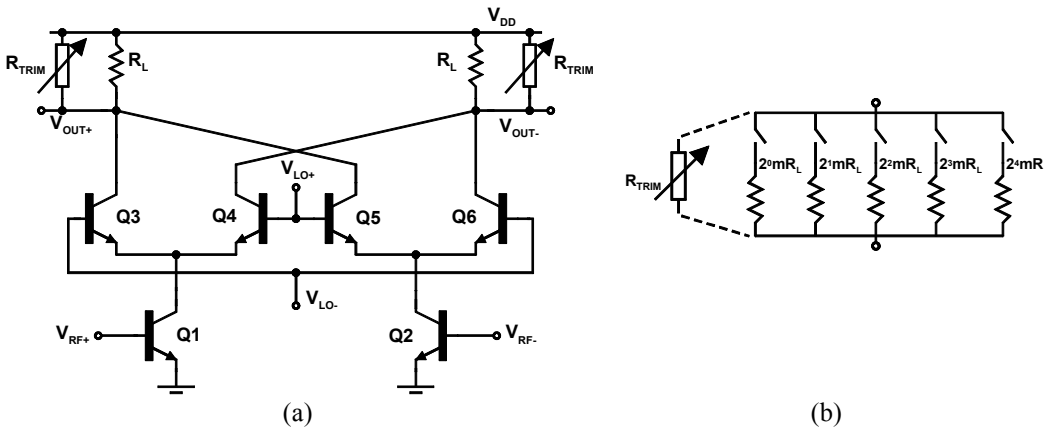


Figure 5.2 *(a) Direct load tuning balanced mixer, and (b) resistive 5-bit binary-weighted balancing element.*

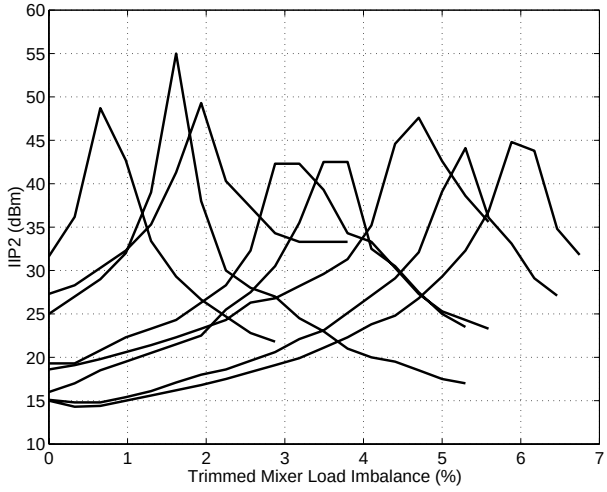


Figure 5.3 *Trimmed receiver IIP2s of several measured chip samples [P7].*

5.2.2 In-direct load tuning

In in-direct load tuning, a similar balancing can be achieved with ac-coupled balancing devices connected in parallel to both mixer outputs, as illustrated in Figure 5.4. As an advantage when compared to the direct load tuning method is the static dc-offset at the mixer output remaining constant during the tuning process. Instead, the required four on-chip ac-coupling capacitors take more die area compared to the direct method in which the balancing devices are dc-coupled.

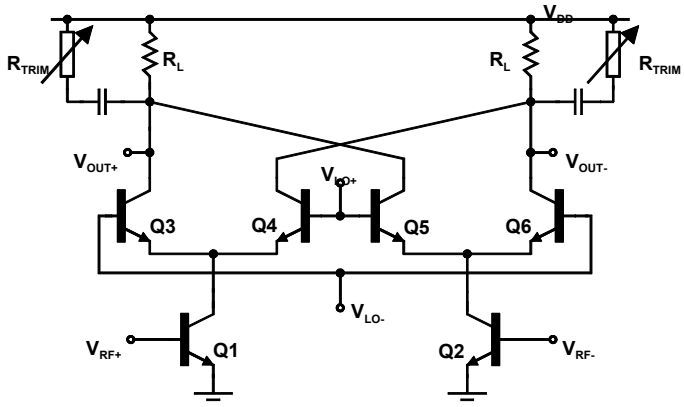


Figure 5.4 *In-directly balanced mixer.*

5.2.3 Differential gain deviation

In a differential gain deviation, similar even-order linearization can be performed with tunable gain amplifiers (Figure 5.5). Separate single-ended tunable gain amplifiers can be realized as an interface to the baseband. These are connected to both mixer outputs. The single-ended amplifiers have to be very linear in order to prevent their linearity to limit the system overall linearity.

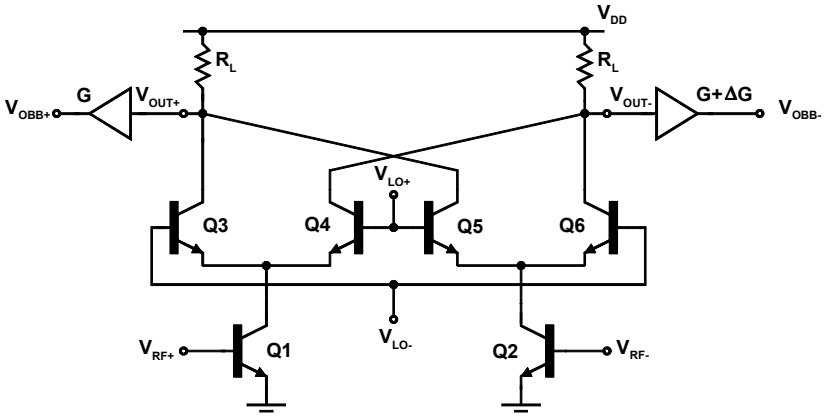


Figure 5.5 *Mixer balanced by deviating the gain of first baseband buffering stage.*

5.2.4 Improvement by LO tuning

In principle, the balancing could also be realized by controlling the conduction angles of the switching devices. The LO duty cycle deviation from the ideal (50%) causes a similar asymmetry factor in a single-balanced mixer, as does the load imbalance [see Equation (5.2)]. However, in double-balanced topology, the non-ideal LO duty-cycle only indirectly affects the IIP2, as illustrated in Equation (5.3). The relationships for IIP2 as functions of several mismatch variables given respectively for single-balanced and double-balanced mixers as

$$iip2_{SINGLE-BALANCED} \approx \frac{2}{\pi\eta_{nom}\alpha'_2\left|\Delta\eta + \Delta R\right|} \tag{5.2}$$

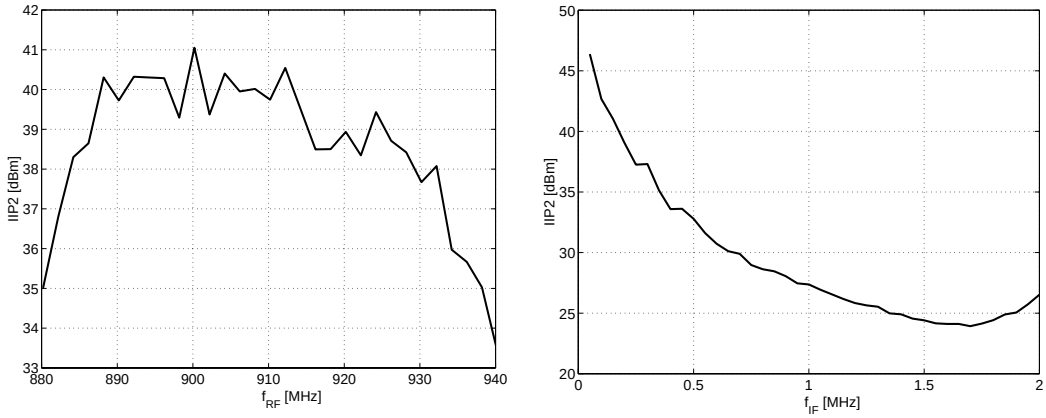
$$iip2_{DOUBLE-BALANCED} \approx \frac{\sqrt{2}}{\pi\eta_{nom}\alpha'_2} \cdot \frac{4}{\left(2\Delta\eta\left(\Delta g_m + \Delta A_{RF}\right) + \Delta R\left(1+\Delta g_m\right)\left(1+\Delta A_{RF}\right)\right)} \tag{5.3}$$

are derived and presented in [P5]. Here, η_{nom} presents the nominal 50% duty-cycle in LO switching, α_2' is the second-order nonlinearity coefficient relative to the linear transconductance in the mixer, $\Delta\eta$, Δg_{m}, ΔA_{RF}, and ΔR are the mismatches in percents of the LO switching duty-cycle, transconductance of the mixer driver stage, RF signal amplitude, and load resistance, respectively.

The controlling of the high frequency LO signal, however, includes much uncertainty. In addition, the suitability of the method to double-balanced mixer is doubtful due to the dependency of $\Delta\eta$ on the amplitude imbalance of the RF signal and the transconductance mismatch of the driver stage. Furthermore, the mixer LO-to-IF port isolation is simultaneously decreased as the LO duty-cycle changes. The single-balanced topology, especially, is very sensitive to the noise induced from the LO-port to the output as was discussed in Chapter 3.

5.2.5 Imperfections of the balancing

The balancing methods illustrated above have only a negligible effect on the other mixer performance parameters, i.e., gain, noise, and IIP3. However, Figure 5.6a illustrates the RF bandwidth of the IIP2 in a directly-tuned single-balanced mixer presented in [P6]. A substantially large bandwidth is needed in radio systems tuned to a wide range of RF carriers. The situation is even more difficult in multi-band receivers, in which the mixer has to be capable of receiving from multiple RF bands. The uncalibrated and calibrated receiver IIP2s shown in Figure 5.6a are +16 dBm and +39 dBm, respectively. It is seen that, although an over 40 MHz (±1 dB) band is achieved, the balancing suffers from frequency dispersion. Hence the tuning must be done separately for different frequency bands.



(a) (b)

Figure 5.6 *(a) Measured sensitivity of improved IIP2 as a function of Rx channel handover. The tuning has been carried out at 910 MHz. (b) Measured downconversion channel response of trimmed IIP2 [P6].*

If an RC pole is implemented in the baseband interface of a mixer as shown in Figure 3.8, the change in the effective resistance balances the mixer but also causes mismatching between the pole frequencies in the differential output. Consequently, the achieved balance might not have wide bandwidth at baseband or IF as shown in Figure 5.6b. However, while the balancing has been made at a fixed downconversion test frequency, it must be preserved over the whole modulation bandwidth. This becomes crucial, especially in the direct tuning and in-direct tuning methods, in which the RC-time constants of the single-ended mixer outputs are trimmed asymmetrically. The options to make the balancing insensitive to frequency at baseband are either to set the pole higher (about 10 times higher than the highest baseband signal frequency) or to establish a pole back compensation. In a way similar, a wideband buffer could be used between the mixer and baseband. However, the buffer should maintain excellent linearity in order to prevent its own nonlinearity and asymmetry from dominating the second-order linearity performance. In the pole back compensation, a tunable capacitor matrix can be used to equalize the single-ended RC-time constants after tuning. The linearizing resistor fingers and capacitor structure for pole shift compensation can be realized from small unit devices. Moreover, they can use the same logic to preserve the matching of the output poles and thus the improved even-order intermodulation rejection is less sensitive to the downconversion frequency. The capacitance value needed in parallel to the actual load capacitor, and thus to compensate the pole shift, can be given as

$$C_a = C_L\left(R_L \big/ R_{TRIM}\right). \tag{5.4}$$

Here, C_L and R_L are the fixed load capacitance and resistance at the mixer output, respectively, and R_{TRIM} is the resistance of the binary-weighted resistive balancing element given in Equation (5.3). The compensating capacitor matrix is straightforward to implement from the parallel binary-weighted unit elements in a way similar to the resistor matrix shown in Figure 5.2b. Figure 5.7a and Figure 5.7b illustrate the R_{TRIM} and C_a as functions of the trimming code. If the in-direct tuning is used, also the ac-coupling capacitors affect the pole frequencies and thus the back compensation becomes more complex. The advantage of using single-ended buffers at the mixer output from which another can be tuned at a time is that the adjustment does not contribute more static dc-offset at the mixer output. However, the implementation is more complex compared to the direct- and in-direct load tuning methods.

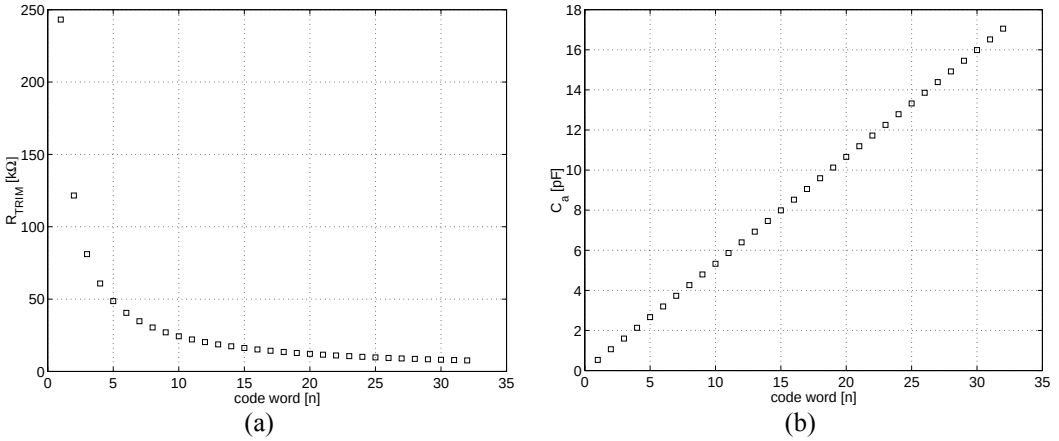


Figure 5.7 *(a) Balancing resistance and (b) pole compensating capacitance value C_a as functions of 5-bit tuning.*

Figure 5.8 illustrates the two possible implementations of the mixer RC loads; both of these use direct tuning as the balancing method. The basic structure, in which the fixed load capacitor is connected in parallel to the resistive loads separately at both outputs, is shown in the left. A more area-efficient way to implement the fixed capacitor between the outputs is shown on the right. However, the tuning of this implementation is not as straightforward, as the tuning of another output reflects also to the pole of the other output.

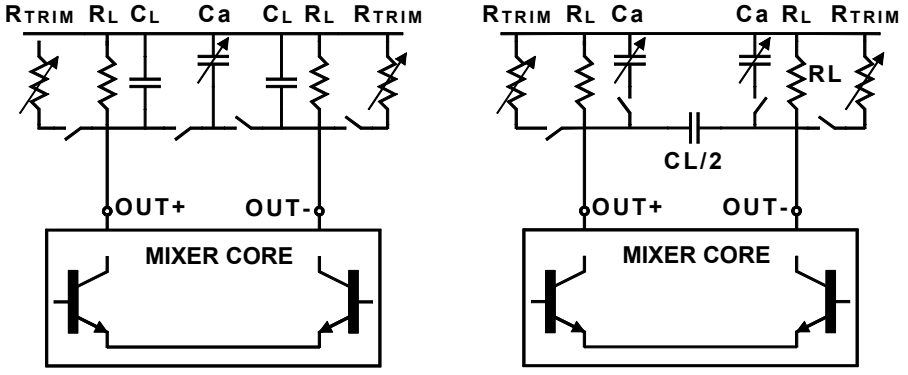


Figure 5.8 *Two different ways of implementation of the mixer RC load.*

The measured IIP2 of a trimmed receiver sample, described in [P6], is shown as a function of temperature in Figure 5.9a. It is seen that below +10 C° the IIP2 is decreased significantly. A supplied fixed code word gives the optimum elsewhere in the tuning range except between –15 and 0 C°. In this range, a different balancing code word gives the maximum as shown with separate measurement points in Figure 5.9a. The fault backtracking simulations show that at the lower temperatures the transistors, from a PMOS cascode current-mirror, which bias the LO switching transistors start to drift into sub-threshold region. In the shown range, this does not prevent the mixing, but causes different mismatches in the current commutating than in the room temperature where the balancing is stable. It is not completely certain that how temperature-stable the calibration really is as the designed mixer is biased separately with respect to the other receiver. While a PTAT current biases the LNA and baseband circuitry, the mixer is biased by a separate external current without temperature compensation. As shown in Figure 5.9b, the total voltage gain of the receiver varies along the temperature. It is obvious that this behavior is mainly because of the mixer. Owing to these reasons, the evaluation of the temperature-dependency of the calibration is not reliable.

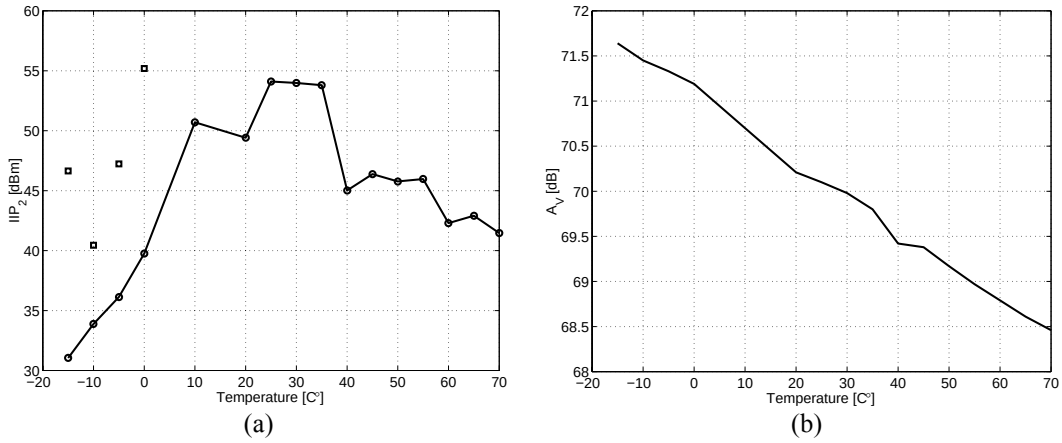


Figure 5.9 *(a) Measured sensitivity of improved IIP2 to temperature variations. (b) Measured receiver voltage gain as a function of temperature.*

Another point of view is that the resistors, bipolar-transistors, and MOS-transistors have different temperature gradients. Therefore, also the mismatching is temperature dependent at least in some extent. The presented temperature behavior is for single-balanced mixer, in which the mismatching effects can be intuitively reduced to those of current-commutating and load resistors. A double-balanced mixer is much more complicated, especially, if BiCMOS technology is used and the mixer consists of both bipolar and MOS transistors.

The aging performance of the test samples is not verified. Although the burning test has not been performed, it has been noticed that the maximum improvement is always repeated by the same code word at the respective frequency range. This gives an assumption that the balancing is not sensitive to aging. Furthermore, some of the measurements have been renewed a couple of times during the one and a half year period.

5.3 IIP2 calibration

The even-order intermodulation rejection of mixer can be improved with the presented methods. However, the application in which the receiver is used as well as the operation environment sets significant requirements for the needed performance. Typically, the MS receiver experiences a more stringent environment than that used in a BS. The BS receiver usually receives from a fixed frequency channel, whereas the moving MS is continuously a subject to the frequency handovers. Moreover, the MS experiences faster temperature changes than the BS. In addition, the battery voltage and, for example, the LO signal amplitude, can vary slightly due to the external conditions; mainly because of the temperature changes, even the temperature-insensitive biasing techniques were used. Typically, the battery discharging can also cause similar effects. The even-order intermodulation rejection, like all performance parameters, should be as insensitive to the external changes as possible. All these design considerations should be taken into account when implementing the calibration.

The calibration concepts can be divided into two categories. In one the intermodulation rejection performance of the receiver can be reliably verified and the receiver can use registered preset calibration coefficients for, e.g., certain reception frequencies and environments. In the other, the receiver monitors and calibrates itself during the idle-times or even during the reception. Both these concepts have certain advantages and disadvantages. The receiver circuitry and its behavior in the different using conditions determine the category. In fact, careful receiver testing is needed to find out how the receiver calibration is most practically carried out. In the following, some possibilities to make the on-chip calibration in the system-level are presented.

5.3.1 Detection of distortion level through the separation of different dc-offsets

The balance can be detected in-directly from the dc-offset at the mixer output. An illustration of how the total dc-offset at the mixer output is cumulated due to several mechanisms is shown in Figure 5.10. The process tolerances cause dc-offset due to the device and biasing mismatch. Secondly, the self-mixing also causes some amount of dc-offset. The self-mixing is typically dominated by the LO leakage. Also, the strong test signal applied to the receiver input causes dc-offset due to the even-order nonlinearity. As discussed in Chapter 4, the CW test signal causes a dc-term when exposed to second-order nonlinearity. This dc-offset is similarly directly proportional to the square of the test signal amplitude, A_{RF}, as is the envelope beat term caused by the second-order nonlinearity and the AM contenting test signal. Therefore, the maximum IIP2, and the highest AM suppression for the downconverter could be achieved by minimizing this portion of the dc-offset.

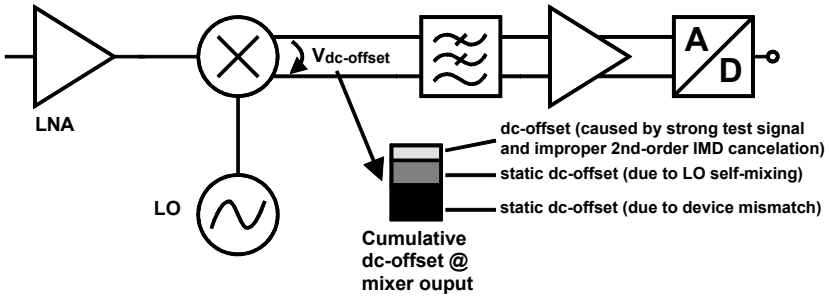


Figure 5.10 *Cumulative dc-offset separated according to the source mechanisms.*

The dc-offset caused by the second-order nonlinearity is basically a common-mode term. In theory, the on-chip calibration can be carried out in the manner illustrated for a single downconversion channel in Figure 5.11. First, the dc-offset is determined from the mixer output when no signal is applied to the LNA input. Then the dc-offset at the mixer output consists of only static dc-mismatch and LO self-mixing based effects. It is practical to use the subsequent analog receiver backend (bypassing the dc-offset compensation circuitry including possible highpass elements) for the measurement. Then any extra analog blocks, except, the balancing loads, are not required for the calibration. Instead, the logic, memory, and registers would be required to control the procedure. This first phase of the measurement is carried out step-by-step for all possible balancing settings. Then a strong out-of-band test signal is applied to the LNA input and the whole trimming range is measured again step-by-step. Finally, the measured cumulative dc-offset is compared to the static dc-offset. Thus it is possible to separate the part that needs to be minimized, and to determine the setting at which the smallest signal-dependent dc-offset is observed. An out-of-band test signal must be used because it has to be strong in order to cause an observable dc-offset. In the test-tone selection, the possible Rx frequency-sensitivity of the calibration, as shown in Figure 5.6a, should be taken into account.

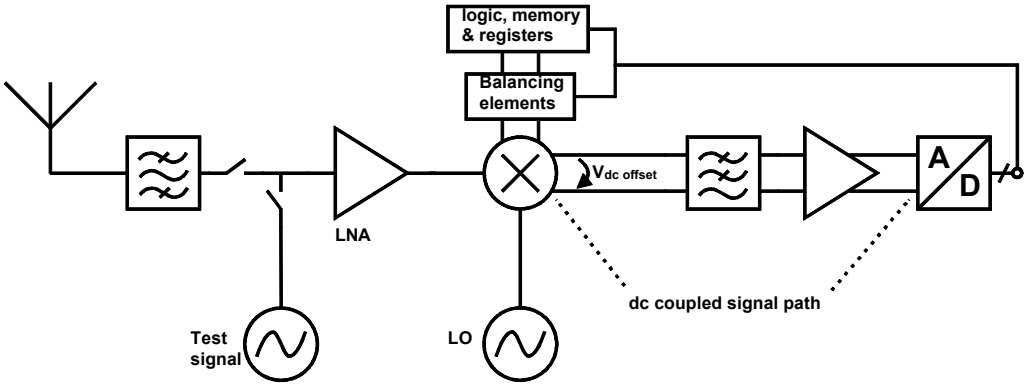


Figure 5.11 *One possible on-chip calibration procedure.*

In Figure 5.12, the calculated dc-offset of a double-balanced transconductance mixer according to Equation (5.5) is shown. The equation is derived in [P5]. The dc-offset floor-level of 4 mV is due to the static dc-offset caused by the load resistor mismatch ΔR=1%. In practice, the only variable is the RF signal amplitude A_{RF}. Its square causes a dc-term. In Figure 5.12, the second-order nonlinearity coefficient α'_2 has also been used as an illustrative variable. It can be referred to a certain IIP2 value in certain imbalance conditions as shown in Figure 5.13 for single-balanced and double-balanced configurations.

$$V_{DC} = R_L \cdot \eta_{nom} \cdot \frac{\Delta R}{2}\left(2I_T + \frac{1}{2} g_m \cdot \alpha_2^{'} \cdot A_{RF}^2 \right) \tag{5.5}$$

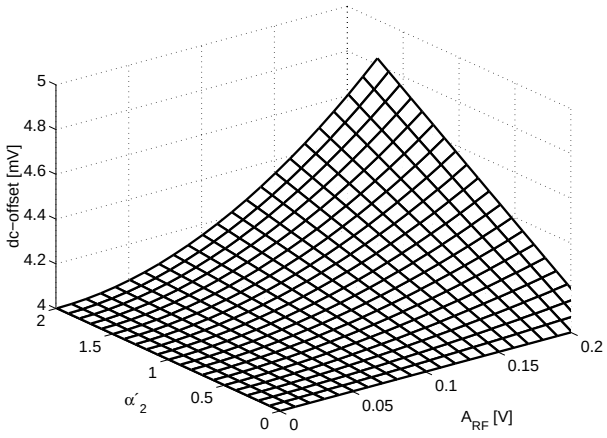


Figure 5.12 *Calculated dc-offset vs. second-order nonlinearity and RF signal amplitude of double-balanced mixer according to Equation (6.5). The values used for parameters R_L, η_{nom}, I_T, and g_m are 400Ω, 0.5, 2mA, and 15mS, respectively.*

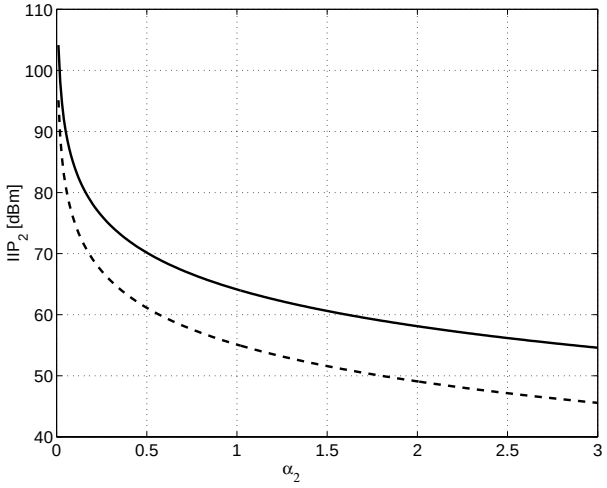


Figure 5.13 *Calculated IIP2 as a function of different α'_2 coefficients in single-balanced and double-balanced mixers. ΔR= 1%.*

5.3.2 Other possible methods to detect the imbalance on-chip

The calibration by monitoring and separating the dc-offsets as described above is only one option for carrying out the mixer balancing. Another rather similar process is to supply an input test signal, which includes a known AM content, to the receiver. Then the single-ended AM-contents are detected, and compared separately from I- and Q-mixers, as described in [82]. The AM-components are then equalized, e.g., in a manner similar to that explained in the previous sub-section. A disadvantage of when compared to the dc-separation method is that the complexity of the analog receiver backend increases because several AM-detectors and comparators are required.

A third potential option to detect the imbalance and calibrate the receiver is to use received signal strength indicator (RSSI)-detection. In [66], Tsurumi et al. present a system-level approach to eliminate the second-order distortion. They monitor the imbalance using RSSI-detection and then make the balancing using the Yamaji's idea of controlling the mixer transconductor bias current [79]. Furthermore, they have noticed temperature-dependence in the improvement method. The RSSI is used in the receiver to monitor the signal strength from the own channel and its neighboring channels. The monitoring can be done alternatively at the symbol-rate frequency or over a wider band because the second-order distortion causes spectral reshaping at low frequencies. Also, the monitoring could be done by a two-tone test, which however, is not practical.

5.4 I/Q-amplitude balancing

In principle, the gain mismatch between the two channels in a radio receiver can be corrected in any position after the division into two branches. In publication [P6], a simple method for I/Q-amplitude-balancing is briefly described. Although the I/Q-errors are usually corrected in the digital backend of the DCR, this method provides an analog option and can be used in, for example, receivers requiring high image-rejection performance.

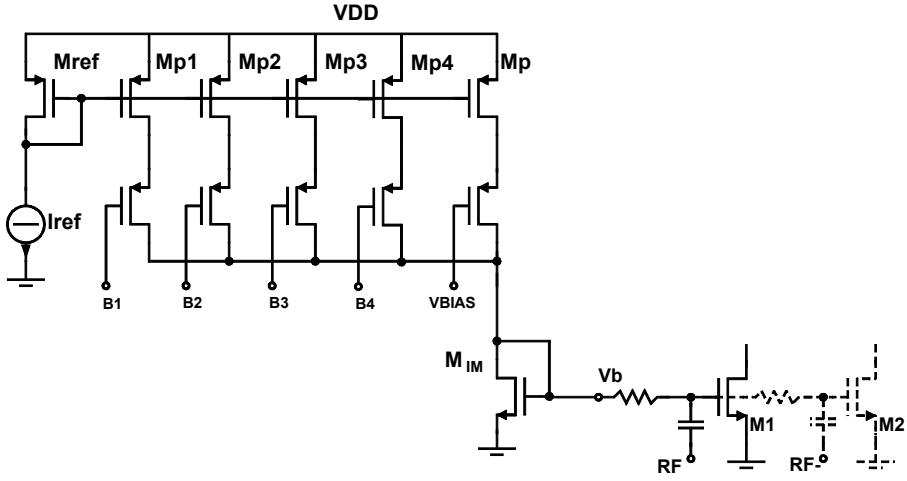


Figure 5.14 *IDAC used to bias I- and Q-mixers separately. Dashed parts illustrate the biasing of the driver stage in double-balanced mixer.*

Figure 5.14 illustrates a schematic of a mixer whose driver stage is biased by an adjustable current source controlled by bits B1-B4. The solid line describes a single-balanced mixer, while the dashed line describes the double-balanced mixer. The voltage conversion gain of the Gilbert-cell type transconductance mixer topologies is proportional to the g_m as follows

$$A_V = 20\lg\left(\frac{2}{\pi} g_m R_L\right), \tag{5.6}$$

where g_m is the transconductance of mixer's input transistor (M_1/M_2), R_L is the load resistance, and $(2/\pi)$ denotes the ideal loss due to the switching. The g_m of MOS transistor is defined as

$$g_m = \sqrt{2K_p \frac{W}{L} I_D} \ . \tag{5.7}$$

Here, K_P is the transistor transconductance coefficient, W and L are the transistor gate width and length, respectively, and I_D is the transistor channel current.

By adjusting the mixer conversion gains the total gain error between the receiver's channels can be practically minimized. A fixed current can bias another mixer while the mixer of the other quadrature branch can be biased using an adjustable bias current. The other option is to use adjustable currents to bias both mixers. In Figure 5.15a and 5.15b, the measured channel balances are shown before and after the gain equalization. Figure 5.16 illustrates the measured I/Q-gains of three receiver samples as functions of the equalization code words.

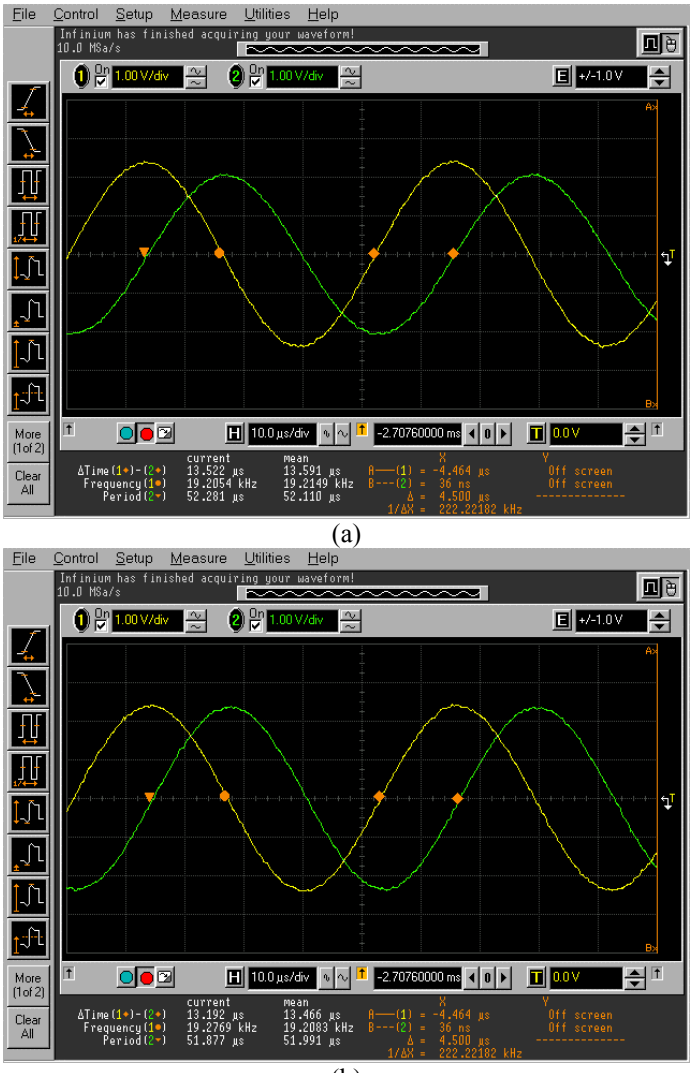


Figure 5.15 *Measured waveforms of the IQ signals (a) before and (b) after tuning of the receiver presented in [P6]. Yellow line represents the fixed (I) and green the adjustable (Q) channel.*

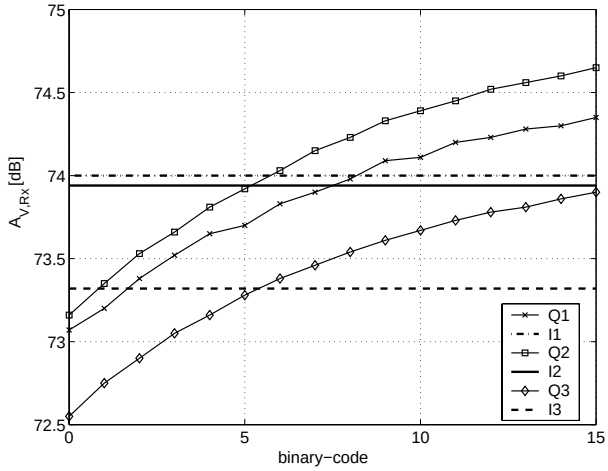


Figure 5.16 *Trimmed IQ balances of three circuit samples presented in [P6].*

6 Summary of publications

In this chapter, a brief overview of each publication is given.

[P1] Active Mixers for Direct Conversion Receivers with 0.35-µm BiCMOS

This paper introduces an analysis of three different active mixers. The emphasis is on the system considerations for the mixers as blocks in the direct conversion receiver. Also, the importance of the proper interface design for the LNA, LO, and baseband is discussed.

The basic idea of the paper is to make a comparison between three slightly different active mixer topologies. The mixers are implemented in the same process run to be able to make a fair comparison. However, the bipolar mixer should have been scaled to the same current as the other two mixers. It could not have been possible without degenerating the input devices. Now the bipolar mixer has much higher gain compared to the other mixers.

The analysis and measurements show that the differences between the mixers are small. However, the LO-to-RF isolations of the mixers are different as well as their behavior as functions of the LO power and supply-voltage. Also, the IIP2 of a mixer is analyzed as a function of load imbalance in this work. Later investigations have shown that the bipolar mixer scaled to the same current than the other mixers would have provided worse linearity with a slightly better noise performance.

[P2] Design of Low-Voltage Active Mixer for Direct Conversion Receivers

This paper gives an evolutionary perspective to several mixer designs. Together with **[P1],** it makes a rather extensive comparison between different active double-balanced mixer topologies analyzed in this thesis. It also takes into account different requirements that are set for a mixer to be used in the integrated direct conversion receiver. The idea of the paper is to give perspective to the low supply-voltage issues in a Gilbert-cell topology. Also, the multimode design considerations of the mixers are briefly overviewed in the paper. The downconversion mixer by itself is quite easily made adaptive for use in different cellular standards at different operating frequencies. Two of the implemented mixers have adjustable conversion gain. However, it turns out that the mixer is not the optimal block to the diverse part of the direct conversion receiver gain control.

[P3] A Dual-Band RF Front-End for WCDMA and GSM Applications

This paper describes the circuit design of a dual-band, dual-mode RF front-end that uses only one signal path, except for the first transistor in the LNA. The implementation has an integrated single-ended to differential converter between the single-ended LNA and fully double-balanced mixers. The presented RF front-end is designed for low supply-voltage of 1.8 V and has low current consumption. The mixer uses a current boost to relax the requirements due to the low supply-voltage. Therefore, the use of larger resistive load at the mixer output is enabled, giving more gain without degradation in noise or linearity performance.

[P4] A 22mA, 3.0dB NF Direct Conversion Receiver for 3G WCDMA

A single-chip direct conversion receiver is presented in this paper. Excellent performance is achieved with very low power consumption. The low power consumption is a consequence of the successful interface design that has enabled the removing of the interstage buffers between the building stages. Also, the current consumption of each single building block has been reduced to a level at which the performance is not yet degraded. The quadrature LO signals are generated from the external LO signal with an on-chip RC poly-phase filter.

[P5] Characterization of IIP2 and DC-Offsets in Transconductance Mixers

In this paper, the dc-offsets and envelope distortion in transconductance mixers are studied. The paper is divided into three parts that supplement each other: theory, simulations, and measurements. The basic idea is that the dc-offset is not necessarily minimized simultaneously when IIP2 of a circuit is maximized. The theoretical work is rather a mismatch analysis than a complex mixer nonlinearity analysis, but gives a good intuitive sense about the relations of dc-offsets and second-order distortion in balanced structures.

[P6] Calibration Techniques of Active BiCMOS Mixers

This paper illustrates a realization of a single-balanced mixer that utilizes direct load tuning as a method to improve the even-order intermodulation rejection. Also, a mixer biasing technique is implemented that can be used to improve the amplitude balance between I- and Q-channels. The design is a part of a prototype receiver including an LNA and baseband filters. The circuit also has LO generation circuitry that includes an ECL divider, and differential bipolar LO buffers. The LO signals are generated from the external double frequency signal. The direct load tuning method is found to operate as predicted theoretically in **[P5]**. This work also takes into account sensitivity of the methods to certain nonidealities, i.e., reception frequency handovers and downconversion band responses.

[P7] Single-Chip Multi-Mode Receiver for GSM900, DCS1800, PCS1900, and WCDMA

A single-chip direct conversion receiver with four input bands and two different baseband bandwidths is presented in this paper. The LNA-mixer interface is made programmable so that an LNA-mixer interface can be selected according to the reception band. The mixer includes circuitry to improve the even-order intermodulation rejection. The method used is direct tuning. The LO signal is generated on-chip from the double frequency LO signal by a divide-by-two circuit. The presented single-chip receiver illustrates very high LO-to-RF isolation, which results from a combination of circuit and layout techniques.

[P8] RF Gain Control in Direct Conversion Receivers

The focus of this paper is on the LO-to-RF isolation and LO self-mixing effects, as well as the dc-offsets and baseband transients. The LO self-mixing itself is a well-known problem in direct conversion receivers. However, the paper introduces a problem that involves to full FDD systems. The LO signal that has leaked to the LNA input goes through the same signal path as the signal itself. If a

part of the receiver gain control is distributed to the RF front-end simultaneously, with the RF gain being changed also, then the strength of the leaked LO signal at the mixer input is changed too. Hence, particularly if the gain chance is rapid, the dc-offset at the mixer output is changed as well, resulting in a large transient.

The paper summarizes three receiver implementations from the LO-to-RF isolation point of view. Finally, by combining several circuit and layout techniques the leaked LO signal power at the RF input below –98 dBm was measured.

7 Conclusions

In this thesis, the design and characterization of downconversion mixers and direct conversion radio receivers for UTRA/FDD WCDMA and GSM standards with the Silicon and Silicon-Germanium BiCMOS technologies are described. The RF front-end, and especially the mixer, limits the performance of direct conversion architecture. The problems relate to dc-offsets, imperfect LO-to-RF isolation, I/Q-channel imbalance, and especially to the second-order distortion. The main focus of the research described in this thesis is on the analysis of second-order distortion in mixers, and techniques to improve their second-order intermodulation rejection. The circuit design and layout techniques to improve the LO-to-RF isolation in receivers are also studied. A mixer-centric approach is adopted in the presentation of the RF front-end and receiver design considerations.

The work summarizes the design of several downconversion mixers. The implementations can be viewed also as an evolutionary process. Three of the implemented mixers are integrated as the downconversion stages in the large direct conversion receiver chips. One is realized, together with the LNA, as an RF front-end. Some stand-alone structures have also been characterized. Two mixers, which have been integrated as single-chip analog receivers, include calibration structures to improve the second-order intermodulation rejection. The theoretical mismatch analysis of the second-order distortion in the mixers gives an intuitive and comprehensive illustration of the phenomenon.

The presented work provides insight into how mixer immunity against second-order distortion can be improved. Promising results have been demonstrated by the implemented calibration structures. The receiver IIP2 of at least +40 dBm is achieved repeatedly. Also the relationship between the dc-offsets and IIP2 that was found in the theoretical work is significant because it establishes one possible procedure for the receiver on-chip calibration. As a result, several methods of detecting the distortion on-chip and the possibility of integrating the automatic on-chip calibration procedures in order to produce a repeatable and high receiver IIP2 are discussed.

The achieved LO-to-RF isolation in the single-chip multi-mode receiver illustrated in [P7] is very high. The LO power measured at the receiver input of –98 dBm is so small that the LO spurious emission becomes negligible. In addition, several high performance downconversion mixers are presented in the publications.

The work presented in this thesis shows that the DCR could compete with the superheterodyne receiver despite the conservative objections of many RFIC designers.

Errata

[P1]

page 22, in Table 1. “20GHz” should read “2.0GHz”.

[P5]

page 1035, in Table II. Improvement for Sample 6 should be 28 dB instead of 50 dB. Also in page 1035, below Fig. 12. “The improvement in performance is at least 15 dB but the highest benefit is even 50 dB.” The highest benefit should be 31 dB instead of the given 50 dB.

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