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Pipeline Analog-to-Digital Converters for Wide-Band Wireless Communications

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Abstract

During the last decade, the development of the analog electronics has been dictated by the enormous growth of the wireless communications. Typical for the new communication standards has been an evolution towards higher data rates, which allows more services to be provided. Simultaneously, the boundary between analog and digital signal processing is moving closer to the antenna, thus aiming for a software defined radio. For analog-to-digital converters (ADCs) of radio receivers this indicates higher sample rate, wider bandwidth, higher resolution, and lower power dissipation.

The radio receiver architectures, showing the greatest potential to meet the commercial trends, include the direct conversion receiver and the super heterodyne receiver with an ADC sampling at the intermediate frequency (IF). The pipelined ADC architecture, based on the switched capacitor (SC) technique, has most successfully covered the widely separated resolution and sample rate requirements of these receiver architectures. In this thesis, the requirements of ADCs in both of these receiver architectures are studied using the system specifications of the 3G WCDMA standard. From the standard and from the limited performance of the circuit building blocks, design constraints for pipeline ADCs, at the architectural and circuit level, are drawn.

At the circuit level, novel topologies for all the essential blocks of the pipeline ADC have been developed. These include a dual-mode operational amplifier, low-power voltage reference circuits with buffering, and a floating-bulk bootstrapped switch for highly-linear IF-sampling. The emphasis has been on dynamic comparators: a new mismatch insensitive topology is proposed and measurement results for three different topologies are presented.

At the architectural level, the optimization of the ADCs in the single-chip direct conversion receivers is discussed: the need for small area, low power, suppression of substrate noise, input and output interfaces, etc. Adaptation of the resolution and sample rate of a pipeline ADC, to be used in more flexible multi-mode receivers, is also an important topic included. A 6-bit 15.36-MS/s embedded CMOS pipeline ADC and an 8-bit 1/15.36-MS/s dual-mode CMOS pipeline ADC, optimized for low-power single-

chip direct conversion receivers with single-channel reception, have been designed.

The bandwidth of a pipeline ADC can be extended by employing parallelism to allow multi-channel reception. The errors resulted from mismatch of parallel signal paths are analyzed and their elimination is presented. Particularly, an optimal partitioning of the resolution between the stages, and the number of parallel channels, in time-interleaved ADCs are derived. A low-power 10-bit 200-MS/s CMOS parallel pipeline ADC employing double sampling and a front-end sample-and-hold (S/H) circuit is implemented.

Emphasis of the thesis is on high-resolution pipeline ADCs with IF-sampling capability. The resolution is extended beyond the limits set by device matching by using calibration, while time interleaving is applied to widen the signal bandwidth. A review of calibration and error averaging techniques is presented. A simple digital self-calibration technique to compensate capacitor mismatch within a single-channel pipeline ADC, and the gain and offset mismatch between the channels of a time-interleaved ADC, is developed. The new calibration method is validated with two high-resolution BiCMOS prototypes, a 13-bit 50-MS/s single-channel and a 14-bit 160-MS/s parallel pipeline ADC, both utilizing a highly linear front-end allowing sampling from 200-MHz IF-band.

Keywords: analog integrated circuit, analog-to-digital conversion, CMOS, BiCMOS, double sampling, IF-sampling, direct conversion, comparator, pipelined analog-to-digital converter, switched capacitor, time-interleaving, multi-mode, calibration.

Preface

The research reported in this thesis has been carried out at the Electronic Circuit Design Laboratory, Helsinki University of Technology between years 1998–2002. The work is done within several research projects funded by Finnish National Technology Agency (TEKES), Nokia Networks, and Nokia Mobile Phones. During these years, I had also a privilege of participating the Graduate School in Electronics, Telecommunications, and Automation (GETA), which partially funded the work. I thank Electronic Circuit Design Laboratory and GETA for making the work possible. I am also grateful for the following foundations for the financial support: Eemil Aaltosen Säätiö, Elektroniikkainsinöörien Säätiö, Nokia Oyj:n Säätiö, Tekniikan edistämissäätiö.

I would like to express my gratitude to my supervisor Prof. Kari Halonen, who has introduced me into the data converter research and given me the opportunity to work relatively freely under these interesting projects. Without his encouragement, thrust, and way of pushing the design goals this work would not have been completed. I also warmly thank Prof. David A. Johns and Prof. Piero Malcovati for reviewing this thesis and for their valuable comments and suggestions.

I am specially grateful for Dr. Mikko Waltari, who has been my supervisor and partner in the A/D converter research. His inexhaustible storage of innovative ideas, sovereign technical competence, and strong commitment to the projects we have carried out together has been indispensable. The valuable technical contribution of the junior team members in these projects, Tuomas Korhonen, Mikko Aho, and Väinö Hakkarainen, is also gratefully acknowledged.

The other team I have been working with consisted of Dr. Aarno Pärssinen, Jarkko Jussila, Dr. Kalle Kivekäs, and Jussi Ryynänen, who all contributed their own technical specialty in the direct conversion receiver research. I am particularly thankful for the highly motivated, but, friendly and cozy atmosphere the team members created. The close cooperation and humorous spirit within this group have been very essential in completing this work.

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They have created an exceptional, effective and comfortable, atmosphere and helped in many of the everyday issues related to the work.

Huge thanks to my friends, especially, for remaining me of more important things than this work. The various activities and hobbies of the 'VirNuMiToVi' association have offered excellent contrast for the day's work. And in particular, my fellow students Dr. Kimmo Kalliola and Jani Ollikainen deserve big thanks for keeping up an inspiring, but, entertaining, academic pressure during the whole studies.

Finally, my warmest thanks for the support and love I have received from my family, my mother Anja, my father Markku, and my sister Kaisa. And the biggest thanks to my dear wife, Nadja, who has supported me during the difficult times, as well as shared the good moments. Her love, care, and liveliness have carried me on in this doctoral work.

Lauri Sumanen
Espoo, November 2002

Symbols and Abbreviations

A	Amplitude, area, amplifier voltage gain
A_f	Voltage gain of feedback amplifier
A_0	Open loop DC-gain
b_i	Number of output codes
B	Bit, effective stage resolution
B_n	Noise bandwidth
C	Capacitance, number of uncorrected bits
C_c	Compensation capacitance
C_f	Feedback capacitance
C_L	Load capacitance
$C_{L,H}$	Effective hold mode load capacitance
$C_{L,tot}$	Total load capacitance
C_{out}	Parasitic output capacitance
C_{ox}	Gate-oxide capacitance
C_{par}	Parasitic input capacitance
$C_{s,i}$	Sampling capacitance
d	Scaling parameter of transistor size
D_i	Multiplier of reference voltage
D_{out}	Digital output

DNL	Differential nonlinearity
e	Noise, error, scaling parameter of transistor current
e_q	Quantization error
e^2	Noise power
E_{conv}	Energy per conversion step
$ENOB$	Effective number of bits
f	Frequency, feedback factor
f_{block}	Frequency of blocker
f_{dig}	Digital signal frequency
f_{in}	Input frequency
f_{LO}	Local oscillator frequency
f_S	Sampling frequency
f_{sig}	Signal frequency
f_{spur}	Frequency of spurious tone
FOM_A	Area figure of merit
g	Conductance
G_i	Interstage gain
G_{code}	Coding gain
G_k	Fourier series coefficient of gain mismatch
g_m	Transconductance
G_P	Processing gain
GBW	Gain bandwidth product
HR	Headroom
i	Stage index
I	Current

I_{amp}	Total amplifier current consumption
I_D	Drain current
I_{max}	Maximal output current of amplifier
I_{ref}	Reference current
IIP	Input intercept point
INL	Integral nonlinearity
IP	Intercept point
j	Capacitor index
k	Boltzmann's coefficient, load capacitance relation, number of stages, error correction coefficient
K	Amplifier current gain, gain error correction coefficient
L	Channel length
m	Capacitor switching parameter, number of different stage resolutions, index
M	Number of parallel channels
M_{IM}	Implementation margin
n	Number of sampling capacitors, index
N	Number of bits, noise power
$N_{aperture}$	Aperture jitter limited resolution
N_H	Number of harmonics
n_{max}	Number of capacitors
N_{TH}	Thermal noise floor
$N_{thermal}$	Thermal noise limited resolution
ND_{ADC}	A/D converter noise distance
NF	Noise figure

MDS	Minimum detectable signal level
OSR	Oversampling ratio
p_1'	Non-dominant pole of amplifier
P_D	Power dissipation
P_{IMD}	Power of the intermodulation product
P_{out}	Output power
PA	Peak-to-average signal power ratio
Q	Quality factor
Q_{ch}	Channel charge
Q_i	Number of quantization steps
r	Redundancy bit, resistance
R	Resistance
r_{ds}	Output resistance of a transistor
R_{eff}	Effective thermal resistance
r_{on}	Switch on-resistance
r_{out}	Amplifier output resistance
R_{ref}	Reference value (current or voltage)
S	Error correction coefficient
S_P	Signal rms power
$SNDR$	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
SR	Slew rate
t	Time
T	Absolute temperature, sampling period
t_{ox}	Oxide thickness

thd	Total harmonic distortion
V	Voltage
V_{DD}	Positive supply voltage
V_{ds}	Drain-source voltage
$V_{ds,sat}$	Drain-source saturation voltage
V_{FS}	Full-scale voltage
V_{gs}	Gate-source voltage
V_{in}	Input voltage
V_k	Fourier series coefficient of offset mismatch
V_{LSB}	Voltage corresponding to the least significant bit
V_{margin}	Safety margin of drain-source saturation voltage
V_{os}	Offset voltage
$V_{os,c}$	Comparator offset voltage
V_{SS}	Negative supply voltage
V_T	Threshold voltage
W	Channel width
X	Input
Y	Output
α	Capacitor mismatch
β	Offset voltage, transistor parameter
γ	Gain error
δ	Relative capacitor mismatch
ε	Error
ε_{A_0}	Amplifier gain settling error
ε_τ	Amplifier GBW settling error

μ	Carrier mobility
ω	Corner frequency
σ	Noise standard deviation, clock jitter
σ_a	Rms aperture jitter
ϕ	Clock phase
ϕ_H	Hold phase
Φ_k	Fourier series coefficient of timing mismatch
ϕ_S	Sample phase
2G	Second-generation
3G	Third-generation
A/D	Analog-to-digital
ADC	Analog-to-digital converter
BB	Baseband
BER	Bit-error rate
BiCMOS	Bipolar complementary metal oxide semiconductor
CDMA	Code division multiple access
CDT	Code density test
CICC	Custom Integrated Circuits Conference
CM	Common mode
CMFB	Common mode feedback
CMOS	Complementary metal oxide semiconductor
CMRR	Common mode rejection ratio
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DFT	Discrete Fourier transform

dBc	Decibel relative to carrier
dBFS	Decibel relative to full-scale
DC	Direct current
DEM	Dynamic element matching
DLL	Delay locked loop
DNL	Differential nonlinearity
DR	Dynamic range
DSP	Digital signal-processing unit
ENOB	Effective number of bits
ERB	Effective resolution bandwidth
FDD	Frequency division duplexing
FFT	Fast Fourier transform
FPGA	Field programmable gate array
GBW	Gain bandwidth
GSM	Global System for Mobile Telecommunications
HD	Harmonic distortion
I	In-phase component
IC	Integrated circuit
IF	Intermediate frequency
IIP	Input intercept point
INL	Integral nonlinearity
I/O	Input-output
IP	Intercept point
IMD	Intermodulation distortion
IR	Image rejection

ISSCC	International Solid-State Circuits Conference
JSSC	Journal of Solid-State Circuits
LMDS	Local Multipoint Distribution System
LNA	Low-noise amplifier
LO	Local oscillator
LSB	Least significant bit
MDAC	Multiplying digital-to-analog converter
MOS	Metal oxide semiconductor
MSB	Most significant bit
NMOS	n-channel metal oxide semiconductor
OSR	Oversampling ratio
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PCS	Personal Communication System
PLL	Phase locked loop
PMOS	p-channel metal oxide semiconductor
PSD	Power spectral density
PSRR	power supply rejection ratio
Q	Quadrature component
QPSK	Quadrature phase-shift keying
RF	Radio frequency
ROM	Read only memory
RRC	Root raised cosine
RSD	Redundant sign digit
SC	Switched capacitor

SFDR	Spurious free dynamic range
S/H	Sample-and-hold
SI	Switched current
SiGe	Silicon-germanium
SNDR	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
SR	Slew rate
SRAM	Static random access memory
sub-ADC	Sub-analog-to-digital converter
THD	Total harmonic distortion
UMTS	Universal Mobile Telecommunication System
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VLSI	Very large-scale integrated circuit
WCDMA	Wideband code division multiple access
WLAN	Wireless Local Area Network
WLL	Wireless Local Loop

Contents

Chapter 1

Introduction

1.1 Motivation for the Thesis

Wireless communications have been the driving force in analog electronics development during the last decade. As the end products are produced for every-day use, the price, size, and weight of the devices play a large part in determining their design. Cost reduction and miniaturization require higher integration levels, while battery lifetime is one of the most critical parameters for the user of hand-held equipment requiring low power. Reasons for a high level of integration that are not so often mentioned are increased reliability and product security. At the same time wireless communication standards, like the Universal Mobile Telecommunication System (UMTS), Wireless Local Area Network (WLAN), Wireless Local Loop (WLL) or Local Multipoint Distribution Services (LMDS), are evolving towards higher data rates, thus allowing more services to be provided. These characteristics are also evolving to the basestation side, where the design is still mostly performance oriented.

High data rates imply wide bandwidths, while a continuously growing complexity of the modulation schemes and the desire for more flexible receivers push the boundary between analog and digital signal processing closer to the antenna, thus aiming for a software defined radio. These two trends set the specifications of the analog-to-digital converter (ADC) in a radio receiver, the ultimate goal being a receiver with an A/D converter directly sampling signals from the radio frequency (RF), depicted in Fig. 1.1. However, this would require an ADC with a sampling rate in the order of the RF input frequencies, which can rise to several giga hertz, and a dynamic range capable of handling signals with nano volt amplitudes in the presence of strong interferers. Because of several technological, technical, and fundamental physical limitations, this is

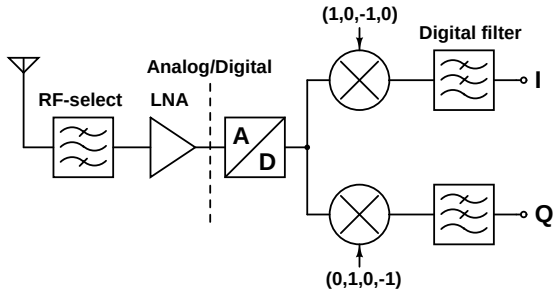

Figure 1.1 Direct A/D conversion of the RF-signal.

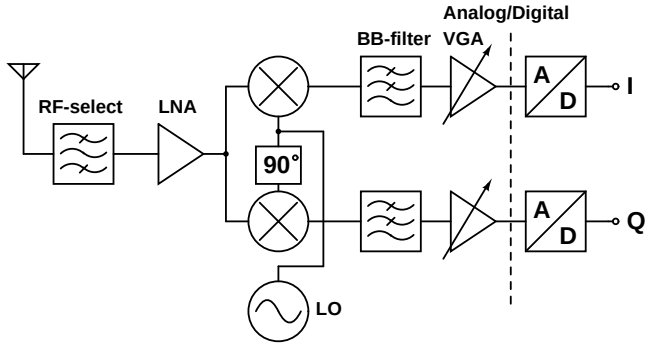

Figure 1.2 The direct conversion architecture.

not feasible with today's technology. To attain higher levels of integration, two realistic receiver architectures are widely developed: the direct conversion receiver, shown in Fig. 1.2 and the super heterodyne receiver where the analog-to-digital boundary is at the intermediate frequency (IF), shown in Fig. 1.3.

The specifications of the A/D converters differ considerably from each other in these two architectures. In the direct conversion receivers, analog channel selection filtering and variable gain amplifiers relax the dynamic range requirement, and thus the resolution, of the ADCs. The desired channel is also around zero frequency, which indicates a small sampling linearity requirement and low sample rate. In the receivers, where even several signal bands are digitized directly from the intermediate frequency, a very high linearity and sample rate are required in addition to high resolution, giving a large dynamic range. As the first architecture is almost solely used on the mobile side, the power dissipation is an important design constraint, while the second architecture is applied in basestations, making the overall performance essential.

Depending on the receiver architecture, analog filtering and gain control range, for A/D converters of such receivers a resolution of 6-14 bits and a sample rate between 10 and 300 MS/s are required. Furthermore, the A/D converter can be integrated with

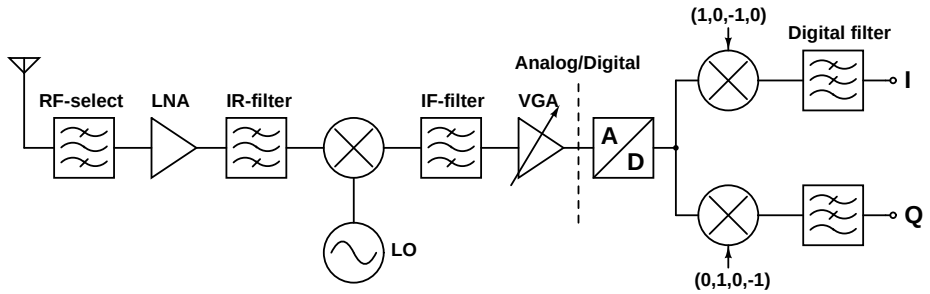

Figure 1.3 The super heterodyne architecture employing IF-sampling.

either analog or digital parts of a receiver, which dictate the technology of the ADC. The leading technology of the former domain is the BiCMOS, while the pure CMOS technology, which outperforms in the digital domain, is spreading to the analog side as well.

The most promising wide-band A/D converter architecture, covering a wide resolution and sample rate range, that can be applied in radio receivers with a high integration level is the pipelined topology, in which several low-resolution stages operating concurrently on different samples are cascaded. Other possible architectures are the two-step flash, sub-ranging, and folding and interpolating ADC topologies. Pipeline A/D converters can operate with supply voltages below 1 V, have potential for low power, are easily calibrated to obtain a higher resolution, and can be fabricated with CMOS, BiCMOS or bipolar processes.

In single-chip direct conversion receivers, power dissipation and area minimization are the most essential design constraints. The mixed-signal processing issues are especially challenging the A/D converter design: very sensitive analog blocks, like, for example, the low-noise amplifier (LNA), must not be disturbed by the digital rail-to-rail signals. Coexistence of several communication systems requires multi-mode receivers, in which ADCs with variable resolution and sample rate are needed.

In a multi-carrier wide-band IF-sampling super heterodyne receiver, the linearity and jitter of the sampling across the signal band, together with a large dynamic range, are required. Specific techniques, like, for example, bootstrapping, have to be applied in the sampling switches to attain high linearity when digitizing the signal directly from the IF of several hundreds of mega hertz. To achieve higher sample rates, parallelism can be introduced to a pipeline A/D converter. Mismatches in the parallel processing of analog signals create unwanted side bands that have to be avoided or compensated. Furthermore, some kind of calibration has to be employed to achieve a resolution greater than 10-12 bits, a limitation set by the accuracy of the integrated circuit (IC) processes,

with a pipeline ADC. The calibration should be to as small an excess in the area and power as possible and it should have a minimal effect on the normal operation.

The research described in this thesis is focused on the issues described above.

1.2 Research Contribution

The research has concentrated on pipeline A/D converters for wide-band direct conversion receivers and IF-sampling super heterodyne architecture. Requirements and optimization of the pipeline ADCs, at the circuit and architectural levels, have been addressed to meet the varying specifications of these target applications. Although the circuits have been designed according to the specifications of the target systems of these receiver architectures, they can be exploited in other applications as well, like video, for example. Based on the results of three projects at the Electronics Circuit Design Laboratory, the new ideas and circuits in this thesis have been partially reported in related publications [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16].

First, the requirements for the resolution and sample rate of an A/D converter, both in a direct conversion receiver and in an IF-sampling super heterodyne receiver, were studied based on the system specifications of a third-generation wide-band code division multiple access (WCDMA) telecommunications standard. Following that, the requirements for the building blocks of a pipeline stage were derived based on the known effects of their limited performance and unavoidable mismatch between the circuit elements. As a result of this analysis, design constraints at the architectural and circuit level were drawn.

The author has designed and implemented low-resolution medium sample rate pipeline A/D converters for direct conversion receivers for WCDMA applications. The first experimental circuit was a chip set [1, 2, 3], while the later three employed single-chip solution [4, 5, 6, 7, 8, 9]. The other members of the five-man research team included Dr. Aarno Pärssinen, Dr. Kalle Kivekäs, Mr. Jussi Ryynänen, and Mr. Jarkko Jussila. Dr. Aarno Pärssinen contributed to the system level design and optimization of the RF parts of the experimental circuits. The LNAs and downconversion mixers were designed by Mr. Jussi Ryynänen and Dr. Kalle Kivekäs, respectively, while Mr. Jarkko Jussila was responsible for the analog baseband circuitry and contributed to the system design. The author was responsible for the design of the A/D converters. Various innovations are related to the optimization of the pipeline ADCs for small substrate noise contribution, low power dissipation, small area, unbuffered interface with the analog baseband circuitry, and multi-mode operation.

Research on parallel pipeline A/D converters was carried out jointly with Dr. Mikko

Waltari. Partitioning of the resolution and the optimal number of parallel channels in time-interleaved pipeline A/D converters were analyzed by the author [10]. The design of the pipeline channel ADCs of the 10-bit prototype circuit was carried out by the author, while Dr. Mikko Waltari was responsible for the other building blocks [11, 12].

Wide-band pipeline A/D converters with IF-sampling capability have been studied by a team consisting of the author, Dr. Mikko Waltari, Mr. Tuomas Korhonen, Mr. Mikko Aho, and Mr. Väinö Hakkarainen. The front-end sample-and-hold circuit of the 13-bit IF-sampling self-calibrated A/D converter [13] was on Dr. Mikko Waltari's responsibility. Again, the author's part of the work has been the design of the pipeline ADC part. The new digital self-calibration method was developed by the author based on the ideas of Dr. Mikko Waltari and the author, while the algorithm was realized by Mr. Tuomas Korhonen [14]. Extrapolation of the calibration method to compensate gain errors between pipeline channel A/D converters of a 14-bit IF-sampling parallel pipeline ADC and circuit design of an experimental prototype were on the author's responsibility. The realizations of the analog circuit design and calibration algorithm were achieved by Mr. Mikko Aho and Mr. Väinö Hakkarainen, respectively.

At the circuit level, the emphasis was on comparators, which utilize low-power dynamic operation. A new dynamic comparator topology was developed [15], the offset properties of which were analyzed and experimentally compared with those of the previous topologies [16]. The offset measurements were carried out by Mr. Väinö Hakkarainen. The author also contributed to the design of various other novel building blocks of pipeline A/D converters, including operational amplifiers, reference voltage buffering, and bootstrapped switches.

1.3 Organization of the Thesis

The thesis is organized into seven chapters. After the introduction, chapter 2 reviews the basic theory of A/D converters and the quantities describing their performance, and the determination of the required resolutions and sample rates in radio receivers. A survey to state-of-the-art ADCs is given in terms of the physical limitations of the sample rate and accuracy, and the designs are compared using two figures of merit.

Chapter 3 covers the pipeline A/D converter architecture in general with its most essential parameters. Factors limiting the resolution and sample rate of pipeline ADCs are summarized and analyzed.

Design of the critical circuit blocks of pipeline A/D converters, including the operational amplifier, dynamic comparator, and reference voltages generating circuit is the topic of chapter 4.

Chapter 5 concentrates on the special requirements of the A/D converters of a single-chip direct conversion receiver. Emphasis is on handling of mixed-signal design issues and minimization of power dissipation and area. Adaptation of the sample rate and resolution in multi-mode applications are also discussed.

In chapter 6 multiplication of the sample rate by introducing parallelism into a pipeline ADC is considered. The parasitic side bands introduced by non-ideal analog parallel signal processing and their compensation are discussed. A simple method to optimize the number of parallel channels and stage resolution for power is derived.

Enhancement of the A/D converter resolution by utilizing self-calibration is handled in chapter 7. The known calibration and error-averaging methods are briefly reviewed and classified and the developed digital self-calibration technique for pipeline ADCs is introduced. Finally, conclusions are drawn.

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Chapter 2

Wide-Band Analog-to-Digital Converters

An analog-to-digital converter quantizes an analog signal into a digital code at discrete time points. According to the sampling theorem [1], the input signal band is limited to half of the sampling frequency to avoid aliasing with the sample rate repeated spectra. The so-called Nyquist rate A/D converters can digitize frequencies up to this frequency and have thus great potential for wide-band wireless communication applications. In this chapter the quantization process is explained and parameters describing the performance of an analog-to-digital converter are presented. Considerations relating to the specification of the A/D converter resolution and sample rate as a part of the system design of a radio receiver are covered as well.

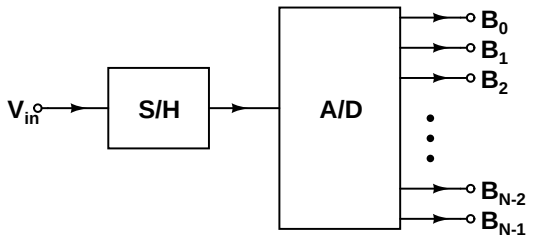

Figure 2.1 General block diagram of an A/D converter.

2.1 Ideal A/D Converter

An analog-to-digital converter performs the quantization of analog signals into a number of amplitude-discrete levels at discrete time points. A basic block diagram of an A/D converter is shown in Fig. 2.1. A sample-and-hold (S/H) amplifier is added to the input to sample the analog input and to hold the signal information at the sampled value during the time needed for the conversion into a digital number. The analog input value V_{in} is converted into an N-bit digital value using the equation

$$\frac{V_{in}}{R_{ref}} = D_{out} + e_q = \sum_{m=0}^{N-1} B_m 2^m + e_q. \tag{2.1}$$

In the equation, R_{ref} represents a reference value, which may be a reference voltage, current or charge. B_{N-1} is the most significant bit (MSB) and B_0 is the least significant bit (LSB) of the converter. The quantization error e_q represents the difference between the analog input signal V_{in} divided by R_{ref} and the quantized digital signal D_{out} when a finite number of quantization levels is used. Eq. 2.1 can be partly rewritten as

$$D_{out} = \sum_{m=0}^{N-1} B_m 2^m. \tag{2.2}$$

The sampling operation of analog signals introduces a repetition of input signal spectra at the sampling frequency and multiples of the sampling frequency. To avoid aliasing of the spectra, the input bandwidth must be limited to not more than half the sampling frequency (Nyquist criterion) [1].

2.2 A/D Converter Specifications

It is essential to understand analog-to-digital converter specifications to get an insight into the design criteria for converters. The DC-specifications for the static linearity are widely known. Dynamic specifications of A/D converters give a better insight into the applicability of a converter in a telecommunications system, where linearity and spectral purity are essential.

2.2.1 Static Specifications

The most important measures of static or DC-linearity of A/D converters are integral nonlinearity (INL) and differential nonlinearity (DNL). These properties actually indicate the accuracy of a converter and include the errors of quantization, nonlinearities,

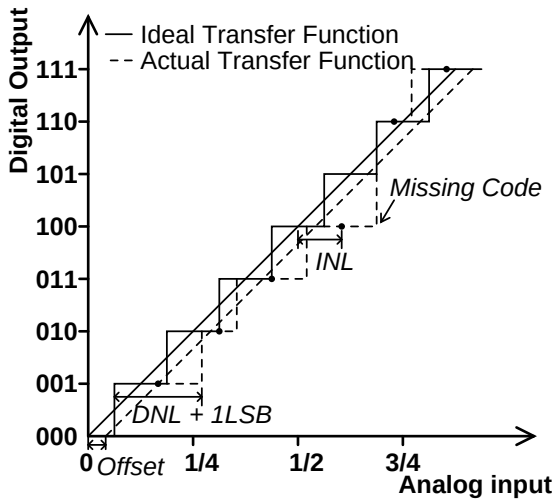

Figure 2.2 Transfer function of a 3-bit A/D converter.

short-term drift, offset and noise. The definitions of static linearity of A/D converters are indicated in the transfer curve of a converter. An example of a transfer curve of a 3-bit A/D converter can be seen in Fig. 2.2. An ideal N-bit analog-to-digital converter converts a continuous, analog input signal into a time discrete, quantized digital word. If the input signal amplitude scale is from zero to the full-scale voltage V_{FS} the ideal step corresponding to the least significant bit of a converter is V_{LSB}

$$V_{LSB} = \frac{V_{FS}}{2^N}. \tag{2.3}$$

Integral nonlinearity (INL), sometimes called relative accuracy, is defined as the deviation of the output code of a converter from the straight line drawn through zero and full-scale excluding a possible zero offset. The nonlinearity should not deviate more than $\pm 1/2$ LSB of the straight line drawn. This INL boundary implies a monotonic behavior of the converter. Monotonicity of an analog-to-digital converter means that no missing codes can occur [2].

Differential nonlinearity (DNL) error gives the difference between two adjacent analog signal values compared to the step size of a converter generated by transitions between adjacent pairs of digital code numbers over the whole range of the converter. The DNL of ADC output D_i can be written as

$$DNL(D_i) = \frac{V_{in}(D_i) - V_{in}(D_{i-1}) - V_{LSB}}{V_{LSB}}, \tag{2.4}$$

where D_i and D_{i-1} are two adjacent digital output codes. There is a direct connection between the INL and DNL. The INL for output D_m can be obtained by integrating the DNL until code m

$$INL(D_m) = \sum_{i=1}^{m} DNL(D_i). \tag{2.5}$$

DNL and INL are determined with a high-frequency input signal using the code density test (CDT) [3, 4].

2.2.2 Dynamic Specifications

Dynamic performance parameters include information about noise, dynamic linearity, distortion, settling time errors, and sampling time uncertainty of an A/D converter. It should be noted that all the measures following are both frequency and signal amplitude dependent. Furthermore, unless otherwise specified, they are obtained with a full-scale input signal.

2.2.2.1 Signal-to-Noise Ratio

The quantization process introduces an irreversible error, which sets the limit for the dynamic range of an A/D converter. Assuming that the quantization error of an ADC is evenly distributed, the power of the generated noise is given by

$$e_q^2 = \frac{V_{LSB}^2}{12}, \tag{2.6}$$

where V_{LSB} is the quantization step. If a single-tone sine wave signal with a maximum amplitude is adopted for a converter with a large number of bits (N$\geq$5), the signal rms power is given by

$$S_P = \frac{V_{FS}^2}{4 \cdot 2}. \tag{2.7}$$

Substituting Eq. 2.3 into Eq. 2.6 the signal-to-noise ratio (SNR) for a single-tone sinusoidal signal can be obtained to be

$$SNR = 2^N \sqrt{\frac{3}{2}} \doteq (6.02 \cdot N + 1.76)\, dB. \tag{2.8}$$

When determining the SNR, the ratio between the frequency of the sine wave and the sampling frequency should be irrational. If the input signal deviates from the sine wave, the constant term, which depends on the amplitude rms value of the waveform, differs from 1.76 dB. Eq. 2.8 indicates that each additional bit, N, gives an enhancement of 6.02 dB to the SNR. If oversampling is used, which means that the sample rate f_S is

much larger than the signal bandwidth f_{sig}, the quantization noise is averaged over a larger bandwidth and the signal-to-noise ratio becomes larger, written as

$$SNR = 2^N \sqrt{\frac{3}{2}} \cdot \sqrt{OSR} \doteq (6.02 \cdot N + 1.76 + 10\log(OSR))\, dB, \tag{2.9}$$

where the oversampling ratio OSR is given by

$$OSR = \frac{f_S}{2 \cdot f_{sig}}. \tag{2.10}$$

In the Nyquist rate A/D converters, the signal bandwidth is normally equal to $f_S/2$ resulting in an OSR equal to one, while Eq. 2.9 suggests that the signal-to-noise ratio increases by 3 dB per octave of oversampling.

2.2.2.2 Total Harmonic Distortion

Any nonlinearity in an A/D converter creates harmonic distortion. In differential implementations, the even order distortion components are ideally canceled. However, the cancellation is not perfect if any mismatch or asymmetry is present. The total harmonic distortion (THD) describes the degradation of the signal-to-distortion ratio caused by the harmonic distortion. By definition, it can be expressed as an absolute value with

$$thd = \frac{\sqrt{\Sigma_{j=2}^{N_H+1} V^2(j \cdot f_{sig})}}{V(f_{sig})}, \tag{2.11}$$

where N_H is the number of harmonics to be considered, $V(f_{sig})$ and $V(j \cdot f_{sig})$ the amplitude of the fundamental and the j^{th} harmonic, respectively.

2.2.2.3 Signal-to-Noise and Distortion Ratio

A more realistic figure of merit for an ADC is the signal-to-noise and distortion ratio (SNDR or SINAD), which is the ratio of the signal energy to the total error energy including all spurs and harmonics. SNDR is determined by employing the sine-fit test, in which a sinusoidal signal is fitted to a measured data and the errors between the ideal and real signal are integrated to get the total power of noise and distortion [3, 5]. If all tones and spurs other than the harmonic distortion are considered as noise, the signal-to-noise ratio can be obtained from the SNDR by subtracting the total harmonic distortion from it

$$snr_{real} = sndr - thd, \tag{2.12}$$

where *sndr* and *thd* are given in absolute values.

2.2.2.4 Spurious Free Dynamic Range

In wireless telecommunication applications, large oversampling ratios are often used and the spectral purity of the A/D converter is important. For such situations, a proper specification is the ratio between the powers of the signal component and the largest spurious component within a certain frequency band, called spurious free dynamic range (SFDR). The SFDR is usually expressed in dBc as

$$SFDR(dBc) = 10 \cdot log\left(\frac{V^2(f_{sig})}{V^2(f_{spur})}\right), \tag{2.13}$$

where $V(f_{sig})$ is the rms value of the fundamental and $V(f_{spur})$ the rms value of the largest spurious. For an exact SFDR definition, the power level of the fundamental signal relative to the full-scale must also be given. Normally the limiting factor of the SFDR in ADCs is harmonic distortion. In most situations, the SFDR should be larger than the signal-to-noise ratio of the converter [6].

2.2.2.5 Effective Number of Bits

In ideal A/D converter systems, the maximum analog bandwidth is equal to half the sampling bandwidth, according to the Nyquist theorem. The effective resolution bandwidth (ERB) is defined as the maximum analog frequency for which the signal-to-noise ratio of the system is decreased by 3 dB or 1/2 LSB with respect to the theoretical value. The number of bits obtained in this way for a single-tone full-scale sinusoidal test signal is called the effective number of bits (ENOB)

$$ENOB = \frac{SNDR - 1.76dB}{6.02dB}. \tag{2.14}$$

2.2.2.6 Dynamic Range

Dynamic range (DR) is the input power range for which the signal-to-noise ratio of the ADC is greater than 0 dB. The dynamic range can be obtained by measuring the SNR as a function of the input power.

2.2.2.7 Intermodulation Distortion

Intermodulation distortion (IMD) is a standard method of describing linearity in radio receivers. This parameter is not commonly used in the case of ADCs because of

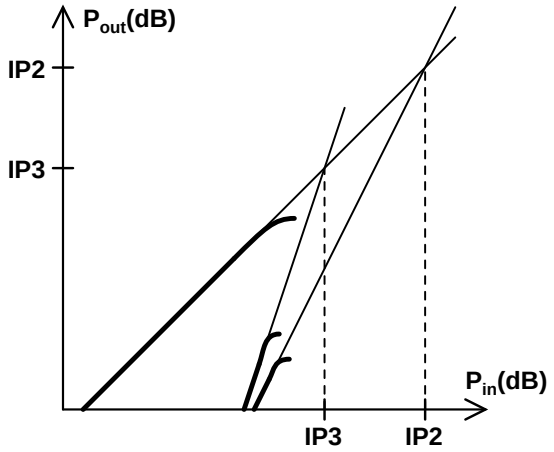

Figure 2.3 Third- and second-order intercept points.

the different nonlinearity characteristics between other analog signal processing blocks and A/D converters. However, special attention has to be paid to the intermodulation characteristics when the received channel is well below the out-of-band interferers at the input of the ADC. This is possible in high-resolution wide-band ADCs for base stations, for example. Therefore, the concept of intermodulation distortion is presented here. Another linearity issue is the compression at high input signal levels, caused in an ADC by the signal clipping when the input signal exceeds the full-scale voltage swing. This can be compared to the input compression in RF parts, although in the case of RF blocks the gain compression is typically smoother. To avoid clipping, the average signal level at the ADC input is typically set well below the full scale.

It is well known that two excitation tones at frequencies f_1 and f_2 cause a third-order intermodulation product at $2f_1 - f_2$ and $2f_2 - f_1$, which are very likely to fall into the signal band. In direct conversion receivers, the second-order distortion results in an intermodulation product at DC and $f_2 - f_1$, which should be considered as well. The nonlinearity performance of the A/D converters in radio receivers is typically specified with the intercept points shown in Fig. 2.3. As the gain of an ADC is nominally one, the input and output intercept points are equal, and usually referred to only as intercept point (IP). The third- and second-order intercept points (IP3 and IP2) are defined using the two-tone test when operating at weakly nonlinear region, i.e. second- and third-order nonlinearities dominate. If the input power is increased by 1 dB, the second- and third-order products rise 2 and 3 dB, respectively. IP2 and IP3 are defined at the points where the nonlinear product would equal the signal level if the components rise as at the small signal levels. The intermodulation points can be expressed as

$$IP3 = \frac{3}{2}P_{out} - \frac{1}{2}P_{IMD3} \tag{2.15}$$

and

$$IP2 = 2P_{out} - P_{IMD2}, \tag{2.16}$$

where P_{out} is the output power, and P_{IMD3} and P_{IMD2} the respective power levels of the intermodulation products.

The intermodulation distortion is closely linked to the harmonic distortion (HD) [7]. Theoretically, the relation between the second intermodulation product power level P_{IMD2} and harmonic distortion components power level P_{HD2} is given by

$$P_{IMD2} = 2P_{HD2}, \tag{2.17}$$

while the relation between the respective third-order products can be calculated to be

$$P_{IMD3} = 3P_{HD3}. \tag{2.18}$$

2.3 Considerations of A/D Converters in Radio Receivers

Wireless communication systems usually define receiver requirements by specifying signal levels referred to the antenna connector in the type-approval test. The requirements for each desired receiver building block can be determined by following appropriate signals down the receiver chain to assign gain, dynamic range, second- and third-order linearity, and noise figure to each block. The resulting specifications for the A/D converter, being the last analog block in the chain, depend strongly on the architecture of the receiver, i.e. on the amount of gain and filtering preceding the ADC. The relevant requirements of the ADC are given in terms of the sample rate, dynamic range, and linearity. Receiver architectures considered here are the direct conversion receiver with a single-channel reception and IF-sampling super heterodyne receiver employing multi-channel reception. The former, depicted in Fig. 1.2, consists of an LNA, downconversion mixers, channel selection filters, and VGAs preceding the two medium-resolution, medium sample rate ADCs. The latter has only an LNA, image rejection filter, mixer, IF-filter, and VGA before the signal is sub-sampled by a high-resolution, high sample rate ADC, as indicated in Fig. 1.3.

As most of the circuits presented in this thesis are intended to be used in third-generation (3G) basestation applications, the specifications below are taken from the

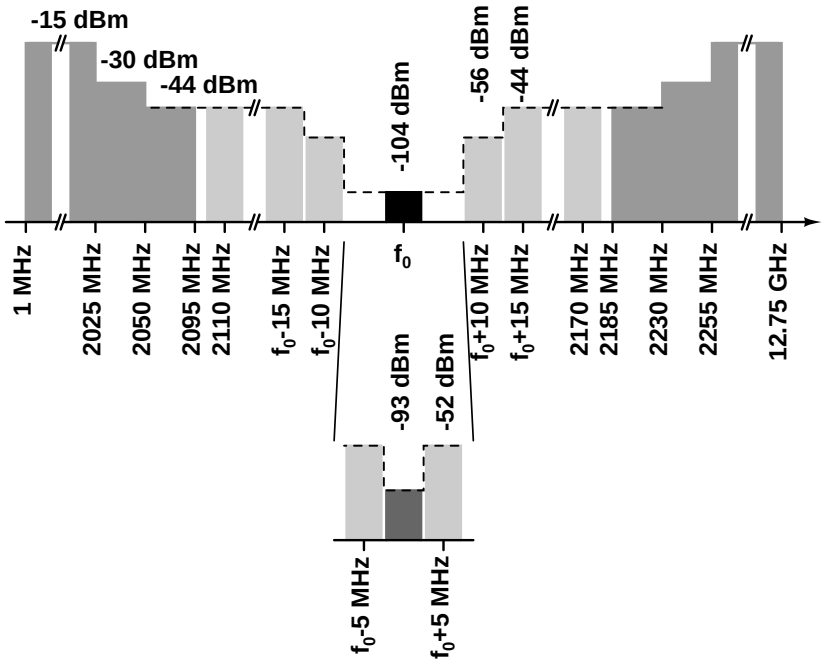

Figure 2.4 Template of adjacent channel and blocking signal levels for WCDMA in down-link.

wide-band code division multiple access (WCDMA) system, developed under the Third Generation Partnership Project. Extensions to other communication systems can be derived according to the respective specifications. The specifications are derived for the mobile terminals, mainly because of two reasons. First, the specification of the up-link direction is less explicit than in the case of the down-link direction. Second, as most of the circuits are intended for small range basestations, the desired performance is closer to the user end. However, the methods and formulas given below, can be similarly applied for the basestation specifications. In Fig. 2.4 is shown the template of interference and blocking signal levels of WCDMA standard in down-link direction, i.e. in the mobile terminal [8]. The wanted channel signal is set to a power level of -93 dBm for the test with the adjacent channel, while, for the channels further apart, the power level is reduced to -104 dBm. The level of the interfering signals with the respective frequency offsets is marked in the figure. An overview of the standard is given in Tab. 2.1.

Table 2.1 WCDMA Standard Overview.

RF frequencies	
Up-link	1920-1980 MHz
Down-link	2110-2170 MHz
Channel separation	5 MHz
Signal bandwidth	3.84 MHz
Chip rate	3.84 Mcps
Spreading factor	4-256
Modulation scheme	QPSK, hybrid-QPSK
Access method	FDD, WCDMA

2.3.1 Sample Rate

According to the sample theorem, the sample rate must be at least twice the signal bandwidth. In a digital communication system, signal bandwidth is expressed as symbol or chip rate. As pointed out in Eqs. 2.9–2.10, SNR, limited by the quantization noise, is raised by 3-dB steps when OSR is increased. Thus, a high sample rate is preferred, while the power dissipation, including also the digital signal-processing unit (DSP), sets the upper limit for the maximization.

To facilitate detection in the digital receiver, the sampling rate should be determined as a multiple of the symbol rate, or chip rate in a CDMA system. Furthermore, when digital signal processing is performed at the symbol rate or some multiple of it, the relative symbol clock frequency error between the transmitter and receiver can be assumed to be constant over the duration of one block of symbols and thus the error can be compensated [9]. In the WCDMA system, the nominal chip rate is set to 3.84 Mcps, which indicates a minimal sample rate of 7.68 MS/s in case of a direct conversion receiver with zero IF.

In IF-sampling super heterodyne receivers, there are more degrees of freedom in the frequency planning, first, with respect to the selection of the sample rate and, second, to the determination of the intermediate frequency. It is desirable to link IF frequency f_{IF} and sample rate f_S. A preferable ratio is $f_{IF} = (n \pm 1/4)\, f_S$, where n is an integer corresponding to the sub-sampling ratio, since it eases quadrature decomposition [10]. However, the IF frequency is typically fixed in the system design of the receiver front-end, and only the sample rate can be selected, following the limitations of the sample theorem. As low a sample rate as possible relative to the signal bandwidth minimizes power dissipation, but the sub-sampling ratio becomes large, which means high noise energy is folded down from the multiples of the sampling frequency.

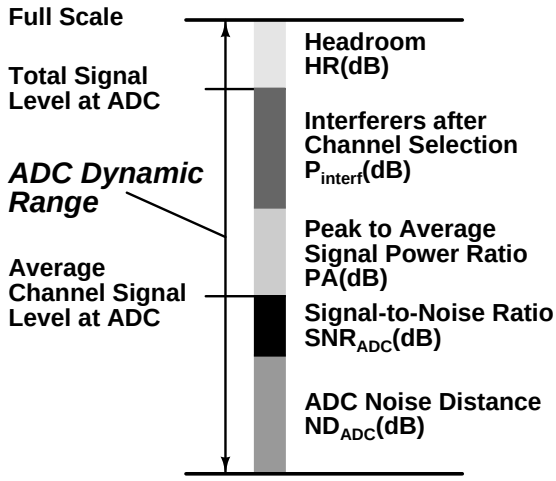

Figure 2.5 ADC dynamic range specification.

2.3.2 Dynamic Range

Resolution of the A/D converter is determined by its dynamic range specification, which can in turn be derived from the sensitivity, maximal input power, and blocking test specifications for a given receiver architecture. A conceptual diagram of the ADC dynamic range with its specifications in decibels is shown in Fig. 2.5. The diagram can be explained as follows. Essentially, the dynamic range, required from the ADC, is based on the desired bit-error rate (BER) of the reception, which in turn sets the minimum signal-to-noise ratio (SNR) at the ADC output. As the A/D converter itself is not allowed to deteriorate the SNR, its noise contribution must be well below the minimal signal-to-noise ratio SNR_{ADC} for a particular BER level. Thus, ADC noise distance ND_{ADC} must be added to the specifications to get the rms channel signal level at ADC. Since clipping of the received signal would generate harmonic distortion, the peak-to-average signal power ratio (PA) must be taken into account. In WCDMA, where QPSK modulation is applied, PA can be as high as 12 dB, while in a constant envelope modulation a minimum of 3 dB is achieved [11]. Depending on the attenuation mask of the channel selection filter, preceded by the ADC, a residual power is left from the adjacent channel and out of band blockers. The required margin P_{interf} can be obtained from the template of Fig. 2.4 and the filter transfer function. Finally, the headroom (HR) on top covers DC-offset, VGA gain errors, and signal amplitude transients.

The signal-to-noise ratio specification at the ADC output can be derived directly from the prescribed BER level. According to simulations, a received energy per bit to the effective noise power density ratio (E_b/N_t), which can be approximated to equal the

Table 2.2 Specification of ADC dynamic range for WCDMA.

Headroom	HR	6–10 dB
Interferers after Channel Selection	P_{interf}	10–40 dB
Peak-to-Average Signal Power Ratio	PA	8–12 dB
Signal-to-Noise Ratio	SNR_{ADC}	-18 dB
ADC Noise Distance	ND_{ADC}	10–20 dB
ADC Dynamic Range	DR	16–64 dB

signal-to-noise ratio (SNR_{min}), of 5.2 dB is sufficient to detect a 12.2 kbps speech signal with BER$\leq 10^{-3}$ [12]. The requirement for the signal-to-noise ratio at ADC (SNR_{ADC}) is relaxed by the processing (G_P) and coding gains (G_{code}), but an implementation margin (M_{IM}) must be reserved for the DSP realization, given in decibels

$$SNR_{ADC} = SNR_{min} - G_P - G_{code} + M_{IM}, \tag{2.19}$$

where G_{code} is a function of the channel and data coding and of the modulation, while G_P is result from the despreading of a CDMA signal [13]. For a speech signal, $G_P + G_{code}$ is approximately 25 dB, while for M_{IM} 2 dB is a good approximation but it depends strongly on the implementation [14]. Using the values above, the SNR specification becomes SNR_{ADC} = -17.8 dB. The signal-to-noise ratio is further decreased by the receiver noise figure (NF) and thermal noise floor (N_{TH}) indicating a minimum detectable signal level (MDS) at the antenna output

$$MDS = SNR_{ADC} + NF + N_{TH}, \tag{2.20}$$

where the thermal noise floor is given in dBms by

$$N_{TH} = 10\log\left(kTB_n \cdot 10^3\right), \tag{2.21}$$

where k is the Boltzmann's constant, T the temperature, and B_n noise bandwidth [13]. The thermal noise floor is typically determined at room temperature (T=290 K), which results N_{TH}=-108.2 dBm for a WCDMA system (B_n=3.84 MHz). If a noise figure of 9 dB is allowed for the receiver, MDS equals -117 dBm, which is the value given in the WCDMA specifications [8].

The factors affecting the dynamic range specification of an ADC together with their approximate numerical values, calculated and collected from the literature, are given in Tab. 2.2. The resulting dynamic range requirement is 16–64 dB, which is calculated for a 3G WCDMA direct conversion receiver with a single-channel reception. Additionally, the dynamic range at the antenna connector can be determined as a ratio of the maxi-

mum and minimum power spectral density (PSD) levels. In the case of a single-channel receiver, this implies the gain control range of the VGA, while in a multi-channel receiver the variation of the rms power of all the received channels must be added to the A/D converter dynamic range. In WCDMA specifications, e.g. the dynamic range at antenna connector in the 3.84 MHz band is -25 dBm-(-106.7 dBm)=81.7 dB.

2.3.3 Linearity

Nonlinearity is another point of major concern in receiver design. The linearity of an A/D converter is commonly characterized by the level of harmonic distortion (HD), which, as presented above, is closely linked to the intermodulation distortion (IMD), which in turn is usually the base of the linearity characterization of a radio receiver [7].

In the case of an IF-sampling super heterodyne receiver, the third-order intercept point, IP3, is of major importance, while in a direct conversion receiver the second-order intercept point, IP2, is of equal interest. Both parameters can be tested for the whole receiver with the two-tone test. The third-order input intercept point of the whole receiver consisting of cascaded stages can be calculated with an equation

$$\frac{1}{iip3} = \frac{1}{iip3_1} + \frac{G_1}{iip3_2} + \frac{G_1 G_2}{iip3_3} + \ldots + \frac{\prod_{i=1}^{n-1} G_i}{iip3_n}, \tag{2.22}$$

where $iip3_i$ and G_i are the input intercept point and power gain of the i^{th} block as absolute values. The last analog block in a receiver chain is the ADC, which results $iip3_n = ip3_{ADC}$. A similar equation holds for $iip2$ as well. The filters attenuating the interferers along the chain must be taken into account. If a steep channel selection filter is placed before the A/D converter, the unwanted tones are filtered sufficiently and the contribution of the ADC to the receiver linearity is negligible. This is the case in a direct conversion receiver, while in an IF-sampling super heterodyne receiver, the attenuation of the IF-filter can be traded with the linearity of the A/D converter.

Specifications for IP2 and IP3 in a WCDMA system can be calculated from the standard [8, 13].

2.4 A/D Converter Survey

The high and medium speed Nyquist rate ADCs reported in the Custom Integrated Circuits Conference (CICC), International Solid-State Circuits Conference (ISSCC), Journal of Solid-Sate Circuits (JSSC), and Symposium on VLSI Circuits during the period 1995-2001 are plotted in Fig. 2.6. The three most common architectures, i.e.

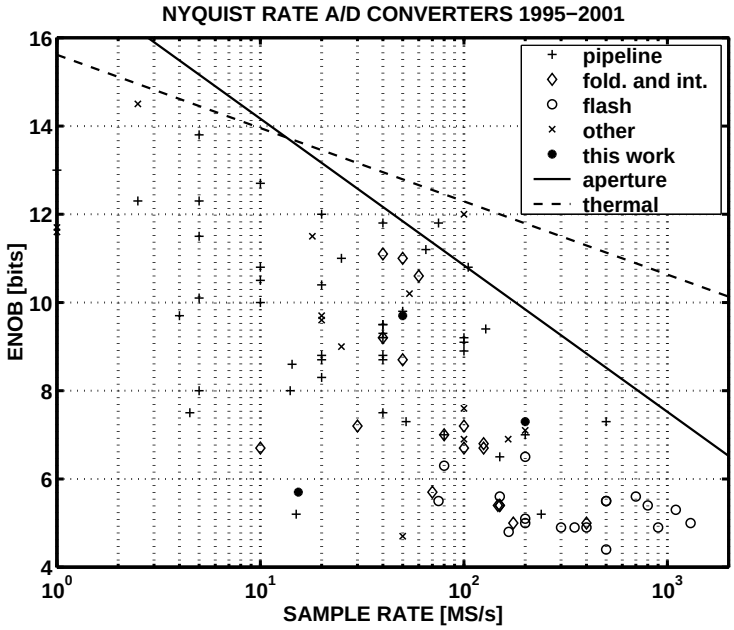

Figure 2.6 High-speed A/D converters from years 1995-2001.

pipelined, folding and interpolating, and flash A/D converters, are labeled, as well as the experimental pipeline ADCs included in this thesis. The trade off between the resolution, in terms of the effective number of bits (ENOB), and sample rate, is apparent. Furthermore, different architectures have specified application ranges. The flash ADCs are optimal for very high sample rate and low resolution, while the folding and interpolating architecture is applied for medium and low resolution up to a 400-MS/s sample rate. The pipeline ADCs cover the largest range reaching from 14-bit 5-MS/s up to 7-bit 500-MS/s performance. $\Delta\Sigma$-modulators, not shown in Fig. 2.6, employ oversampling and noise-shaping to achieve the best performance at signal frequencies up to a few megahertz.

At high resolutions the spectral noise density at the A/D converter input is dominated by the thermal noise inherited from the sampling operation. If the thermal noise is considered as the only noise source, the attainable resolution $N_{thermal}$ is calculated in appendix A to be

$$N_{thermal} = \frac{1}{2}\log_2\left(\frac{V_{FS}^2}{6kTR_{eff}f_S}\right) - 1, \tag{2.23}$$

where k is the Boltzmann's constant, T the temperature, f_S the sample rate, and R_{eff} an effective thermal resistance, which includes the effects of all noise sources. Especially at high sample rates, the resolution is limited, in turn, by the aperture uncertainty

resulting from a random deviation of the sample interval. An rms aperture jitter σ_a is shown in appendix A to limit the effective resolution to

$$N_{aperture} = \log_2\left(\frac{2}{\sqrt{3}\pi f_S \sigma_a}\right) - 1. \tag{2.24}$$

Both of these ADC resolution boundaries are plotted as references in Fig. 2.6 with parameters $R_{eff} = 3000\ \Omega$ and $\sigma_a = 3$ ps. The thermal noise is actually becoming to limit the resolution above 14-bit, and is thus more suitable to characterize $\Delta\Sigma$-modulators. The resolution boundary set by the aperture jitter is clearly more relevant when Nyquist rate ADCs are considered. As crystals with a relative dependence of the jitter on the frequency are used as ADC clocks, the aperture jitter is actually increasing with the sample rate. This is visible in Fig. 2.6 as a steeper slope for the attainable resolution at a given sample rate than that calculated from Eq. 2.24. However, neither of these limitations is even close to the ultimate limits dictated by physical laws, like, for example, Heisenberg uncertainty principle, leaving an attractive field for engineers to improve the implementations [15].

When quantifying the efficiency of the A/D converter implementations, power dissipation should be included in the resolution and sample rate. However, power dissipation is a nonlinear function of the resolution and sample rate and a wide variety of figures of merit exist to relate all these parameters. The most widely accepted measure of the effectiveness of the design is the energy per conversion step, defined as

$$E_{conv} = \frac{P_D}{2^N \cdot f_S}, \tag{2.25}$$

where P_D is the power dissipation, N the resolution, and f_S the sample rate. Comparison of the same designs using Eq. 2.25 is given in Fig. 2.7, where power dissipation is plotted as a function of $2^N \cdot f_S$. The lower the energy per conversion step the better the ADC. However, it should be noted that the reported A/D converter power dissipations are often excluding output buffers and references. The solid and dash dotted lines, within which all the state-of-the-art Nyquist rate ADCs fall, represent constant E_{conv} levels of 0.5 pJ and 50 pJ, respectively. The pipeline A/D converters tend to be more efficient than those that are folding and interpolating, while the flash ADCs show the highest energy per conversion step. The designs presented in this thesis employ good energy efficiency.

In addition to the power dissipation, the silicon area contributes significantly to the effectiveness of an A/D converter implementation. A similar figure of merit that relates

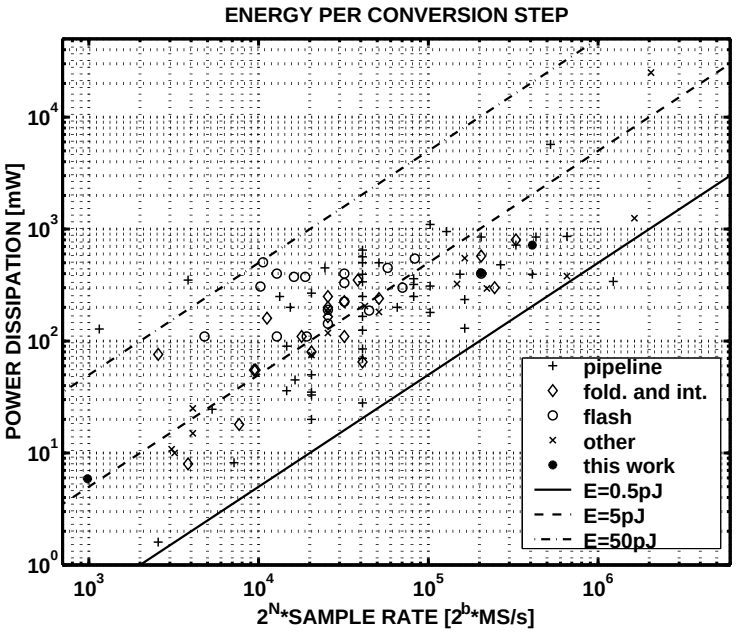

Figure 2.7 Power dissipation plotted as a function of the number of the quantization levels times sample rate for Nyquist rate ADCs published 1995-2001.

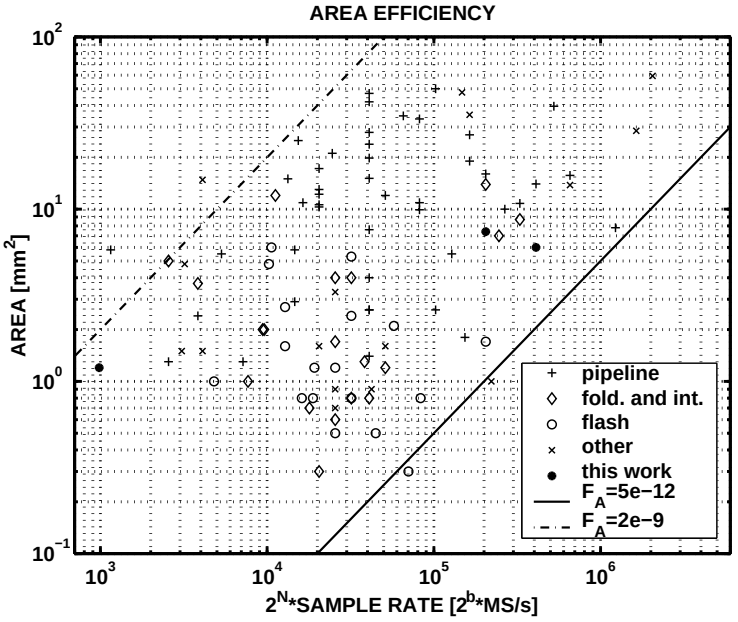

Figure 2.8 Active area plotted as a function of the number of the quantization levels times sample rate for Nyquist rate ADCs published 1995-2001.

the area A, resolution N and sample rate f_S can be derived from equation

$$FOM_A = \frac{A}{2^N \cdot f_S}. \tag{2.26}$$

In Fig. 2.8 the active silicon area of the recently reported ADCs is plotted as a function of the number of conversion steps times the sample rate. It should be noted that the total die area only was reported for some of the referred designs, which distorts the comparison. The straight lines in Fig. 2.8 represent the figure of merit levels of $5 \cdot 10^{-12} m^2/Hz$ and $2 \cdot 10^{-9} m^2/Hz$. Compared to the efficiency figure of the same A/D converters, the spread is much larger in the case of FOM_A and no clear tendencies between the different architectures exist. Furthermore, as most of the published Nyquist rate A/D converters are academic demonstration circuits, their layout is seldom area-optimized and no state-of-the-art silicon process is employed. As can be seen, the prototypes included in this thesis do very well when compared to other pipeline ADCs. The flash ADCs tend to be area-efficient, while the pipeline ones have the worst figures of merit, which is a result of the predominating switched capacitor (SC) realization leading to a large area consumption. However, the efficiency per conversion step is a better figure of merit than the area when comparing the designs.

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Chapter 3

Pipeline Analog-to-Digital Converter Architecture

In a pipeline A/D converter, the quantization is distributed along a pipelined signal chain resulting in an effective architecture for high-resolution high-speed ADCs. By pipelining the signal, a very high throughput can be achieved by introducing a latency time that is linearly dependent on the number of stages. In this chapter, the pipeline ADC architecture is reviewed in general and the principle of redundant sign digit (RSD) coding, which is assumed to be applied from now on unless otherwise stated, is presented. The error sources of a switched capacitor (SC) pipeline stage and their effect on the ADC performance are compiled and the design constraints of the pipeline ADC presented.

A general block diagram of a pipeline A/D converter is shown in Fig. 3.1. It consists of *k* low-resolution stages, delay elements synchronizing the stage outputs, and digital

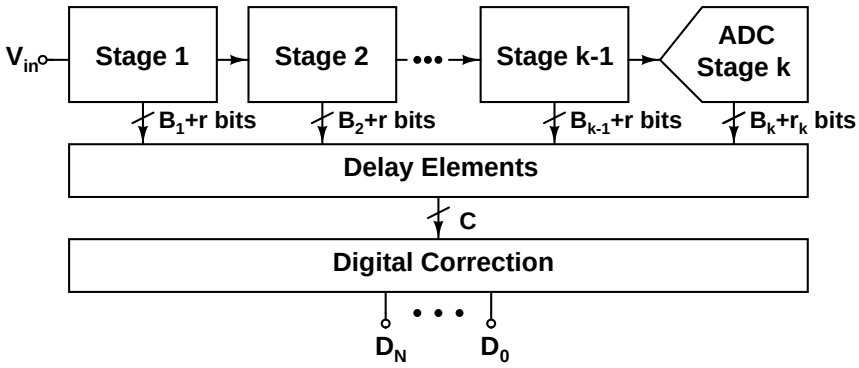

Figure 3.1 Block diagram of a pipeline A/D converter.

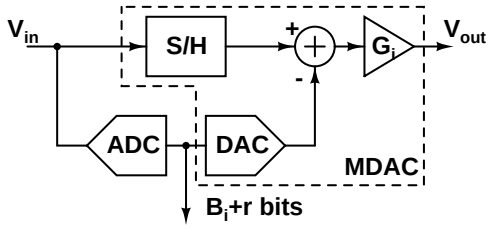

Figure 3.2 Block diagram of one pipeline stage.

correction logic. Each stage has a resolution of $B_i + r_i$ bits, of which B_i represents the effective stage resolution and r_i the redundancy for a comparator offset correction algorithm. The first $k-1$ normal pipeline stages described below usually have equal resolution, i.e. $B_1 \ldots B_{k-1}$ are equal, or the resolution might even differ from stage to stage. The redundancy in these stages is constant $r_i = r$ for $i = 1 \ldots k-1$, and $r = 1$ if error correction is employed, while in the case of no redundancy $r = 0$. The last stage consists only of a sub-quantizer that does not usually employ redundancy ($r_k = 0$). The total resolution N of a pipeline ADC with m different stage resolutions B_j, k_j units of each, is given by

$$N = \sum_{j=1}^{m} k_j B_j + B_k, \tag{3.1}$$

where B_k is the resolution of the last stage. The effective stage resolution in a pipeline A/D converter is typically in the range of 1-4 bits.

In Fig. 3.2 a block diagram of one pipeline stage is presented. Each stage comprises a low-resolution sub-analog-to-digital converter (sub-ADC) and an arithmetic unit called the multiplying digital-to-analog converter (MDAC) that performs a sample-and-hold (S/H) operation, coarse D/A conversion, subtraction, and amplification. In operation, each stage performs an A/D conversion of B_i effective bits with r-bit redundancy, converts the digital output back to analog and subtracts it from the sampled and held analog input. This residue is amplified with a gain of

$$G_i = 2^{B_i+1-r} \tag{3.2}$$

and fed to the next stage. The stages operate concurrently; that is, at any time, the first stage operates on the most resent sample while all other stages operate on residues from previous samples. Serial stages operate in opposite clock phases. The digital outputs of the stages $B_1 + r \ldots B_k + r_k$ are delayed so that their value correspond to the same input

sample. The resulting total C bits are fed to the correction circuitry

$$C = \sum_{i=1}^{k} (B_i + r_i) . \tag{3.3}$$

The analog transfer function of a $B_i + r$-bit pipeline stage follows the equation

$$V_{out,i} = G_i V_{in,i} + D_i V_{ref}, \tag{3.4}$$

where D_i is an integer, the value of which is dependent on the output of the sub-ADC and $D_i \in [-(2B_i - 1), +(2B_i - 1)]$ with a step of 2 when $r = 0$ and 1 otherwise. The other terms G_i and $V_{in,i}$ and the addition in Eq. 3.4 are provided by the MDAC.

Several techniques to improve the speed and accuracy of the pipeline A/D converter architecture has been developed after the basic concept of cascading of low-resolution stages was introduced in 1987 [1]. A sophisticated digital correction algorithm with 1 bit of redundancy ($r = 1$) in each stage is commonly used in the pipeline A/D converters to relax the quantization accuracy specifications in sub-ADCs [2]. The conversion speed of a pipeline A/D converter can be increased by placing several chains of time-interleaved pipeline ADCs in parallel [3]. The input signal is sampled with the full sampling frequency while the sample rate of each pipeline chain is reduced by the number of parallel channels. Parallel pipeline ADCs are discussed in detail in chapter 6. The resolution can be enhanced by introducing dithering to average out the effect of constant errors, or by trimming or calibrating the effect of component mismatch [4]. Self-calibration of a pipeline ADC is the topic of chapter 7.

Traditionally pipeline A/D converters have been implemented using the SC technique. The resolution of the reported designs has varied between 6 and 16 bits, while the highest sample rate achieved at 10-bit level with CMOS is around 200 MHz [5]. Probably the best state-of-the-art pipeline ADC reported has a resolution of 14 bits with a sample rate 75 MS/s [6]. Current mode techniques have been exploited as well to achieve a resolution of 10 bits at 32 MS/s sample rate [7]. At 8-bit accuracy, a conversion rate as high as 4 GS/s is reached [8].

3.1 Redundant Sign Digit Coding (RSD)

A sophisticated digital correction algorithm, called redundant sign digit (RSD) coding, with 1 bit of redundancy ($r = 1$) in each stage is commonly used in pipeline A/D converters to relax the quantization accuracy specifications in sub-ADCs [2]. Adding a redundant bit means increasing the stage resolution by one bit minus one quantization

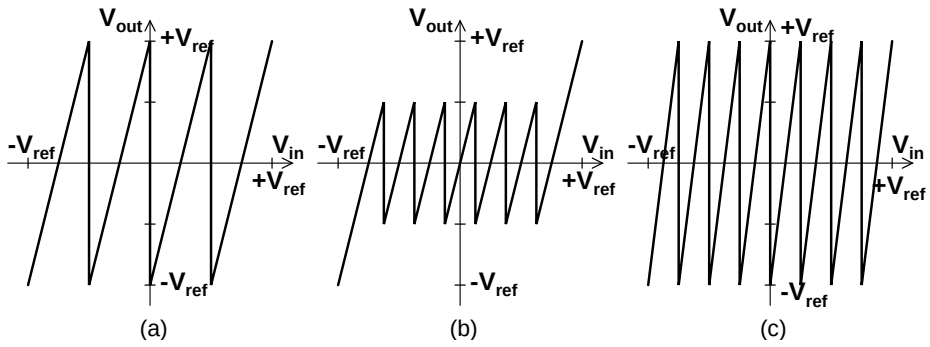

Figure 3.3 Transfer functions of (a) a 2-bit ($B_i = 2$, $r = 0$), (b) 2.5-bit ($B_i = 2$, $r = 1$), and 3-bit stages ($B_i = 3$, $r = 0$).

level. Thus, the amount of redundancy is commonly referred as 0.5 bits. The principle of RSD coding with voltage references is depicted in Fig. 3.3 where a 2-bit ($B_i = 2$, $r = 0$) and a 3-bit ($B_i = 3$, $r = 0$) stage without redundancy are compared to that of a 2.5-bit ($B_i = 2$, $r = 1$) stage. By introducing redundancy, the number of quantization levels is increased from four to six while the gain is kept at four. Furthermore, compared to the 3-bit stage, there is one quantization level less in the 2.5-bit stage but the distance between two levels is equal. The locations of these levels are shifted by $V_{ref}/8$ and the gain is four instead of eight. As a result, the output of a 2.5-bit stage stays between $\pm V_{ref}/2$ for input voltages of $\pm 7V_{ref}/8$.

The effect of RSD coding can be obtained from Fig. 3.4, where the transfer functions of a 2-bit and 2.5-bit stages are plotted under the presence of equal quantization errors. The low-resolution A/D conversion is realized using comparators with threshold voltages equal to the quantization step locations. Thus, any offset in the comparator threshold level is translated into a quantization error and appears as a shift in the location of the quantization step, which is indicated with V_{os} in Fig. 3.4. As seen from the dashed line of the 2-bit stage, the comparator offset causes an overflow of the stage output saturating the next stage and resulting in an erroneous quantization. However, in the 2.5-bit stage, marked with the solid line, an equal comparator offset results in a stage output greater than $V_{ref}/2$ but smaller than V_{ref}. Thus, no information is lost and a correct quantization result can be reconstructed using the digital output of the next stage. The amount of comparator offset the redundant sign digit coding can tolerate is in this case $\pm V_{ref}/8$, which guarantees that the stage output stays within $\pm V_{ref}$.

In general, when $r = 0$ the B_i bits of stage i are resolved with $2^{B_i} - 1$ quantization steps, while the redundancy of $r = 1$ increases the number of quantization steps to

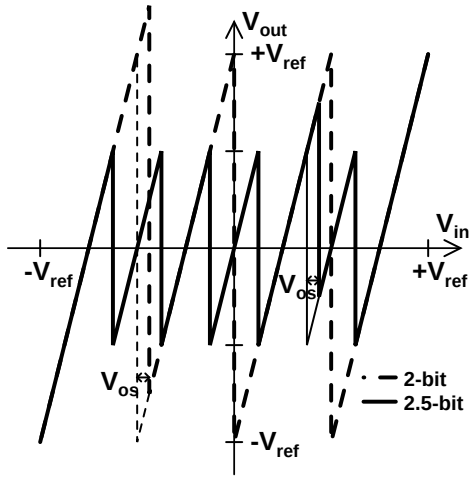

Figure 3.4 Effect of ADC offset voltages in 2-bit and 2.5-bit stages.

$2^{B_i+r}-2$. The number of quantization steps Q_i is given by

$$Q_i = 2^{B_i+r} - r - 1. \tag{3.5}$$

The locations of these quantization steps relative to the reference voltage V_{ref}, which corresponds to the full-scale input amplitude are

$$\pm V_{ref,n} = \pm \left(\frac{n}{2^{B_i}} + \frac{r}{2^{B_i+r}} \right) V_{ref}, \tag{3.6}$$

where n is an integer for which $n \in [0, n_{max}]$, where

$$n_{max} = 2^{B_i+r-1} - r - 1. \tag{3.7}$$

The same applies for a current mode design with a reference current of I_{ref} instead of V_{ref}. The number of stage output codes b_i is in turn given by

$$b_i = Q_i + 1 = 2^{B_i+r} - r. \tag{3.8}$$

In the example case of a 2-bit stage with and without redundancy, $Q_{i,2} = 3$ and $Q_{i,2.5} = 6$. The number of output codes is correspondingly $b_{i,2} = 4$ (00, 01, 10, and 11) and $b_{i,2.5} = 7$ (000, 001, 010, 011, 100, 101, and 110).

The amount of offset voltage that can be tolerated for stage i when the RSD coding is employed is in general

$$V_{os,c} = \pm \frac{r}{2^{B_i+r}} V_{ref}, \tag{3.9}$$

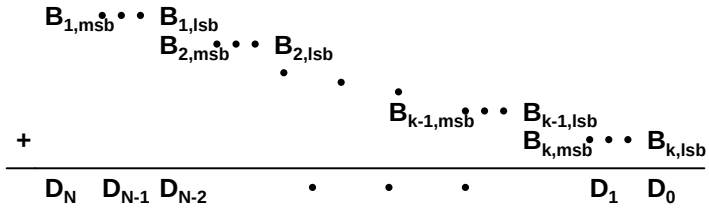

Figure 3.5 Reconstruction of RSD coded stage outputs into an N-bit output.

when $r > 0$. A similar equation holds for the current offset $I_{os,c}$ and reference current I_{ref} in a current mode design. The tolerable offset $V_{os,i}$ is equal to half of the spacing between two quantization steps $V_{ref,n}$. It is also noticeable that the accuracy of the sub-quantization is now relative to the stage resolution and independent of the total resolution of the ADC.

Reconstruction of the redundant sign digit coded digital stage outputs is performed by adding up the properly delayed stage outputs C with one-bit overlap: the MSB of stage i is added to the LSB of the previous stage $i-1$, as indicated in Fig. 3.5. The LSB of the last stage B_k is not corrected, which suggests that the last stage must be a full flash without redundancy, or the output word is cut to exclude D_0. To illustrate the effect of the RSD correction, first the operation of two serial 1-bit stages without redundancy in an ideal case and with a comparator offset in stage 1 is presented in Figs. 3.6(a) and 3.6(b), respectively. A small comparator offset voltage in stage 1 results in an erroneous combined output of 01 instead of the ideal 10. Additionally, an overflow occurs at the output of stage 1. In Figs. 3.7(a) and 3.7(b) a similar comparison for two serial 1.5-bit stages is depicted. Now, in both cases, the RSD corrected combined output gives 01, excluding the uncorrected LSB. Furthermore, no overflow of the stage 1 output occurs.

The excess in hardware caused by the RSD correction is very small. In a pipeline stage, the number of comparators of the sub-ADC is approximately doubled, but in the MDAC, only a few extra switches are required, while the total capacitance and amplifier specifications remain unchanged. However, as the comparator specifications are simultaneously relaxed significantly, the effects on area and power minimization are positive. For the reconstruction in the digital domain, only a small adder is required. Furthermore, the RSD correction makes the accuracy of the sub-ADCs independent on the total resolution of the pipeline A/D converter providing potential for power and area savings simultaneously.

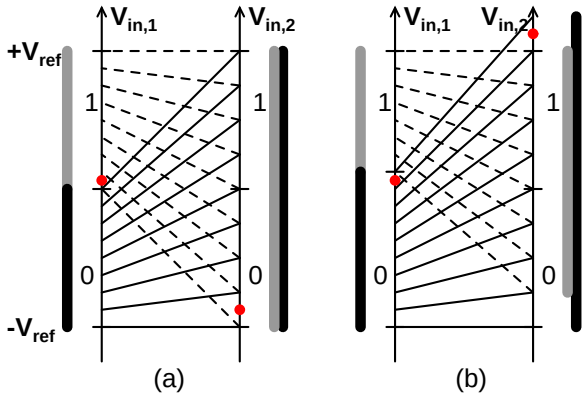

Figure 3.6 Operation of two serial 1-bit stages in (a) ideal case and (b) with comparator offset in stage 1.

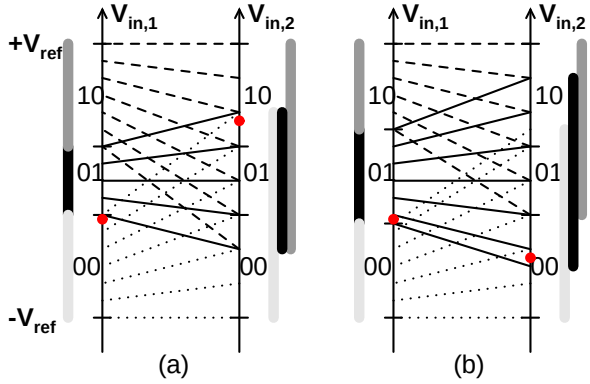

Figure 3.7 Operation of two serial 1.5-bit stages in (a) ideal case and (b) with comparator offset in stage 1.

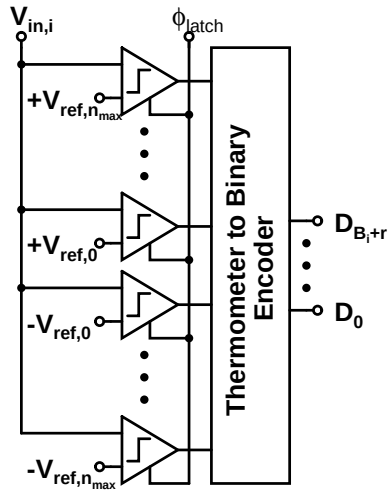

Figure 3.8 Block diagram of a $B_i + r$-bit flash A/D converter.

3.2 Sub-Analog-to-Digital Converter (sub-ADC)

The $B_i + r$-bit coarse quantization in each pipeline stage is performed with a sub-analog-to-digital converter as described earlier. Usually, the sub-ADCs sense directly the stage input and operate simultaneously with the S/H circuit in parallel, as shown Fig. 3.2. Thus, especially in the first stage, which has an uniform continuous time input signal, the timing aperture between the sampling of the S/H and signal quantization in the sub-ADC should be minimized to avoid signal-dependent conversion errors. Furthermore, to maximize the settling time of the MDAC output, i.e. to achieve a high conversion speed, the sub-ADCs should be able to provide its output to the sub-DAC as soon as possible after the S/H circuit samples the input and enters the hold mode. Therefore, almost without exception, the sub-ADCs of pipeline and algorithmic A/D converters are of parallel, flash type.

A flash A/D converter consists of parallel voltage (or current) comparators, one for each quantization step Q_i, which compare the stage input to the corresponding reference voltages $V_{ref,n}$ (or currents). In Fig. 3.8 a block diagram of a flash-type sub-ADC of a $B_i + r$-bit pipeline stage is depicted. If no redundancy is applied, the comparators at $\pm V_{ref,0}$ melt together, having a reference voltage equal to zero according to Eq. 3.4, while with 1-bit redundancy they are at separate levels. The operation of the flash ADC is straightforward; if the stage input voltage V_{in} is greater than the reference voltage $V_{ref,n}$ of a specific comparator, it gives an output corresponding to logic one, otherwise the output is at logic zero. The comparison results in a Q_i-bit thermometer code, where ideally the least significant bits are equal to one up to the point where the input signal

becomes smaller than the reference of the comparator corresponding to the code bit forcing the most significant bits to zero. Finally, the thermometer code is encoded into a binary $B_i + r$-bit output. As the sub-ADC output is also used in the D/A conversion, the thermometer code has to be encoded into a proper form for the MDAC as well.

The accuracy requirement for the sub-ADCs is determined by the resolution of the coarse A/D conversion of the stage if the RSD coding is applied: the A/D conversion accuracy specification for each stage is equal to their effective stage resolutions B_i. The performance of a low-resolution flash A/D converter is in turn limited primarily by the accuracy of the comparators and secondarily by the accuracy of the reference. Both of these can be modeled as an offset in the comparator threshold level. The largest comparator offset voltage (or current) allowed was given in Eq. 3.9 to be $\pm V_{ref}/2^{B_i}$, which is in the order of hundreds of millivolts if $B_i \leq 3$, even for a low supply voltage design.

The threshold level of a comparator is normally determined directly by the reference voltage at its input. The different reference voltage levels needed are usually implemented with a resistor string, which rely on the relative matching of the resistors. When the redundant sign digit coding is applied, the matching requirements can easily be achieved without any high-precision components. The relaxed offset voltage specifications allow the adjustment of the threshold voltage level also with a built-in adjusting circuitry in some comparator topologies.

A very popular way to implement a comparator is to have an input sensing pre-amplifier followed by a regenerative latch [9]. The offset voltage, generated by the component mismatch and process parameter variations, is reduced by the pre-amplification and can be further minimized by applying special techniques, like, for example, auto-zeroing. However, with the loose offset specifications because of the RSD coding, more robust and less power and area consuming dynamic comparators without any continuous time pre-amplification can be used in the sub-ADCs. These no DC-current dissipating comparators are discussed more detailed in chapter 4.

In addition to the quantizing comparator bank, a thermometer to binary encoder and a small decoding logic to generate the control signals of the MDAC are needed in the sub-ADCs. The former can be implemented either with logic gates in very low resolution stages or by using a read only memory (ROM) if the stage resolution is high [9]. The latter consists typically of logic gates, delay minimization of which is important, especially in high-speed pipeline ADCs.

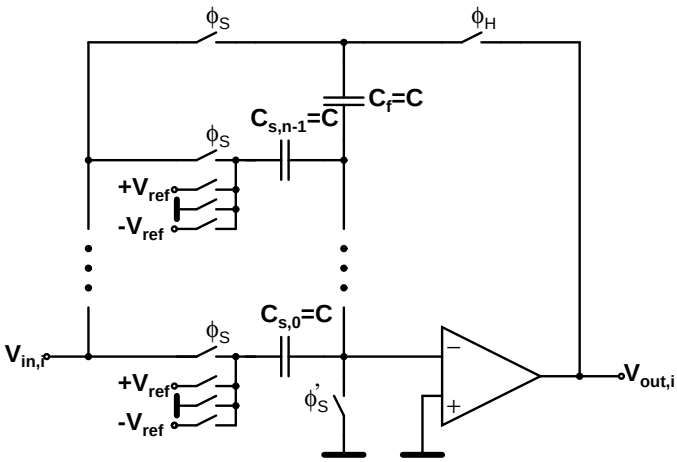

Figure 3.9 A unit capacitor switched capacitor MDAC.

3.3 Multiplying Digital-to-Analog Converter (MDAC)

The most critical block of a pipeline stage is the multiplying D/A converter (MDAC), which performs the D/A conversion of the sub-ADC output, subtraction of the resulting analog signal from the sampled and held input signal, and amplification of the residue. Traditionally, an MDAC is implemented using the switched capacitor technique, the core of the MDAC being essentially an SC integrator formed around an operational amplifier. The analysis below is based on the unit capacitor MDAC, but can be easily expanded for other MDAC topologies, discussed only briefly here.

A general unit capacitor MDAC of a $B_i + r$-bit pipeline stage is presented in Fig. 3.9 as a single-ended configuration for simplicity. It consists of 2^{B_i} unit capacitors ($C_{s,0} \ldots C_{s,n-1}$, C_f), switches that operate in the sample (ϕ_S) or hold (ϕ_H) phase, and an operational amplifier. During the sample phase ϕ_S, the bottom plates of all the unit capacitors ($C_{s,0} \ldots C_{s,n-1}$, C_f) are connected to the stage input voltage $V_{in,i}$ while the top plates of the capacitors are grounded through one switch. The so-called bottom-plate sampling can be employed by opening the common sampling switch to the ground in phase ϕ'_S, slightly before the input connecting switches in phase ϕ_S. After entering the hold phase ϕ_H, the bottom plate of the feedback capacitor C_f is connected to the operational amplifier output, while the sampling capacitors $C_{s,0} \ldots C_{s,n-1}$ are set to $-V_{ref}$, 0, or $+V_{ref}$ depending on the output of the sub-ADC. The stage output voltage $V_{out,i}$ follows Eq. 3.4, which is rewritten

$$V_{out,i} = G_i V_{in} + D_i V_{ref}, \tag{3.10}$$

where D_i is an integer corresponding to the output of the sub-ADC with $D_i \in [-(2B_i-1), +(2B_i-1)]$. For the MDAC of Fig. 3.9, the output voltage can be written based on the operation described above

$$V_{out,i} = \frac{C_f + \sum_{j=0}^{n-1} C_{s,j}}{C_f} V_{in,i} - \frac{\sum_{j=0}^{n-1} (m_j \cdot C_{s,j})}{C_f} V_{ref}, \tag{3.11}$$

where

$$n = 2^{B_i} - 1 \tag{3.12}$$

is the number of the sampling capacitors and m_j is a constant multiplier equal to -1, 0 or $+1$ depending on the output of the sub-ADC $B_i + r$. Eq. 3.11 can be rewritten using the unit capacitance C

$$V_{out,i} = \frac{C + \sum_{j=0}^{n-1} C}{C} V_{in,i} - \frac{\sum_{j=0}^{n-1} (m_j \cdot C)}{C} V_{ref}. \tag{3.13}$$

The relation between the $B_i + r$-bit word and the term m_j can be expressed as an equation between a $1 \times b_i$ vector and an $n \times b_i$ matrix, where b_i is given by Eq. 3.8 and the rows correspond to each other. For a 1-bit stage ($B_i = 1$, $r = 0$, $n = 1$) holds

$$\begin{bmatrix} B_i + r \\ 0 \\ 1 \end{bmatrix} \doteq \begin{bmatrix} m_0 \\ -1 \\ +1 \end{bmatrix}. \tag{3.14}$$

For a 1.5-bit stage ($B_i = 1$, $r = 1$, $n = 1$) the relation is given by

$$\begin{bmatrix} B_i + r \\ 00 \\ 01 \\ 10 \end{bmatrix} \doteq \begin{bmatrix} m_0 \\ -1 \\ 0 \\ +1 \end{bmatrix}. \tag{3.15}$$

The relation for a 2-bit stage ($B_i = 2$, $r = 0$, $n = 3$) is given by

$$\begin{bmatrix} B_i + r \\ 00 \\ 01 \\ 10 \\ 11 \end{bmatrix} \doteq \begin{bmatrix} m_0 & m_1 & m_2 \\ -1 & -1 & -1 \\ -1 & 0 & 0 \\ +1 & 0 & 0 \\ +1 & +1 & +1 \end{bmatrix}. \tag{3.16}$$

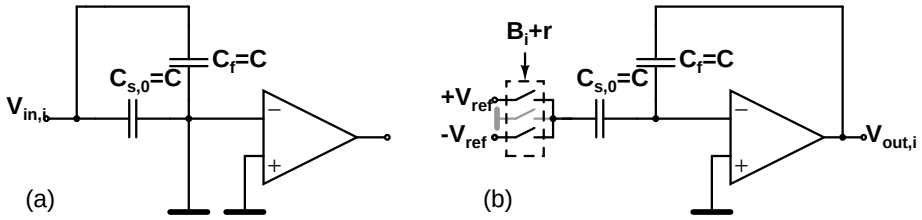

Figure 3.10 A 1-bit or 1.5-bit unit capacitor MDAC in the (a) sample and (b) hold modes.

For a 2.5-bits stage ($B_i = 2$, $r = 1$, $n = 3$) the proportionality is

$$\begin{bmatrix} B_i + r \\ 000 \\ 001 \\ 010 \\ 011 \\ 100 \\ 101 \\ 110 \end{bmatrix} \doteq \begin{bmatrix} m_0 & m_1 & m_2 \\ -1 & -1 & -1 \\ -1 & -1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \\ +1 & 0 & 0 \\ +1 & +1 & 0 \\ +1 & +1 & +1 \end{bmatrix} \tag{3.17}$$

and the equations for higher stage resolutions can be derived similarly.

The operation of the simplest multiplying D/A converter, i.e. a 1-bit or 1.5-bit stage, in the sample and hold modes is depicted in Fig. 3.10. The difference in the MDAC between these cases with ($r = 1$) and without ($r = 0$) redundancy is only one switch connecting the capacitor $C_{s,0}$ to ground, plotted in gray in the figure. It can easily be shown that the MDAC follows Eqs. 3.4–3.15.

Instead of unit capacitors, a binary weighted capacitor array can be used in a switched capacitor MDAC when $B_i \geq 2$. This is especially attractive when no redundancy is applied, which is also indicated in Eq. 3.16. In Fig. 3.11, one possible implementation of a general binary weighted capacitive MDAC is shown. Compared to the unit capacitor case, now only $n = 2^{B_i - 1}$ binary weighted sampling capacitors, the size of which varies between $2^0 C \ldots 2^{n-1} C$, are required. The transfer function of Eq. 3.11 is still valid, but, using the unit capacitance C, it can be rewritten

$$V_{out,i} = \frac{C + \sum_{j=0}^{n-1} 2^j C}{C} V_{in,i} - \frac{\sum_{j=0}^{n-1} \left(m_j \cdot 2^j C \right)}{C} V_{ref}. \tag{3.18}$$

The reduced complexity of the stage is manifested in the parameter m_j for which now

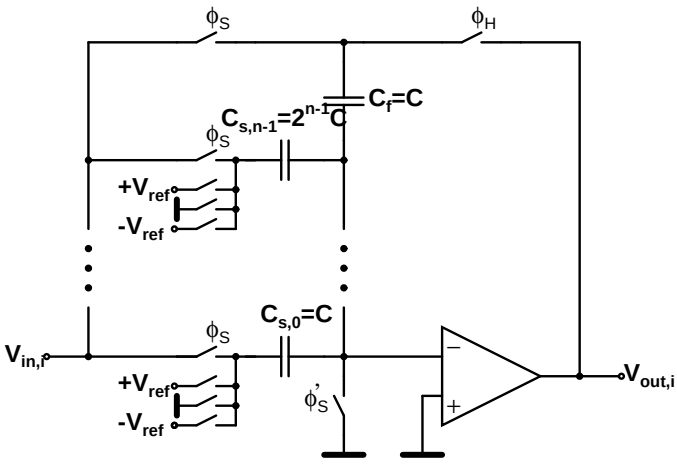

Figure 3.11 A binary weighted capacitive MDAC.

holds the relation, e.g. in the case of a 2-bit stage ($B_i = 2$, $r = 0$, $n = 2$)

$$\begin{bmatrix} B_i + r \\ 00 \\ 01 \\ 10 \\ 11 \end{bmatrix} \doteq \begin{bmatrix} m_0 & m_1 \\ -1 & -1 \\ -1 & 0 \\ +1 & 0 \\ +1 & +1 \end{bmatrix}. \tag{3.19}$$

The amount of switches is reduced by three, while for a 2.5-bit stage ($B_i = 2$, $r = 1$, $n = 2$) the relation is correspondingly

$$\begin{bmatrix} B_i + r \\ 000 \\ 001 \\ 010 \\ 011 \\ 100 \\ 101 \\ 110 \end{bmatrix} \doteq \begin{bmatrix} m_0 & m_1 \\ -1 & -1 \\ 0 & -1 \\ -1 & 0 \\ 0 & 0 \\ +1 & 0 \\ 0 & +1 \\ +1 & +1 \end{bmatrix}, \tag{3.20}$$

where the number of switches is also reduced by three compared to a unit capacitor MDAC. However, the decoding between $B_i + r$ and m_j is more complex when redundancy is employed. The total capacitance, and thus the area, is equal in both topologies. Binary weighted capacitors have been successfully employed, especially in medium-

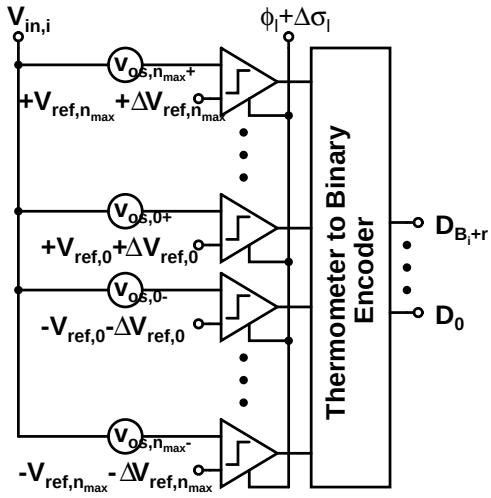

Figure 3.12 Flash A/D converter with its main error sources.

resolution MDACs [4, 10].

In addition to an SC implementation of the multiplying D/A converter, many other topologies have been proposed. These alternative topologies are not handled in detail here as they follow the same principle as the SC MDAC. A technology competing with the switched capacitor technique is the switched current (SI) technique, with which, in theory, a very high conversion rate could be achieved [7, 11]. However, the resolution is limited to below the level attained with the SC technique. In a standard CMOS process, where no high quality passives are available, a medium resolution D/A conversion can be performed by using current division in a R-2R ladder, implemented with MOS switches [12]. Also the D/A converter topology, common in high-resolution high-speed DACs based on binary weighted current sources, is used, especially in the front-end stages with fairly high resolution [13].

It is noticeable, that the S/H operation, D/A conversion, subtraction, and amplification of the residue have to fulfill an accuracy requirement equal to the resolution of the remaining pipeline stages. Thus, the resolution of a pipeline A/D converter is limited by the accuracy of the MDAC, i.e. the performance of the operational amplifier and component matching.

3.4 Nonidealities and Error Sources of Pipeline Stages

In Figs. 3.12–3.13 the most important nonidealities that deteriorate the performance of a pipeline stage are summarized. The first figure presents the factors affecting the

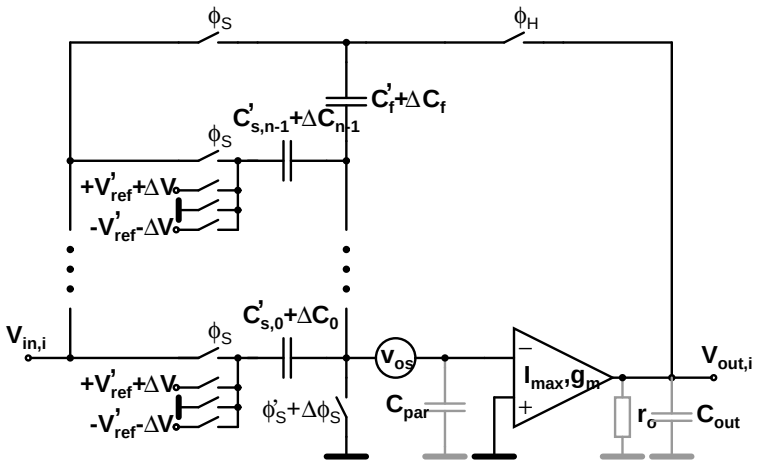

Figure 3.13 Nonidealities of a switched capacitor MDAC.

sub-ADC, i.e. comparator offset voltages $v_{os,n}$, timing error in the latching signal $\Delta\sigma_l$, deviation of the reference voltages $\Delta V_{ref,n}$. Additionally, ambitious stages may occur in the comparators, which is not shown in Fig. 3.12. The second figure summarizes the error sources in a unit capacitor MDAC, including the amplifier parasitics: finite transconductance g_m, maximal output current I_{max}, output resistance r_o, parasitic input capacitance C_{par}, and offset voltage v_{os}. Other error sources are the capacitor mismatches $\Delta C_{s,j}$ and ΔC_f, reference voltage mismatch ΔV_{ref}, timing error in the sampling clock $\Delta\phi_S$, and charge injection from the switches. In the following consideration on the effects of these nonidealities, a $B_i + r$-bit flash sub-ADC and a unit capacitor MDAC employing RSD correction are assumed. The results can naturally be extrapolated to cover other topologies as well.

3.4.1 Errors in Sub-A/D Conversion

The main error source of the sub-quantization in a pipeline stage is the offset voltage of the comparators. An offset voltage shifts the decision level of the comparator introducing a quantization error to the $B_i + r$-bit output of the stage. The effect of the threshold level shifting on the transfer function of a 1.5-bit stage is presented in Fig. 3.14, where the non-zero comparator offset voltages are assumed to be the only nonidealities present. The comparator offset voltage is originated from several sources. The main component is inherited from the device mismatch, the combined effect of which can be reduced into the comparator input. Deviation in the reference voltage levels $\Delta V_{ref,n}$ can also be included in the input referred offset voltage. If no redundancy is exploited, the

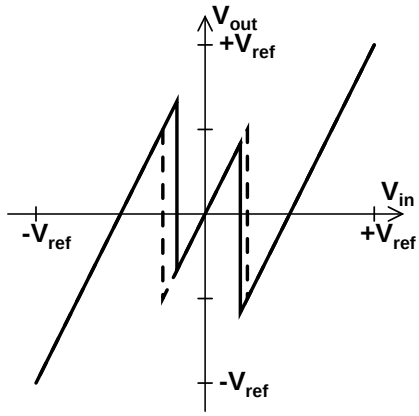

Figure 3.14 Effect of the comparator offset on the transfer function of a 1.5-bit stage.

error in the output voltage of each stage must be less than half of the LSB referred to the resolution of the remaining back-end pipeline ADC. The maximal error allowed in the output of the m^{th} stage is given by

$$\Delta V_{out,m} = \frac{1}{2} \cdot \frac{1}{2^{N-\sum_{i=1}^{m-1} B_i}} \cdot V_{FS}, \tag{3.21}$$

where $V_{FS} = 2V_{ref}$ is the full-scale output voltage. Referred to the stage input, the maximal allowed comparator input referred offset is given by

$$V_{os,c,m} = \frac{V_{ref}}{2^{N+B_m-\sum_{i=0}^{m-1} B_i}}. \tag{3.22}$$

When the RSD correction with one-bit redundancy is employed, the comparator offset requirement is given by Eq. 3.9, the value of which is much larger than that of Eq. 3.22 and furthermore, independent of the order of the stage.

Any time variation $\Delta\phi_l$ in the latching signal introduces a signal-dependent error, especially in the first pipeline stage where the input is time continuous. The time variation consists of a systematic part Δt_{ls} and a random part σ_a. Systematic error is inherited from the time deviation between the latching signal and sample clock of the MDAC. Latching and sampling cannot be simultaneous to avoid coupling of the comparator kickback noise to the sampled signal. Random error is caused by the clock jitter, which makes the edge of the latching signal to vary randomly. The error between the input voltage of the comparators and the sampled value owing to the time deviation between

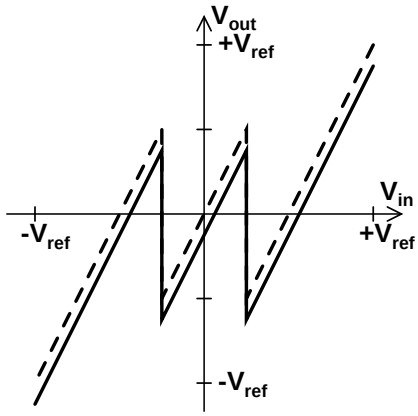

Figure 3.15 Effect of the amplifier offset on the transfer function of a 1.5-bit stage.

latching and sampling is given by

$$\Delta V_{in,i} = \frac{d}{dt} V_{in,i}(t) \cdot \Delta\phi_l, \tag{3.23}$$

where $\Delta\phi_l$ is the timing error. The deviation in the input voltage $\Delta V_{in,i}$ is converted into an equal shift of all the comparator threshold levels in the stage transfer function. However, the shift is signal-dependent and has a random term as well. Usually this is not a problem in the back-end stages in which the input signal varies very slowly, being almost constant at the latching and sampling moments. In the first pipeline stage, the problem can be solved by using a front-end sample-and-hold circuit, which provides a constant held input for the pipeline ADC.

3.4.2 Operational Amplifier Performance

The performance of the operational amplifier in the MDAC is one of the most critical nonidealities affecting both the static and dynamic linearity of the stage, and thus of the whole ADC. The amplifier output of an MDAC must settle to the accuracy of the remaining pipeline A/D converter within half of a clock cycle. The essential nonidealities related to the operational amplifier are its offset, limited gain bandwidth, slew rate, and finite open loop DC-gain.

3.4.2.1 Offset

The effect of the amplifier offset voltage in a unit capacitor MDAC can be obtained using the schematic of Fig. 3.13, in which a voltage source v_{os} is placed in series with

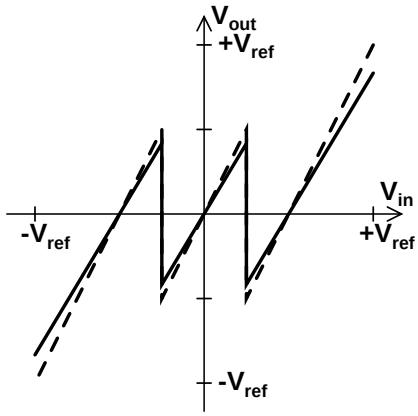

Figure 3.16 Effect of the finite amplifier DC-gain on the transfer function of a 1.5-bit stage.

the inverting amplifier input. As the offset is superimposed to the input signal, the capacitors $C_{s,j}$ and C_f can be considered to be connected to the signal ground during the sample phase ϕ_S. Since both plates of the capacitors are grounded, no charge is stored in them. In the hold mode ϕ_H the sampling switch is opened and the amplifier offset voltage v_{os} appears across the sampling capacitors $C_{s,j}$, while the top plate of the feedback capacitor is at v_{os} and the bottom plate at the output voltage level. Based on the charge preservation, the effect of the amplifier offset voltage at the output $V_{os,i}$ can be obtained to be

$$V_{os,i} = \frac{C_f + \sum_{j=0}^{n-1} C_{s,j}}{C_f} v_{os}. \tag{3.24}$$

The amplifier offset at the stage output can be calculated similarly for other MDAC topologies as well. In conclusion, the operational amplifier offset voltage introduces a constant error of $V_{os,i}$, which is directly translated to an equal, constant shift of the output voltage $V_{out,i}$ as depicted for a negative offset of a 1.5-bit stage in Fig. 3.15. The shift can cause the stage output to overflow and saturate the remaining pipeline stages. The effect of this offset voltage can be minimized by using well known circuit techniques like auto-zeroing, i.e. connecting the amplifier in unity gain feedback during the sample phase, or measuring and compensating the offset analogically or digitally.

In addition to the operational amplifier, other offset voltage sources can be identified in a multiplying D/A converter. Main contributions to these second-order sources originate from the clock feedthrough and charge injection of the switches. Their effect on the stage transfer function is identical to the operational amplifier offset.

3.4.2.2 Finite Open Loop DC-gain

Static errors result from the finite open loop DC-gain A_0, which is given in this case by $A_0 = g_m r_o$, and from the parasitic input capacitance C_{par}, which changes the feedback factor. For the general unit capacitor MDAC of Fig. 3.13, omitting all nonidealities other than the finite open loop DC-gain A_0, it can be written based on the charge preservation in the sample and hold mode

$$V_{in,i}\left(C_f + \sum_{j=0}^{n-1} C_{s,j}\right) =$$

$$V_{out,i}\left(\left(1+\frac{1}{A_0}\right)\cdot C_f + \frac{\sum_{j=0}^{n-1} C_{s,j}}{A_0} + \frac{C_{par}}{A_0}\right) + V_{ref}\left(\sum_{j=0}^{n-1} m_j \cdot C_{s,j}\right). \tag{3.25}$$

Solving for $V_{out,i}$ yields

$$V_{out,i} = \left(\frac{C_f + \sum_{j=0}^{n-1} C_{s,j}}{C_f} V_{in,i} - \frac{\sum_{j=0}^{n-1} m_j \cdot C_{s,j}}{C_f} V_{ref}\right) \cdot \frac{1}{1+\frac{1}{A_o \cdot f}}, \tag{3.26}$$

where the parameter f is called the feedback factor and is given by

$$f = \frac{C_f}{C_f + \sum_{j=0}^{n-1} C_{s,j} + C_{par}}. \tag{3.27}$$

The effect of the amplifier parasitic input capacitance on the feedback factor is also manifested in Eq. 3.27. By comparing Eq. 3.26 to the ideal transfer function of Eq. 3.11 it can be observed that the error introduced by the amplifier finite open loop DC-gain is given by the last term in Eq. 3.26, for which, when $1/A_0 \cdot f \gg 1$, it approximately holds

$$\frac{1}{1+\frac{1}{A_0 \cdot f}} \approx 1 - \frac{1}{A_0 \cdot f}. \tag{3.28}$$

Thus, the amplifier finite DC-gain decreases the gain and steps at the comparator thresholds in the transfer function by an error term ε_{A_0} of

$$\varepsilon_{A_0} = \frac{1}{A_0 \cdot f}. \tag{3.29}$$

The effect of the resulting signal-independent gain error introduced to the transfer function of a 1.5-bit stage is depicted exaggeratedly by the solid line in Fig. 3.16. The effect of this gain error should be decreased below the quantization noise level, which is further analyzed in section 3.5.

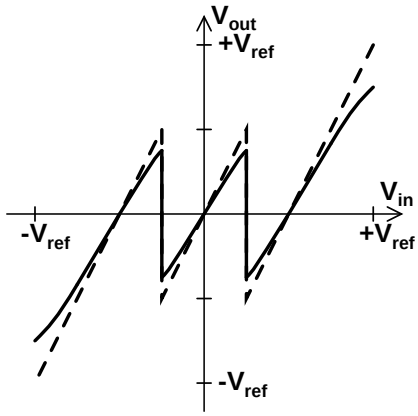

Figure 3.17 Effect of the amplifier GBW on the transfer function of a 1.5-bit stage.

3.4.2.3 Slew Rate and Gain Bandwidth

A more severe dynamic error in the stage transfer function is caused by the incomplete settling of the amplifier output because of the finite slew rate (SR) and gain bandwidth (GBW) of the operational amplifier. At the beginning of the hold mode, the operational amplifier enters slewing, providing its maximal output current I_{max}, after which it settles exponentially towards the ideal stage output voltage, the settling now being limited by the amplifier transconductance g_m and the effective load capacitance in this mode $C_{L,H}$. For the slew rate limited part of the settling, it is a good practice to reserve one third of the total settling time of $T/2$, where T is the sample clock period, relating to the sample frequency by $f_S = 1/T$. The load capacitance, which has to be charged or discharged during the settling, depends on the capacitor charging in the previous sample phase. In the worst case, the total load capacitance during the slewing is $C_{L,tot} + C_f$, resulting

$$SR = \frac{I_{max}}{C_{L,tot} + C_f}, \tag{3.30}$$

where $C_{L,tot} = C_L + C_{out}$ is the total load capacitance including the parasitic capacitance at the amplifier output C_{out}. The stage output voltage is linearly dependent on the slew rate and at the end of this phase given by

$$V_{out,i}\left(\frac{T}{6}\right) = \frac{SR}{6 f_S}. \tag{3.31}$$

During the exponential settling, the stage output approaches the ideal output $V'_{out,i}$ according to the equation

$$V_{out,i}(t) = \left(1 - e^{-\omega_{-3dB}t}\right) \cdot V'_{out,i}, \tag{3.32}$$

where the -3dB corner frequency is given by

$$\omega_{-3dB} = \omega_u \cdot f = \frac{g_m}{C_{L,H}} \cdot f. \tag{3.33}$$

The effective hold mode load capacitance $C_{L,H}$ of the MDAC in Fig. 3.13 with a load capacitance C_L is given by

$$C_{L,H} = C_L + C_{out} + \frac{C_f \left(\sum_{j=0}^{n-1} C_{s,j} + C_{par}\right)}{C_f + \sum_{j=0}^{n-1} C_{s,j} + C_{par}}. \tag{3.34}$$

From Eqs. 3.33–3.34, the -3dB corner frequency is

$$\omega_{-3dB} = \frac{g_m}{\frac{C_{L,tot}}{f} + \sum_{j=0}^{n-1} C_{s,j} + C_{par}}. \tag{3.35}$$

As the slewing took one third of the settling time, the remaining time for the exponential settling is $t = T/3 = 1/3 f_S$. Substituting Eq. 3.35 into Eq. 3.32 the settling error of the stage output voltage at the end of the hold phase ε_τ can be derived to be

$$\varepsilon_\tau = e^{-\frac{g_m}{\frac{C_{L,tot}}{f} + \sum_{j=0}^{n-1} C_{s,j} + C_{par}} \cdot \frac{1}{3 f_S}}. \tag{3.36}$$

The settling error ε_τ, being time dependent, creates signal-dependent errors, which in turn leads to harmonic distortion. Signal-dependent errors are very difficult to cancel or calibrate, which makes the consideration of the amplifier settling behavior very important. Specifying the GBW of the operational amplifier is discussed in section 3.5. The effect of the finite GBW of the amplifier on the transfer function of a 1.5-bit stage is depicted in Fig. 3.17. The error is proportional to the output voltage being larger for stage outputs close to the full scale, which is not the case in the error originated from the amplifier finite gain depicted in Fig. 3.16.

The gain ε_{A_0} and settling ε_τ errors can be considered as non-correlating, as can the amplifier offset voltage $V_{os,i}$; their superimposed effect on the stage transfer function can be written as

$$V_{out,i} = (1 - \varepsilon_{A_0}) \cdot (1 - \varepsilon_\tau) \cdot \left(V'_{out,i} + V_{os,i}\right), \tag{3.37}$$

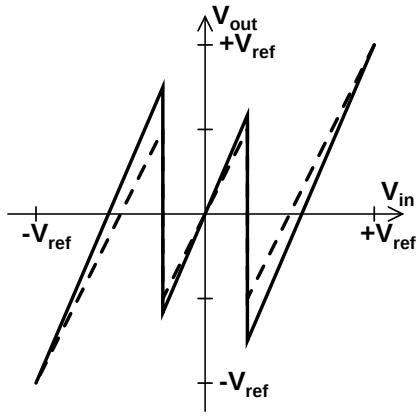

Figure 3.18 Effect of the capacitor mismatch on the transfer function of a 1.5-bit stage.

where $V'_{out,i}$ is the stage output excluding the errors caused by the limited performance of the operational amplifier.

3.4.3 Capacitor Mismatch

In switched capacitor MDACs, mismatch of the sampling $C_{s,j}$ and feedback C_f capacitors is a major error source. Each of the capacitors can be modeled to consist of an ideal part $C'_{s,j}$ and C_f plus a mismatch $\Delta C_{s,j}$ and ΔC_f, respectively, corresponding to the noting in Fig. 3.13. Including the capacitor mismatch in the transfer function of a switched capacitor MDAC in Eq. 3.11 results in

$$V_{out,i} = \frac{C'_f + \Delta C_f + \sum_{j=0}^{n-1}\left(C'_{s,j} + \Delta C_{s,j}\right)}{C'_f + \Delta C_f} V_{in,i} - \frac{\sum_{j=0}^{n-1}\left(m_j \cdot \left(C'_{s,j} + \Delta C_{s,j}\right)\right)}{C'_f + \Delta C_f} V_{ref}. \tag{3.38}$$

The multiplier of the input $V_{in,i}$ represents a gain error, while the multiplier in the second term introduces an error in the height of the voltage steps at the comparator threshold levels. For a unit capacitor MDAC, by exploiting the property $C'_{s,j} = C'_f = C$, Eq. 3.38 can be rewritten as

$$\begin{aligned} V_{out,i} &= \left(1 + \sum_{j=0}^{n-1}(1+\alpha_j)\right) \cdot V_{in,i} - \sum_{j=0}^{n-1}(m_j \cdot (1+\alpha_j)) \cdot V_{ref} \\ &= (n+\alpha) \cdot V_{in,i} - \sum_{j=0}^{n-1}(m_j \cdot (1+\alpha_j)) \cdot V_{ref}, \end{aligned} \tag{3.39}$$

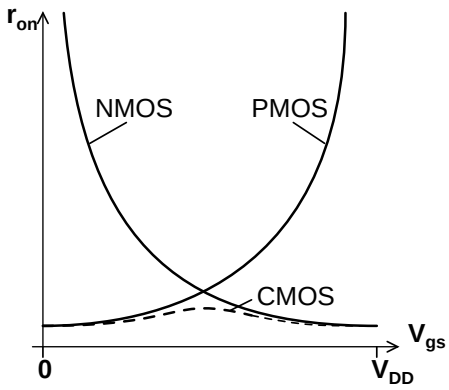

Figure 3.19 On-resistances of different MOS switches.

where for the unit capacitor mismatches α_j hold

$$1+\alpha_j = \frac{C+\Delta C_{s,j}}{C+\Delta C_f} = \frac{1+\frac{\Delta C_{s,j}}{C}}{1+\frac{\Delta C_f}{C}} \tag{3.40}$$

and the total mismatch α is

$$\alpha = \sum_{j=0}^{n-1} \alpha_j. \tag{3.41}$$

For an MDAC with a binary weighted capacitor array, a similar equation can be derived from the general expression of Eq. 3.38. The effect of the capacitor mismatch on the stage transfer function is depicted in Fig. 3.18 for a 1.5-bit stage. It is noticed that when $V_{in,i} = \pm V_{ref}$, no error results. The gain error and deviation of the voltage steps at the comparator threshold levels are clearly visible from the figure.

3.4.4 MOS Switches

In switched capacitor circuits, almost without exception, MOS switches are used. The nonidealities and error sources attached to them deserve careful consideration when designing SC MDACs. The major topics being the bandwidth limitation inherited from the non-zero and non-linear on-resistance of the switch, clock feedthrough, and injection of the signal-dependent channel charge of the MOS transistor. In references [14, 9, 15], the errors attached to MOS switches are thoroughly handled, only a brief review of which is given here to get a complete picture.

During the sample phase, the switch with an on-resistance r_{on} forms an RC circuit, the time constant of which defines the maximum signal bandwidth. A commonly used design rule for the time constant is that it should be at least five times larger than the

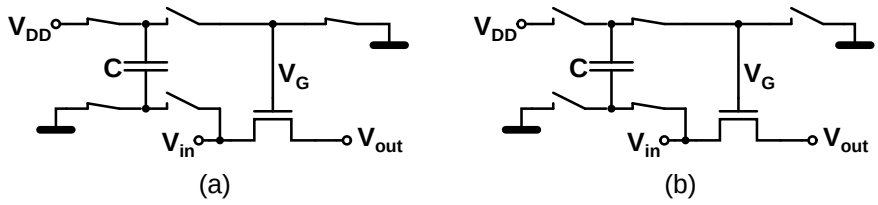

Figure 3.20 Principle of bootstrapping (a) switch open and (b) closed.

settling time. However, the on-resistance r_{on} of an NMOS or PMOS switch is strongly dependent on the gate-source voltage V_{gs} of the transistor

$$r_{on} = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_T)}, \tag{3.42}$$

where μ is the mobility, W and L are the width and length of the MOS transistor, respectively, C_{ox} is the gate oxide capacitance, and V_T the threshold voltage. This is visualized in Fig. 3.19, where the on-resistances of an NMOS, PMOS, and CMOS switch are plotted as a function of the gate-source voltage. This non-linearity of the switch on-resistance generates distortion, which limits the allowable input signal swing. A CMOS switch consisting of parallel NMOS and PMOS transistors achieves a much higher linearity than the NMOS or PMOS alone. Nevertheless, it is still too high when aiming for high resolution ADCs.

From the discussion above, it is evident that the linearity of MOS switch can be significantly improved if its gate-source voltage can be kept constant. This can be accomplished by using so called bootstrapping technique, depicted in Fig. 3.20 [15,16]. Operation of the bootstrapped switch is as follows. When the switch is open, a capacitor C is precharged to V_{DD} and the switch transistor gate is short-circuited to ground, as shown in Fig. 3.20(a). When the switch is closed in Fig. 3.20(b), the transistor gate is disconnected from ground and the capacitor C is connected between the gate and source giving signal independently a gate over-drive of V_{DD}. As V_{gs} never exceeds the supply voltage, reliability and brake-down voltage rules of the process are not violated.

During the sample phase, when the switch is closed and the drain-source voltage V_{ds} is almost zero, a charge Q_{ch} is formed in the channel of the transistor

$$Q_{ch} = -WLC_{ox}(V_{gs} - V_T). \tag{3.43}$$

After the switch is opened by driving V_{gs} below V_T, the charge stored in the channel is distributed to the drain and source with a ratio depending on the impedance of these nodes and on the fall time of the driving gate signal. The injected charge being signal-

dependent through V_{gs}, the resulting error in the capacitor charging generates distortion. A common way to cope with the problem is to use bottom-plate sampling, which makes the charge injection constant [14]. With NMOS switches, a half size dummy NMOS switch, with its drain and source short-circuited and clocked in the inverse phase, can be used to cancel the effect of the charge injection. Similarly, in a CMOS switch with equally sized NMOS and PMOS transistors having the same V_{gs} and clocked exactly simultaneously, the charge injection of the complementary transistors cancel each other. However, in reality, these constraints are never fulfilled and the cancellation is incomplete. In a bootstrapped switch, described above, the charge injection is always signal-independent since the gate-source voltage is kept constant.

Through the parasitic gate capacitances of a MOS switch the clock signal is connected to the signal propagating in the channel between the source and drain. Thus, the fast voltage gradients at the rising and falling clock edges cause an error in the charge sampled in a capacitor. The quantity of this clock feedthrough error is proportional to the relation of the coupling and sampling capacitors and to the gradients of the clock signal. Clock feedthrough can be eliminated or minimized with the same circuit techniques as minimizing the charge injection and by using small switch transistors, which have small parasitic gate capacitances. In fully balanced differential structures, the error from the clock feedthrough affects only the common mode voltage level, the effect of which is attenuated by the common mode rejection ratio (CMRR).

3.4.5 Thermal Noise

In addition to the deterministic errors limiting the performance of a pipeline A/D converter, there are random errors originated from noise of the circuit elements and clock signals. In switched capacitor pipeline ADCs, the dominating thermal noise components are the noise of the operational amplifiers and sampling circuit, latter of which being the dominating source in medium- and low-resolution applications. The noise of the sampling circuit is called kT/C-noise since the thermal noise of the sampling switch is stored to the sampling capacitor resulting in a noise power of

$$e^2_{kT/C,i} = \frac{kT}{C_f + \sum_{j=0}^{n-1} C_{s,j}}, \tag{3.44}$$

where k is the Boltzmann's constant, T absolute temperature, and the total sampling capacitance consists of the feedback capacitor C_f and $n-1$ sampling capacitors $C_{s,j}$. This holds for, for example, the MDACs of Figs. 3.9 and 3.11. Considering the kT/C-noise as the only noise source, the signal-to-noise ratio of one stage for a sinusoidal

signal with a full-scale amplitude of $V_{FS}/2$ is given by

$$SNR_{kT/C,i} = \frac{V_{FS}^2\left(C_f + \Sigma_{j=0}^{n-1} C_{s,j}\right)}{8kT}. \tag{3.45}$$

Especially in high-resolution pipeline A/D converters, the total kT/C-noise contribution of all the MDACs of a pipeline ADC determine the minimum size of the capacitors and full-scale voltage which does not degrade the SNR below the quantization noise level. This is further analyzed in section 3.5.

The noise of the operational amplifiers of the SC MDACs must also be taken into account in the design. The thermal noise of an amplifier is dependent on the circuit topology and can be considered separately superimposed on the kT/C-noise.

3.4.6 Sampling Clock Jitter

The most critical clocking signal in the MDAC is the sampling clock, the falling edge of which determines the sampling moment. Random variations of the falling edge, referred as clock jitter or aperture uncertainty σ_a, are unavoidable. Because of its random nature, the sampling clock jitter does not introduce any fixed pattern tones in the output spectrum but degrades the signal-to-noise ratio. For an input sinusoid of amplitude $V_{FS}/2$ and frequency of f_{in}, a sampling jitter with a standard deviation σ_a is derived in appendix A and results in an rms voltage error of

$$v_{rms,a} = V_{FS}\pi f_{in}\sigma_a, \tag{3.46}$$

which corresponds to an output noise power of

$$e_{\sigma_a}^2 = \frac{v_{rms}^2}{2} = \frac{\pi^2}{2} V_{FS}^2 f_{in}^2 \sigma_a^2, \tag{3.47}$$

which adds to the quantization noise and degrades the SNR.

In the back-end pipeline stages, which have an almost constant exponentially settling output of the previous stage as their input, the sampling clock jitter is of much less importance than in the first stage. The time varying output of a pipeline stage is given by Eqs. 3.32–3.35, the derivative of which for stage $i-1$ is given by

$$\frac{d}{dt}V_{out,i-1}(t) = -\frac{g_m}{\frac{C_{L,tot}}{f} + \Sigma_{j=0}^{n-1} C_{s,j} + C_{par}} \cdot e^{-\frac{g_m}{\frac{C_{L,tot}}{f} + \Sigma_{j=0}^{n-1} C_{s,j} + C_{par}} \cdot t} \cdot V'_{out,i-1}. \tag{3.48}$$

Rms voltage error at the sampling moment of stage i, which is at the end of the hold

phase of stage $i-1$, i.e. $t = \frac{1}{3f_S}$, can be obtained similarly as above to be

$$v_{rms,a} = \frac{d}{dt} V_{out,i-1}\left(\frac{1}{3f_S}\right) \cdot \sigma_a. \tag{3.49}$$

The corresponding noise power being

$$e^2_{\sigma_a} = \frac{1}{2}\left(\frac{g_m \sigma_a}{\frac{C_{L,tot}}{f} + \sum_{j=0}^{n-1} C_{s,j} + C_{par}}\right)^2 \cdot e^{-\frac{2g_m}{\frac{C_{L,tot}}{f} + \sum_{j=0}^{n-1} C_{s,j} + C_{par}} \cdot \frac{1}{3f_S}}. \tag{3.50}$$

The noise contribution of Eq. 3.50 is usually much below that of Eq. 3.47.

3.5 Design Constraints of Pipeline A/D Converters

In this section, the dependency of the thermal noise is presented, as well as the amplifier open loop DC-gain, bandwidth and slew rate on the speed and resolution requirements of the whole ADC.

3.5.1 Capacitor Sizing and Scaling

An extensive analysis of the capacitor sizing in pipelined A/D converters, based on the power dissipation and the thermal noise, is given in [17]. A short overview only is given here to give a complete picture of the constraints limiting the design of a pipeline ADC. The dominant noise source of a switched capacitor based MDAC is the thermal noise inherited from the sampling operation—so-called kT/C-noise. In principle, it sets the lower limit for the capacitor sizes used in the stages of a pipeline A/D converter. However, up to a resolution of 10 bits, the capacitor size is typically determined by the matching properties of the process. In addition to the thermal noise of the sampling switch, the noise of the operational amplifier must be included in the calculations. In medium-resolution pipeline ADCs, the noise of the opamp is usually well below the kT/C-noise, while, when aiming for higher total resolution, its contribution to the noise budget becomes significant. The total noise power of a pipeline A/D converter with k stages, reduced to its input, is given by

$$e^2_{tot} = e^2_1 + \frac{e^2_2}{G_1} + \ldots + \frac{e^2_k}{\prod_{i=1}^{k-1} G_i}, \tag{3.51}$$

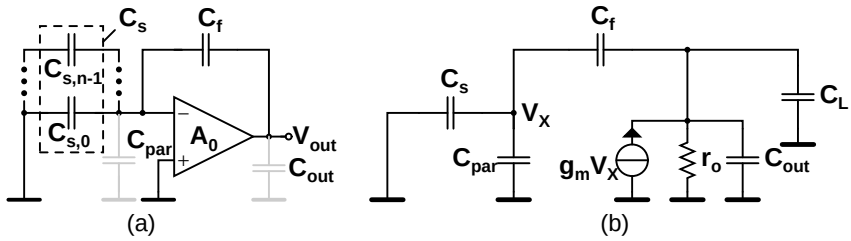

Figure 3.21 A single-ended MDAC (a) in the hold mode and (b) the corresponding small-signal model.

where e_i^2 is the noise power at the stage input, and G_i the interstage gain of the i^{th} stage. As the noise contribution of the subsequent stages is attenuated by the interstage gains of the proceeding stages, the capacitor size of the back-end stages can be scaled down to attain power savings through relaxed opamp specifications. It has been shown that in medium-resolution pipeline ADCs, a minimal stage resolution combined with capacitor scaling with a factor of one half until the matching limit leads to a power dissipation minimum [18]. In high-resolution ADCs, on the contrary, it is favorable to place a high-resolution stage utilizing a large interstage gain in the front to attenuate the noise contribution of the back-end stages [19].

3.5.2 Open Loop DC-Gain of the Amplifier

As discussed in the previous section, the DC-gain of the amplifier in a MDAC is determined by the resolution, and the slew rate and GBW specifications can be derived from the sampling speed of the A/D converter. The analysis below applies for the one stage operational transconductance amplifiers (OTAs) and for amplifiers with two or three stages having a folded or telescope cascode first stage when the slew rate (SR) is limited by charging and discharging the compensation capacitor C_c between the first and second stage.

The MDAC topology used in the calculations below, including the amplifier input parasitic capacitances C_{par} and C_{out}, is shown in the hold mode in Fig. 3.21(a) as a single-ended configuration for simplicity. However, all the calculations are performed for a fully differential topology. The input signal is sampled to the sampling capacitors $C_s = \sum_{j=0}^{n} C_{s,j}$ and feedback capacitor C_f. The small-signal model of the MDAC configuration is shown in Fig. 3.21(b). The analysis can easily be expanded to other topologies as well.

The open loop DC-gain of the amplifier can be determined from the tolerable gain error at the output of each pipeline stage. The total error ε_{tot} in the input of an N-bit

converter should be less than LSB/2, which corresponds to the condition: $\varepsilon_{tot} < 1/2^{N+1}$. The errors $\varepsilon_{A_0,i}$, resulted from the finite DC-gains of the amplifiers $A_{0,i}$, are assumed to be correlated in the $m = k-1$ pipeline stages with resolutions of $B_i + r$ bits. In appendix B, the inequality for the dimensioning of the operational amplifier open loop DC-gains, is derived to be in the general case

$$\sum_{i=1}^{m} \frac{2^{B_i}}{A_{0,i} \cdot \prod_{l=1}^{i} 2^{B_l}} < \frac{1}{2^{N+1}}. \tag{3.52}$$

There are two interesting special cases simplifying the condition given by Eq. 3.52. First, a pipeline ADC consisting of stages employing two different stage resolutions: a front-end stages with an effective resolution of B_a bits and $b = m - a$ back-end stages with B_b effective bits with amplifier DC-gains of $A_{0,a}$ and $A_{0,b}$, respectively. Under the conditions $a \cdot B_a$, $(m-a) \cdot B_b \gg 1$, the inequality for an input referred error less than LSB/2 is now

$$\frac{2^{B_a}}{A_{0,a}\,(2^{B_a}-1)} + \frac{2^{B_b - aB_a}}{A_{0,b}\,(2^{B_b}-1)} < \frac{1}{2^{N+1}}. \tag{3.53}$$

If identical amplifiers are used, i.e. $A_{0,a} = A_{0,b}$, Eq. 3.53 has a single solution. In the case of $A_{0,a} \neq A_{0,b}$, Eq. 3.53 can be iteratively used to dimension the open loop DC-gains of the front-end and back-end stages.

The second special case applies for the case of identical stages with an effective resolution of $B_i = B$ and amplifier open loop DC-gain of $A_{0,i} = A_0$. If the number of stages m is large, Eq. 3.52 can be rewritten to result in

$$A_0 > \frac{2^{N+B+1}}{2^B - 1}. \tag{3.54}$$

From Eq. 3.54 it can be directly seen that for $B = 1$ the minimum DC-gain is 2^{N+2} and as B increases A_0 approaches 2^{N+1}. In the logarithmic scale this difference corresponds to 3 dB, which is negligible for high-resolution ADCs. Furthermore, the DC-gain requirement of the amplifier can typically be affected only a little by the device size and bias current but affects the choice of the amplifier topology.

3.5.3 Settling of the Amplifier

The sampling speed of a pipeline A/D converter is in turn dictated by the settling time of the amplifier in the MDAC. The successive pipeline stages operate in opposite clock phases indicating a settling time of a half of the clock cycle ($T/2$). The settling time is determined first by the slew rate (SR) and finally by the gain bandwidth (GBW) of the amplifier, as clarified in section 3.4. It is a good practice to reserve one third of the

settling time for the slewing and the rest for the GBW limited part.

The error ε_τ, resulted from the incomplete exponential settling during $T/3 = 1/(3f_S)$, was derived in Eq. 3.36. In order to fulfill the resolution requirement, the settling error of the stage i must be within half of the LSB of the remaining pipeline ADC. This, according to appendix B, results in the amplifier transconductance g_m, being in condition

$$g_m > 3\ln 2 \cdot 2^{B_i} \cdot (N_i + 1) \cdot f_S \cdot kC_{L,tot}, \tag{3.55}$$

where N_i is the resolution of the remaining back-end pipeline including the i^{th} stage, $C_{L,tot} = C_L + C_{out}$ the total load capacitance, and the constant $k > 1$ the ratio between the effective load capacitance during the hold mode $C_{L,H}$ and in open loop $C_{L,tot}$, resulting in

$$k = \frac{C_{L,H}}{C_{L,tot}} = 1 + \frac{C_f \left(\sum_{j=0}^{n-1} C_{s,j} + C_{par}\right)}{(C_L + C_{out}) \cdot \left(C_f + \sum_{j=0}^{n-1} C_{s,j} + C_{par}\right)}. \tag{3.56}$$

Using simple transistor current equations, the minimum drain current of one transistor of the amplifier input differential pair I_D has the proportionality

$$I_D \cdot \frac{W}{L} > \frac{9\ln^2 2}{2\mu C_{ox}} \cdot (f_S (N_i + 1))^2 \cdot \left(2^{B_i} C_{L,tot} + \sum_{j=0}^{n-1} C_{s,j} + C_{par}\right)^2, \tag{3.57}$$

where the mobility μ and the gate oxide capacitance C_{ox} are process-dependent parameters and cannot be affected. It can be directly noticed that to minimize the amplifier current consumption, the stage resolution B_i should be as low as possible. Furthermore, the current I_D is proportional to the square of the resolution N_i and sample rate f_S. By making the input differential pair W/L ratio large, a smaller current I_D fulfills the inequality. Nevertheless, simultaneously C_{par} is increased, which has an opposite effect.

Eq. 3.57 can be expressed in terms of the minimal gain bandwidth

$$GBW > \frac{3\ln 2}{2\pi} \cdot f_S (N_i + 1) \cdot \left(2^{B_i} + \frac{\sum_{j=0}^{n-1} C_{s,j} + C_{par}}{C_{L,tot}}\right), \tag{3.58}$$

which can be used to specify the operational amplifier performance.

An interesting special case occurs when all the stages are identical, similarly to the second special case when dimensioning the open loop DC-gain. As derived in appendix B, Eqs. 3.55 and 3.57 reduce to

$$g_m > 3\left((N+1)\cdot\ln 2 - \ln\left(2^B - 1\right)\right) \cdot 2^B \cdot f_S \cdot kC_{L,tot} \tag{3.59}$$

and

$$I_D \cdot \frac{W}{L} > \frac{9}{2\mu C_{ox}} \left((N+1)\cdot \ln 2 - \ln\left(2^B - 1\right)\right)^2 \cdot f_S^2 \cdot \left(2^B C_{L,tot} + \sum_{j=0}^{n-1} C_{s,j} + C_{par}\right)^2, \tag{3.60}$$

respectively. It is noticeable that the interstage gain reduces the effect of the stage resolution B on the current consumption, which is not included in Eq. 3.57.

For a one-stage OTA, like a folded cascode amplifier, the slew rate is linearly dependent on I_D, the drain current of one transistor in the input pair. To assure symmetrical slewing of the output, the currents of the output stages have to be equal to the current of the input stage. In a pipeline stage, the load capacitance, which has to be charged or discharged, depends on the capacitor charging in the previous operation phase. In the worst case, the total load capacitance during the slewing is $C_{L,tot} + C_f$. Using the symbols of Fig. 3.21(b) the slew rate is given in this case by

$$SR = \frac{2I_D}{C_{L,tot} + C_f}. \tag{3.61}$$

The minimum drain current set by the slew rate is derived in appendix B to give

$$I_D > 3 \cdot f_S \cdot V_{FS,diff} \left(C_{L,tot} + C_f\right), \tag{3.62}$$

where a worst-case differential full-scale slewing of $V_{FS,diff}$ is assumed. From Eq. 3.62 it can be seen that the minimum drain current dictated by the slew rate limited part of the settling is linearly dependent on the conversion rate f_S, but independent on the ADC resolution N. Also, as a first order approximation, it is not dependent on the process parameters.

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Chapter 4

Circuit Techniques for Pipeline Analog-to-Digital Converters

A pipeline stage consists essentially of a sub-analog-to-digital converter (sub-ADC) and a multiplying digital-to-analog converter (MDAC). The performance of a sub-ADC is determined by the properties of the quantization process performing comparators, which are usually implemented using dynamic topologies. The performance of a pipeline A/D converter as a whole is limited by the MDACs, implemented in most cases as switched capacitor (SC) circuits including an operational amplifier (opamp). In this chapter, alternative topologies for the essential circuit building blocks of pipeline ADCs, including dynamic comparators, operational amplifiers, and voltage references, are presented and compared.

4.1 Dynamic Comparators

Whenever redundancy is applied to relax the comparator offset requirements, dynamic comparators are preferred in low-resolution pipeline stages because of their potential for low power and small area. The concept of a dynamic comparator is, in this context, restricted to single-stage topologies without static power dissipation. Most of the published topologies are based on sense amplifiers used in static random access memories (SRAM), which are very close to comparators in function [1, 2]. As a dynamic comparator is turned off when inactive and very small transistors are preferred to minimize power and area, it is inevitably sensitive for larger offsets. This is mainly owing to transistor mismatch emphasized by the switching transients. In spite of the loose

specification, offset might become a limiting factor of the performance of the whole ADC.

The most important comparator specifications are offset, power consumption and immunity to noise and mismatch. In a mixed-signal circuit such as an ADC, fully differential analog signals are preferred as a means of getting a better power supply rejection and immunity to common mode noise. A number of single-stage, fully differential dynamic comparator topologies, including differential reference voltages, for pipeline ADCs have been proposed [3, 4, 6]. They dissipate power only when latched and their trip point can be adjusted by introducing imbalance in the transistor [3, 4] or capacitor sizing [6]. The analysis and experimental results of these three dynamic comparator topologies below is published in [7].

4.1.1 Resistive Divider Comparator

A widely used dynamic comparator in pipeline A/D converters is based on a differential sensing amplifier. This so-called resistive divider dynamic comparator, presented in Fig. 4.1, was introduced in [3]. Transistors M_1–M_4, biased in linear region, adjust the threshold resistively and above them transistors M_5–M_{12} form a latch.

The operation of the comparator is as follows. When the latch control signal is low ($V_{latch} = 0$ V), the transistors M_9 and M_{12} are conducting and M_7 and M_8 are cut off, which forces both differential outputs to V_{dd} and no current path exists between the supply voltages. Simultaneously M_{10} and M_{11} are cut off and the transistors M_5 and M_6 conduct. This implies that M_7 and M_8 have a voltage of V_{dd} over them. When the comparator is latched ($V_{latch} \rightarrow V_{dd}$) M_7 and M_8 are turned on. Immediately after the regeneration moment, the gates of the transistors M_5 and M_6 are still at V_{dd} and they enter saturation, amplifying the voltage difference between their sources. If all transistors M_5–M_{12} are assumed to be perfectly matched, the imbalance of the conductances of the left and right input branches, formed by M_1–M_2 and M_3–M_4, determines which of the outputs goes to V_{dd} and which to 0 V. After a static situation is reached (V_{latch} is high), both branches are cut off and the outputs preserve their values until the comparator is reset again by switching V_{latch} to 0 V.

The transistors M_1–M_4 connected to the input and reference are in the triode region and act like voltage controlled resistors. The conductances of the left and right input branches g_L and g_R can be written as

$$g_L = \mu_0 C_{ox} \left(\frac{W_2}{L} \left(V_{in}^+ - V_T - V_{ds1,2} \right) + \frac{W_1}{L} \left(V_{ref}^- - V_T - V_{ds1,2} \right) \right) \qquad (4.1)$$

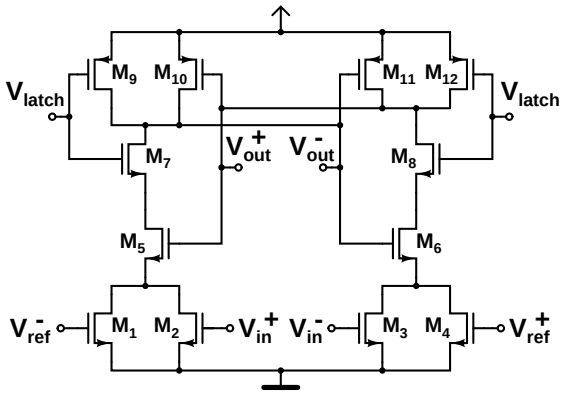

Figure 4.1 Resistive divider comparator.

and

$$g_R = \mu_0 C_{ox} \left(\frac{W_4}{L} \left(V_{in}^- - V_T - V_{ds3,4} \right) + \frac{W_3}{L} \left(V_{ref}^+ - V_T - V_{ds3,4} \right) \right), \tag{4.2}$$

where V_T is the threshold voltage and $V_{ds1,2,3,4}$ the drain-source voltage of the corresponding transistor. If no mismatch is present the comparator changes its output when the conductances of the left and right input branches are equal $g_L = g_R$. By denoting $W_A = W_2 = W_4$ and $W_B = W_1 = W_3$ the input voltage at which the comparator changes its state is given by

$$V_{in}^+ - V_{in}^- = \frac{W_B}{W_A} \left(V_{ref}^+ - V_{ref}^- \right). \tag{4.3}$$

By dimensioning of the transistor widths W_A and W_B, the threshold of the comparator can be adjusted to the desired level.

Eq. 4.3 implies that the offset of the comparator depends on the mismatch of transistors M_1–M_4. This is true only when all other transistors M_5–M_{12} are assumed to match perfectly. The transconductance of the transistors M_1–M_4 operating in the linear region, is directly proportional to the drain-source voltage of the corresponding transistor $V_{ds1,2,3,4}$, while for the transistors M_5–M_6 the transconductance is proportional to $V_{gs5,6} - V_T$, where V_T is the threshold voltage and $V_{gs5,6}$ are the corresponding gate-source voltages. At the beginning of the latching process, $V_{ds1,2,3,4} \approx 0$ while $V_{gs5,6} - V_T \approx V_{dd}$. Thus, $g_{m5,6} \gg g_{m1,2,3,4}$, which makes the matching of M_5 and M_6 dominant in determining the latching balance. As small transistors are preferred, offset voltages of a few hundred millivolts are easily resulted. Mismatch in transistors M_7–M_{12} are attenuated by the gain of M_5 and M_6, which makes them less critical. The offset voltage of the input transistors M_1–M_4 affects directly the total offset, but the

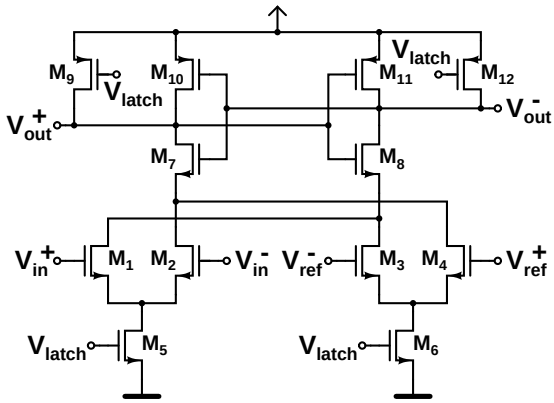

Figure 4.2 Differential pair comparator.

input-referred offset $V_{os5,in}$ of the transistor M_5 (and M_6) has a proportionality

$$V_{os5,in} = V_{os5}\frac{g_{ds1}}{g_{m1}} \sim V_{os5}\frac{V_{gs1}-V_T}{V_{ds1}}, \tag{4.4}$$

from which it can be concluded that the lower the common mode voltage, and thus V_{gs1}, the smaller the effect of the offset of transistors M_5–M_6.

To cope with the mismatch problem, the layout of the critical transistors must be drawn as symmetric as possible. In addition to the mismatch sensitivity, the latch is also very sensitive to an asymmetry in the load capacitance. This can be avoided by adding an extra latch or inverters as a buffering stage after the comparator core outputs.

The resistive divider dynamic comparator topology has one clear benefit, which is its low kickback noise. This results from the fact that the voltage variation at the drains of the input transistors M_1–M_4 is very small. On the other hand, the speed and resolution of the topology are relatively poor because of the small gain of the transistors biased in the linear region.

4.1.2 Differential Pair Comparator

A fully differential dynamic comparator based on two cross-coupled differential pairs with switched current sources loaded with a CMOS latch is shown in Fig. 4.2 [4]. The trip point of the comparator can be set by introducing imbalance between the source-coupled pairs. Because of the dynamic current sources together with the latch, connected directly between the differential pairs and the supply voltage, the comparator does not dissipate DC-power.

The operation of the comparator can be described as follows. When the comparator

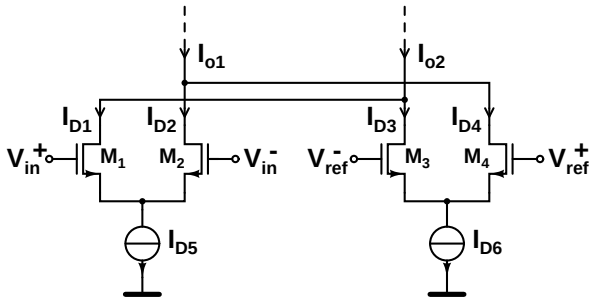

Figure 4.3 Simplified model of the differential pair comparator.

is inactive the latch signal V_{latch} is at 0 V, which means that the current source transistors M_5 and M_6 are switched off and no current path between the supply voltages exists. Simultaneously, the PMOS switch transistors M_9 and M_{12} reset the outputs by shorting them to V_{dd}. The NMOS transistors M_7 and M_8 of the latch conduct and also force the drains of all the input transistors M_1–M_4 to V_{dd} , while the drain voltage of M_5 and M_6 are dependent on the comparator input voltages. When V_{latch} is raised to V_{dd}, the outputs are disconnected from the positive supply, the switching current sources M_5 and M_6 turn on, and M_1–M_4 compare $V_{in}^+ - V_{in}^-$ with $V_{ref}^+ - V_{ref}^-$. Since the latch devices M_7–M_8 are conducting, the circuit regeneratively amplifies the voltage difference at the drains of the input pairs. The threshold voltage of the comparator is determined by the current division in the differential pairs and between the cross-coupled branches.

The threshold level of the comparator can be derived using large signal current equations for the differential pairs, as indicated in Fig. 4.3. Using the symbols indicated in the figure and having different dimensioning in the source-coupled pairs ($W_1 = W_2$, $W_3 = W_4$) the transistors M_1–M_4 follow the large signal current equations

$$I_{D1} - I_{D2} = \beta_1 V_{in} \sqrt{\frac{2I_{D5}}{\beta_1} - V_{in}^2} \tag{4.5}$$

and

$$I_{D4} - I_{D3} = \beta_3 V_{ref} \sqrt{\frac{2I_{D6}}{\beta_3} - V_{ref}^2}, \tag{4.6}$$

where $\beta_i = \frac{1}{2}K'\frac{W_i}{L} = \frac{1}{2}\mu C_{ox}\frac{W_i}{L}$, $V_{in} = V_{in}^+ - V_{in}^-$ and $V_{ref} = V_{ref}^+ - V_{ref}^-$. The mobility μ and gate oxide capacitance C_{ox} are process-dependent constants. The comparator changes its stage when the currents $I_{o1} = I_{D1} + I_{D3}$ and $I_{o2} = I_{D2} + I_{D4}$ of the both output branches are equal. Assuming the relation of the source-coupled pair bias currents to be $I_{D5} = d \cdot I_{D6}$ and by marking the threshold point with parameter e so that $V_{in} = e \cdot V_{ref}$,

this results in a condition

$$2de^2 I_{D6}\frac{W_1}{L} - K'e^4 V_{ref}^2\left(\frac{W_1}{L}\right)^2 = 2I_{D6}\frac{W_3}{L} - K'V_{ref}^2\left(\frac{W_3}{L}\right)^2. \tag{4.7}$$

When the parameters d and e are chosen according to the desired trip point of the comparator, the transistor dimensions W_1 and W_3 can be interpolated from Eq. 4.7. It can be concluded that as there are terms depending on the transistor dimensions with different signs at both sides of Eq. 4.7, transistor mismatches are partly canceled, which indicates robustness against mismatches.

The total offset voltage of the comparator consists of the sum of the offsets of both source-coupled pairs. The offset of one differential pair has the well-known dependency on the mismatch of the threshold voltage ΔV_T, load resistance ΔR_L and transistor dimensions $\Delta\beta$ and their corresponding average values V_T, R_L, and β

$$V_{os} = \Delta V_T + \frac{V_{gs} - V_T}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta\beta}{\beta}\right). \tag{4.8}$$

The offset voltage is in this case dominated by the mismatch of the transistor dimensions $\Delta\beta$, while the $V_{gs} - V_T$ is set by the tail currents I_{D5} and I_{D6}.

The effect of the mismatches of the other transistors M_7–M_{12} is in this topology not completely critical, because the input is amplified by M_1–M_4 before M_7–M_{10} latch. The drains of the cross-coupled differential pairs are high impedance nodes and the transconductances of the threshold-voltage-determining transistors M_1–M_4 large.

A drawback of the differential pair dynamic comparator is its high kickback noise: large transients in the drain nodes of the input transistors are coupled to the input nodes through the parasitic gate-drain capacitances. In low-resolution pipeline stages, with only a few comparators connected to the stage input, this is not a severe problem. If required, however, there are techniques to reduce the kickback noise, e.g. by cross coupling dummy transistors from the differential inputs to the drain nodes [5]. The differential pair topology achieves a high speed and resolution, which results from the built-in dynamic amplification.

4.1.3 Charge Distribution Comparator

A fully differential comparator can also be realized by employing a charge summation circuit rather than a current addition circuit, like in the previous topologies. The implementation consists of a latch stage preceded by coupling capacitors that are precharged to the input and reference voltages during the reset phase. A possible capacitive differential pair comparator topology, derived from the circuit used in [6], is shown in

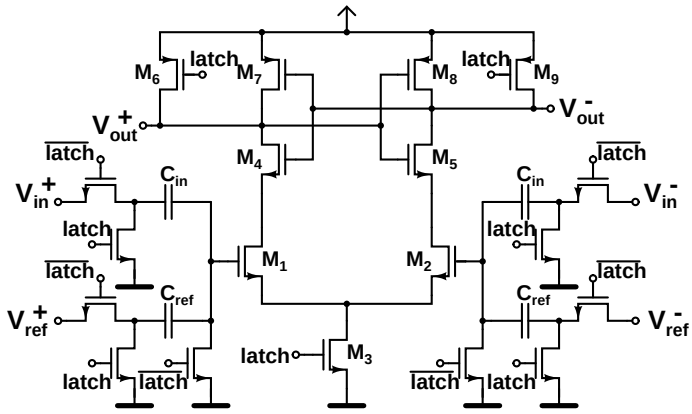

Figure 4.4 Capacitive differential pair comparator.

Fig. 4.4. The comparator core is similar to the previous topology consisting this time of a single, switched differential amplifier with a CMOS latch load.

The comparator of Fig. 4.4 requires a two-phase clock; during the phase $\overline{latch}$ one coupling capacitor pair is precharged to $V_{in} = V_{in}^{+} - V_{in}^{-}$ and the other pair to $V_{ref} = V_{ref}^{+} - V_{ref}^{-}$. The comparator core is inactive and the switch transistors M_6 and M_9 are resetting the complementary outputs to V_{dd}, which forces M_4–M_5 to conduct, also forcing the drains of the input pair to V_{dd} while the dynamic tail current source M_3 is switched off. When the signal *latch* is released, the differential pair amplifier becomes active, the outputs are disconnected from the supply voltage, and the capacitor bottom plates are grounded allowing the charges of the input (C_{in}) and reference capacitors (C_{ref}) to be transfered between their top plates. The differential pair amplifies the difference in the summing nodes and the latch is regenerated. According to the preservation of the charge, the threshold of the comparator is given by

$$V_{in}^{+} - V_{in}^{-} = \frac{C_{ref}}{C_{in}} \left(V_{ref}^{+} - V_{ref}^{-} \right). \tag{4.9}$$

Eq. 4.9 implies that the threshold voltage of the comparator can be adjusted linearly with the capacitance ratio.

Offset of this comparator topology is determined by two major factors. First, the offset voltage is directly proportional to mismatch between the capacitors C_{in} and C_{ref}. Even in a pure CMOS process without dedicated capacitors, capacitor matching that is enough for the RSD correction is easily achieved. Second, the offset of the differential pair amplifier follows Eq. 4.8 and the same conclusions as for the differential pair comparator hold.

Contrary to the two previous topologies, in this case a two-phase clock is required and the area of the comparator is larger because of the capacitors. On the other hand, the capacitive threshold level adjusting is linear and very robust. The kickback noise of this topology is determined in the first order by the charge injection from the switches. The fairly large noise, originated from the switching of the dynamic differential pair, is well isolated from the inputs. Speed of the charge division comparator is limited by the required time to switch from the sample mode ($\overline{latch}$ goes low) to the hold and comparison mode ($latch$ goes high).

4.1.4 Experimental Results

The performance of the dynamic comparator topologies was verified and compared by measuring test structures, fabricated in a 0.35-μm BiCMOS process—only MOS transistors were used. Comparators employing the three topologies introduced, occupying approximately the same area and dissipating almost equal power, were designed. The input stages of the comparators are dimensioned to place the threshold voltage to $V_{in} = 1/4V_{ref}$, when nominally $V_{ref}^{-} = 1.1$ V and $V_{ref}^{+} = 1.9$ V. The supply and common mode voltages are 3.0 V and 1.5 V, respectively. To reduce offset, the minimum gate length of the transistors was set to 0.5 μm. Additionally, a resistive divider comparator with a minimum gate length of 0.35 μm and scaled transistor widths was added on the test chip to examine the effect of transistor mismatch. Because of the limited number of samples, statistical analysis is not possible. However, the measurement results agree very well with statistical simulations, in which only the transistor mismatch of the critical devices is taken into account [4].

4.1.4.1 Offset

In Tab. 4.1 the offset performance of the resistive divider comparators (Comparator 1 and Comparator 2), the differential pair comparator (Comparator 3), and the charge distribution comparator (Comparator 4) are summarized. The simulated power dissipation (P_D) of the comparator cores at 100 MS/s and the worst measured offset voltage ($V_{os,max}$) with the nominal V_{ref} of 0.8 V are given. It can be seen that power dissipation and area of the comparator topologies are proportional to the transistor dimensions. As predicted, the resistive divider comparator has the largest offset, which is dominated by the mismatch of the saturated latch transistors, and the charge distribution topology the smallest. The differential pair comparator also features very small offset voltage.

The effect of the common mode voltage level is illustrated in Fig. 4.5. The offset voltage is plotted as a function of the common mode voltage of V_{in} and V_{ref} for the same

Table 4.1 Performance of the comparators.

	No	A [μm^2]	P_D [mW]	$V_{os,max}$ [mV]
Resistive divider (0.35μm)	1	760	0.36	200
Resistive divider	2	1200	0.32	290
Differential pair	3	1520	0.58	80
Charge distribution	4	2800	0.81	75

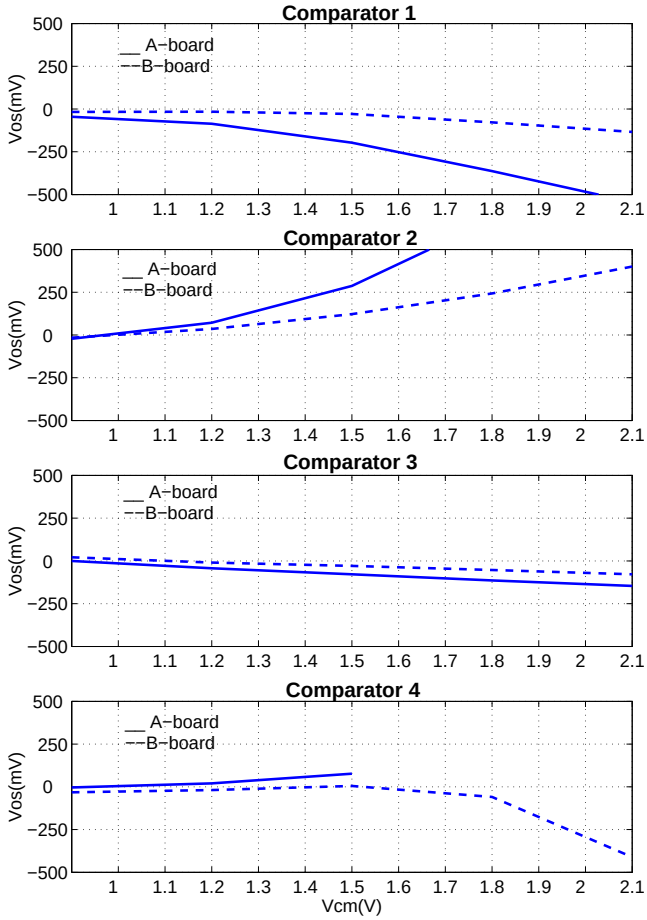

Figure 4.5 Offset as a function of the common mode voltage.

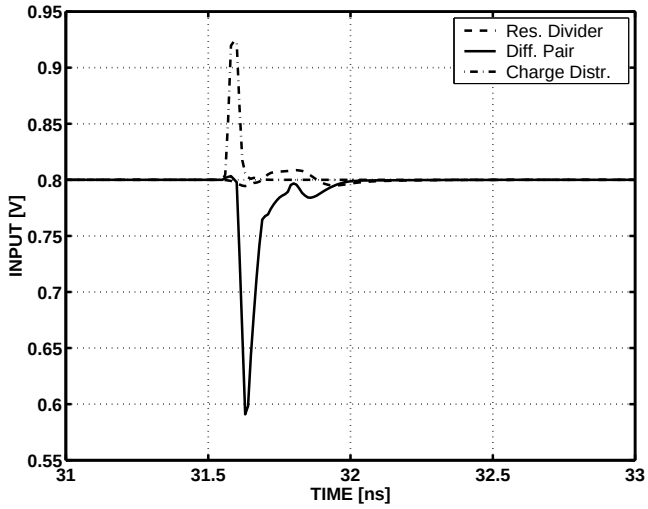

Figure 4.6 Simulated kickback noise of the dynamic comparators.

comparators with $V_{ref} = 0.8$ V. The measurement results of two extreme test samples are shown (best and worst case). The offset of the resistive divider comparators grows rapidly with an increasing common mode voltage, while the differential pair comparator is fairly insensitive to that variation. The charge distribution comparator also operates very reliably with a small offset voltage until the input differential pair becomes non-functional. The sensitivity of the resistive divider comparators to the common mode voltage level can be already predicted from Eq. 4.4.

4.1.4.2 Kickback Noise and Speed

In Fig. 4.6 the simulated kickback noise caused to the differential inputs of the same test structures as earlier is compared. The differential comparator inputs at the latching moment, taken from a voltage source with an internal impedance of 1 kΩ, are shown in the worst case, which appears when the differential input is at its maximum. As predicted, the differential pair topology has the largest kickback noise and the resistive divider comparator the lowest. When the comparison speed, and, actually, also the resolution, of the topologies are examined, the order of the topologies changes. As seen from Fig. 4.7, where the simulated differential outputs of the comparators are plotted when a 2-mV deviation from the nominal trip point is applied to the comparator inputs, the differential pair comparator is the fastest to make the decision and the charge division topology the slowest.

It should be noted that the kickback noise is not a severe issue in low-resolution

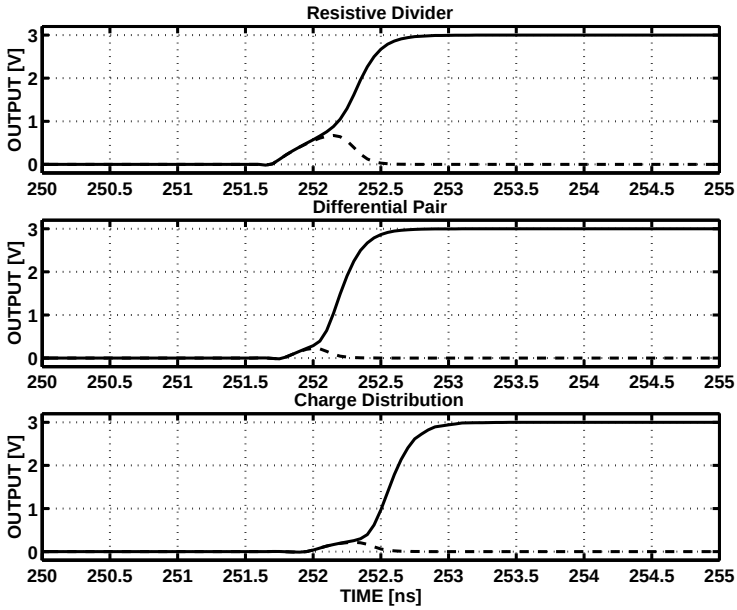

Figure 4.7 Simulated decision speed of the dynamic comparators.

pipeline stages: the number of comparators connected to the input is small, the RSD correction allows fairly large variations of the trip point, and the sub-ADC can be latched shortly after the MDAC performs the sampling operation, avoiding the kickback noise to deteriorate the stored analog input value.

4.1.5 Summary: Dynamic Comparators

In conclusion, with similar area and power dissipation, the topologies based on charge distribution, and one or two cross-coupled differential pairs with little amplification were found to be more robust against process variations and transistor mismatches. The sensitivity to common mode voltage variations was especially high in the topology, in which the input devices are biased in the linear region. The drawback of the differential pair comparator is a large kickback noise. However, in a low-resolution pipeline stage this can usually be tolerated.

4.2 Operational Amplifiers

The operational amplifier, forming the core of an SC multiplying D/A converter, is the most critical block of a pipeline stage. The resolution and speed of the whole ADC

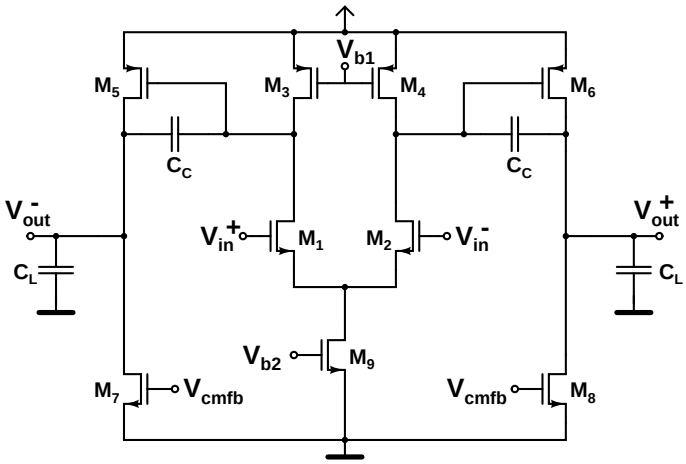

Figure 4.8 Two-stage amplifier with Miller compensation.

is usually determined by the operational amplifiers of the MDACs. In general, the amplifiers open loop DC-gain limits the settling accuracy of the amplifier output, while the bandwidth and slew rate of the amplifier determine the maximal clock frequency. To maximize the signal-to-noise ratio, the operational amplifier should also utilize a large signal swing at the output. The amplifier specifications relative to the resolution and sample rate were handled in detail in chapter 3.

In conclusion, in high-resolution high-speed pipeline A/D converters a very large open loop DC-gain, a wide bandwidth and a high slew rate are required from the amplifier. The simplest way to meet these requirements is to use one-stage amplifiers, like the folded and telescopic cascode amplifiers, with gain boosting. The drawback of these topologies, especially with low supply voltage, is a limited signal swing and a complicated settling behavior because of the regulation amplifiers. High open loop DC-gain can also be achieved with a two- or three-stage amplifier. In multi-stage amplifiers, a trade off in the frequency compensation exists between the stability and bandwidth. The operational amplifier topologies and their design are the main topics of various books and publications [8, 9, 10] and is out of the scope of this thesis. However, a short introduction to the most common amplifier topologies is given below to address the pipeline ADC design issues.

4.2.1 Miller Compensated Amplifier

Of the several alternative two-stage amplifiers, Fig. 4.8 shows a simple Miller compensated amplifier [10]. With all the transistors in the output stage of this amplifier placed

in the saturation region, it has a differential output swing of $2V_{dd} - 4V_{ds,sat}$, where V_{dd} is the supply voltage and $V_{ds,sat}$ is the saturation voltage of a transistor. For a typical $V_{ds,sat}$ of 200 mV, the resulting differential swing is $2V_{dd} - 0.8\,V$, which is better than that of most other topologies. The non-dominant pole, arising from the output node, is located at

$$p_1' = -\frac{g_{m5}}{C_L\left(1+\frac{C_{L1}}{C_C}\right)+C_{L1}}, \tag{4.10}$$

where g_{m5} is the transconductance of M_5 and M_6, C_{L1} is the load capacitance of the first stage, C_C the compensation capacitor and C_L is the load capacitance. Since this pole is determined dominantly by an explicit load capacitance, the amplifier has a compromised frequency response.

The gain bandwidth product (GBW) of a Miller compensated amplifier is given approximately by

$$GBW = \frac{g_{m1}}{C_C}, \tag{4.11}$$

where g_{m1} is the transconductance of M_1 and M_2. It can be shown that the amplifier should be dimensioned so that $GBW \leq \frac{1}{2}p_1'$. This restriction limits the bandwidth of a Miller compensated amplifier. In general, the open loop DC-gain of the basic configuration is not large enough for high-resolution applications. Gain can be enhanced by using cascoding, which has, however, a negative effect on the signal swing and bandwidth. Another drawback of this architecture is a poor power supply rejection at high frequencies because of the connection of V_{dd} through the gate-source capacitance $C_{gs5,6}$ of M_5 and M_6 and C_C in Fig. 4.8.

4.2.2 Ahuja-Style Compensated Amplifier

The performance of a two-stage amplifier can be significantly enhanced by using the so-called Ahuja-style frequency compensation [11] shown in Fig. 4.9. In this architecture, the compensation capacitor is connected back to a low impedance node, which makes the amplifier faster than with the standard Miller compensation. This way, the GBW limiting property of the right half plane zero caused by the compensation capacitor in the Miller compensated amplifier can be eliminated. Also, the open loop DC-gain becomes larger because of the large gain first stage, but the output swing remains the same as for the Miller compensated amplifier [10]. The non-dominant pole is shifted to

$$p_1' = -\frac{C_C}{C_{L1}} \cdot \frac{g_{m9}}{C_L + C_C}, \tag{4.12}$$

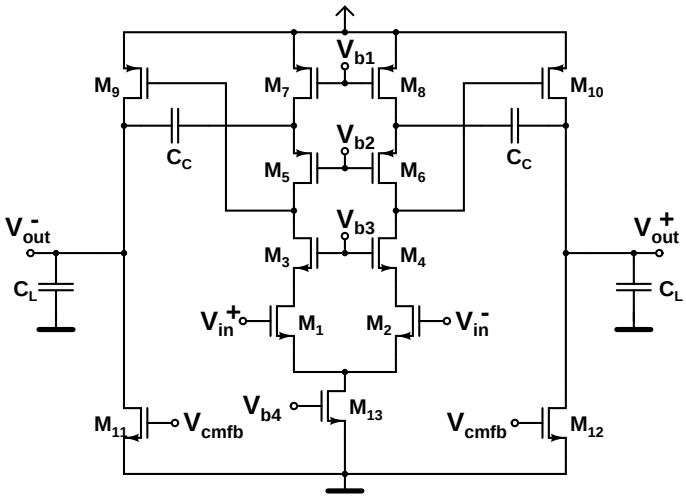

Figure 4.9 Two-stage amplifier with Ahuja style compensation.

where g_{m9} is the transconductance of M_9 and M_{10}. The improvement factor compared to the Miller compensated amplifier is C_C/C_{L1}. The GBW of an Ahuja-style compensated amplifier follows in principle Eq. 4.11 of the Miller compensated amplifier and the same restriction $GBW \leq \frac{1}{2}p_1'$ holds as well. In conclusion, the bandwidth is improved by the same factor C_C/C_{L1}. In addition, the power supply rejection ratio is improved compared to the Miller compensated amplifier.

The compensation capacitor results in a complex pole pair, which causes a slight gain peak just below the transition frequency, which deteriorates the phase margin. The gain peak can even grow above unity gain and cause stability problems. One solution is to add Miller capacitors to push the dominant pole to a lower frequency—effectively killing the gain peak [12].

4.2.3 Telescopic Cascode Amplifier

The simplest approach for a high-gain operational amplifier is the one-stage telescopic cascode amplifier of Fig. 4.10. With this architecture, a high open loop DC-gain can be achieved and it is capable of high speed when closed loop gain is low. The single-stage architecture naturally suggests low power consumption. The biggest disadvantage of a telescopic cascode amplifier is its low maximum differential output swing, which is shown to be $2V_{dd} - 10V_{ds,sat} - 6V_{margin}$, where V_{margin} is a small safety margin added to $V_{ds,sat}$. With a voltage margin of 100 mV, this gives $2V_{dd} - 2.6$ V, which is much smaller than that of a Miller compensated amplifier. The high-frequency response is the result of the fact that the second pole corresponding to the source nodes of the n-channel

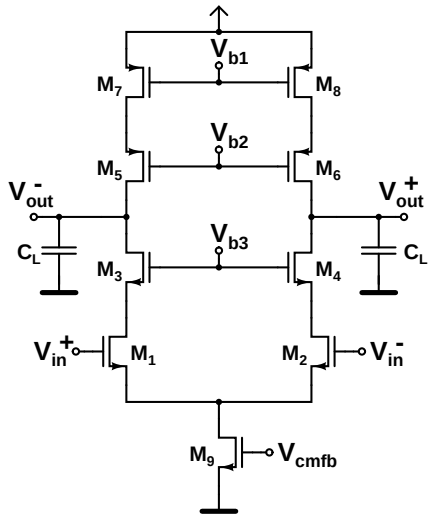

Figure 4.10 Telescopic cascode amplifier.

cascode devices, determined by the transconductance of the n-channel devices, arises only from two transistors. Also, because the compensation of this amplifier terminates to ground in contrast to the two-stage amplifier case, it has a better high frequency power supply rejection. The GBW of the amplifier is given by

$$GBW = \frac{g_{m1}}{C_L}, \tag{4.13}$$

where g_{m1} is the transconductance of transistors M_1 and M_2 and C_L is the load capacitance. Thus, the GBW is limited by the load capacitance. Because of the simple topology and dimensioning, the telescopic cascode amplifier is preferred, if its output swing is large enough for the specific application.

The output signal swing of this architecture has been widened by driving the transistors M_7 – M_9 into the linear region [9]. In order to preserve the good common mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) properties of the topology, additional feedback circuits for compensation have been added to these variations.

4.2.4 Folded Cascode Amplifier

The folded cascode amplifier topology is shown in Fig. 4.11. The swing of this design is constrained by its cascoded output stage. Taking into account the safety margins, and the $V_{ds,sat}$ required across the cascode devices, the differential output swing is

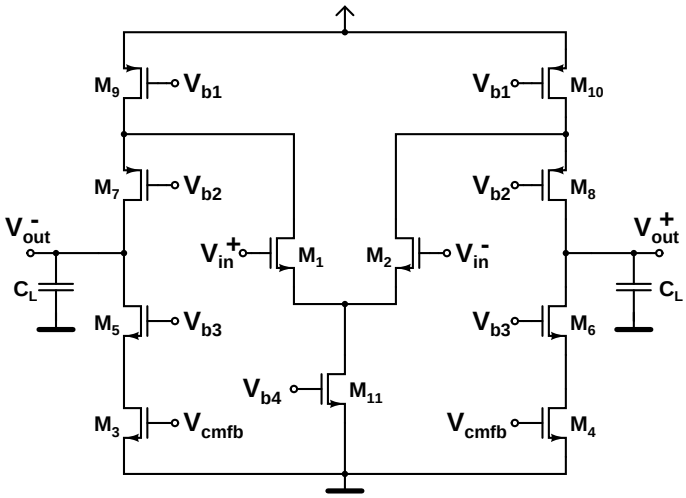

Figure 4.11 Folded cascode amplifier.

$2V_{dd} - 8V_{ds,sat} - 4V_{margin}$. Under the same circumstances as before, this is estimated to be $2V_{dd} - 2.0$ V, which is much less than that for a Miller compensated amplifier but better than for a telescopic cascode amplifier. The second pole of this amplifier is located at g_{m7}/C_{par}, where g_{m7} is the transconductance of M_7 or M_8 and C_{par} is the sum of the parasitic capacitances from transistors M_1, M_7 and M_9 at the source node of transistor M_7. The frequency response of this amplifier is deteriorated from that of the telescopic cascode amplifier because of a smaller transconductance of the p-channel device and a larger parasitic capacitance. Still, compared to the Miller compensated amplifier, a larger bandwidth can be achieved.

To assure symmetrical slewing, the output stage current is usually made equal to that of the input stage. The power dissipation of the folded cascode amplifier is thus comparable to that of a two-stage amplifier. On the other hand, owing to the folded topology there are more degrees of freedom in trading between the input and output stage currents, gain and bandwidth. The GBW of the folded cascode amplifier is also given by Eq. 4.13. The same arguments as for the telescopic cascode amplifier also stand for the good PSRR and CMRR properties of the topology. Gain boosting by using regulation amplifiers can also be applied in the folded cascode amplifier architecture. Another way to raise the amplifier DC-gain is to add cascode transistors above the input differential pair. However, the improvement in the gain is not enough for a high-resolution pipeline ADC [13].

The open loop DC-gain of amplifiers having cascode transistors can be boosted by regulating the gate voltages of the cascode transistors [14]. The regulation is realized

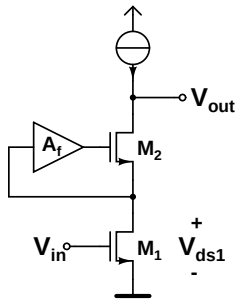

Figure 4.12 Regulated cascode gain stage.

by adding an extra gain stage as shown in Fig. 4.12. This stage reduces the feedback from the output to the drain of the input transistors. Thus, the output impedance of the circuit is increased by the gain of the additional amplifier stage with a gain of A_f

$$r_{out} = g_{m2} r_{ds1} r_{ds2} (A_f + 1) + r_{ds1} + r_{ds2} \approx g_{m2} r_{ds1} r_{ds2} A_f, \tag{4.14}$$

where g_{m2} is the transconductance of M_2, r_{ds1} and r_{ds2} are the output resistances of M_1 and M_2, respectively. In this way, the DC-gain of the amplifier can be increased by several orders of magnitude. The dependency of the stability of the whole amplifier on the feedback amplifier bandwidth deserves great attention. If the parasitic pole introduced by the feedback amplifier can be kept at high frequencies, a single-pole roll-off and settling behavior can be obtained. Furthermore, the increase in power and chip area can be kept very small with an appropriate feedback amplifier architecture [14].

The choice of the feedback amplifier topology also has a strong effect on the reduction of the output swing of the amplifier. As indicated in Fig. 4.12, the feedback amplifier input voltage equals the drain-source voltage of the transistor M_1. In many topologies, the lower limit of V_{ds1} is set by the feedback amplifier. A more severe performance limitation of a regulated cascode amplifier can be obtained in SC circuits where the amplifier enters slewing. From the settling behavior of a typical regulated cascode amplifier in a feedback configuration, it can be seen that after the beginning of the slewing there is a delay before the regulation amplifier is working again. This delay makes the settling of the amplifier output slower, which may cause problems in SC circuits with fairly high voltage swings.

4.3 Voltage Reference Circuits

In a pipeline A/D converter, reference voltages $\pm V_{ref,0}, \ldots, \pm V_{ref,n-1}$ (or currents) are required in each stage for the coarse A/D conversion performed by a flash ADC, as well as $\pm V_{ref}$ for the multiplying D/A converter when forming the stage output. Global voltage references for the entire ADC are generally preferred instead of local ones because of better matching and lower total power dissipation. However, if the common mode voltage level is set by an on-chip bandgap reference, the absolute values of these reference voltages varies with the process parameters and temperature.

The number of the voltage references of the sub-ADC depends on the stage resolution, the number of different stage resolutions, and comparator topology employed as discussed in section 4.1. These references are typically only connected to a small capacitive load formed by the gates of MOS transistors and no buffering is required. Inaccuracy in the voltage reference adds to the offset voltage of a comparator, deteriorating its accuracy. In pipeline ADCs with RSD correction the comparator accuracy requirement is relaxed and can easily be achieved by a resistor string with a symmetrical lay out.

In switched capacitor realizations, the full-scale amplitude determining reference voltages of the MDACs have, on the contrary, high accuracy specifications. They must charge a variable capacitance formed by the sampling capacitors of the MDACs and settle within the accuracy of the whole pipeline ADC during half of a clock cycle. Especially in high-speed converters, this implies inevitably buffering of the references, with high gain to achieve the accuracy and settling time specifications.

4.3.1 Resistor String

A resistor string, dimensioned to provide proper tap voltages, is a straightforward solution for a voltage reference. If the resistor string is placed directly between the supply voltages, the reference voltages follow the variations of the power supply maintaining their relative magnitudes. This is desirable when the signal swing is also proportional to the supply voltages. If this is not the case, the potential of either the highest or the lowest node of the resistor string can be controlled to keep the tap voltages constant. To minimize power dissipation, the total resistance of the string should be maximized, which is limited by the settling requirement of the reference voltages; the RC time constant of each capacitively loaded node of the string must be well below the settling time.

The reference voltage levels can be adjusted to follow the analog reference voltage, originated from, for example, a bandgap reference, by using a current source controlled

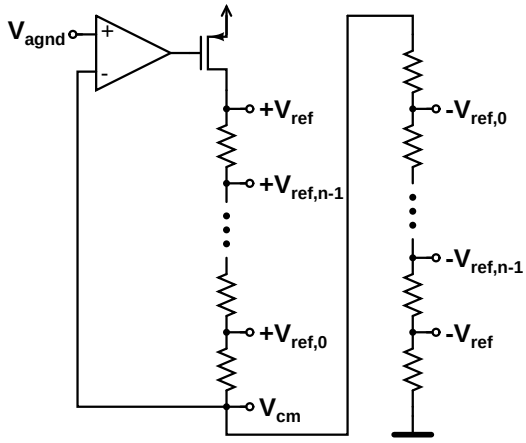

Figure 4.13 Resistor string combined with amplifier.

with a feedback amplifier, as shown in Fig. 4.13. The negative feedback forces the common mode voltage V_{cm} to follow the analog ground V_{agnd}, despite the supply voltage and process variations. Furthermore, the settling of the reference voltages after a switching transient is faster than in a resistor string without feedback, because of the current source. The absolute accuracy is not improved, but the relative error in the comparator and MDAC reference voltages is within the requirements of a medium-resolution pipeline A/D converter. As a feedback amplifier, a single-stage differential pair gives enough gain, but, for stability reasons, an extra capacitor is typically needed at the amplifier output. This reference topology has been successfully implemented in single-chip direct conversion receivers [15, 16].

4.3.2 Push-Pull Buffer

In a high-resolution pipeline A/D converter, a large number of stages with large capacitors in their MDACs increase the load of the voltage reference nodes. To guarantee that the reference does not limit the settling speed, its output impedance has to be very low. This means that a resistor string implementation of the reference would have a very large quiescent current, or, alternatively, a large external capacitor has to be used. A more reasonable power consumption without an external capacitor is obtained with the circuit proposed in Fig. 4.14(a). A low impedance, corresponding to a high conductance, voltage output is provided by a class AB push-pull buffer constructed of complementary transistors. The output conductance of the buffer is a sum of the transconductances of the PMOS and NMOS transistors and can be maximized with a reasonable bias current by using very large transistors. The reference voltage V_{ref} can

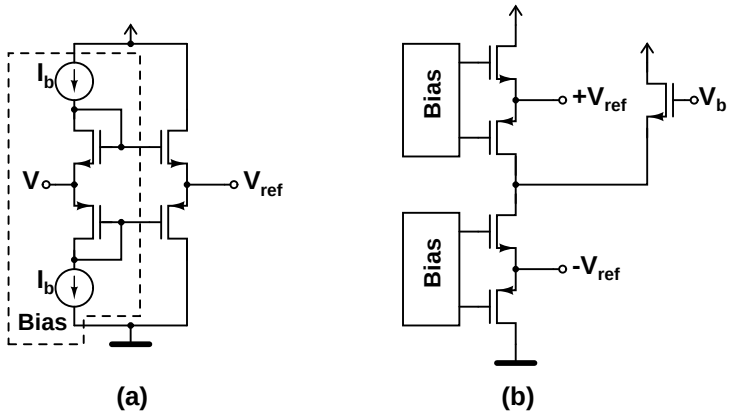

Figure 4.14 Push-pull reference buffer for (a) a single voltage and (b) total circuit.

be tuned by an external voltage V.

Steady state power dissipation of the reference voltage buffer can be further reduced by cascoding the buffers for the positive and the negative references, as depicted in Fig. 4.14(b). Additionally, a source follower is utilized to set the voltage of the floating node between the negative and positive reference buffers. The major drawback of this buffer circuit is the limited spacing between the MDAC reference voltages $\pm V_{ref}$; one gate-source voltage plus voltage over a bias current source I_b is the minimal distance to the supply voltages. Even if the current sources are biased in the linear region, the reference voltages are at least about one volt from the ground and positive supply. Nevertheless, the topology has been successfully employed with a 3-V supply in a low-power 10-bit pipeline A/D converter [17].

4.3.3 Multi-Stage Buffer

To achieve very high speed and resolution from a pipeline A/D converter, the MDAC reference voltages must be buffered in order to attain the required accuracy and settling time. Using a conventional opamp buffer with resistive feedback leads easily to high power dissipation because of the very high opamp bandwidth requirement together with a large capacitive load. Furthermore, a large transconductance is needed to achieve high accuracy. An alternative approach to a fast settling buffer is to make it sufficiently slow by stabilizing the reference voltages within the accuracy required for a predefined resolution. This can be accomplished with a buffer depicted in Fig. 4.15, in which a multi-stage buffer with a very large transconductance is combined with an external stabilization capacitor [18, 19].

Operation of the multi-stage buffer is illustrated in Fig. 4.16, where the output

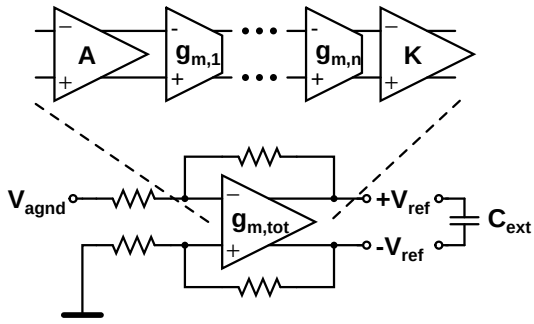

Figure 4.15 Multi-stage reference buffer.

impedance of the buffer is plotted as a function of the frequency. At low frequencies, the transconductance of the buffer $g_{m,tot}$, plotted with a solid line, determines the output impedance, while the external capacitance C_{ext}, dashed line, begins to dominate as the frequency is increased. In order to get the output impedance sufficiently low, $g_{m,tot}$ must be considerably enlarged. When implementing transconductances in the order of 1 S with a single g_m stage, process variations result in significant fluctuations of the transconductance value. A more robust realization can be obtained when several transconductance elements $g_{m,j}$, preceded by one or more voltage amplifiers A_i and proceeded by a number of current amplifiers K_k are utilized to achieve a total transconductance of

$$g_{m,tot} = \prod_{i=1}^{n_A} A_i \cdot \prod_{j=1}^{n_g} g_{m,j} \cdot \prod_{k=1}^{n_K} K_k, \tag{4.15}$$

where n_A, n_g, and n_K are the number of the respective elements [19]. The multi-stage structure is shown in Fig. 4.15 as well.

The size of the external capacitor, including its parasitics, is determined by the desired corner frequency and high-frequency impedance, shown in Fig. 4.16. Utilization of an external component for stabilization requires careful consideration of the parasitic resistances, capacitances, and inductances of the package and off-chip components. In particular, the parasitic inductance inherited from the bondwires and package pin parasitics cause ringing, which must be compensated with a damping circuit.

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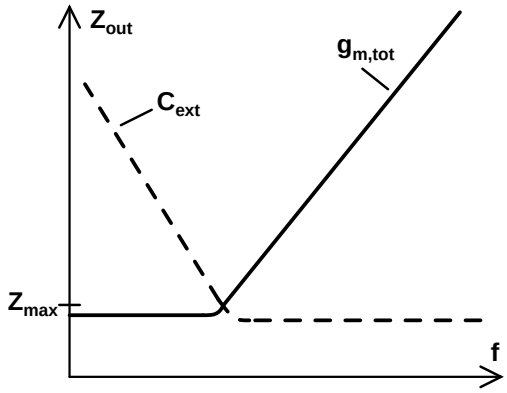

Figure 4.16 Output impedance of the multi-stage reference buffer as a function of the frequency.

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Chapter 5

Analog-to-Digital Converters for Direct Conversion Receivers

In wireless communications, receiver architectures that have on-chip channel selection filters, like direct conversion or low-IF, are preferred for increasing the integration density. Combining digital signal processing with analog circuits on the same chip is desirable in miniaturization. However, sensitive RF inputs followed by a gain of 80–100 dB on the same chip with digital blocks having rail-to-rail signals create potential problems in the system. The first block employing mixed-signal or digital signal processing in the receiver chain is the analog-to-digital converter. The resolution and sample rate of the A/D converter of a receiver depends on the target system and the topology and performance of the RF and baseband blocks. In this chapter, general consideration is given to the single-chip direct conversion receiver and the specifications of its embedded A/D converters, while the third-generation wide-band CDMA system is discussed in particular, as this is the target application.

5.1 Single-Chip Direct Conversion Receivers

The choice of receiver architecture depends on the system specifications and on the radio spectrum at all possible image frequencies of the mixers in the receiver. Furthermore, miniaturization and programmability by monolithic integration is strongly preferred to attain low cost, small power dissipation, and modularity. The most common super heterodyne receiver architecture requires external filters for RF image rejection and channel selection at the IF. Integration of those high-Q filters on the same die is not

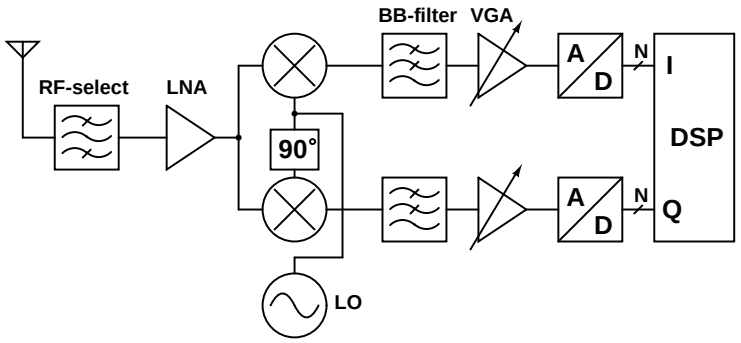

Figure 5.1 Block diagram of a direct conversion receiver.

feasible. Low-IF architecture [1] has been established to allow single-chip integration including channel selection filtering at the baseband (BB) and to avoid the DC-offset problems of the direct conversion architecture. However, this architecture requires good image suppression, which is limited by the phase and gain mismatches.

The direct conversion architecture has great potential for monolithic integration and avoids the image suppression problem—the image consists of the channel itself at zero IF. There is no need to drive external matched nodes, and the internal impedance levels can be optimized for maximal performance. However, the architecture has several drawbacks, a time varying DC-component originated from different noise and distortion sources being the most severe one, which must be considered in the design [3, 2, 4]. In Fig. 5.1 a block diagram of a direct conversion receiver is depicted. A preselection filter (RF-select) precedes a low-noise amplifier (LNA). Two quadrature downconversion mixers having a 90° phase shift in the local oscillator (LO) signal generate the in-phase (I) and quadrature (Q) components. The components have separate baseband filtering (BB-filter) and variable gain amplifiers (VGA) for channel selection and adjustment of the signal power before they are fed to the A/D converters. The signal is reconstructed and demodulated from the I and Q components using one or more digital signal processing (DSP) units, usually integrated on a separate die.

The main challenges, specific to the direct conversion receiver design, apply to the RF front-end and baseband circuitry. Analysis and solutions of these problems can be obtained from references [4, 5], and the following discussion includes only the topics related to the A/D converters.

5.1.1 Wide-Band CDMA

The target application in all the designs presented in this thesis is the third-generation wide-band code division multiple access (WCDMA) developed under the Third Generation Partnership Project, also referred as Universal Mobile Telecommunication Systems (UMTS) [6]. An overview of the standard was given in chapter 2. Additionally, extensions of frequency allocation are reserved for the second-generation personal communication system (PCS) and applied only in North America. When the experimental circuits included in this chapter were designed, optional extensions in the channel separation, signal bandwidth, and chip rate existed as well. Depending on the quality of the channel and type of the transferred data, the spreading factor varies between 4 and 256, the latter of which is for speech transmission. The modulation scheme applied in down-link is quadrature phase-shift keying (QPSK) and root raised cosine (RRC) filter with a roll-off factor of 0.22, while in up-link a more complex hybrid-QPSK is utilized.

5.2 Embedded A/D Converters of Direct Conversion Receivers

The most suitable A/D converter architectures for wide-band single-chip direct conversion receivers are $\Delta\Sigma$-modulators with low oversampling ratio, flash, and pipeline A/D converters. With the flash and pipeline architectures, no decimation filter is needed and the digital system clock can be used directly in the conversion. A lower clock frequency also reduces coupling of the clock signal to the RF input in addition to lower power dissipation in DSP. Compared to the flash architecture, the number of simultaneously switching substrate noise generating comparators is smaller in the pipeline ADC. Furthermore, a low power dissipation and small area can be obtained utilizing dynamic comparators and amplifier sharing in a medium-resolution pipeline ADC. Both $\Delta\Sigma$-modulators and pipeline ADCs allow adaptation of the resolution and sample rate in multi-standard receivers with small circuit modifications.

5.2.1 Resolution and Sample Rate

The resolution and sample rate of the A/D converters of a direct conversion receiver are determined by the receiver requirements defined in cellular standards, as referred to in detail in chapter 2. In general, the resolution is derived from the necessary dynamic range for signal detection and decoding with a signal-to-noise ratio that is sufficient for a given bit-error rate (BER), while the minimum sample rate is dictated by the signal

bandwidth. However, the dynamic range present at antenna is affected by the preselection filter, LNA, BB-filter and VGA, making the A/D converter resolution strongly dependent on the system design of the whole receiver. For the detection and decoding of the direct sequence spread-spectrum signal of WCDMA system a 4-bit resolution would be enough when the baseband circuit provides a large range VGA and the adjacent channel attenuation is sufficient [7]. In practice, leaving some headroom for a non-optimal DSP realization and relaxing the baseband dynamic range and linearity specifications, 6–8 bits of resolution is required implying an SNDR of 38–50 dB.

Nonlinearity is another point that relates to the resolution and performance of the A/D converter. For direct conversion receivers, it is usually characterized by the second-order (IP2) and third-order intercept points (IP3). The relation between the intercept points and the corresponding harmonic distortion components, which are more familiar terms in A/D converter characterization, was presented in chapter 2. Typically, in a direct conversion receiver, the linearity is limited by the RF and baseband parts. However, it should be confirmed that the A/D converter fulfills the specifications for the linearity parameters.

According to the sampling theorem, the sample rate must be at least twice the signal bandwidth, which is the same as the symbol or chip rate. Furthermore, to facilitate detection in the digital receiver and to simplify the symbol clock frequency error compensation, the sample rate should be some multiple of the symbol or chip rate, preferably four [8]. In the 3G WCDMA standard this implies a sample rate of 15.36 MS/s for the 3.84-Mcps chip rate.

5.2.2 Noise and Clock Distortion

In wide-band communications, interferers at single frequencies falling into the signal band deteriorate the signal-to-noise ratio (SNR) only a little. This property is further emphasized in systems employing the code division multiple access (CDMA), where narrow-band spurious signals will be spread over the band when the channel is decorrelated. Nevertheless, as the receiver gain is typically from 80 to 100 dB amplifying the weak signals at RF input to an appropriate level for the A/D converters, even a minor coupling of harmonics of the digital noise to the RF input might deteriorate the performance. High-speed digital signals require fast rise and fall times, which generate harmonics with significant amplitude up to the RF frequencies [9,10]. All digital signals are at frequencies that are sub-harmonics of the system clock. Thus, these phenomena can be referred to as clock distortion in mixed-signal radio receivers. The harmonic content and the leakage depend on several factors, which are difficult to predict. Substrate coupling, direct capacitive coupling between long metal lines on-chip and on the

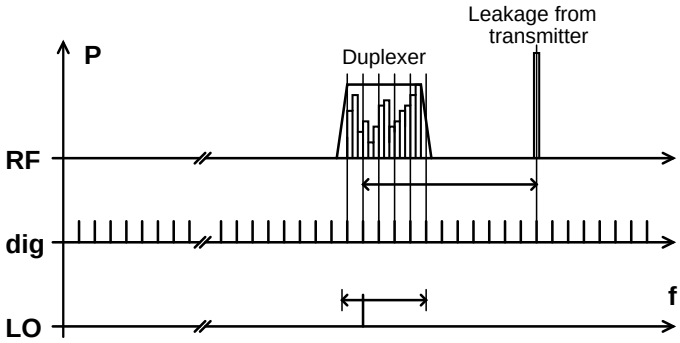

Figure 5.2 Spectra of the RF, digital, and LO signals. The range of possible LO frequencies and transmitter signal as a blocker are marked with arrows.

printed circuit board (PCB), inductive coupling between bondwires or package pins are all possible mechanisms for the unwanted leakage. Spurious tones can be generated at frequencies

$$f_{spur} = m f_{LO} \pm f_{block} \pm n f_{dig}, \tag{5.1}$$

where f_{LO} is the local oscillator frequency, f_{block} frequency of the blocker, and f_{dig} frequency of the digital signal, e.g. A/D converter clock. The signals and their conceptual harmonic components are shown in Fig. 5.2.

The system clock in a mixed-signal radio receiver operates typically at some multiple of the symbol rate, or chip rate in CDMA systems. The channel spacing must be somewhat larger than the chip rate to avoid leaking of the adjacent channel spectra with realizable filters. Hence, the system clock cannot be selected to be a sub-harmonic of the LO signal at all carrier frequencies, and at some channels the mixing products of the LO, clock, and their harmonics fall at the pass band of the channel selection filter. Based on Eq. 5.1, the frequencies of the potential spurious signals that fall on the signal band can be calculated and taken into account in the frequency planning. The spurious signal degrades the receiver sensitivity and noise figure. Isolation required between the digital noise source and sensitive node can be determined in terms of the allowed decrease in the sensitivity and noise figure [9].

Minimization of the substrate, capacitive, and inductive coupling of the digital noise to the sensitive nodes is one of the key issues in the design of an embedded A/D converter. Suppression of capacitive and inductive coupling is straightforward by increasing distance between the lines, pins, and bondwires and by reducing mutual inductance with orthogonality whenever possible [11]. Direct coupling between signal lines occurs between two adjacent, long on-chip metal lines of the same layer as well as in the crossing points of two lines. Parallel signal lines can be isolated by placing a thin ground

Figure 5.3 Isolation of (a) parallel and (b) crossing analog (Ana.) and digital (Digi.) signals using ground plate (GND) in between.

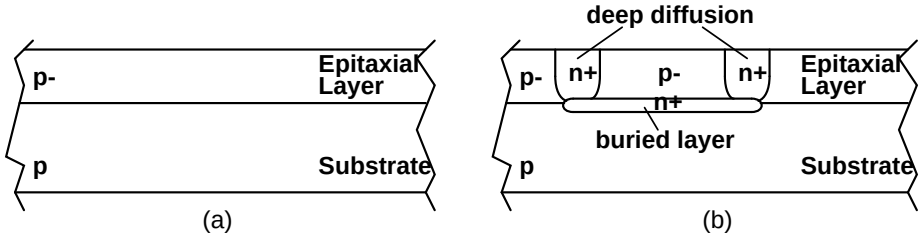

Figure 5.4 Cross section of (a) hybrid-substrate and (b) hybrid-substrate with separate p-well.

line on the same metal layer (M1) between them, as shown in Fig. 5.3(a). Crossing signals can be similarly decoupled using an intermediate metal layer (M2) ground plate vertically between the signal lines (M1 and M3), which is depicted in Fig. 5.3(b). The copper lines on the PCB are also very critical, as are the signal cables. Digital cables are typically unshielded bundles of wires acting like antennas and radiating digital noise, which can be received by the RF cables despite the fact that they are mostly shielded coaxial cables. Equally, the PCB can operate as a receiving antenna providing a path for noise coupling. In the worst case, the sensitivity of the receiver becomes dependent on the position and angle between the cables and printed circuit board.

Substrate coupling issues and floorplan strategies of mixed-signal circuits, an overview of which is given, for example, in references [12, 13], are issues of their own and cannot be handled in detail here. However, a coarse separation between the design and decoupling strategies can be made based on the type of the substrate; depending on the technology, the substrate is weakly or highly doped. In sub-micron CMOS processes almost unexceptionally highly doped p-type substrates covered by a weakly doped p-type epitaxial layer are employed [12, 14]. The transistors are processed into the epitaxial layer. A similar structure is also used in the modern BiCMOS technologies as well. A cross section of such a substrate structure is shown in Fig. 5.4(a). The shielding effect of the traditional guard rings around the sensitive and noisy transistors can prevent surface currents from flowing but, however, isolation is limited to a few decibels.

To effectively prevent the coupling, the sensitive and noisy circuits should be placed into separate isolated p-wells formed from the epitaxial substrate. This is easily accomplished with an n-type buried layer grown between the p-type substrate and epitaxial layer, together with deep n-type diffusions providing a connection to the buried layer as shown in Fig. 5.4(b). If the diffusions are contacted to the positive supply while the substrate is contacted to ground, two reverse biased pn-junctions then isolate the p-wells from each other, also vertically. It should be notified that all the transistors inside the isolated p-well should be connected to the same supply potential as the deep n-diffusions to prevent latch-up. Furthermore, since the diffusions carry noise, and vice versa provide a path for power supply noise to couple into the substrate, care must be taken in connecting them to an appropriate supply line. In BiCMOS processes similar structures are intrinsically available using the collector diffusion of an NPN transistor, while extra process steps are added to some deep sub-micron CMOS technologies to implement these isolation structures in mixed-signal circuits as well [14].

5.2.3 Interfaces

One of the biggest advances in single-chip receivers is the possibility of optimizing the interface between the receiver blocks; the internal impedance level can be freely selected, while buffering between the blocks eliminated. On the other hand, unbuffered internal interfaces restrict the circuit design since the impedance level, voltage swing, and driving capability between two consecutive blocks must be harmonized. Despite the restrictions, considerable benefit, especially in terms of power dissipation and area, can be obtained by eliminating the interstage buffers.

5.2.3.1 Input

The A/D converter input is provided by the baseband circuitry, a variable gain amplifier and low-pass filter, which are typically implemented with continuous time RC or g_mC techniques. The ADC voltage swing, and common mode level in differential designs, have thus to be adapted to the baseband output signal. A larger signal swing decreases linearity of the baseband, while in the A/D converter SNR is increased. The common mode voltage level of the ADC can be adjusted to follow that of the baseband output by controlling the voltage references [9] or the common mode voltages of the blocks can be made independent by using level shifting. The input impedance of a pipeline ADC, determined mainly by the first stage sampling capacitor, in turn sets the driving capacity requirement of the baseband circuitry and limits the maximization of the A/D converter SNR by increasing the size of the sampling capacitors. The continuous time baseband

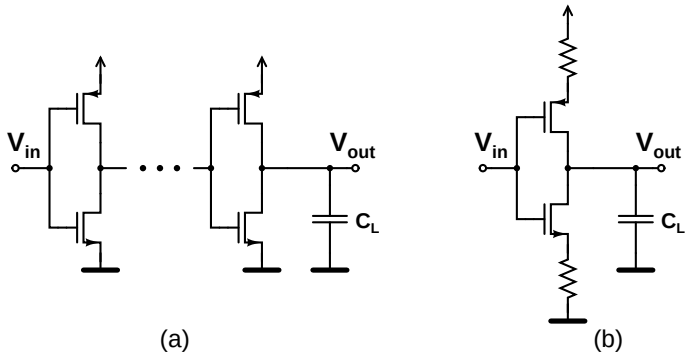

Figure 5.5 (a) CMOS output buffer in basic configuration and (b) low slew rate buffer.

output stage must provide enough current to charge and discharge the sampling capacitors of the first pipeline ADC stage with an acceptable linearity. Furthermore, the load of the baseband output is not constant but varies between the ADC clock phases, which indicates potential stability problems. To stabilize the load of the baseband, a dummy sampler with equal device sizes and operating in the opposite clock phase can be placed in parallel with the real ADC input [9].

5.2.3.2 Output

When the DSP blocks are implemented on separate chips, the A/D converter outputs drive large off-chip capacitive loads making their buffering inevitable. The load at the output is dependent on the package and usually not well-defined, implying overhead in the driving capacity of the output buffers. In standard logic cell libraries the output buffers are realized using cascaded CMOS inverters, shown in Fig. 5.5(a), which provide sharp rail-to-rail voltage signals. Thus, the output buffers and the following bondwires are potential sources of large substrate noise and inductive coupling contributions. The biggest disadvantage of CMOS logic in terms of disturbances is inherited from the large current spikes drawn from the power supplies during the switching. Current spikes result in a drop of the supply voltage because of the non-zero resistance of the supply lines generating both substrate and power supply noise, especially in a mixed-signal circuit with a common supply for the analog and digital parts. This phenomenon is known as ground bounce.

Output buffer topologies other than CMOS inverters, e.g. current mode circuits, provide better performance in this sense, but their utilization is often not possible owing to incompatible logic levels or excess in the design time and effort. Nevertheless, the current drain of a CMOS inverter can be reduced by, for example, reducing its slew

rate. This can be accomplished by having resistors in series with the supply line connections to squeeze the current path and to increase the rise and fall times as depicted in Fig. 5.5(b). In practice, the resistors are implemented with transistors, which are biased in the linear region. To reduce substrate noise generation, the digital power supply lines should not be used to provide the bulk connections in the logic; to do this dedicated low-noise lines requiring custom design are preferred. Separate supply lines and pads for the output buffers, at least on-chip, with large decoupling capacitors are also very effective in minimizing power supply noise.

5.2.4 Power Dissipation and Area

When increasing integration density, minimization of power dissipation and area are essential. Design and optimization for low power is not only an issue in circuits aimed for handheld equipment because of several reasons. First, with increasing the level of integration, power density is simultaneously increased radically, which leads to a rise in the temperature of the silicon die. To avoid a decrease in performance and reliability, the produced heat must be lead out through the package, which sets high requirements for packaging and assembly of the chip, thus affecting the costs. Second, the higher the power consumption, the larger the power supply noise in general. This is because of the crosstalk between the increased number of bondwires and metal lines. Furthermore, a high number of power supply pads increases the area and thus the costs.

The desire to minimize area results mainly from considerations of cost effectiveness. Even though a single-chip solution reduces the component assembly, logistic, and storage costs compared to a solution with several off-chip components, a custom integrated circuit is always an expensive component. Thus, the A/D converters of I and Q branches of a direct conversion receiver should occupy minimal silicon area. As discussed in chapter 2, pipeline ADCs tend to have fairly low area efficiency because of the capacitors. However, by optimizing the pipeline architecture for low area, very small 6–8-bit A/D converters can be realized. Even though, the A/D converters present only a small part of the receiver total area and power consumption [5, 15], their optimization is extremely important.

Minimization of power usually leads to minimal area also. It is well known, that the largest savings in both power and area can be obtained by optimization at the architectural level—the smallest at the transistor level. In pipeline A/D converters, the property of consecutive stages operating in opposite clock phases can be exploited by sharing as many circuit blocks as possible between the two serial stages. For example, the operational amplifier of the MDAC is used only in the hold mode, which enables amplifier sharing between two stages [16]. One sub-ADC can also be alternated be-

tween two stages. Furthermore, as the accuracy requirement of the back-end stages is reduced by the gain of the preceding stages, less accurate amplifier settling, larger capacitor mismatch, and higher thermal noise contribution are allowed when proceeding from towards the least significant stages. This enables scaling of the capacitors and transistor sizes of the operational amplifiers [17]. Additionally, power and area minimization at the circuit level can be employed, by using, for example, low-power opamps and dynamic comparators. Optimization of the pipeline A/D converter architecture for small area and low power is discussed in more detail in chapter 6.

5.3 Reconfigurable Pipeline A/D Converters

The trend towards an increasing variety of different standards employed in communication applications, demands radio receivers that can be adapted to operate over a variety of specifications. To maintain the cost benefit and flexibility of such a multi-standard receiver, area and power dissipation should be minimized by having the receiver circuit blocks electrically reconfigurable with as few extra components as possible. For analog-to-digital converters, the requirement is manifested as adaptation of the resolution, sample rate and power dissipation on the specifications of several standards. A single A/D converter with a reconfigurable topology and performance would be able to achieve this goal.

The ADC architectures, like flash, pipeline, cyclic, and $\Delta\Sigma$-converters, work optimally only at a narrow range of resolution, bandwidth, and power. A sophisticated solution to cover a wide resolution and bandwidth range is to combine these topologies in a single ADC. The similarity of the realization of an SC resonator circuit in a $\Delta\Sigma$-converter and the MDAC of a pipeline ADC has been exploited by morphing the converter into the $\Delta\Sigma$-topology when high resolution is required, and into the pipeline topology if a medium-resolution with high bandwidth is needed [18]. If only a limited resolution and bandwidth configurability is desired, the requirements can be achieved by adapting the building blocks within a single ADC architecture. Examples of such converters include a cyclic A/D converter that can be configured for 8, 13, or 16 bits of resolution [19] and a flash ADC with two settings [20].

The pipeline A/D converter topology has inherently great potential for reconfiguration because of its modular structure; the resolution can be configured by varying the number of the cascaded low-resolution stages, while the current consumption of the MDAC amplifiers can be adapted to the sample rate. The applicable resolution and sample rate range of pipeline A/D converters vary from 6 bits and hundreds of megahertz to 15 bits and a few megahertz, as pointed out in chapter 2.

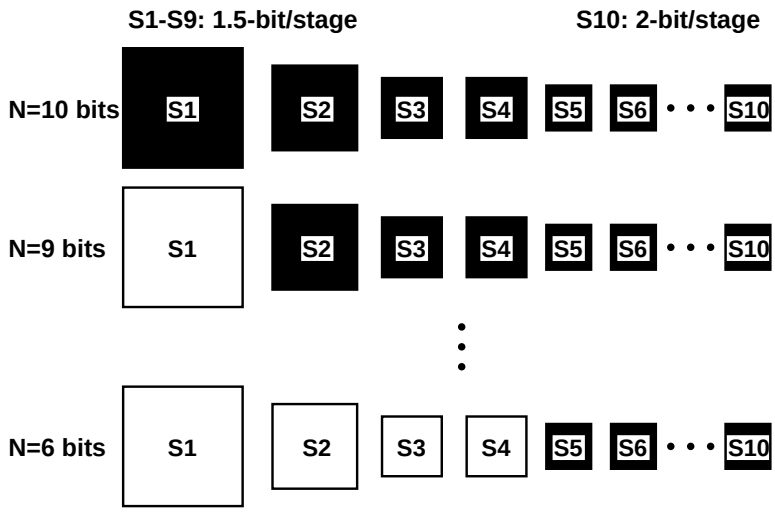

Figure 5.6 Resolution variation in a 6–10-bit pipeline ADC.

5.3.1 Resolution

Configuration of the resolution in a pipeline A/D converter can be implemented simply by varying the number of the stages. The principle of the resolution variation in a pipeline ADC for resolutions of 6, 7, 8, 9, or 10 bits is conceptually depicted in Fig. 5.6. Configuration in the three resolution modes is indicated by black active stages and white non-functional stages. The converter employs RSD correction and consists of nine 1.5-bit stages, with the last stage being a 2-bit flash, all of which when activated corresponds to the configuration in the highest 10-bit resolution mode. As discussed in chapter 3, the first pipeline stage has the strictest requirements in terms of the settling accuracy of the MDAC output and thermal kT/C-noise. The specifications of the following stages are relaxed by a factor equal to the value of the interstage gain. To minimize power dissipation, capacitor and amplifier scaling is employed by a factor of 1/2 between the stages S1, S2, and S3, as well as between S4 and S5, which is indicated by the different sizes of the boxes in Fig. 5.6. As a result, the power dissipation is also scaled down roughly with the same factor. In the 9-bit mode, twice as much noise is tolerated as in the 10-bit mode, which explains the shift of the first stage from stage S1 to S2 between these modes. Similarly, to minimize the power in each mode, shifting of the first stage is performed until stage S5, which acts as the first stage in the 6-bit mode. The inactive stages can be switched off.

In practice, there are several restrictions that limit the reconfigurability of a pipeline ADC, especially at high resolutions. Parallel or series switches, which reduce the per-

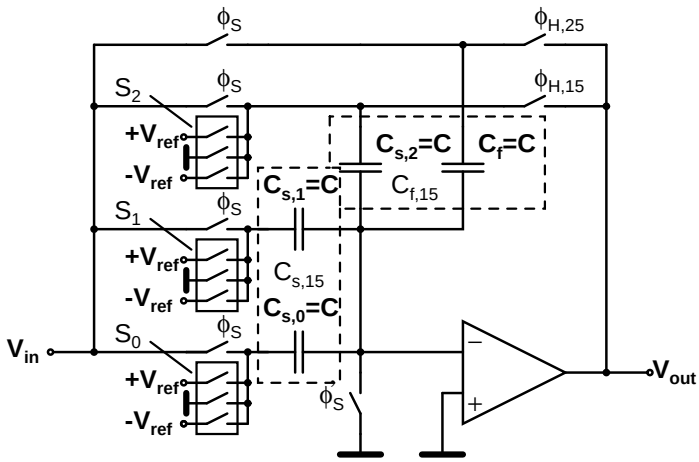

Figure 5.7 Reconfigurable MDAC for 1.5-bit and 2.5-bit operation.

formance, have to be added in or between the stages to realize the selection of the first stage. As the input of the first stage is the most critical point in the analog signal path, it is sometimes preferable to overtake some stages somewhere in the middle or at the end of the chain rather than shift the first stage. Switching between the configurations also requires some clock cycles settling time before the stages that were powered down reach their operation points.

An alternative approach to make the resolution of a pipeline A/D converter adaptive, is to reconfigure the resolution of a single stage. An example of a reconfigurable unit capacitor MDAC employing 1.5-bit and 2.5-bit operation is shown in Fig. 5.7. When operating at the 1.5-bit resolution the capacitors $C_{s,0}$ and $C_{s,1}$ are acting as a single sampling capacitor $C_{s,15}$ and the reference switches in S_0 and S_1 operate identically. Similarly, the capacitors $C_{s,2}$ and C_f are tied together forming one feedback capacitor $C_{f,15}$, which is accomplished by making the reference switches in S_2 inactive and activating the feedback switch with clock phase $\phi_{H,15}$. In the 2.5-bit resolution mode, all the unit capacitors are separated and the reference switches in S_2 are controlled by the sub-ADC, while the feedback switch with clock phase $\phi_{H,15}$ is inactive. In order to get any benefit in power dissipation, the quiescent current of the operational amplifier must also be scalable. When changing the amplifier bias current, load, and feedback factor, care must be taken that the opamp maintains its operation point, and, in the case of a two-stage amplifier, the stability as well. Adaptation of the frequency compensation of a Miller amplifier can be realized with, for example, a switched compensation capacitor [21]. Another drawback of reconfigurable stages is that the sub-ADC and digital part, including the RSD correction, must also adapt to all possible stage resolutions.

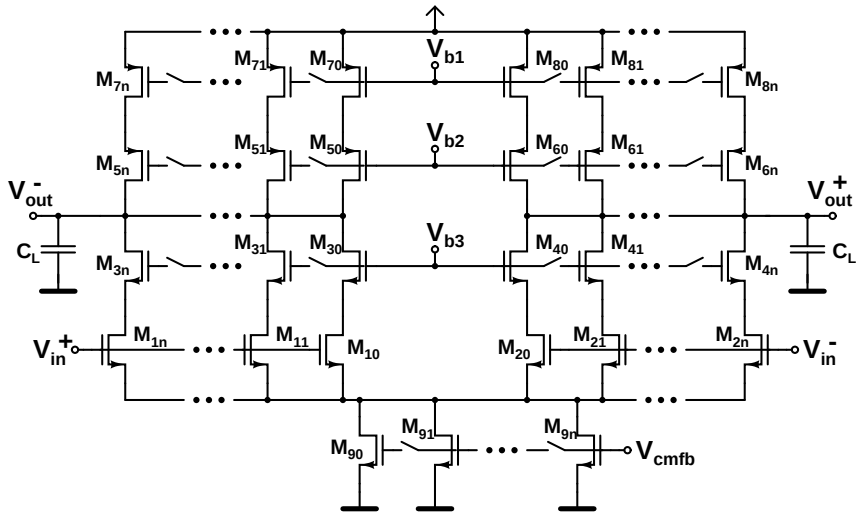

Figure 5.8 Reconfigurable telescopic cascode amplifier.

5.3.2 Sample Rate

Adaptation of the power dissipation to the changes in the signal bandwidth, i.e. in the sample rate, can be achieved by altering the operational amplifier quiescent currents accordingly. Bias current of the opamps can be made to track the changes in the clock frequency automatically by utilizing a phased locked loop (PLL) with a voltage controlled oscillator (VCO) [18]. As mentioned above, changing the opamp bias current leads easily to problems in maintaining the correct operation point and stability.

Adaptation of the amplifier to different bias currents can be accomplished by constructing the opamp from several amplifiers employing scaled transistor dimensions and having the possibility to be connected in parallel. A telescopic cascode amplifier consisting of parallel amplifiers that can be activated by switching the bias voltages on and off on the transistor gates, is conceptually depicted in Fig. 5.8. The excess in area is very small compared to an amplifier corresponding to the configuration where all the parallel amplifiers are activated. No first order stability problems result, while a single biasing circuit and one common mode feedback circuit can generate the required voltages V_{b1}–V_{b3}, and V_{cmfb}.

In order to gain more power savings, other blocks, the bias current of which scales with the sample rate, can also be made reconfigurable. Such blocks include the reference voltage generator, clock generator with its buffers, digital output buffers, etc.

5.4 Application Case I: A Single-Amplifier 6-bit CMOS Pipeline A/D Converter for WCDMA Receivers

5.4.1 Introduction

Mobile internet is currently available in extended narrow-band cellular systems but the wider channel bandwidths in the third-generation systems will further improve multimedia services and capacity. The direct conversion receiver is a distinct alternative to wide-band direct sequence CDMA systems allowing a high degree of integration. However, the wide bandwidth in the 3.84-Mcps transmission easily leads to high power consumption, especially in the A/D converters (ADCs). Single-chip receivers including digital blocks on the same die with the RF and baseband analog blocks are sensitive to clock feedthrough to the RF input. Only a few millivolts of clock distortion are acceptable at the output of the receiver having almost a 100 dB of gain. Thus, a very low substrate noise generation of the ADCs, and an extremely good isolation between the analog and digital blocks are required even in CDMA systems.

$\Delta\Sigma$-converters with a low oversampling ratio and pipeline A/D converters are the most attractive ADC architectures for single-chip WCDMA receivers, especially in CMOS. By using a simple redundant sign digit (RSD) error correction, which allows the use of low-power dynamic comparators, by optimizing the stage resolution for power and by sharing the operational amplifier with two stages make it possible to implement a pipeline ADC with very low power dissipation and area. In the pipeline architecture no decimation filter is needed and the digital system clock can directly be used in the conversion. Furthermore, with an advanced circuit topology design, good isolation and decoupling structures and careful layout design coupling of the clock signal into the sensitive RF input can be made almost insignificant in single-chip solutions.

The 6-bit 15.36-MS/s A/D converter presented is a part of a single-chip direct conversion receiver for 3G WCDMA, which includes two ADCs, for I and Q channels [5].

5.4.2 Circuit Description

The two 6-bit 15.36-MS/s CMOS pipeline A/D converters for the I and Q channels are implemented using two 2.5-bit (three bits minus one level) stages followed by a 2-bit flash, as indicated in the block diagram of Fig. 5.9. Each 2.5-bit stage consists of a multiplying D/A converter (MDAC) and sub-ADC with a small decoding logic. The properly delayed output bits of each stage are fed to an RSD correction circuitry [22] and finally buffered out of the chip in parallel. The two A/D converters have a common on-chip current reference and share a one-stage clock amplifier.

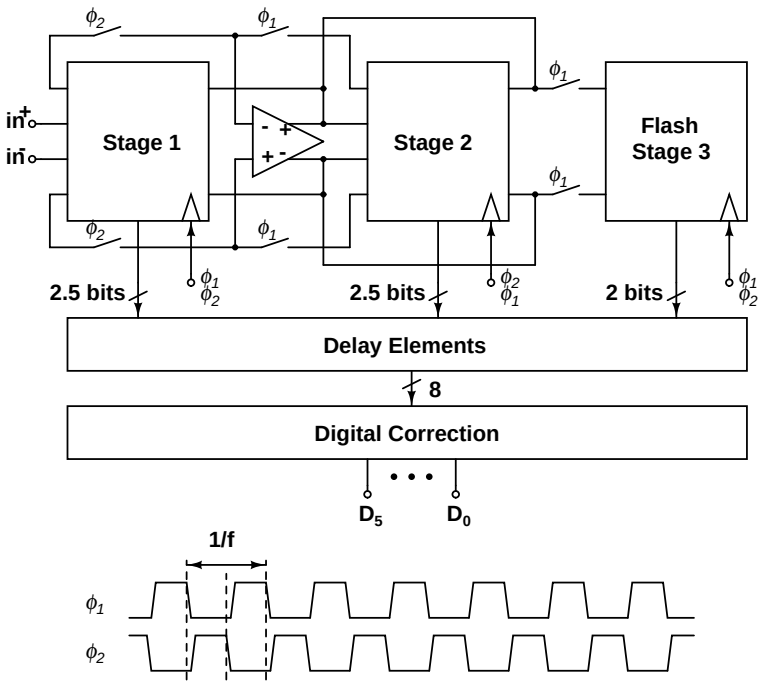

Figure 5.9 Block diagram and timing of the ADC.

5.4.2.1 Amplifier Sharing

After examining the settling of the output of a switch capacitor (SC) pipeline stage, it can be concluded that at low sample rates a high stage resolution minimizes the amplifier current consumption. On the other hand, the number of comparators and their offset requirement grow squarely with the stage resolution [23]. With the 2.5 bits/stage architecture, two pipeline stages with nominally two amplifiers are required, in addition to fifteen comparators. To reduce power dissipation, the property of successive pipeline stages working in opposite clock phases can be exploited by alternating one operational amplifier between the two cascaded stages [16]; while the first stage samples the input during phase (ϕ_1), the second stage is in the hold mode during phase (ϕ_2), using the common amplifier and vice versa, as depicted in Fig. 5.9. The price paid is the need for two extra switches per stage and a minor growth in the amplifier load capacitance. Both pipeline stages have their own sub-ADCs, keeping the number of comparators at fifteen.

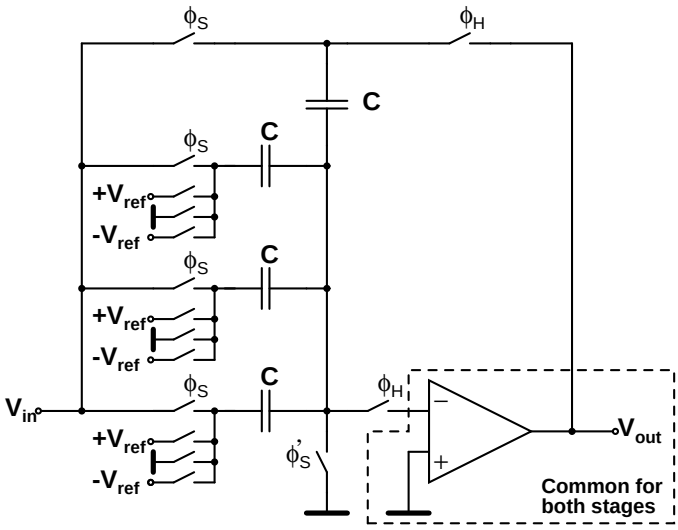

Figure 5.10 2.5-bit MDAC of the pipeline stage.

5.4.2.2 Multiplying D/A Converter (MDAC)

The capacitive MDAC of the pipeline stage is shown in Fig. 5.10 as a single-ended configuration for simplicity. Input signal is sampled into the four equal capacitors during the sample phase (ϕ_S) while the amplifier is disconnected. In the hold mode (ϕ_H) one of the capacitors is in feedback and the three other capacitors are connected to $-V_{ref}$, 0 or $+V_{ref}$ according to the output of the sub-ADC giving a transfer function

$$V_{out} = 4 \cdot V_{in} - D_{sub} \cdot V_{ref}, \tag{5.2}$$

where D_{sub} is an integer between $-3 \ldots 3$, according to the binary sub-ADC outputs $000 \ldots 110$, respectively.

The two MDACs share a common telescopic cascode amplifier with an SC common mode feedback circuit. With this topology, high DC-gain and large bandwidth are achieved with low current consumption. A nominal open loop DC-gain of 62 dB and a GBW of 250 MHz are achieved with a 1.2-V_{pp} differential signal swing.

5.4.2.3 Differential Pair Dynamic Comparator

The sub-ADCs of the 2.5-bit pipeline stages are of flash type and consist of six comparators. The comparators drive the switches of the MDAC and a small decoding logic that converts the thermometer code into binary output. The low stage resolution, together with the RSD correction, relaxes the offset voltage specification. This in turn

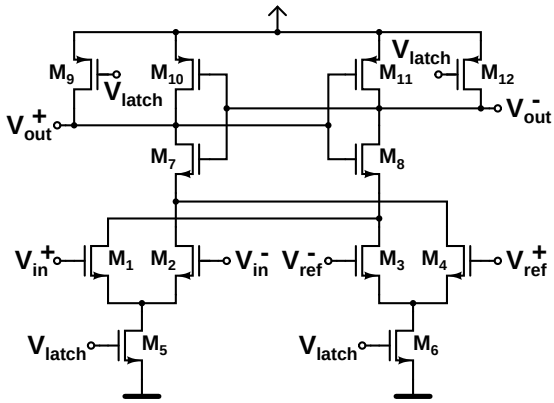

Figure 5.11 Differential pair dynamic comparator.

allows the use of dynamic comparators, which consume no DC-power. The sub-ADCs utilize a differential pair dynamic comparator of Fig. 5.11, which is very insensitive to mismatches. It is based on two cross-coupled differential pairs with switching current sources. A CMOS latch is connected directly over the source-coupled pairs and the outputs are buffered with small inverters [24]. According to simulations transistor mismatches up to 20 % result in offset voltages less than 20 mV, which clearly fulfills the specification of $\pm V_{ref}/8$.

The eight reference voltages needed in A/D conversion (V_{refp5}, V_{refp3}, V_{refp1}, V_{refm1}, V_{refm3}, V_{refm5}) and D/A conversion (V_{refp} and V_{refm}) are generated with the resistor string shown in Fig. 5.12. The reference voltages are adjusted to follow the reference analog ground voltage (V_{agnd}) by setting the resistor string as a part of the output stage of a Miller compensated amplifier, which additionally guarantees a fast settling of the references. The circuitry of Fig. 5.12 also keeps the accuracy of the reference levels within the 6-bit resolution when the supply voltage alters between 2.7–3.0 V.

5.4.2.4 Substrate Noise Reduction

Because of the sensitivity of the LNA input to clock feedthrough, special attention had to be paid to the isolation between analog and digital blocks. The contribution of the ADCs to the substrate noise is reduced by using a differential sinusoidal clock input with a low amplitude, which is amplified with a single-stage differential pair amplifier. The complementary outputs of the amplifier are sharpened into rail-to-rail clock signals with three cascaded inverters and fed to the ADCs of the I and Q channel. The non-overlapping clock signals and the corresponding control signals for the sampling switches of the MDACs with earlier falling edges, needed for the odd and even pipeline

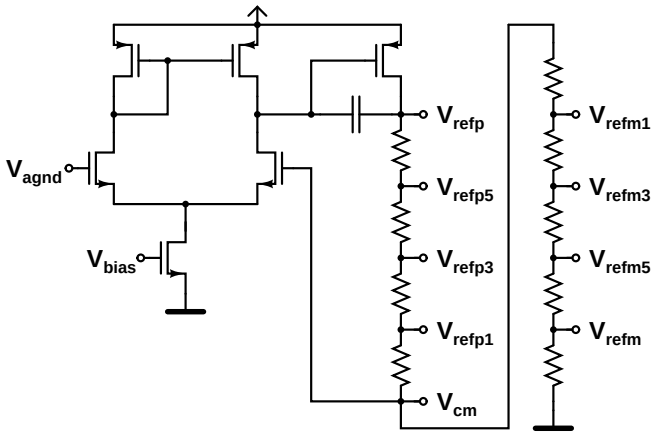

Figure 5.12 Reference circuit.

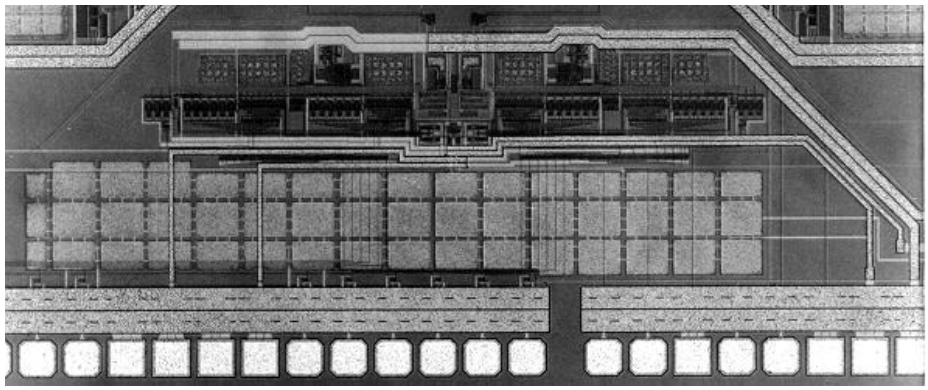

Figure 5.13 Chip microphotograph.

stages, are generated in the ADCs with separate clock generator circuits.

All digital blocks are isolated into separate p-wells exploiting the triple well process. The output buffers are designed to have low rise and fall times to reduce the power supply and substrate noise. There are three separate supply voltages, for the analog and digital blocks and the output buffers have an own supply line. Further power supply noise reduction is attained by using large on-chip decoupling capacitors in the supply voltage lines. The largest clock spurious at the output of the single-chip receiver is smaller than 20 mV, causing less than 0.1-dB degradation in the total noise figure of the receiver [5].

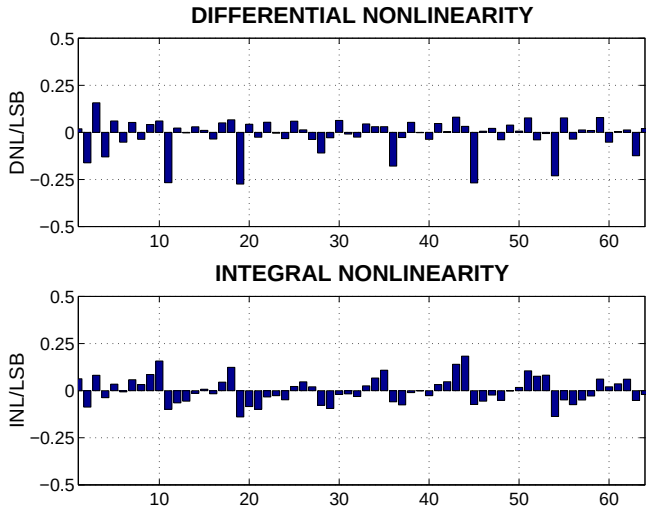

Figure 5.14 Measured DNL and INL as a function of code.

5.4.3 Experimental Results

A prototype circuit is fabricated using a 0.35-μm BiCMOS process with only CMOS transistors used. The total active area of the two ADCs is 0.45 mm^2 and the die photo is shown in Fig. 5.13. The ADCs are designed to be driven directly by the baseband circuitry without any buffering. The following measurements are performed by using a sinusoidal input from an external signal generator, while all the other receiver blocks are switched off. The DNL and INL, shown in Fig. 5.14, were found with the code density test to be 0.27 LSB and 0.18 LSB, respectively.

The SFDR of the converter was measured with the FFT-characterization. An example spectrum with a 7.03-MHz input at 15.36-MS/s sample rate is shown in Fig. 5.15. The SFDR is limited by the third-order distortion and it was found to be more than 50 dB over the whole Nyquist band, while the THD is better than 46 dB in the same range, as indicated in Fig. 5.16. The SNDR, determined using sine wave fitting, is very flat being better than 38 dB, which corresponds to an ENOB of 5.8 bits. Although the nominal sample rate of the ADC was set to 15.36 MS/s, in Fig. 5.17 the SFDR and THD are plotted for sample rates up to 43 MS/s for a 3.02-MHz input signal. The figure shows that the THD of the A/D converter is better than 40 dB up to 36 MS/s. The ADC worked properly up to a 45-MS/s clock rate. In Fig. 5.18, the SNDR is plotted as a function of the input power.

The measured current consumption of the I and Q channel ADCs together is 4.5 mA from a 2.7 V supply, giving a total power dissipation of 12 mW. The measured perfor-

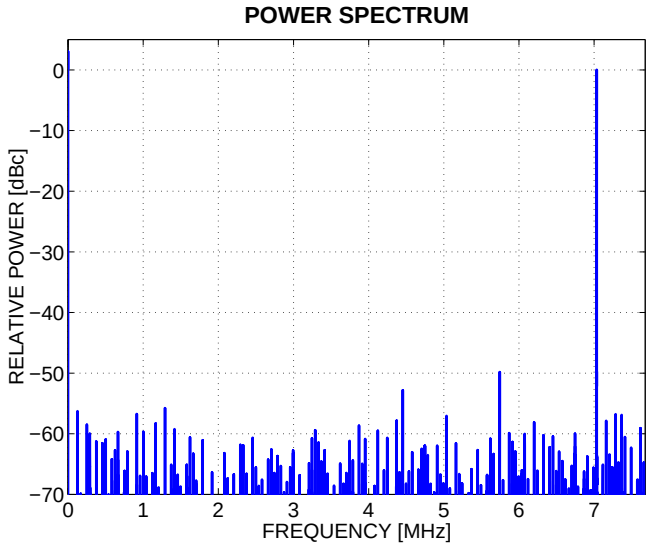

Figure 5.15 Example ADC output spectrum with 7.03-MHz input signal at 15.36-MS/s sample rate.

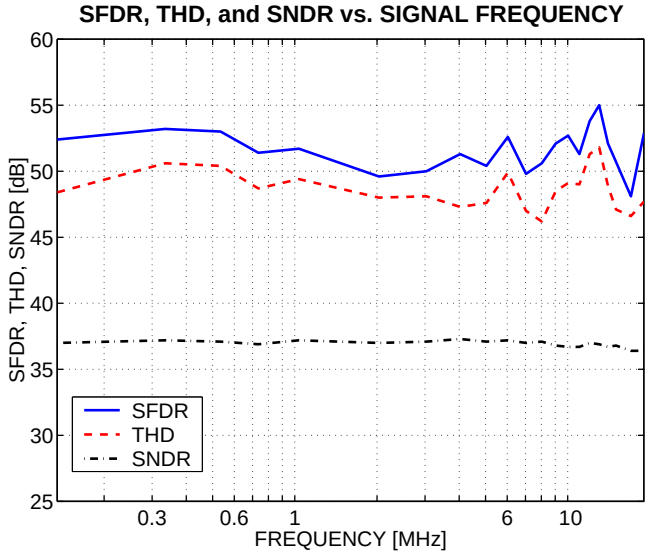

Figure 5.16 SFDR, THD, and SNDR as functions of the signal frequency at 15.36 MS/s.

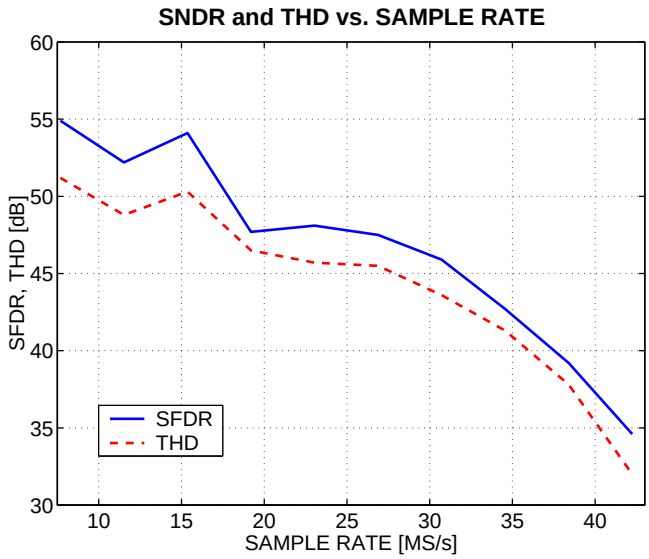

Figure 5.17 SFDR and THD as functions of the sample rate with 3.02-MHz signal.

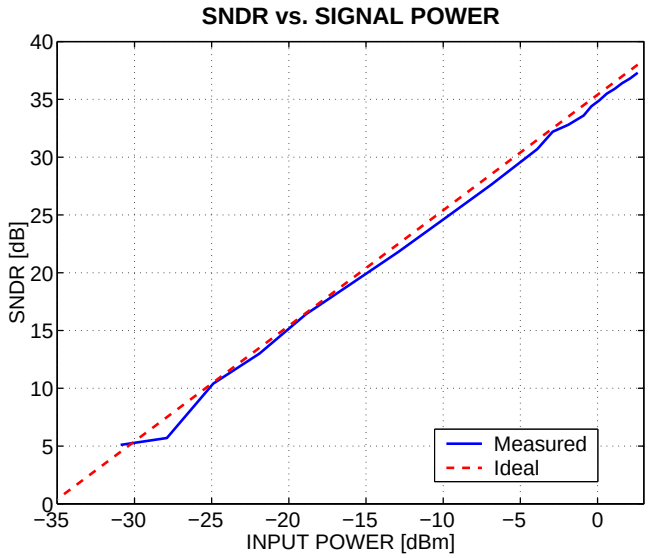

Figure 5.18 SNDR as a function of the signal frequency with 4.02-MHz signal.

Table 5.1 Measured results of the A/D converter.

Resolution	6 bits
Nominal Conversion Rate	15.36 MS/s
Differential Input Voltage	1.2 V_{pp}
DNL	0.27 LSB
INL	0.18 LSB
SFDR	50 dB
THD	46 dB
SNDR	38 dB
ENOB	5.8 bits
Power Dissipation @ 2.7 V*	12 mW
E_{conv}	6.1 pJ
Active Area*	1.42 x 0.32 mm^2

*)I and Q channel ADCs together

mance is summarized in Tab. 5.1.

5.4.4 Conclusions

An embedded single-amplifier 6-bit CMOS pipeline ADC for a single-chip 3G WCDMA receiver was presented. Sharing of the amplifier of successive stages and utilizing a mismatch insensitive dynamic comparator have enabled suppression of the power consumption to 12 mW for the two ADCs. The prototype 6-bit 15.36-MS/s pipeline ADC achieves a DNL and INL of 0.27 LSB and 0.18 LSB while the SFDR and SNDR are 50 dB and 36 dB, respectively.

The studies and results presented in this section have been published in [5, 25].

5.5 Application Case II: A Dual-Mode Pipeline A/D Converter for Direct Conversion Receivers

5.5.1 Introduction

Third-generation (3G) systems are currently being utilized. However, high costs of the required new infrastructure will keep the second-generation (2G) cellular systems coexisting, at least in rural areas—a need for multi-mode transceivers is evident. In order to keep the size, cost, and power dissipation of such devices attractively low, as many building blocks as possible must be shared between different systems, also in the analog front-end. The direct-conversion receiver architecture offers high integration density and adaptation capability. Reconfigurable analog-to-digital converters (ADCs)

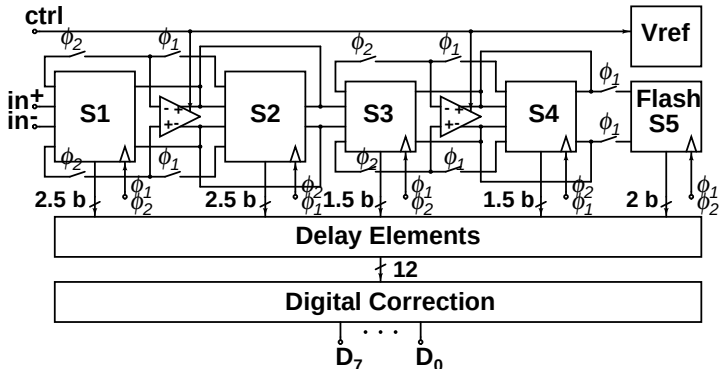

Figure 5.19 Block diagram of the dual-mode pipeline ADC.

with variable sample rate, even with exchangeable resolution, are key building blocks in multi-mode radio receivers.

The pipeline ADC architecture is inherently suitable for reconfiguration because of its modular structure [22]. Minimization of the current dissipation can be realized by optimizing the resolution partitioning and employing scaling between the stages, by using dynamic comparators, and by applying amplifier sharing within two consecutive stages. The relaxed settling time specification of the 200-kHz narrow-band signal compared to the 3.84-MHz wide-band channel, can be exploited by utilizing adaptive operational amplifiers (opamps) and a reconfigurable voltage reference circuit. With a reconfigurable multi-mode analog front-end preceding the ADCs, the dynamic range requirement for the ADCs corresponds to 8-bit resolution in both modes.

5.5.2 Circuit Description

A block diagram of the dual-mode 8-bit 1/15.36-MS/s CMOS pipeline ADC is shown in Fig. 5.19. The first two stages have a resolution of 2.5 bits, while the next two are 1.5-bit stages and the last one is a 2-bit flash ADC. Each pipeline stage consists of a multiplying D/A converter (MDAC) and sub-ADC. The output bits of the stages are delayed properly in a shift register and fed to the redundant sign digit (RSD) correction circuitry [22]. The architecture is optimized for low power dissipation, which is explained as follows. It has been shown that in a medium-resolution pipeline ADC, a high stage resolution minimizes the total amplifier power dissipation at low sample rate [23]. On the other hand, the number of comparators in the sub-ADCs increases exponentially with increasing stage resolution. Furthermore, despite the relaxed comparator accuracy requirements owing to the RSD correction, the offset of the no DC-power consuming dynamic comparators sets limitations for the stage resolution. The adjacent

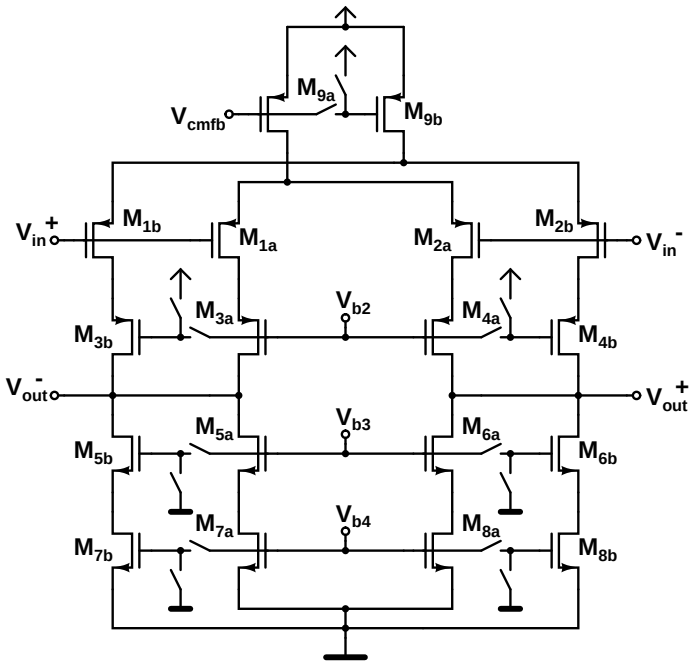

Figure 5.20 Proposed reconfigurable telescopic cascode amplifier.

stages operate in opposite clock phases using the opamp only in the hold mode, which allows a single amplifier to alternate between two consecutive stages [16]. By having two 2.5-bit stages, which share one opamp, in the front and two 1.5-bit stages with downscaled dimensioning in the shared amplifier and capacitor sizes, only two opamps and 19 loosely specified comparators. All the stages have separate sub-ADCs because the dynamic comparator occupies a very small area and dissipates power only when latched.

The circuit blocks of a pipeline ADC, the requirements and power dissipation of which are strongly dependent on the sample rate, are the opamps and the voltage reference circuitry; power dissipation of dynamic comparators and CMOS logic scales inherently with the clock frequency. The operational amplifier topology was selected to be based on the telescopic cascode amplifier, because of its low current consumption, high DC-gain, and large gain bandwidth (GBW). A differential signal swing of ± 0.6 V was achieved. Adaptation of the amplifier GBW to the according sample rate of the GSM and WCDMA modes is realized by constructing both opamps actually of two parallel amplifiers, as indicated in Fig. 5.20. In the GSM mode, the outer amplifier is powered down by connecting the cascode and current source transistors M_{3b}– M_{9b} either to the positive supply or ground voltage. The amplifier GBW is raised roughly

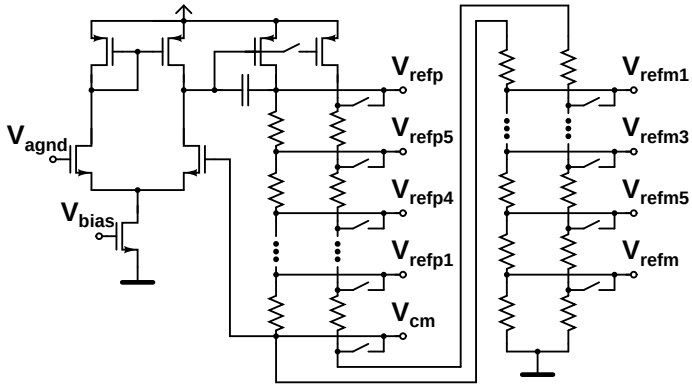

Figure 5.21 Dual-mode reference voltages generating circuits.

a decade in the WCDMA mode by connecting the outer transistors, the dimensions of which correspond to nine times the W/L-relation of that of the inner counterparts, in parallel with the inner amplifier. The bias circuit of the amplifier remains unchanged within both operation modes. Thereby, the current density is kept constant in both configurations, which in turn maintains the operating points constant. Furthermore, the series switches in the transistor gates introduce no stability problems. A standard switched capacitor type common mode feedback circuit is employed in the opamps, and the bias current and transistor dimensions of the opamp of the 1.5-bit stages are scaled down with a factor of four.

The reference circuit, generating the reference voltages for the comparators (V_{refmn}, V_{refpn}, n=1...5) and for the MDACs (V_{refm}, V_{refp}), is realized by placing a resistor string as a part of the output stage of a Miller compensated amplifier, shown in Fig. 5.21. The circuit keeps the reference voltages within the 8-bit accuracy under the variations of the supply voltage, and of the 1.1-V analog ground voltage (V_{agnd}), generated in a band-gap voltage reference. The over a decade longer settling time in the narrow-band mode is exploited by splitting the resistor string into two parts with the switches shown in Fig. 5.21. In the GSM mode only, the string with a total resistance of 11.2 kΩ is activated, while, in the WCDMA mode, the 2.8-kΩ string is switched in parallel to the larger string. To guarantee proper operation, the tap switches must have significantly lower on-resistances than the corresponding resistor string impedance. The compensation capacitor is dimensioned as a compromise of the stability requirements of both modes. Selection of the operation mode, in both the opamps and reference circuitry, is accomplished by a one-bit control signal.

Two dual-mode 8-bit 1/15.36-MS/s pipeline ADCs, for the I and Q branches of a single-chip quad-mode direct conversion receiver, were designed. A differential sinu-

Table 5.2 Simulated performance of the A/D converters.

	GSM Mode	WCDMA Mode
Resolution	8 bits	
Sample Rate	1 MS/s	15.36 MS/s
Diff. Input Swing	$\pm$ 0.6 V	
SFDR	54 dB	58 dB
SNDR	47 dB	49 dB
ENOB	7.5 bits	7.8 bits
Current Dissipation	1.7 mA	6.2 mA
Supply Voltage	2.7 ... 3.0 V	
Technology	0.35-μm CMOS	

soidal clock signal was led to a common clock amplifier, where it is recovered into a rail-to-rail digital clock for the clock generators of both ADCs. A total of seven bias currents of the two ADCs were mirrored from one on-chip current reference. The resulting 8+8-bit RSD corrected data is led out off the chip in parallel. The technology employed was a 0.35-μm BiCMOS process, with only CMOS transistors used.

5.5.3 Simulation Results

Simulations for the designed pipeline ADCs were performed at transistor level using a sample rate of 15.36 MS/s in the WCDMA mode and 1 MS/s in the GSM mode with a 2.7-V supply. The performance of the ADCs is summarized in Tab. 5.2. According to the simulations, the ADCs achieve a spurious free dynamic range (SFDR) of more than 54 dB over the whole Nyquist band in both modes. Example spectra with a 1.99-MHz signal in the WCDMA mode and 97.2-kHz in the GSM mode are shown in Fig. 5.22. The signal-to-noise and distortion ratios (SNDR) achieved correspond to a number of effective bits (ENOB) better than 7.5 bits. The total current consumption of the ADCs of the I and Q channels, including the output buffers with 0.4-pF external load, is only 6.2 mA in the WCDMA mode and reduces to 1.7 mA in the GSM mode.

5.5.4 Conclusions

A dual-mode 8-bit 1/15.36-MS/s pipeline ADC was presented. A very low power dissipation was achieved by optimization of the architecture and utilization of a reconfigurable opamp and reference circuitry.

The studies and results presented in this section have been published in [26].

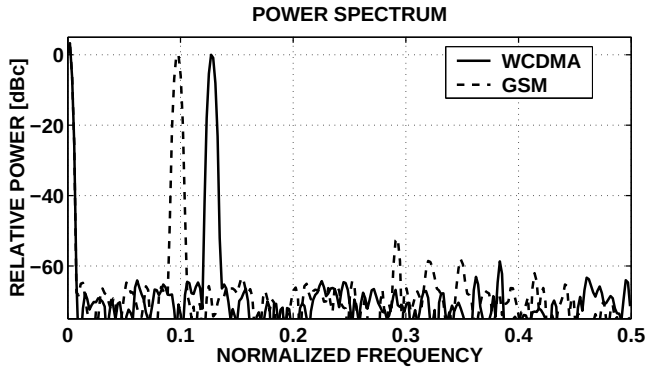

Figure 5.22 Example spectra in GSM (1 MS/s) and WCDMA (15.36 MS/s) modes.

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Chapter 6

Parallel Pipeline A/D Converters

An effective way to increase the throughput of a pipeline A/D converter is to introduce parallelism by placing several pipeline ADCs, operating at a fraction of the total sample rate of the ADC, in a time-interleaved configuration [1, 2]. However, mismatch in the offset, gain, and timing of the channel ADCs introduce unwanted spectral tones and side-bands, which must be controlled or compensated. Utilization of parallelism brings an additional design parameter in terms of minimization of the power and area dissipation as a function of the degree of parallelism. To attain further area and power savings, circuit blocks can be shared across the channels.

In this chapter, the concept of the parallel time-interleaved pipeline A/D converter is presented, including the effects inherited from mismatch in the parallel analog signal processing. Also, a method to minimize the power by optimizing the number of parallel channels and stage resolution as a function of the sample rate is introduced.

6.1 Time-Interleaved Parallel Pipeline A/D Converter

A conceptual view of a parallel time-interleaved pipeline analog-to-digital converter is shown in Fig. 6.1 as a four-channel example. The input signal is demultiplexed in the analog domain to an array of multi-stage pipelined ADCs. The channel ADCs operate time-interleaved as illustrated in the example timing diagram shown in Fig. 6.2. The concurrency across the channels is indicated in a four-channel case: $1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 1$. All the channel pipeline ADCs have the same resolution as the whole A/D converter and are equal in the structure. If the A/D converter has a conversion rate of f_S, the individual M parallel channel ADCs sample at f_S/M. Within each channel, the adjacent pipeline stages operate concurrently 180° out of phase.

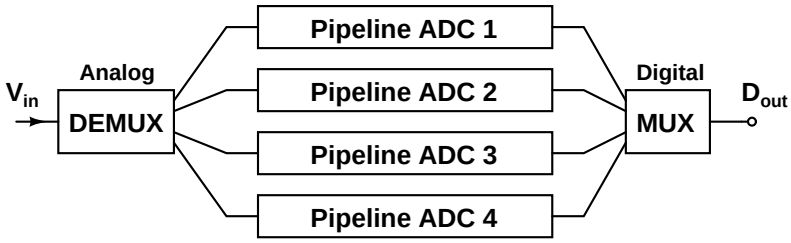

Figure 6.1 Block diagram of parallel pipeline architecture.

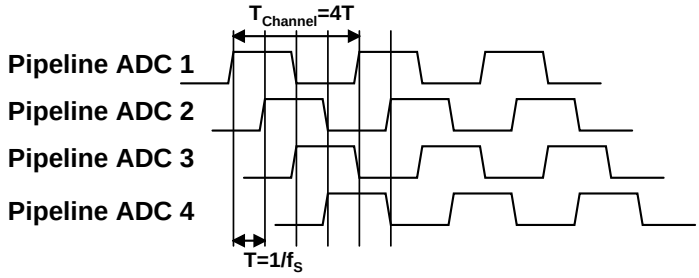

Figure 6.2 Timing diagram of parallel pipeline ADC.

The output bits of the channel ADCs are multiplexed, after which the correction algorithm can be exploited. For the digital output word D_{out}, compensation and correction of the errors because of the analog parallel signal processing can be accomplished, especially in the high-resolution converters. Digital post-processing is discussed in chapter 7.

6.2 Double-Sampling

The property of the successive pipeline stages working in opposite clock phases can be exploited by sharing the operational amplifiers between two sequential or parallel component ADCs. With the first approach, the number of amplifiers, and thus also the power dissipation, can be reduced significantly, but the throughput remains the same [3]. The latter approach employs the widely known double-sampling concept of switched capacitor circuits [4]. By using double-sampling, the throughput of the converter is almost doubled by introducing parallelism, but still the power dissipation remains almost the same as for an ADC having traditional single sampled pipeline stages with half the sample rate. On the other hand, the complexity of the pipeline stage is increased and, for the switches of a MDAC, more clock signals with different phases are needed. However, the effect of the increased complexity on the power consumption is minimal compared

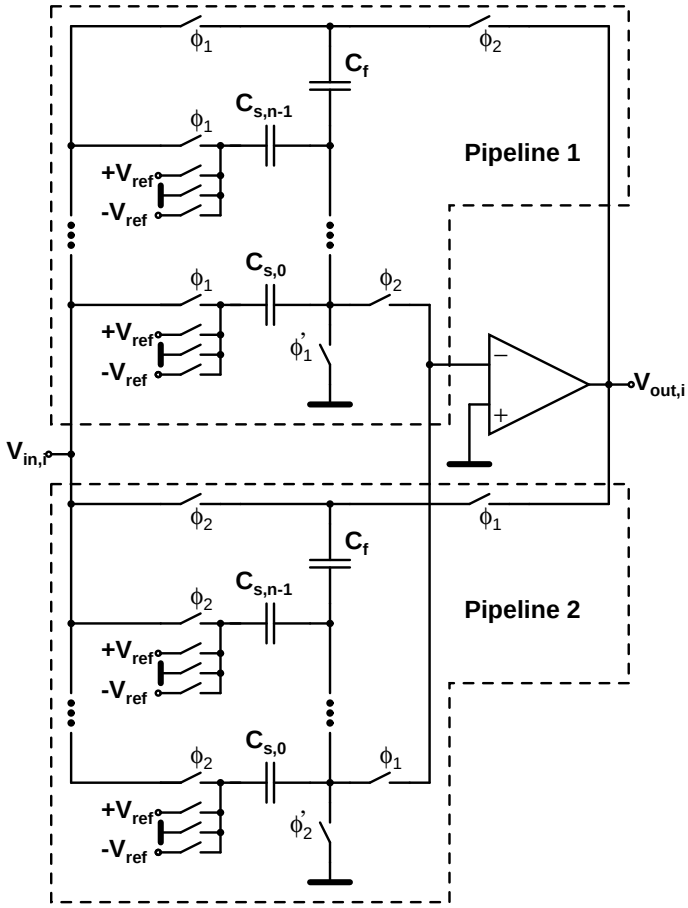

Figure 6.3 A double-sampling MDAC.

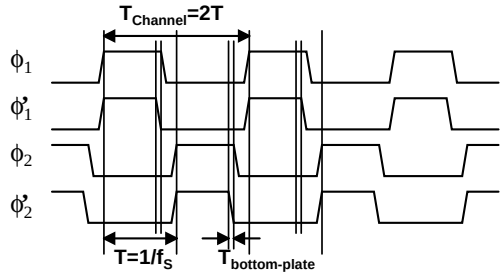

Figure 6.4 Timing diagram of double-sampling MDAC.

to the benefit gained from the amplifier sharing.

Two important side effects are caused by the amplifier sharing. First, the increased load capacitance of the amplifier affects the bandwidth requirement of the amplifier, which can be taken into account in the simulations. Second, the nonzero input voltage of the amplifier is never reset, which causes every sample to be affected by the finite-gain error from the previous sample. This so-called memory effect can be tolerated with an adequate amplifier open loop DC-gain. As the concept of double-sampling turns the ADC into a time-interleaved array, also the general performance limitations of parallel pipeline ADCs have to be taken into account.

An example topology of a double-sampling multiplying D/A converter is shown for simplicity as a single-ended configuration in Fig. 6.3. The capacitor arrays of two parallel channels working in 180° phase shift use the same amplifier. The non-overlapping clock signals of the double-sampling MDAC are shown in Fig. 6.4. Depending on the comparator topology and clocking, the sub-ADC can also be shared across the two pipeline channels or both channels have their own sub-ADCs. With separate comparator arrays, the logic for the switch control signals becomes simpler and thus the delay of the switches can be more easily minimized. On the other hand, this also doubles the number of comparators needed. However, the low-resolution comparators used in the sub-ADCs have usually a very small power dissipation and area.

6.3 Performance Limitations of Parallel Pipeline A/D Converters

The conversion speed of each channel in a parallel pipeline ADC is limited by the settling of the S/H, which in turn is determined by an operational amplifier settling time. In the time-interleaved parallel pipeline A/D converters, the use of parallelism in the analog domain also introduces limitations that do not arise in parallel digital systems. These errors include offset, gain and timing mismatches of the parallel channels [1, 2]. In the following, the errors caused by these mismatches will be discussed assuming that the system sample rate is f_S and M channels are used in the parallel structure.

6.3.1 Channel Offset Mismatch

Channel offset mismatch is caused by operational amplifier and charge injection mismatches across the array. It gives rise to fixed pattern noise, which is indicated in Fig. 6.5. Channel offset can be modeled as a voltage source connected in series with the pipelined stages (v_{OSi}) of each channel. In the worst case, for a DC-input, each

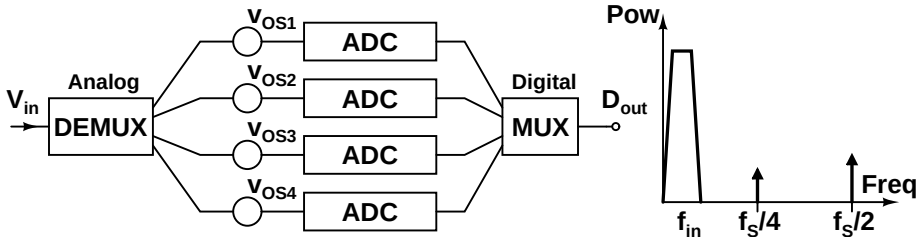

Figure 6.5 Channel offset mismatch and its effect in the frequency domain when M=4.

channel produces a different output code. This is manifested in the frequency domain as tones at multiples of f_S/M, as shown in Fig. 6.5.

Assuming that the offsets of the M channels are time invariant in the output, a periodic sequence $\{v_{OSi}, i = 0, 1, 2, \ldots\}$ with a period M can be seen. With the discrete Fourier transform (DFT), the Fourier series coefficients V_k

$$V_k = \sum_{i=0}^{M-1} v_{OSi} \cdot e^{-j\left(\frac{2\pi}{M}\right)ki}. \tag{6.1}$$

The effect of channel offset mismatch is additive and independent from the input signal level and frequency. Thus, only tones at multiples of channel sample rate f_S/M results [5, 6].

For the channel offset mismatch cancellation, two possible solution approaches exist: analog and digital. Analog offset cancellation techniques can be employed by, for example, using an auxiliary input stage to store a representation of the operational amplifier offset and the charge injection offset on capacitors [7]. The offset calibration can be done as well in the digital domain—i.e., the offset for each channel is measured digitally and subtracted from the digital output code of each channel [2, 8]. To assure that the offset is less than 1/2 LSB, one extra bit of resolution must be used. This extra bit necessitates only a modest increase in hardware. The advantage of the analog method is that it does not reduce the signal range. One limitation of the digital method from the system point of view is the fact that the static offset has to be measured before the calibration. The required idle time of the A/D converter is not possible in all systems. Alternatively, chopping of the channel input signals, controlled with a pseudo-random signal, together with de-chopping of the channel ADC outputs, can be employed [9]. The robustness achieved with the digital calibration usually makes the method preferable, despite the small reduction in the signal range.

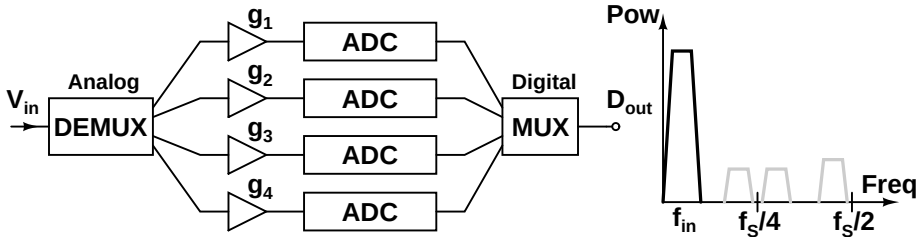

Figure 6.6 Channel gain mismatch and its effect in the frequency domain when M=4.

6.3.2 Channel Gain Mismatch

Channel gain mismatch is illustrated schematically in Fig. 6.6. In the frequency domain, it results in side bands centered around multiples of f_S/M. This can be intuitively understood to occur because each channel samples the input signal at a rate of f_S/M causing the input spectrum to be repeated periodically at intervals of f_S/M. If the channels are perfectly matched, the periodic repetitions cancel each other, except at integer multiples of f_S (fundamental for sampling).

Mathematically the channel gain mismatch can be modeled as an extra gain stage in series with the ideal pipeline stages as indicated in Fig. 6.6. The gain multiplied to the outputs in the time domain manifests in the frequency domain as a convolution of the gain mismatch and the output spectrum. Again assuming that the gain mismatch is time invariant, a periodic sequence $\{g_i, i = 0, 1, 2, \ldots\}$ with period M can be seen at the output node. If the input spectrum is $X(j\omega)$, the output spectrum $Y(j\omega)$ is

$$Y(j\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty} G_k X\left(j\left(\omega - \frac{2\pi k}{MT}\right)\right), \tag{6.2}$$

where the Fourier series coefficients G_k are given by

$$G_k = \sum_{i=0}^{M-1} g_i \cdot e^{-j\left(\frac{2\pi}{M}\right)ki}. \tag{6.3}$$

The convolution results in side bands around multiples of f_S/M [6]. It is noticeable that G_k is also periodic. In a special case when no mismatch is present in the system, all the g_i have the same value resulting in $G_1 = 1$ and $G_i = 0$, if $i > 1$ [2].

There are two major circuit causes of gain mismatch in the parallel pipeline ADC architecture, capacitor mismatch in different channels and the DAC levels mismatch across the channels. With careful sizing and layout, capacitor matching sufficient for 10–12-bit level, depending on the process, is achievable. In pipeline ADCs, a resistor string DAC level generator is usually being shared over the array, which ideally guaran-

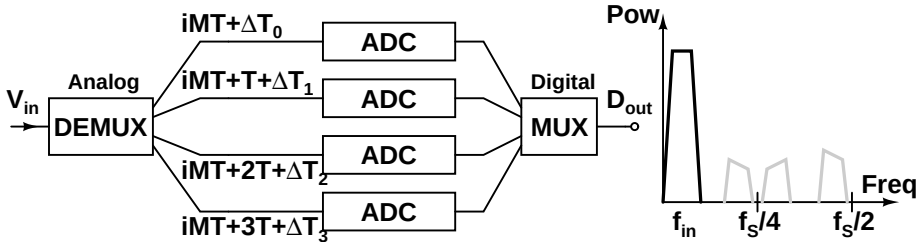

Figure 6.7 Timing mismatch and its effect in the frequency domain when M=4.

tees a perfect DAC matching. However, the nonideal settling of the reference levels can cause significant gain mismatch between the channels. Furthermore, by dimensioning the open loop DC-gain of the operational amplifiers large enough, the effect of their mismatch is suppressed below the quantization noise level.

The gain mismatch can be calibrated digitally by measuring the DAC reference levels and storing them in a memory. The ideal output code can be recovered using these measured reference levels [10]. Calibration of the gain error between parallel pipeline channels is one of the topics in the next chapter. An alternative approach to suppress the gain error is to alternate identical sample and feedback capacitors randomly within the stage, averaging out the effect of their mismatch [11].

6.3.3 Timing Mismatch

Clock generation for a parallel pipeline A/D converter involves several considerations. For the M parallel channels, M multi-phase clocks are required. Furthermore, within each channel, two-phase non-overlapping clocks and delayed sampling edges for the bottom-plate sampling are required. Bottom-plate sampling is used in SC-circuits whenever possible in order to minimize the signal-dependent charge injection effects. In the time-interleaved ADCs, two types of nonidealities exist: first, random sampling jitter or sampling time aperture uncertainty, and second, the systematic sample time mismatches between the channels.

The random sampling jitter is potentially an issue for single channel as well as for multi-channel A/D converters. Because of its random nature the aperture uncertainty does not cause any fixed pattern tones in the output spectrum but degrades the signal-to-noise ratio. For an input sinusoid of amplitude A and angular frequency ω_{in}, a sampling jitter of variance σ_t^2 results in output noise power given by $1/2A^2\omega_{in}^2\sigma_t^2$. One way to address this problem is to implement the clock generation using a voltage-controlled delay line in a delay locked loop (DLL). A DLL topology has intrinsically lower jitter than a phase locked loop (PLL) since it does not exhibit jitter accumulation [2]. A simpler

way to implement a generator of non-overlapping clocks without jitter accumulation is to use cross-coupled NOR-gates and an inverter chain to adjust the non-overlap time.

The fixed sample time mismatches between the channels, contrary to the random sampling jitter, cause fixed side bands in the output spectrum. As indicated in Fig. 6.7, the timing instants are ideally at the multiples of T. The actual timing instant of the parallel pipeline channel n deviates by ΔT_i from the ideal one. Then the output spectrum $Y(j\omega)$, in terms of the input spectrum $X(j\omega)$, is

$$Y(j\omega) = \frac{1}{T} \sum_{k=-\infty}^{\infty} \Phi_k(\omega)\, X\left(j\left(\omega - \frac{2\pi k}{MT}\right)\right), \tag{6.4}$$

where $\Phi_k(\omega)$ is

$$\Phi_k(\omega) = \sum_{i=0}^{M-1} e^{j\left(\omega - \frac{2\pi i}{MT}\right)\Delta T_n} \cdot e^{-j\left(\frac{2\pi}{M}\right)ki}. \tag{6.5}$$

Comparing the output spectrum with timing mismatch and the output spectrum with gain mismatch it can be seen that both cause side bands around f_S/M [5, 6], as shown in Fig. 6.7. However, in the timing mismatch case, the magnitude of the side bands is frequency-dependent, which can also be seen from Eq. 6.5.

The most straightforward way to avoid the timing skew between the channels is to employ a front-end sample-and-hold (S/H) circuit. After the front-end S/H circuit, which operates at the full sampling frequency f_S, the signal is not any more time continuous. The first stage of each pipeline channel samples then ideally a constant signal, for which the actual sampling moment is not critical. Alternatively, if distributed S/H circuits in the pipeline channels are employed, the skew between their sampling clocks can be calibrated by measuring its value and controlling tunable delays of a DLL [12]. Calibration of the skew between S/H circuits has two drawbacks. First, measurement of the skew is difficult and second, tuning of the delays requires high accuracy from the calibration hardware and algorithm. Timing skew calibration is further discussed in the next chapter.

6.4 Optimizing the Parallel Pipeline A/D Converter Topology for Power

It is obvious that increasing the number of parallel channels raises the conversion rate and lowers the slew rate and bandwidth requirements of the MDAC amplifier. The current consumption of an operational amplifier is a nonlinear function of the bandwidth, which indicates that there exists an optimum degree of parallelism with respect to the

Table 6.1 Process parameters used in the optimization.

Parameter	Value
Process	0.5μm CMOS
Mobility (μ)	$58.84 \cdot 10^{-3}\ m^2/Vs$
Gate Oxide Thickness (t)	$1.00 \cdot 10^{-8}\ m$
Gate Oxide Capacitance (C_{ox})	$3.45 \cdot 10^{-3}\ F/m^2$

sample rate and power dissipation. On the other hand, errors from channel offset and gain mismatch and skew in clock signals limit the performance of parallel ADCs and require special actions for compensation or correction. The area also increases linearly and the clock generation becomes more and more difficult with the increasing number of parallel channels. A power- and area-effective way to construct a parallel pipeline ADC is to use double-sampling.

Because of the RSD correction, robust low-power comparators can be used, making the power dissipation of the sub-ADC non-dominant. The critical block for the current consumption is the multiplying D/A converter, which feeds the analog output of the stage to the next pipeline stage. The MDAC output has to settle to the corresponding accuracy of the stage during the hold time. Thus, the power dissipation of a parallel pipeline A/D converter is to a great extent determined by the current consumption of the operational amplifiers of the MDACs. As derived in chapter 3, the bias current an amplifier is dependent on both the slew rate and GBW specification, in the latter case, even nonlinearly. This can be used to draw simple optimization formulas for the number of channels and the stage resolution of a parallel pipeline ADC. A thorough analysis of the effect of the stage resolution on the linearity and speed is presented in [13].

The most illustrative way to consider the optimization is to examine the current consumption of all amplifiers as a function of the sampling speed for different parallel pipeline A/D converter architectures [14]. The architectural parameters considered here are the number of parallel channels and the resolution of one stage. Because the current consumption is strongly dependent on the total resolution of the ADC, several different resolutions N are examined. For simplicity, identical stages are assumed and the redundant sign digit coding is employed. Whenever possible, the scheme of double-sampling is exploited in the parallel channels because of the significant power saving it offers. The process parameters of a standard double-poly, triple-metal 0.5-μm CMOS technology used in the calculations are given in Tab. 6.1.

6.4.1 Number of Parallel Channels

In chapter 3, minimal amplifier bias currents for a given settling time and accuracy were given in Eqs. 3.60 and 3.62 for GBW and slew rate limited settling, respectively. The number of channels M in a parallel pipeline A/D converter can be included in considerations. If all the stages have an equal stage resolution with $B_i = B$ effective bits, in an N-bit ADC, a worst-case slewing equal to the differential signal swing $V_{FS,diff}$, Eq. 3.62 gives a total amplifier current consumption of

$$I_{amp,SR} = 12\left(\frac{N}{B}-1\right)\cdot\frac{f_S}{M}\cdot V_{FS,diff}\left(C_{L,tot}+C_f\right), \tag{6.6}$$

where f_S is the sample frequency ($T = 1/f_S$), $C_{L,tot}$ the total amplifier load capacitance including all parasitics, and C_f the feedback capacitor. Similarly, Eq. 3.60 indicates for the $N/B-1$ stages a total current of

$$I_{amp,GBW} = \frac{18}{\mu C_{ox}}\cdot\frac{L}{W}\left(\frac{N}{B}-1\right)\cdot\left((N+1)\cdot\ln 2-\ln\left(2^B-1\right)\right)^2 \cdot\left(\frac{f_S}{M}\right)^2\cdot\left(2^B C_{L,tot}+\sum_{j=0}^{n-1}C_{s,j}+C_{par}\right)^2, \tag{6.7}$$

where L and W are the gate length and width of the amplifier input transistors, respectively. In Fig. 6.8, the current consumption of the amplifiers is plotted as a function of the sample rate for a 10-bit pipeline ADC with a stage resolution of 1.5 bits. Curves for a single-channel pipeline ADC and for two- and four-channel ADCs employing double sampling are given. It can be seen that, up to a particular, process-dependent sample rate, the current consumption is linearly dependent on the sample rate. In this part of the curve, the current is determined by the minimum slew rate given by Eq. 6.6 and the GBW can be adjusted by the W/L ratio of the input transistors according to Eq. 6.7. Beyond this sample rate, the current consumption is dictated by the GBW requirement, given by Eq. 6.7 and the power dissipation grows squarely.

From Fig. 6.8, the remarkable current saving property of double-sampling is also clearly visible. Sharing the amplifiers with two parallel channels effectively halves the current consumption in the linear, slew rate limited, part of the curve. In the GBW limited section the difference is even larger. The effect of parallelism manifests itself in the current consumption through a lengthened settling time of the stage output. The settling time for a pipeline stage of an M-channel parallel pipeline ADC is $M\cdot T/2$. This means that, as indicated in Fig. 6.8, the current consumption in the linear part of the curve is in the first order independent from the degree of parallelism, if the double-

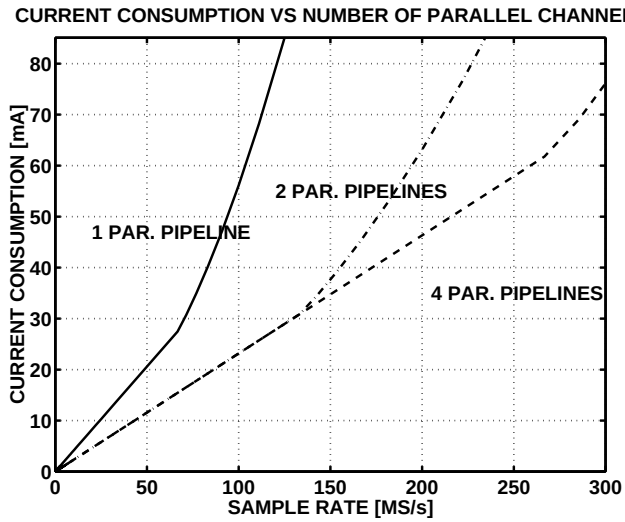

Figure 6.8 Current consumption of the amplifiers of one, two and four parallel 10-bit pipeline ADCs.

sampling is not encountered. Additionally, a less steep rise in the GBW limited parts of the curves results from the same property.

In Figs. 6.9 and 6.10, the corresponding amplifier current consumption curves are plotted for resolutions of 8 and 12 bits, respectively. From the curves, it can easily be seen that if a sample rate of 200 MS/s is desired the optimum number of channels with an 8-bit resolution is two. With 10-bit and 12-bit resolutions, the optimum degree of parallelism is four. The corresponding current consumptions of the amplifiers for 8-, 10- and 12-bit resolutions are 36 mA, 46 mA and 57 mA, respectively.

The effect of the total A/D converter resolution on the current consumption of the amplifiers in a parallel pipeline ADC is illustrated in Fig. 6.11. Curves for a resolution of 8, 10 and 12 bits are plotted when the stage resolution is kept in 1.5 bits and an architecture with two parallel double-sampled channels is used. It can be seen that the corner frequency, where the slew rate limitation changes to the GBW speed limitation, decreases linearly from the 8-bit ADC to the 12-bit ADC. The current consumption of the corresponding corner sample rate is thus linearly dependent on the total resolution and decreases with resolution.

Increasing the number of parallel channels also linearly increases the number of comparators. However, when a low stage resolution and the digital correction are used, the power dissipation of comparators is very small. In time-interleaved ADCs, the problems rising from timing mismatch of the parallel channels are commonly avoided by adding a front-end sample-and-hold circuit. This S/H circuit, which is also based

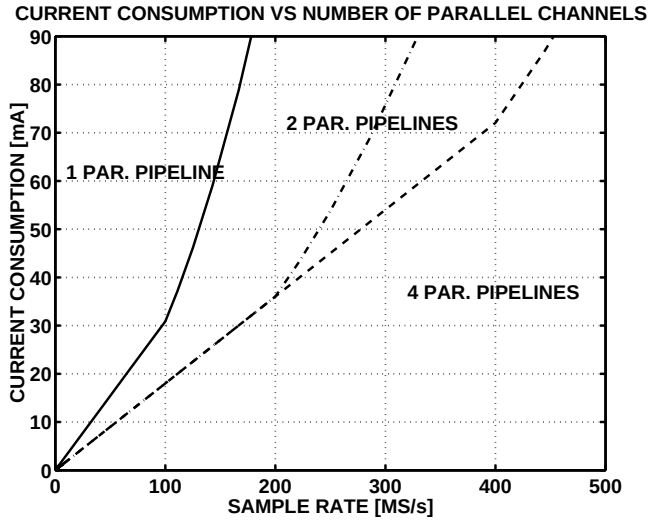

Figure 6.9 Current consumption of the amplifiers of one, two and four parallel 8-bit pipeline ADCs.

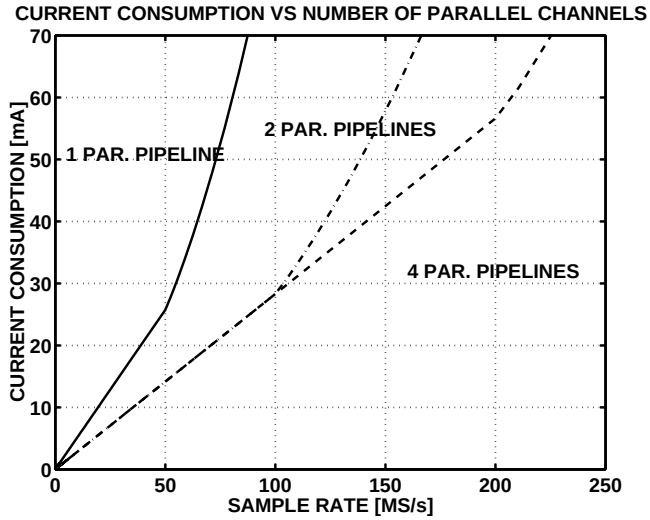

Figure 6.10 Current consumption of the amplifiers of one, two and four parallel 12-bit pipeline ADCs.

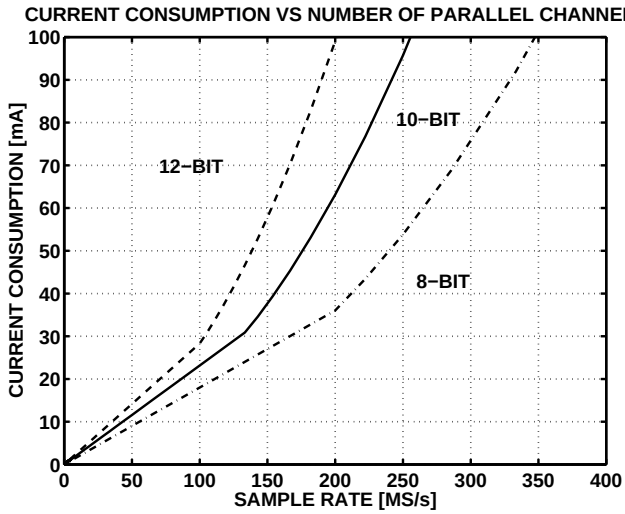

Figure 6.11 Current consumption of the amplifiers of two parallel pipeline ADCs with a resolution of 8, 10 and 12 bits.

on a SC integrator, must sample with the full conversion rate of the ADC and its power dissipation has to be added to the total current consumption. Also the die area grows linearly with the number of parallel channels.

6.4.2 Stage Resolution

The resolution of a pipeline stage can also be optimized for the sample rate and power dissipation. The effect of the stage resolution on the current consumption and on the corner frequency manifests itself in Eqs. 6.6 and 6.7. The former indicates a linear decrease of the slew rate determined current consumption with an increasing effective stage resolution B, which results from the reduced number of amplifiers. The latter in turn has an additional exponential dependency on B, which increases the total amplifier current consumption rapidly in the sample rate range, limited by the GBW.

Using the same conditions as above, the current consumption of the amplifiers of a 10-bit pipeline ADC with one channel and two different stage resolutions (1.5 and 2.5 bits) is plotted in Fig. 6.12. In the calculations, the capacitor C_s has been kept constant and the capacitor C_f is made smaller to get the proper closed loop gain. This can be accomplished because of the smaller noise contribution of the end stages in a pipeline channel. Now the number of amplifiers needed is smaller in the case of 2.5 bits per stage, but the corner frequency, where the GBW limited part begins, is lower, and, because of the smaller feedback factor, the current consumption rises very rapidly with

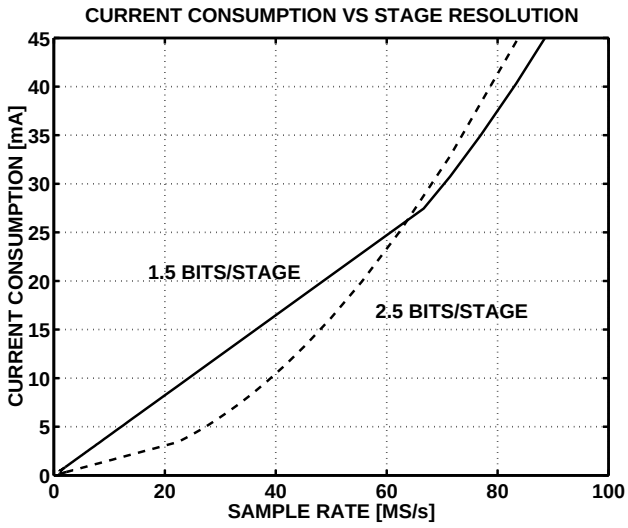

Figure 6.12 Current consumption of the amplifiers of 10-bit pipeline ADCs with 1.5-bit and 2.5-bit stage resolution.

the sample rate. In addition to that, the offset specification of the comparators and the number of comparators per stage grow exponentially with the stage resolution.

In Figs. 6.13 and 6.14, the same plots are presented for 8-bit and 12-bit pipeline ADCs. It is clear that for the 8-bit resolution the cross point of the two curves with different stage resolution is at a higher frequency than for the 12-bit resolution. Also, the benefit of the higher stage resolution at low sample rates is not so big when the overall resolution is high. However, these calculations do not consider the noise contribution of the stages. It has been shown that in high-resolution pipeline ADCs the stage resolution should also be high because of the large interstage gain, which reduces the total noise referred to the input [13].

It can be concluded from Fig. 6.15, where the 1.5-bit and 2.5-bit stage resolutions are compared to 8-bit, 10-bit and 12-bit pipeline ADCs, that, for a low sample rate, a large stage resolution gives a smaller power dissipation. However, there exists a process-dependent sample rate, beyond which a lower stage resolution gives a smaller current consumption.

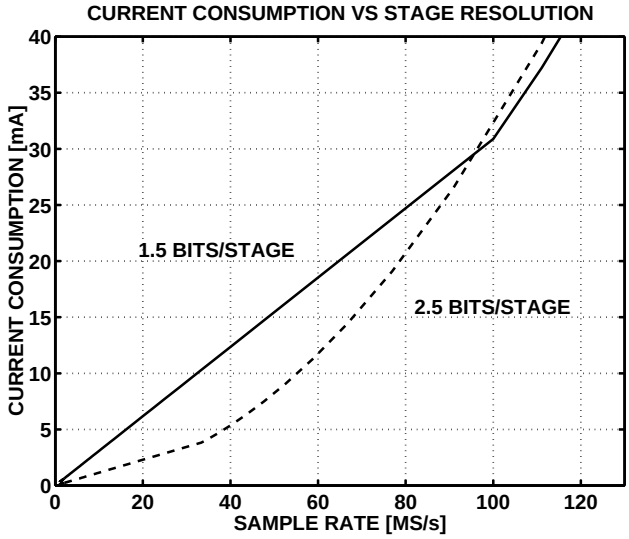

Figure 6.13 Current consumption of the amplifiers of 8-bit pipeline ADCs with 1.5-bit and 2.5-bit stage resolution.

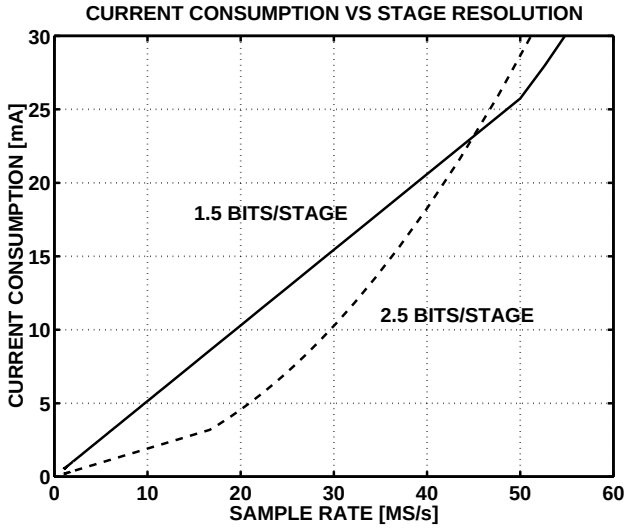

Figure 6.14 Current consumption of the amplifiers of 12-bit pipeline ADCs with 1.5-bit and 2.5-bit stage resolution.

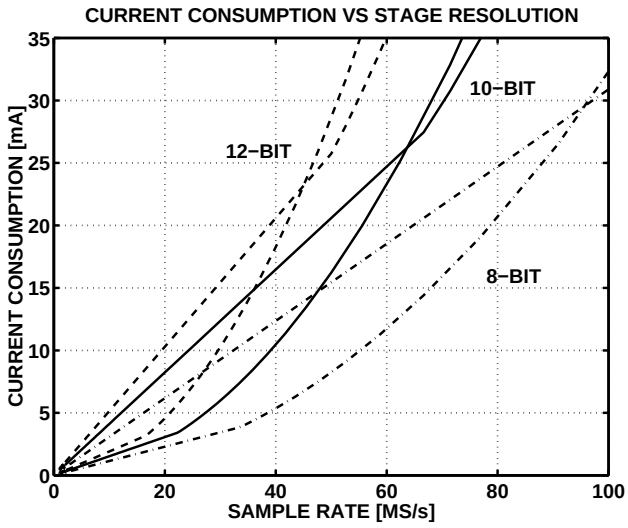

Figure 6.15 Current consumption of the amplifiers of pipeline ADCs with 1.5-bit and 2.5-bit stage resolution and total resolutions of 8, 10 and 12 bits.

6.5 Application Case: A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter

6.5.1 Introduction

The increasing range of wide-band wireless communication standards, like the Universal Mobile Telecommunication System (UMTS), Wireless Local Loop (WLL) and Local Multipoint Distribution Services (LMDS), will evolve to high data rate applications within the next few years. At the same time, the boundary between analog and digital signal processing is moving closer to the antenna, following the trend toward software-defined radio. This creates a need for high resolution and very high sampling rate analog-to-digital converters (ADCs). The 10-bit 200-MS/s A/D converter presented in this section demonstrates the capability of meeting these requirements with a standard double-poly triple-metal 0.5-μm CMOS process without complicated calibration methods.

The most promising topology for a high-resolution high-speed A/D converter implemented in a CMOS process is the pipeline architecture [15, 16, 17, 19, 18]. Parallel pipeline ADCs with several time-interleaved component ADCs have been introduced to attain very high sampling rates with acceptable power consumption [1, 2]. A resolution of ten bits and conversion rates of up to 100 MS/s have been reported [18]. Their power dissipation, however, has risen very high, especially with high sampling rates. Em-

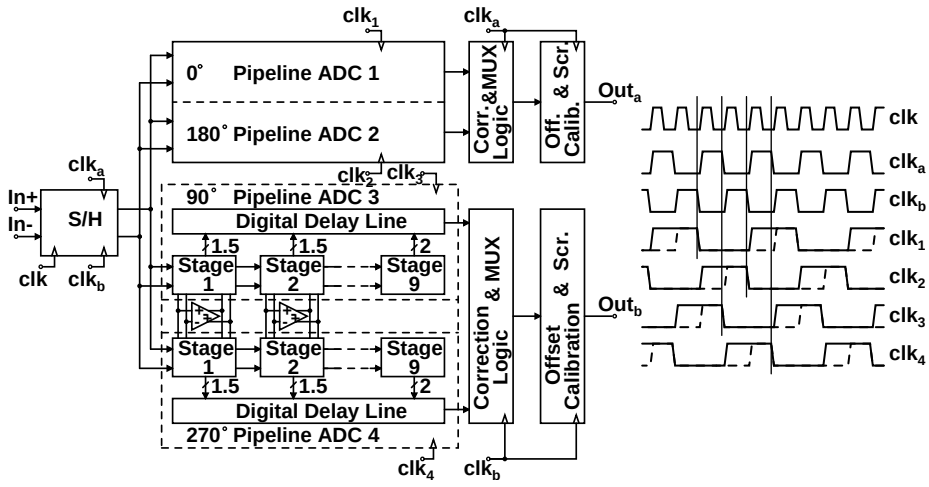

Figure 6.16 Block diagram and clock signals of the parallel pipeline ADC.

ploying double-sampling and parallelism with time-interleaved pipeline ADCs, a very competitive power and area consumption can be obtained [19].

6.5.2 Circuit Description

The well-known problems in the time-interleaved ADCs arise from mismatch between the parallel channels. These errors are offset, gain mismatch, and skew in the clock signals [1]. The offset is seen as tones at multiples f_S/M, where M is the number of the parallel channels and f_S the sampling rate. Both the gain mismatch and the timing skew generate spectral images of the signal around the same frequencies. It is not possible to achieve the 10-bit resolution with the 200-MS/s sampling rate without addressing special actions to eliminate these errors.

The most straightforward way to avoid the timing skew, also used in this design, is to employ a front-end sample-and-hold (S/H) circuit. Digital calibration is chosen for eliminating the offset, which is mainly originated from the offset voltages of the operational amplifiers. The gain error, rising predominantly from the capacitor mismatch, is left uncalibrated since it can be adequately suppressed by a careful layout design for the 10-bit accuracy requirement.

A block diagram and the clock signals of the 10-bit 200-MS/s pipeline A/D converter are shown in Fig. 6.16. The core of the converter consists of two parallel double-sampling pipeline ADCs. The differential analog input is time-interleaved to the four component ADCs in the order indicated in Fig. 6.16 by a double-sampling S/H circuit. The digital outputs of the stages of the parallel ADCs are corrected and multiplexed to

two 100-MHz time-interleaved outputs, which are offset compensated.

6.5.2.1 Pipeline Component A/D Converters

The four pipeline component A/D converters employ the 1.5 bit/stage topology with RSD error correction [20]. The feedback factor of the stage SC amplifier being ideally 0.5 maximizes the conversion speed [13]. The eight pipeline stages with one effective bit and 0.5-bit redundancy are followed by a two-bit flash ADC, as indicated in Fig. 6.16. The property of the successive pipeline stages working in opposite clock phases is exploited by sharing the operational amplifiers between two parallel component ADCs.

In the double-sampling MDAC, the capacitor arrays, operating in a 180° phase shift, have their own three-level sub-ADCs, which minimizes the delay of the switch control signals but doubles the number of the comparators needed. However, the dynamic comparators used in the sub-ADCs have a very small power dissipation and area. In the MDACs, the switches whose timing is critical, and the switches connected to the input of the amplifier, are NMOS-switches. In all other switches, a more linear response in the signal voltage range and minimization of the clock feedthrough errors are achieved utilizing CMOS-switches. In the first pipeline stage, the input switches tracking the output of the S/H circuit are realized with the bootstrapped MOS-switch described later.

The RSD digital correction algorithm can tolerate comparator offset voltages up to $\pm V_{ref}/2^B$ for a B-bit stage when the reference voltage is V_{ref}, which is equal to the maximum signal amplitude. This allows the use of no-static-power-dissipating dynamic comparators without any continuous time pre-amplification. In the sub-ADCs, a differential pair dynamic comparator is utilized. It is based on two unequally sized cross-coupled differential pairs with switched tail current sources and a CMOS latch as the load [21].

6.5.2.2 High-Swing Regulated Folded Cascode Amplifier

The circuit schematic of the amplifier utilized in the ADC is shown in Fig. 6.17. It uses the folded cascode configuration with an NMOS input pair offering a large bandwidth of 450 MHz to a 1.7-pF load according to the simulations. The open loop DC-gain of the amplifier is enhanced to 110 dB by introducing gain boosting with the complementary high-swing low-voltage regulation amplifiers shown in Fig. 6.17. This gives enough implementation margin to the level required for a 10-bit accuracy and omits the effects of the amplifier gain mismatch between the channels. The input of the regulation amplifiers is at transistor sources [22, 23] and they operate with very low bias currents and

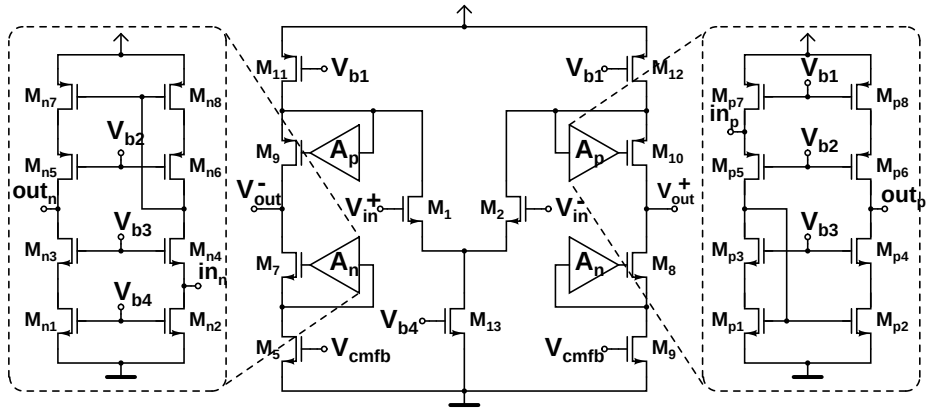

Figure 6.17 Regulated high-swing low-voltage folded cascode amplifier.

can be constructed from almost minimum size transistors, thus minimizing the decrease of GBW. Furthermore, the same bias circuit can be used for the core amplifier and for the regulation amplifiers. Contrary to many other regulation amplifier topologies, the output signal swing is not reduced, since only a voltage of V_{ds} is required between the feedback amplifier inputs and the supply rails, resulting in a reasonable signal swing of 0.8 V at the output. To attain an accurate settling behavior of the SC gain stage, the feedback amplifiers are band limited by adding small capacitors in their outputs. The amplifier uses an SC common-mode feedback (CMFB) circuit [24], which is connected to the node V_{CMFB}.

6.5.2.3 Timing Skew Insensitive Double-Sampled S/H Circuit

A simple unity gain SC sample-and-hold circuit ideally achieves twice the speed of a 1.5-bit/stage pipeline ADC because of the larger feedback factor in the SC amplifier circuit. Consequently, the S/H circuit is capable of driving two parallel converters. A four-channel ADC can be constructed by introducing the double-sampling technique, both in the pipelined component ADCs and in the S/H circuit.

Applying the double-sampling in the S/H circuit, however, creates a new problem: because of the inherent parallelism of this technique, the circuit becomes susceptible to the timing skew and thus incapable of performing its main task—to remove the skew. By modifying the standard double-sampled circuit, it can be made insensitive to the skew [25]. The main idea in this modification is to take away the parallelism from the sampling operation. This is accomplished by replacing the two parallel sampling switches with a single shared switch that is controlled with short pulses at the full sampling rate. A simplified schematic of the circuit and its timing diagram are shown

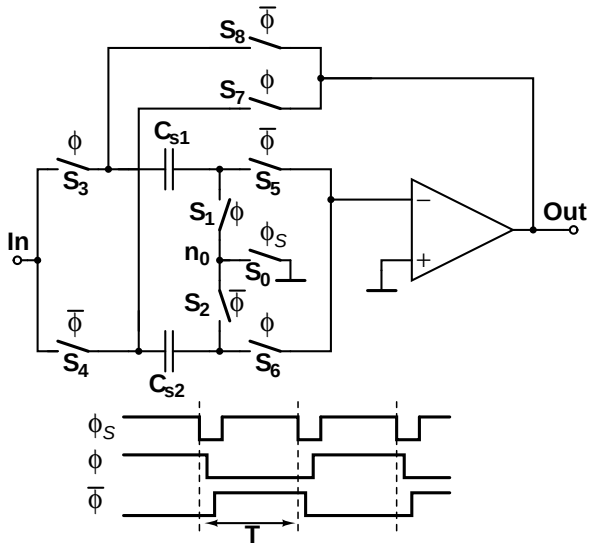

Figure 6.18 Skew insensitive double-sampled S/H circuit and its timing.

in Fig. 6.18.

The sampling to the upper capacitor is done by applying a short zero pulse to the switch S_0 during which the switches S_1 and S_3 are opened. Consequently, the input voltage is sampled in the capacitor C_{s1} that is next connected into the feedback configuration around the opamp. Right after the sampling pulse, the lower half circuit can begin its tracking phase, which will be concluded to a similar sampling event.

The load capacitance of the S/H circuit is minimized by allowing only one component ADC to be connected in the S/H output at a time. The price is the need for extra clock signals in the first pipeline stages.

6.5.2.4 Bootstrapped MOS-Switch

In high-speed low-voltage designs, the MOS switch on-resistance is a significant limitation on the tracking speed and the settling time. Moreover, the on-resistance has a nonlinear voltage dependence, which produces distortion when tracking continuous time signals.

To reduce the on-resistance, a voltage higher than the supply can be used to control the switches. In a typical realization, the switch transistor gate is locally boosted with a charge pump circuit. It is also possible to make the switch gate voltage to track the switch input voltage with some offset (typically V_{dd}). This gives two advantages. First, the circuit's long-term reliability is improved since the gate-drain voltage of the

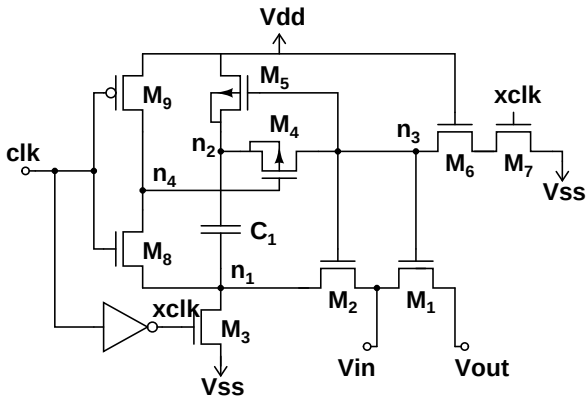

Figure 6.19 Bootstrapped MOS-switch.

switch transistor never exceeds V_{dd}. Second, the on-resistance becomes almost constant, which significantly reduces the distortion.

The employed switch circuit [26, 27] is shown in Fig. 6.19. Since the circuit is quite complicated, it has been used only in two critical places: as the input switches in the S/H circuit and in the first pipeline stages of the ADCs, which have only a quarter of the clock period for tracking.

6.5.2.5 Clock Generation

As shown in Fig. 6.16, there is a need for clock signals at three different rates: a full-rate clock and complementary half-rate clocks in the S/H circuit and four quarter-rate clocks with a 90° phase difference in the pipeline ADCs. The clock generator circuit is fed with an external full-rate clock from which the lower rates are constructed with a synchronous divide-by-two and a divide-by-four circuit. The dividers are followed by three standard clock generator cores for producing the non-overlapping clock phases: one for the S/H circuit and one for each of the two double-sampled pipelines. The 25% duty cycle clocks, utilized in the first pipeline stage, are formed as a logic operation of the half and the quarter rate signals.

6.5.2.6 Reference Voltage Driver

The large number of pipeline stages using common reference voltages increases the capacitive load in the reference nodes to several picofarad. To guarantee that the reference does not limit the settling speed, its output impedance has to be in the order of a couple of tens of ohms. This means that a resistor string implementation of the reference would have a very large quiescent current, or alternatively a large external capacitor has to be

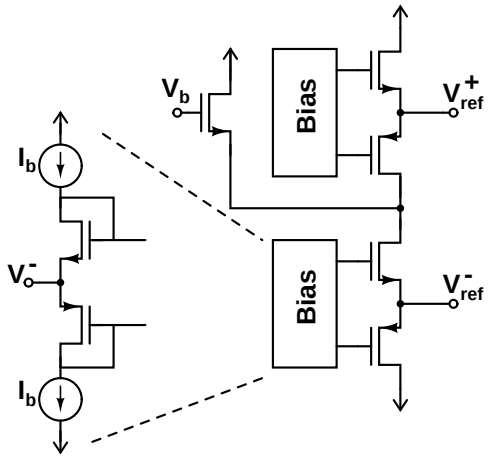

Figure 6.20 Simplified schematic of the reference driver.

used. A more reasonable power consumption without an external capacitor is obtained with the circuit proposed in Fig. 6.20. There, the low-impedance voltage outputs are provided by class AB buffers constructed of complementary transistors. The buffers for the positive and the negative reference are cascoded in order to minimize the steady state current consumption.

6.5.2.7 Offset Calibration and Output Scrambling

The main source of offset is the input offset voltage of the operational amplifiers utilized in the pipeline stages. Because of the double sampling, there is no idle time that can be used to auto zero the amplifier offset, and thus the problem has to be handled some other way. The methods to suppress the offset in parallel ADCs include digital [2] and analog [17] calibration, and digital post filtering in case of a two-channel ADC [28]. In the analog calibration, the offset is measured from the digital output, and, using a D/A converter, a canceling signal is injected into the channel input. The digital calibration does the canceling in the digital domain simply by subtracting the measured offset from each sample. The advantage of the analog method is that it does not reduce the signal range. However, the robustness achieved with the digital calibration usually makes the method preferable, despite the small reduction in the signal range.

In this design, the digital offset calibration is applied in the multiplexed half rate output of the double-sampled channel pair. It is assumed that there is no significant offset, and thus no need for calibration, between the signal paths inside the double-sampled pipeline. This is caused by the fact that the opamps, which are the main source of the offset, are the same for both the signal channels. During the offset measurement,

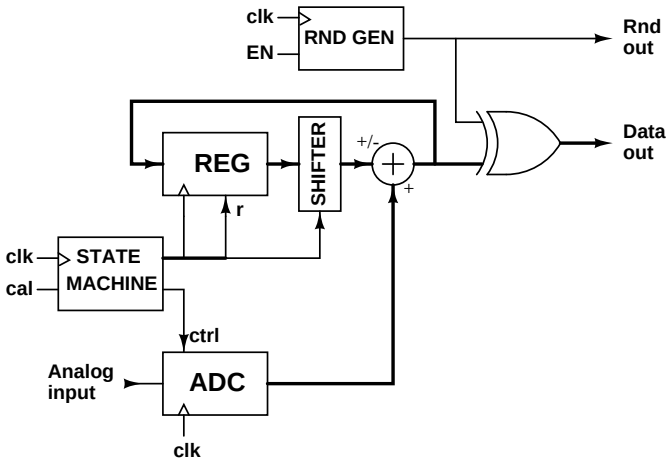

Figure 6.21 Offset calibration and scrambling of the output.

the normal operation of the converter has to be suspended. It can, however, be usually performed at the power up or during some idle periods.

The calibration circuit consists of an adder, a register for storing the measured offset, and a state machine that provides the control signals for the logic and the ADC. During the calibration, the ADC input is shorted to ground and the offset is obtained by averaging the output signal over 16 clock cycles. The averaging is realized simply by adding together 16 consecutive output codes and performing a bit shift of four for the result. The calibration is activated with an external one-bit control signal.

The most significant ADC output bits have strong correlation to the analog input signal. This is utilized to investigate the signal feedthrough from the output to the input by adding a possibility of scrambling the outgoing digital words with a pseudo random bit-stream [29]. The scrambling is realized by putting XOR gates before each output buffer and applying the random bit to their other input. For descrambling, the random bits are taken out through an extra package pin. A simplified block diagram of the calibration and scrambling circuit is depicted in Fig. 6.21.

6.5.3 Experimental Results

The prototype circuit is fabricated using a 0.5-μm triple-metal double-poly CMOS process. The total area of the chip is 7.4 mm^2 and its die photo is shown in Fig. 6.22. The circuit is measured with a 3.0-V supply with a differential input swing of 1.6 V_{pp}.

The static linearity curves obtained with the code density test are presented in Fig. 6.23, which shows the DNL being within $\pm$0.8 LSB and the INL within $\pm$0.9 LSB.

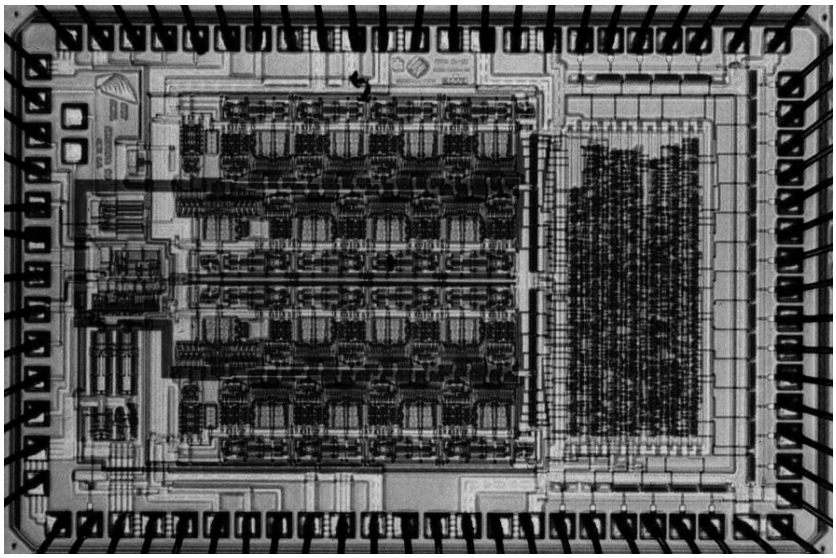

Figure 6.22 Chip photo.

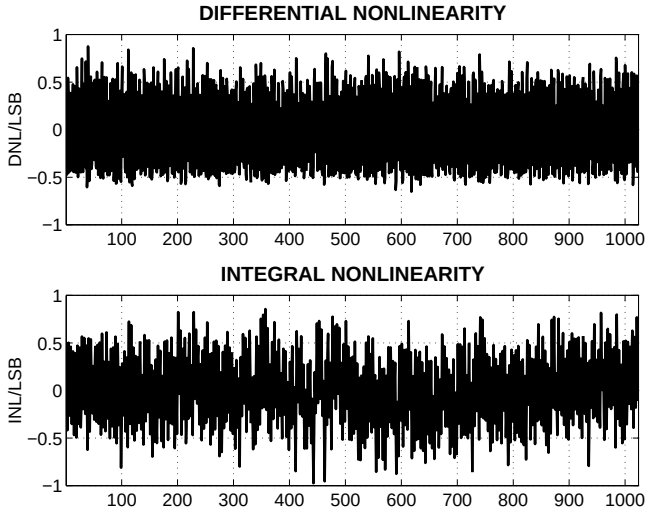

Figure 6.23 Measured static linearity.

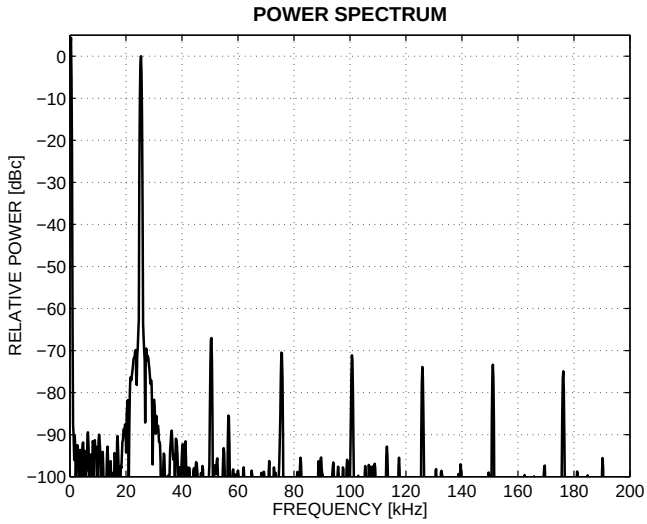

Figure 6.24 Spectrum obtained with 200-MHz beat frequency test.

A spectrum obtained with a 199.975-MHz beat frequency at a 200-MHz clock rate is shown in Fig. 6.24. In Fig. 6.25 a 71.3-MHz full-scale signal is sampled at the full clock rate resulting in a spurious-free dynamic range (SFDR) of 55 dB. From the spectrum, it can be seen that the offset tone at 50 MHz is more than 56 dBc below the signal level and the gain mismatch tones around $f_S/4$ and $f_S/2$ remain below the noise level. The mismatch tone around half the sample rate rises normally to limit the SFDR at high signal frequencies. The total harmonic distortion (THD) as a function of the signal frequency is plotted in Fig. 6.26. THD starts from around 55 dB, becoming about 46 dB around the Nyquist frequency, and rising again to the 55-dB level near the sampling frequency. This repeatable behavior imply that the performance of the ADC is limited by the pipeline component ADCs rather than by the S/H circuit. Furthermore, for the stand-alone prototype of the S/H circuit measured SFDR of better than 65 dB up to 73-MHz inputs [25] indicate that the overall performance is limited by the channel ADCs.

The mismatch tone probably results from the improperly operating common mode feedback, which creates asymmetry between the two double-sampled pipeline ADCs. This also limits the signal-to-noise and distortion ratio (SNDR) at high signal frequencies to 43 dB. However, excluding the mismatch tone the spectral performance indicates that the ADC can sample narrow IF bands around 200 MHz with a THD of 55 dB. The measured power consumption without and with the digital output drivers is 280 mW and 405 mW at a 3.0-V supply, respectively. Tab. 6.2 summarizes the overall performance.

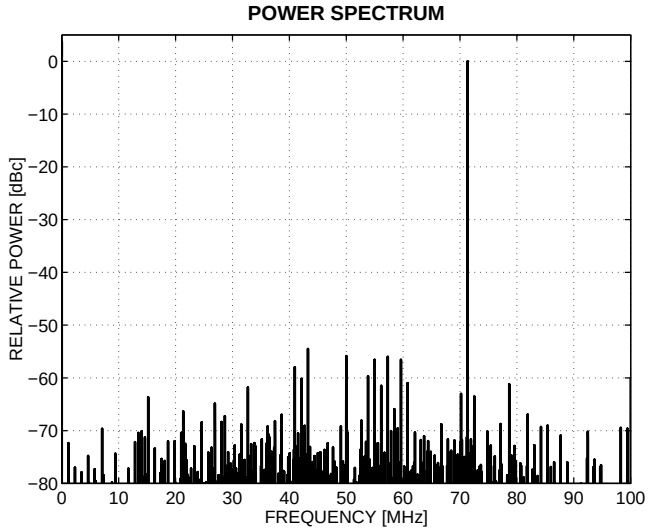

Figure 6.25 Measured spectrum where a 71.3-MHz signal is sampled at 200-MHz clock rate.

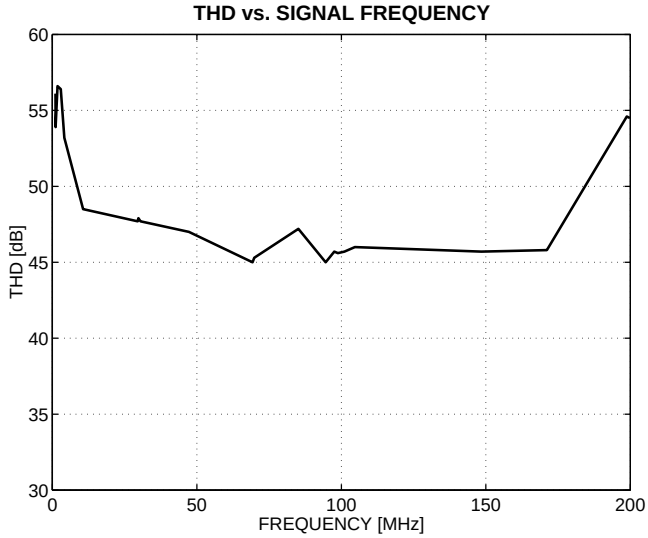

Figure 6.26 THD as a function of the signal frequency.

Table 6.2 Summarized performance of the ADC.

Technology	0.5-μm CMOS
Resolution	10 bits
Sample Rate	200 MS/s
Supply Voltage	3.0 V
Area	7.4 mm^2
DNL	$\pm$0.8 LSB
INL	$\pm$0.9 LSB
THD	46 dB
SNDR	43 dB
ENOB	6.9 bits
Power Dissipation of Core ADC	280 mW
Power Dissipation including Output Buffers	405 mW
E_{conv}	2.0 pJ

6.5.4 Conclusions

A 10-bit 200-MS/s CMOS ADC based on parallel pipeline architecture and capable of sampling input frequencies above 200 MHz has been described. The converter architecture was optimized for power in terms of the number of the parallel channels and the stage resolution. The extensive use of parallelism and careful consideration of the circuit blocks, like the double-sampling S/H circuit, the high-swing regulated amplifier, the differential-pair dynamic comparator, the voltage reference, and the bootstrapped MOS-switch, have enabled the power consumption to be squeezed to 280 mW from 3.0-V supply at 200 MS/s. So far in CMOS technologies, only the flash-type ADCs have been able to attain clock rates of hundreds of megahertz. The circuit presented in this paper demonstrates that, using a standard CMOS process, sampling rates exceeding 200 MS/s can also be achieved with the time-interleaved parallel pipeline architecture.

The studies and results presented in this section have been published in [8].

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Chapter 7

Calibration of Pipeline A/D Converters

The main error sources limiting the performance of a switched capacitor pipeline stage, and thus the accuracy of the whole A/D converter, were presented in chapter 3. The inaccuracy of the sub-ADC, mainly inherited from the comparator offsets, can easily be suppressed below the required level for low-resolution stages by employing the redundant sign digit (RSD) coding. However, in the light of publications and commercial products, the matching of circuit elements limits the precision of the MDACs, and the attainable resolution of pipeline A/D converters thereof, somewhere below 12 bits. To attain resolutions higher than this, some kind of trimming, calibration, or error shaping has to be utilized to compensate for the process mismatch. In this chapter, the combined effect of the nonidealities of switched capacitor MDACs on the ADC transfer function are presented. Reported calibration techniques to correct the resulting nonlinearity are categorized and briefly reviewed. The developed digital self-calibration method to correct capacitor mismatch and gain error is introduced in detail.

7.1 Error Sources in Pipeline A/D Converters

The essential nonidealities and error sources of a pipeline stage, including a flash-type sub-ADC and an SC MDAC, were handled in detail in chapter 3 and their combined effect on the ADC linearity is summarized here. As a conclusion, if low-resolution stages are employed, the accuracy of the sub-analog-to-digital converters does limit the resolution of a pipeline A/D converter—when the RSD coding is applied, the total amount

of comparator offsets and their reference voltage mismatch in the order of hundreds of millivolts can be tolerated, even for a low-voltage design. Typically, the limiting factor in a switched capacitor realization of the multiplying D/A converter is the capacitor mismatch. Other error sources in SC pipeline stages include the finite operational amplifier open loop DC-gain, gain bandwidth, and offset voltage, reference voltage mismatch, and charge injection from switches. Additionally, second order effects, like the memory effect of the amplifier, deteriorate the settling accuracy of a stage. The transfer function of a pipeline stage i, including the essential nonidealities and error sources of a switched capacitor MDAC, is given by

$$V_{out,i} = (1-\varepsilon_{A_0})\cdot(1-\varepsilon_\tau)\cdot\left[\left(1+\frac{\sum_{j=0}^{n-1}\left(C'_{s,j}+\Delta C_{s,j}\right)}{C'_f+\Delta C_f}\right)\cdot\left(V'_{in,i}+\Delta V_{in,i}\right)\right.$$
$$\left.-\frac{\sum_{j=0}^{n-1}\left(m_j\cdot\left(C'_{s,j}+\Delta C_{s,j}\right)\right)}{C'_f+\Delta C_f}\left(V'_{ref}+\Delta V_{ref}\right)+V_{os,i}\right], \qquad (7.1)$$

where ε_{A_0}, rewritten from Eq. 3.29

$$\varepsilon_{A_0} = \frac{1}{A_0\cdot f} \qquad (7.2)$$

and ε_τ, rewritten from Eq. 3.36

$$\varepsilon_\tau = e^{-\frac{g_m}{\frac{C_{L,tot}}{f}+\sum_{j=0}^{n-1}C_{s,j}+C_{par}}\cdot\frac{1}{3f_S}}, \qquad (7.3)$$

are the errors caused by the finite open loop DC-gain and settling speed of the opamp, respectively. $\Delta C_{s,j}$ and ΔC_f present the capacitor mismatch, ΔV_{in} the error in the sampled input voltage because of timing skew and jitter, ΔV_{ref} the reference voltage mismatch, and $V_{os,i}$ the constant offset, rewritten from Eq. 3.24

$$V_{os,i} = \frac{C_f+\sum_{j=0}^{n-1}C_{s,j}}{C_f}v_{os}. \qquad (7.4)$$

The effects of the MDAC nonidealities on the stage transfer function are summarized in Fig. 7.1(a) for a 1.5-bit stage, where the solid line indicates the real transfer function and dashed line the ideal case. A constant negative gain error resulted from capacitor mismatch and finite open loop DC-gain of the amplifier is clearly visible. The finite gain bandwidth of the opamp would result an amplitude-dependent gain error, which is not depicted in Fig. 7.1(a). The capacitor and reference voltage mismatch to-

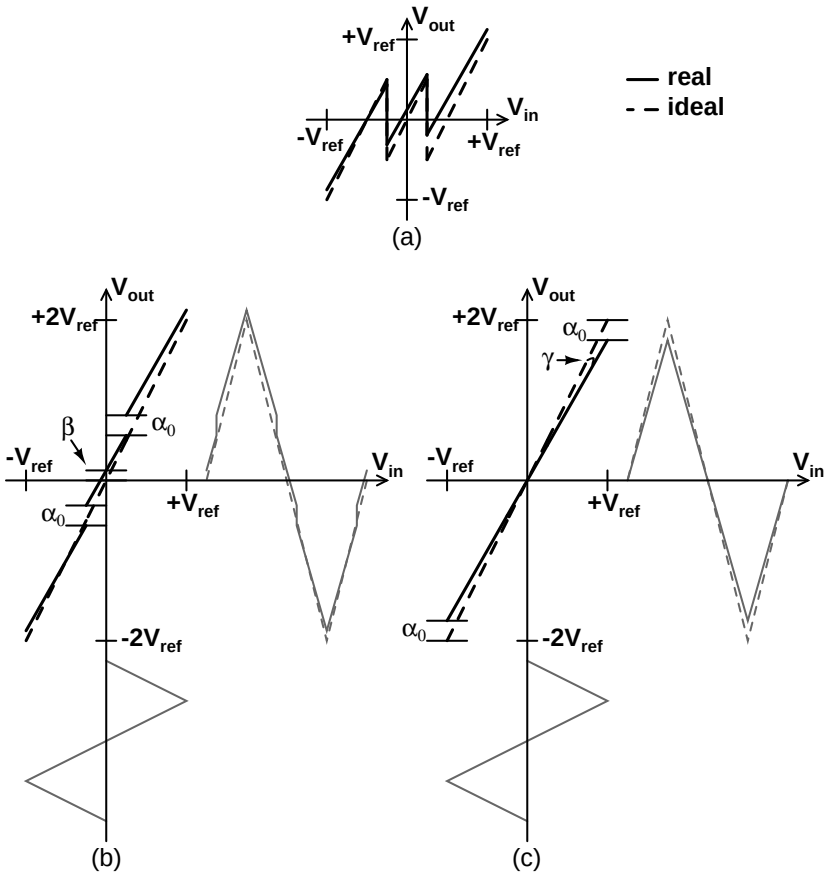

Figure 7.1 Effects of the MDAC nonidealities (a) on the transfer function of a 1.5-bit stage and on its reconstructed linear transfer curve (b) before and (c) after linearizing.

gether with the finite DC-gain of the amplifier also result in a deviation from the ideal step size of V_{ref} at the comparator threshold levels. Additionally, the offset voltage of the opamp and the charge injection from switches cause a constant offset in the transfer function.

To illustrate the effect of these errors, a reconstructed linear transfer curve and distortion of an example signal are shown in Fig. 7.1(b) for the same 1.5-bit stage than above. Reconstruction is performed by adding ideal reference voltage values $\mp V_{ref}$ to the stage output in the regions where the MDAC subtracts $\pm V_{ref}$. Two discontinuities with an equal step size of α_0 are located at the comparator threshold levels and the whole transfer curve is shifted by an offset of β. The discontinuous nonlinear transfer function distorts the triangular test signal as depicted in Fig. 7.1(b). After linearizing the stage transfer curve by adding and subtracting a correction term equal to α_0, de-

pending on the section, and by subtracting the offset β, the transfer curve of Fig. 7.1(c) results. This corresponds to the operation principle of the most existing calibration algorithms. It is noticeable that even though the transfer curve is linearized, a constant gain error remains, indicated with γ in Fig. 7.1(c). However, this gain error does not deteriorate the accuracy of the ADC but results only in an erroneous absolute amplitude of the quantized signal and is normally of no importance. This is also visible in the triangle test signal. Similarly, the offset can be left uncorrected and a small headroom can be reserved for it to avoid overflow in the stage outputs. However, in case of the parallel time-interleaved pipeline ADCs, both the gain and offset between the channels must be corrected as discussed in the previous chapter.

The output of each stage must settle within the accuracy of the remaining pipeline ADC during half of a clock cycle. The settling errors of all the pipeline stages reduced to the input of the whole converter must be below LSB/2, which corresponds to the condition

$$\varepsilon_{tot} = \frac{\varepsilon_1}{G_1} + \frac{\varepsilon_2}{G_1 \cdot G_2} + \ldots + \frac{\varepsilon_{k-1}}{\prod_i^{k-1} G_i} < \frac{1}{2^{N+1}}, \tag{7.5}$$

where G_i is the gain of the i^{th} stage, ε_i the combined settling error of its output resulted from the factors given above, and N is the ADC resolution. In Eq. 7.5 one important property of the pipeline A/D converter architecture is also manifested, i.e. the accuracy requirement is most stringent for the front-end stages while the settling error of the back-end stages is reduced by the preceding gain. Therefore, if calibration is needed for the target resolution, only the front-end stages have to be linearized. Furthermore, high-resolution front-end stages with large interstage gain G_i relax the accuracy requirements of the back-end stages leading potentially to low power dissipation. On the other hand, the opamp feedback factor is halved with each additional bit and comparator offset specifications are tightened with increasing stage resolution, setting an upper limit for the resolution of the front-end stages. From Eq. 7.5, the need for trimming or calibration can be calculated for a certain capacitor and reference voltage mismatch, set by the process variations, and for a given amplifier performance including the open loop DC-gain and offset voltage.

Linearizing the stage transfer functions as described above can be realized by applying either trimming as a part of the fabrication process or by employing analog or digital calibration. In fact, as the IC processes have evolved, different calibration methods have gained much more popularity than trimming, which is usually more expensive and less flexible.

7.2 Calibration Methods

A wide variety of calibration techniques to linearize the transfer function of a pipeline ADC has been proposed. The basic idea in these methods is to minimize or correct the steps causing discontinuities in the stage transfer functions. The mismatch and error attached to each step can either be averaged out, or their magnitude can be measured and corrected. In the former case, either the error can be corrected or the error energy is spread as evenly as possible over the full bandwidth, while in the latter case the error energy is always minimized. The first calibration methods proposed were analog and based on trimming. However, digital methods have gained much more popularity, mainly because of the increased computational capacity, their good and well predefined accuracy, and flexibility. Analog calibration methods include in this context the techniques in which adjusting or compensation of component values is performed with analog circuitry, while the calculation and storing of the correction coefficient can be digital. Besides the coarse classification to error-averaging, analog, and digital calibration methods, the techniques can be divided into foreground and background methods, depending on whether the normal operation is interrupted or not.

The pipeline A/D converter architecture offers an interesting benefit for realization of calibration: the back-end pipeline can be used to measure the errors of the front-end stages. This so-called self-calibration principle is utilized in the majority of the calibration algorithms. A lot of power and area can be saved if the accuracy of the back-end stages is good enough for self-calibration avoiding the use of a high precession reference or measurement ADC.

7.2.1 Capacitor Error Averaging

By using error-averaging techniques, compact nonlinearity compensation methods without calibration cycle can be realized. A relatively simple technique, called capacitor error averaging, was proposed in [1]. The basic idea in the capacitor error averaging is, rather than fix the sampling and feedback capacitors in the MDAC, to swap their roles. By adding an extra clock phase, during which the sampling and feedback capacitors are interchanged, the gain error resulting from the mismatch between the feedback capacitor and sampling capacitors is compensated, as indicated in Fig. 7.2. The capacitor error averaging is very sensitive to amplifier nonidealities as well as charge injection. The complexity of MDAC realizations is also increased requiring, for example, an extra amplifier and a three-phase non-overlapping clock.

Alternatively, the roles of the capacitors can be commutated in the different segments of the stage transfer function. Depending on whether the feedback capacitor

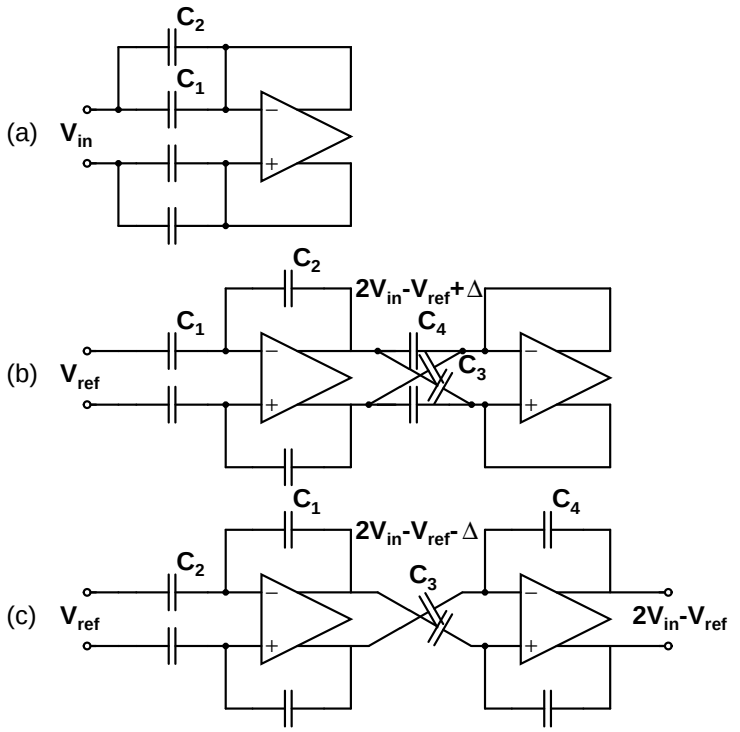

Figure 7.2 Capacitor mismatch error-averaging technique: (a) sampling phase, (b) amplification phase, and (c) decision phase [1].

swapping is systematic [2, 3] or random-like, employing actually dynamic element matching (DEM) [4], missing codes at the segment borders are changed into a fixed-pattern or pseudo-random noise, respectively. Consequently, the differential nonlinearity (DNL) is reduced significantly, but the integral nonlinearity (INL), as well as the signal-to-noise and distortion ratio (SNDR), is not improved. Thus, this method is most suitable for imaging applications. In most cases, capacitor error averaging also requires a lot of extra hardware.

To further reduce the DNL, dithering can be combined with the capacitor error averaging or DEM [4]. In dithering, a pseudo-random value is subtracted from the analog input, and later added digitally in an error correction adder. This results in an averaging or smoothing effect of the code errors. Many other improvements and variations to the capacitor averaging technique have been proposed [5, 6].

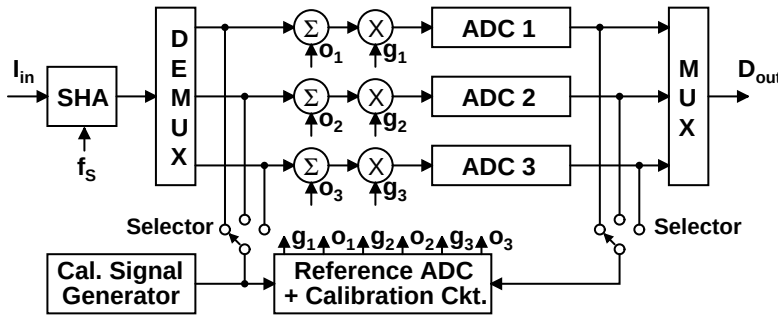

Figure 7.3 Block diagram of the analog background calibrated ADC system [11].

7.2.2 Analog Calibration Methods

The first self-calibration techniques introduced employed digital calibration coefficient calculation using the back-end pipeline ADC to measure the code errors causing component mismatch, while the correction was made in analog domain. A straightforward method is to measure the mismatch of each capacitor in an MDAC and store them in memory during the calibration cycle. During normal operation, they are read from the memory to be subtracted in the analog domain using a calibration DAC in parallel with the MDAC [7]. Alternatively, the sampling capacitors of an MDAC can be compared with the integration capacitor one by one and adjusted to the correct setting by utilizing small trim capacitors attached to each sampling capacitor [8, 9]. A similar technique has been adopted for MDACs employing current mode references instead of capacitors [10]. Even though a very good performance has been achieved with these methods, they employ complex algorithms and require a high precision calibration DAC or trim capacitor matrix.

In [11], an analog calibration method has been proposed for time-interleaved pipeline A/D converters using a mixed-signal adaptive loop. The least mean square (LMS) loop adjusts the gain and offset of the ADC channel through analog integrators until the error power between the ADC under calibration and the reference ADC is minimized. A block diagram of a time-interleaved ADC system employing the adaptive analog calibration loop is shown in Fig. 7.3. The calibration algorithm operates in the background for one pipeline channel ADC at a time, while the other two perform the normal time-interleaved operation. The resolution achieved is 10 bits at 20 MS/s channel clock rate [11].

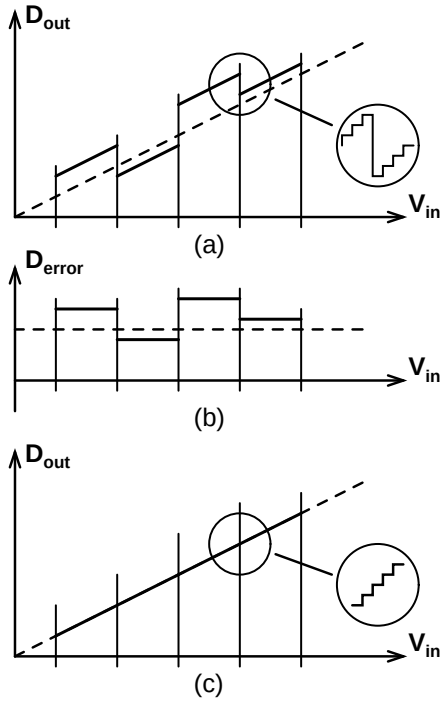

Figure 7.4 Digital-domain code error calibration principle: (a) uncalibrated transfer curve, (b) digital errors, and (c) transfer curve after code error calibration [12].

7.2.3 Digital Calibration Methods

As discussed above, because of the limited component matching accuracy of a capacitive MDAC, nonlinearity results at the major code transitions. As a result, if less significant digital output codes of an ADC are grouped as segments, each segment is dislocated by a certain amount from the ideal straight line, as shown in Fig. 7.4(a). The digital amounts of dislocation, measured from the ideal line, can be defined as code errors, indicated in Fig. 7.4(b). That is, the erroneous segments can be moved back to the straight line by digitally subtracting the amount of dislocation from each digital output occurring in that range as in Fig. 7.4(c). The amounts of dislocation are directly measured during the calibration cycle and stored in the memory. During normal operation, these code errors are addressed and recalled using the raw digital outputs of the calibrated stage. This principle is the basis of digital calibration [12, 13]. If the first stage is not the only stage calibrated, the effect resulted from the gain error remaining after the calibration can be minimized using a gain proration technique [14].

Based on the same principle, a simple digital self-calibration technique for multiple stages employing 1-bit resolution was presented in [15]. The principle of the method is

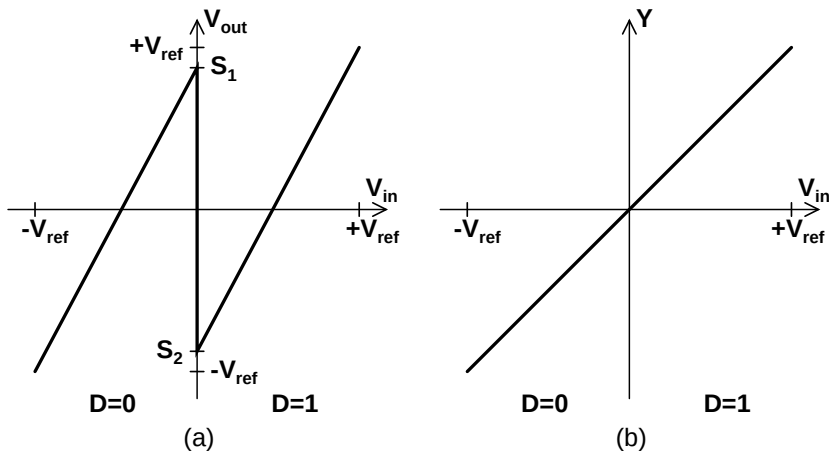

Figure 7.5 Principle of digital self-calibration (a) error coefficient measurement and (b) missing code elimination [15].

depicted in Fig. 7.5. The sub-ADC outputs D and raw digital outputs X are presented for the calibration logic, along with calibration constants S_1 and S_2, identified in Fig. 7.5(a). According to the calibration algorithm the corrected stage output Y are

$$Y = X, \, if \, D = 0 \tag{7.6}$$

and

$$Y = X + S_1 - S_2, \, if \, D = 1. \tag{7.7}$$

In order to avoid overflow of the stage output because of comparator offset and possible positive gain error, the interstage gain is set below the nominal value of 2. The correction term S_1 is determined by setting the analog input to zero and forcing the MDAC input to 0. The value of the stage analog output, measured using the back-end pipeline, in this condition, is equal to S_1. In an analogous manner, S_2 is determined by forcing the MDAC input to 1. By aligning points S_1 and S_2 the calibration accounts for capacitor mismatch, charge injection, and finite operational amplifier gain. After the calibration of the least significant stage is accomplished, the calibration of higher-level stages can proceed until the first stage. It should be noted that extrapolation of the algorithm to cover higher stage resolutions introduce a difficulty of producing accurate reference voltages at the respective comparator threshold levels. Both of the described digital calibration methods utilize a very simple algorithm, have the flexibility of digital signal processing, increase only the digital domain complexity, and have provided good experimental results [12, 15].

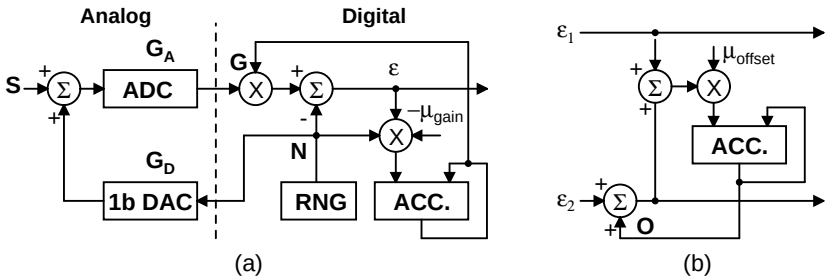

Figure 7.6 Block diagrams of digital calibration of parallel pipeline ADCs: (a) gain error calibration and (b) offset calibration system of two interleaved ADCs [19].

Instead of directly measuring the code errors, statistical methods can be applied for a large amount of output samples of a pre-determined input to digitally determine correction coefficients. These methods include two-dimensional look-up tables, sine wave fitting, and histogram based algorithms. The method, referred as 'phase plane compensation', uses a 2-D error table [17]. The addresses of the table are either the current sample and an estimate of the associated derivative, or the current sample and the prior sample. Errors for filling the table are determined by collecting a large number of samples of uncorrected ADC output for input sine waves with a range of different amplitudes and frequencies. Alternatively, histograms of sinusoidal input signals can be used to obtain estimates of expected error for each state of the ADC, which in turn provide least square curve fits of error-versus-slope [18]. Statistical methods offer dynamic error correction when extensive computation and memory capacity are available. One of the main challenges in these algorithms is the selection of proper test signals for fast convergence of the correction table coefficients.

The gain and offset errors between two parallel channels in time-interleaved pipeline A/D converters can be accomplished adaptively with a digital self-calibration algorithm presented in Fig. 7.6 [19]. A pseudo-random number N converted to analog with a 1-bit DAC is added to the input S of the ADC and later subtracted at the digital output, taking the resulting difference ε as ADC output. When ε is multiplied with the same pseudo-random number N, the contribution of signal S is averaged out and only a term proportional to the gain error between G_A and G_D results. Using the LMS algorithm, a gain correction term G can be iteratively updated. The offset correction term O between two parallel channels can be similarly calculated according to Fig. 7.6(b). Consequently, the nonlinearity resulting from capacitor mismatch is not corrected. Another drawback of this method is the reduction of the signal dynamic range because of the noise signal added to the ADC input.

7.2.4 Background Calibration

In some applications, where the calibration coefficients drift significantly with the time because of temperature variations, for example, and no idle time exists in the system to update the coefficients, the calibration measurements must run in the background without interrupting the normal operation. Typically, the background calibration techniques are developed from the same algorithms as the foreground methods by adding redundant hardware or software to perform the calibration coefficient measurements transparent to the normal operation. On the other hand, some algorithms are originally intended for background operation. A typical example of the first approach is the analog self-calibration of time-interleaved ADCs requiring an extra channel [11]. Alternatively, an extra stage and stage commutation between the first two and the extra stage can be utilized [20]. If the converter input is sampled by an S/H circuit slower than the clock rate of the ADC, part of the conversion cycles can be continuously used for calibration measurements [21]. Furthermore, some of the ADC output codes can be taken for calibration, while the missing samples are digitally interpolated [22].

An example of the second type of the background calibration concepts has been demonstrated using a resistor string DAC, calibrated by a highly accurate first-order $\Delta\Sigma$ converter, which measures resistor ratio errors [23]. Another example of a transparent calibration method is the adaptive digital gain and offset correction technique for parallel pipeline ADCs discussed in the previous section [19]. It should also be noticed that the capacitor error-averaging techniques could be classified as background correction methods. In general, the maximum sample rate and attainable resolution are equal for foreground and background calibration techniques, while the latter approach ends up with more complex realizations requiring redundant hardware or excessive digital signal processing.

7.2.5 Timing Error Calibration

Signal-dependent nonlinearity resulting from skew in the sampling clocks of the parallel channels in a time-interleaved A/D converter was discussed in chapter 6. A front-end S/H circuit was provided as a typical solution to omit these timing errors. However, as the sample rate is increased, the settling time of the S/H circuit, as well as the tracking time of the channel inputs, decrease and start to limit the conversion rate. Recently, calibration methods to compensate timing error effects have been proposed. Fully digital methods using either complex calculation in frequency domain [24] or interpolation in time domain [25] have been presented. In both of these methods, the actual timing skew between the channels must be known, which is actually the most challenging

part of the calibration: the performance increment is determined by the accuracy of the timing skew estimation. To measure the timing offsets, in the first algorithm, a frequency domain approach is used, in which the offsets are calculated from a sine wave test signal using inverse Fourier transform [26]. The second algorithm proposes a background method to extract the clock skew from an additive ramp signal injected to the ADC input. According to simulations, the estimation accuracy is enough for a 14-bit resolution.

An adaptive digital algorithm for timing skew correction is presented in [27]. By using a chopper-based offset calibration, the adaptive gain calibration [19], and a phase detector for the adaptive timing error calibration, a resolution of 10 bits at 120 MS/s is achieved.

Instead of using digital signal processing to the output data, timing errors between the ADC channels can be corrected in the analog domain by adding digitally controllable delay elements to the sampling clocks of each channel [26]. However, the timing skew has to be known prior to the correction. Using this approach, a resolution of 8 bits at an input sample rate of 4 GS/s has been achieved for 32 parallel channels [28].

7.2.6 Calibration Methods: Summary

As presented in this section, a huge variety of error-averaging and calibration techniques exist. Comparison of the different techniques is difficult because of different target applications, resolutions, ADC topologies, processes, etc. It is evident, however, that some calibration (or error-averaging) method has to be exploited to enhance the resolution of a pipeline ADC above the limit set by device matching. This is illustrated in Fig. 7.7, in which the recently published pipeline A/D converters are compared based on weather they employ calibration or not. It can be directly noticed that excluding two ADCs all the other pipeline ADCs achieving an ENOB of 10 bits or more utilize some kind of calibration. The effect of calibration on the figures of merit describing the energy and area efficiency, derived in chapter 2, can be derived from Fig. 7.8: calibration does not have any clear effect on the energy per conversion step but, obviously exceeds the area because of the extra hardware. The improvement in performance varies between different techniques and within the realizations. In general, the static linearity describing INL is reduced by 0.5 LSB up to tens of LSBs, while the dynamic linearity determining SFDR and SNDR are improved by 10–30 dB, corresponding to a resolution enhancement of 1.5–5 bits.

Tab. 7.1 shows a coarse comparison of the presented error-averaging and calibration techniques based on the classification made earlier in this chapter. It should be noted that there are significant differences between the realizations as well as improvements

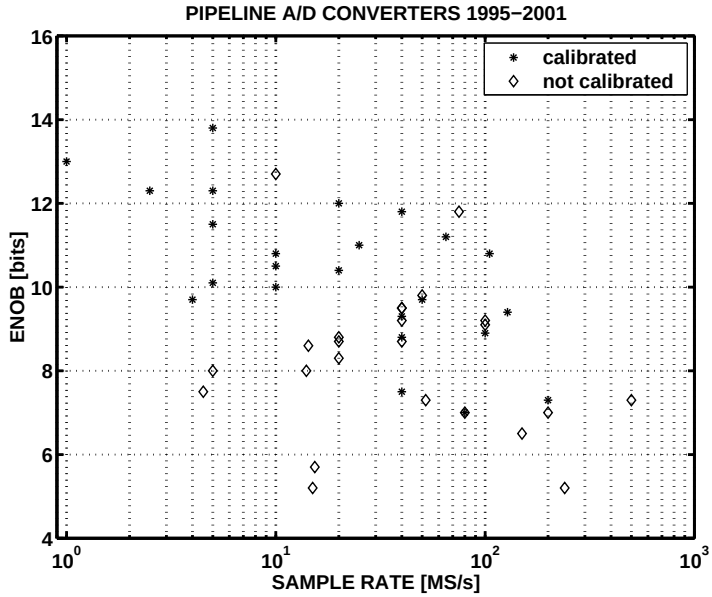

Figure 7.7 Effective number of bits as a function of sample rate for the recently published pipeline A/D converters.

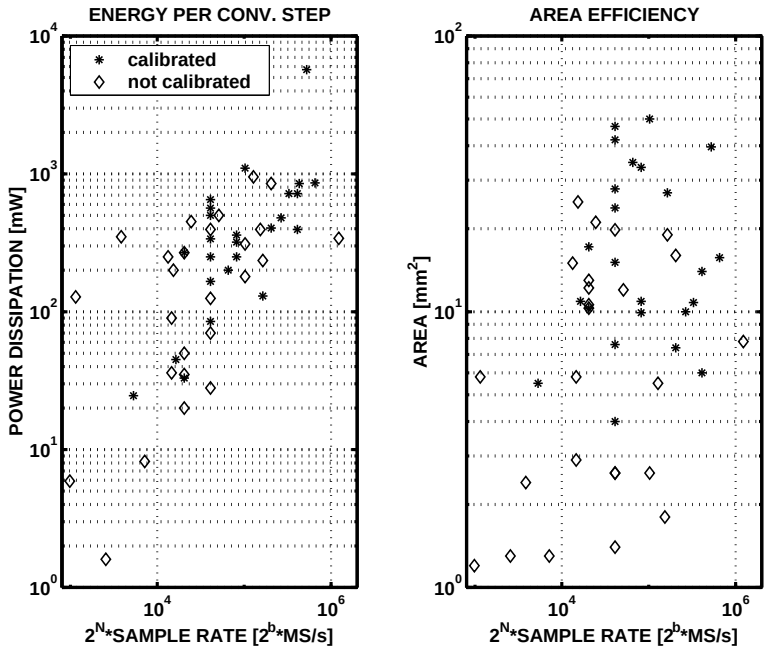

Figure 7.8 Figures of merit for the recently published pipeline A/D converters.

Table 7.1 Comparison of the calibration methods.

	Cap. Error Averaging	Analog Cap. Trimming	Digital Code Calibration	Digital LMS	Statistical Methods
Performance Improvement	+	+	+	+	++
Complexity	-	-	++	-	–
Power Dissipation	+	+	+	+	-
Area	+	-	++	+	-
Flexibility	-	+	+	-	++
Max. Speed	-	++	++	+	++

to the basic methods affecting the comparison. The digital code error calibration having no severe drawbacks usually leads to good performance. However, in most cases the choice of calibration technique is application specific.

7.3 Developed Digital Self-Calibration

As discussed in section 7.1, the static errors requiring calibration in a high-resolution switched-capacitor pipeline ADC include gain and nonlinearity errors inherited from capacitor mismatch, finite open loop DC-gain and offset of the operational amplifier, and charge injection from switches. It is assumed that comparator offsets are compensated by the RSD correction. Of the previously reported calibration methods, the digital self-calibration algorithms proposed in [12, 13, 14, 15] offer a good starting point for the development of a simple, area and power efficient calibration algorithm aiming for a 14–16-bit resolution with a pipeline, or algorithmic ADC. The basic idea in these methods is to measure the errors attached to each segment of the stage transfer function, store them in a memory and subtract these errors from the ADC output during the normal operation. The calibration proceeds from the least significant stage to be calibrated towards the first stage. However, there are some problems when applying these techniques to multi-bit unit capacitor MDACs. For example, the method introduced in [12] is intended for binary weighted capacitor arrays and the generation of input signals at the comparator threshold levels of a multi-bit pipeline stage that are required for the method proposed in [15] is power and area consuming.

7.3.1 Capacitor Mismatch Correction

In the developed calibration method, the error attached to each reference unit capacitor is measured separately, exploiting an extra capacitor and using the back-end pipeline

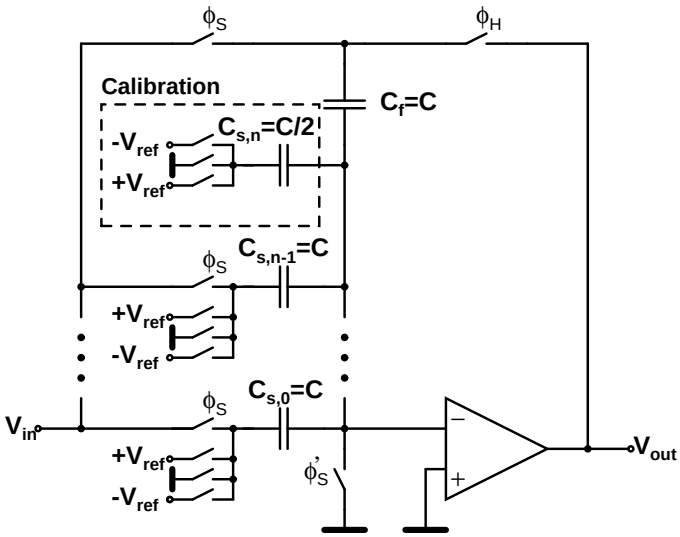

Figure 7.9 A unit capacitor MDAC employing the proposed calibration method.

with enhanced resolution as an error quantizer. The correction coefficients for the stage output codes, including the offset, can be cumulatively calculated from these measurements. The algorithm simultaneously takes into account the effects of the finite open loop DC-gain of the opamp as well as the reference voltage mismatch. Multiple stages can be calibrated one at a time proceeding from the least significant stage to be calibrated towards the higher-level stage. Since the main objective of the developed calibration method was to correct the errors resulting from capacitor mismatch, the explanation and analysis below concentrates on this aspect. The effect of other error sources is handled briefly at the end.

7.3.2 Calibration MDAC

The schematic of a general unit capacitor MDAC employing the proposed calibration method is shown in Fig. 7.9 as a single-ended configuration for simplicity. The calibrated MDAC utilizes, in addition to the $n-1$ sampling capacitors $C_{s,k}$ and feedback capacitor C_f of a conventional capacitive multiplying D/A converter, an extra calibration capacitor $C_{s,n}$, the size of which is half of the unit capacitance. The principle of the operation in the sample and hold mode is depicted in Fig. 7.10. The stage under calibration always samples the signal ground voltage. When measuring the mismatch attached to capacitor $C_{s,0}$ for negative inputs, in the hold mode, the capacitor $C_{s,0}$ is connected to $-V_{ref}$, while the extra calibration capacitor is connected to $+V_{ref}$ and the

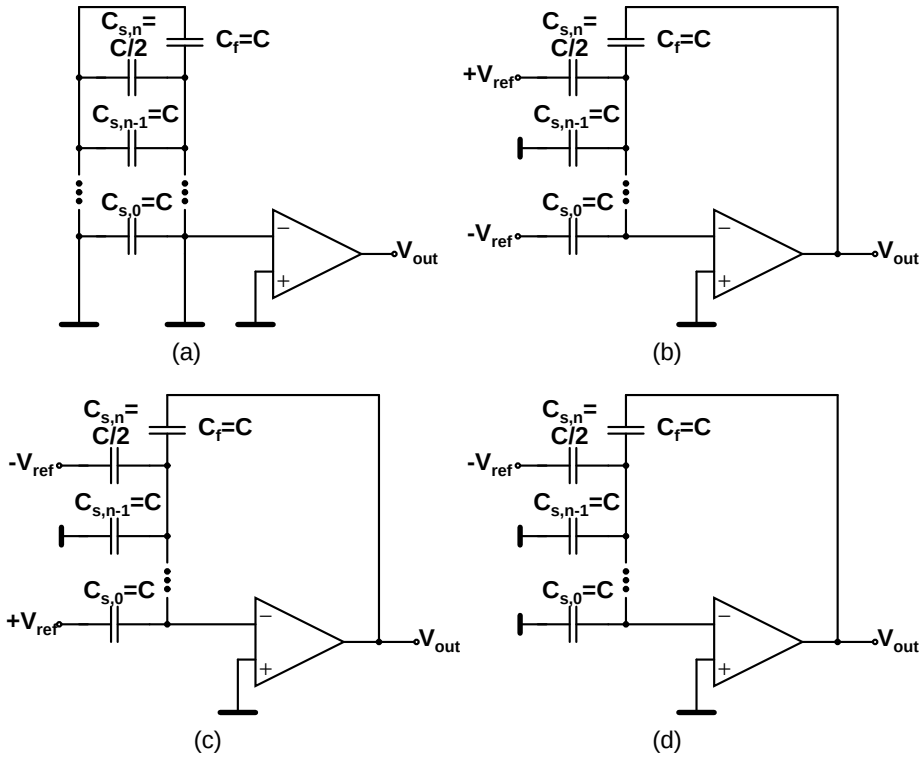

Figure 7.10 The unit capacitor MDAC during the error measurements (a) in the sample mode, in the hold mode when measuring capacitor $C_{s,0}$ for (b) negative and (c) positive inputs, and (d) calibration capacitor $C_{s,n}$ for negative input values.

other capacitors to ground, as shown in Fig. 7.10(b). The deviation of the MDAC output from the ideal, $+V_{ref}/2$ in this case, is measured using the back-end pipeline ADC. The errors attached to the other sampling capacitors $C_{s,1} \ldots C_{s,n-1}$ for negative inputs can be similarly determined. The corresponding errors attached to positive inputs can be measured by changing the polarity of V_{ref} to which the sampling capacitors are connected during the hold mode, shown in Fig. 7.10(c). In a differential MDAC, the stage offset can be simultaneously determined by combining the measurement results for the negative and positive inputs. The capacitor errors excluding the offset are ideally equal in magnitude but have the opposite polarity. Finally, the error of the calibration capacitor $C_{s,n}$ can be measured by connecting only this capacitor either to $-V_{ref}$ or to $+V_{ref}$ in the hold mode, as depicted in Fig. 7.10(d).

In general, when measuring the mismatch $\Delta C_{s,k}$, attached to the capacitor $C_{s,k}$, for

negative input voltages, the MDAC output is given by

$$V_{out,k-} = \frac{C'_{s,k} + \Delta C_{s,k} - C'_{s,n} - \Delta C_{s,n}}{C'_f + \Delta C_f} V_{ref} + \frac{\sum_{j=0}^{n} \left(C'_{s,j} + \Delta C_{s,j} \right) + C'_f + \Delta C_f}{C'_f + \Delta C_f} v_{os}$$

$$= \frac{1}{1+\delta} \left[\left(\frac{1}{2} + \frac{\Delta C_{s,k} - \Delta C_{s,n}}{C'_f} \right) V_{ref} + \beta v_{os} \right], \tag{7.8}$$

where $C'_{s,k} = C'_f = 2C'_{s,n} = 2C$ is the ideal unit capacitance, v_{os} is the offset voltage at the amplifier input, $\delta = \Delta C_f / C'_f$ is the relative error of capacitor C_f, and β is a constant amplification term of the offset voltage given by

$$\beta = 1 + \frac{\sum_{j=0}^{n} (C_{s,j} + \Delta C_{s,j})}{C'_f + \Delta C_f}. \tag{7.9}$$

The resulting deviation of the output from the ideal $V_{ref}/2$ is measured and quantized with the back-end pipeline. Similarly, the error $\Delta C_{s,n}$ attached to the calibration capacitor $C_{s,n}$ can be measured resulting in an MDAC output voltage of

$$V_{out,n-} = \frac{C'_{s,n} + \Delta C_{s,n}}{C'_f + \Delta C_f} V_{ref} + \frac{\sum_{j=0}^{n} \left(C'_{s,j} + \Delta C_{s,j} \right) + C'_f + \Delta C_f}{C'_f + \Delta C_f} v_{os}$$

$$= \frac{1}{1+\delta} \left[\left(\frac{1}{2} + \frac{\Delta C_{s,n}}{C'_f} \right) V_{ref} + \beta v_{os} \right]. \tag{7.10}$$

By adding up these results, the error attached to the calibration capacitor is eliminated and we get

$$\Delta V_{out,k-} = V_{out,k-} + V_{out,n-} = \frac{1}{1+\delta} \left[\left(1 + \frac{\Delta C_{s,k}}{C'_f} \right) V_{ref} + 2\beta v_{os} \right]. \tag{7.11}$$

When the same mismatch for positive input voltages $V_{out,k+}$is measured using the opposite polarity reference voltages, the offset term can be calculated from, for example, the calibration capacitor error measurements by

$$V_{os} = V_{out,n-} + V_{out,n+} = \frac{1}{1+\delta} 2\beta v_{os} \tag{7.12}$$

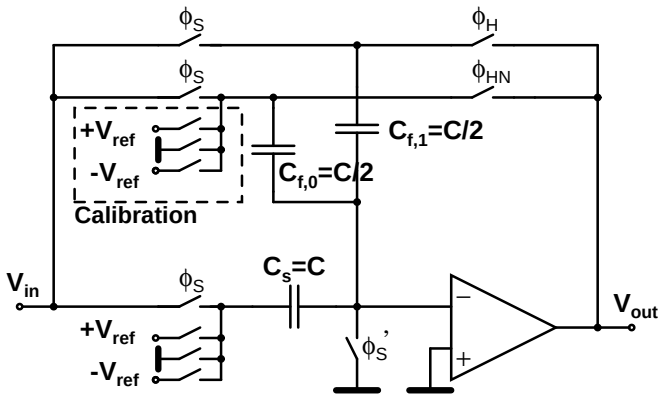

Figure 7.11 An 1.5-bit MDAC with enhanced gain.

and subtracted from Eq. 7.11 giving

$$\Delta V_{out,k-} - V_{os} = \frac{1}{1+\delta}\left(1+\frac{\Delta C_{s,k}}{C'_f}\right)V_{ref}. \tag{7.13}$$

The deviation of the quantized result of Eq. 7.13 from V_{ref} is taken as the code error attached to the capacitor $C_{s,k}$. The remaining gain error term δ, resulting from the feedback capacitor mismatch, introduces only a linear gain error and does not have to be corrected in a single-channel pipeline ADC. However, it can be corrected even using the same measurement results of the capacitor errors as described later.

Without the extra capacitor, the stage output during the measurements would be either $\pm V_{ref}$, which would easily saturate the back-end stages in the presence of even small mismatches, or ± 0, which excludes the effect of the finite amplifier DC-gain and the reference voltage mismatch. Furthermore, the amplifier operates in this case on the same voltage swing range ($\pm V_{ref}/2$) as transfer function steps during normal operation, while in a differential multi-bit stage also the value of the offset voltage can be determined and added to the coefficients.

7.3.3 Enhanced Gain Stage

The output of the last calibrated stage falls near $\pm V_{ref}/2$ when its own capacitors are being measured, or in the vicinity of ± 0 during the measurement of the stages in front of it. Thus, the first stages of the back-end pipeline are actually used as amplifiers. If 1.5-bit stages are employed in the back-end pipeline, the resolution of the measurement can be enhanced by a factor of two simply by doubling the gain of the first 1.5-bit stage. This is accomplished by halving the MDAC feedback capacitor during the cali-

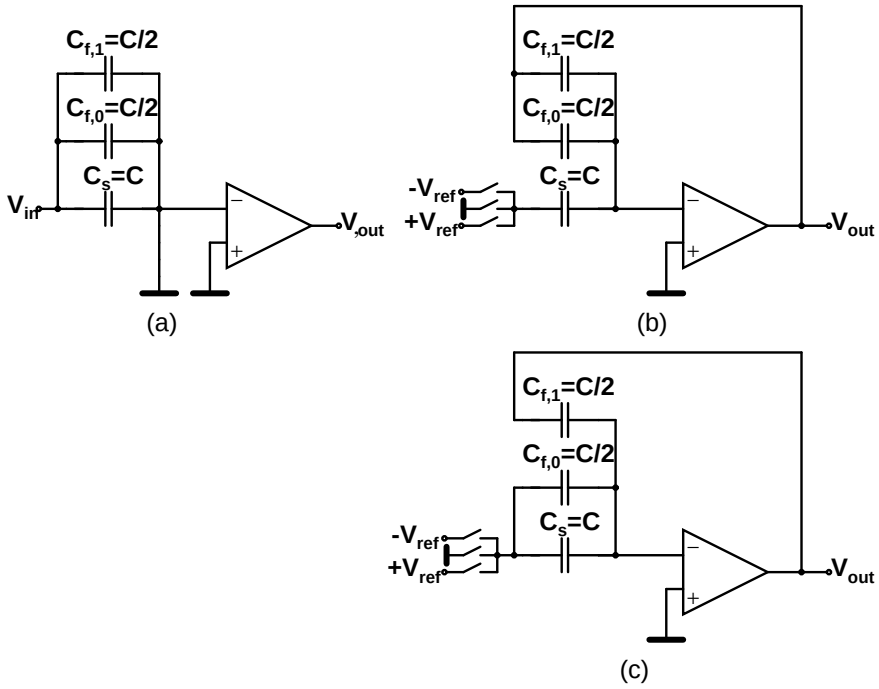

Figure 7.12 Enhanced gain stage in the (a) sample mode and hold mode (b) during normal gain-of-two operation and (c) employing gain-of-four.

bration, as shown in Fig. 7.11. Normally, the two halves are tied together, as indicated in Fig. 7.12(b), and used as a single feedback capacitor, but during calibration one half is connected in parallel with the sampling capacitor, Fig. 7.12(c), and its bottom plate is switched to the respective reference voltage. A doubling of the interstage gain can be utilized for the following back-end stages as well, until the expected error ranges exceed the allowed input range of the gain-of-four stage.

It is straightforward to derive that the transfer function is ideally given by

$$V_{out,i} = 4V_{in,i} - D_{sub} \cdot 2V_{ref}, \tag{7.14}$$

where D_{sub} is -1, 0, or $+1$ according to the binary sub-ADC outputs 00, 01, or 10, respectively. The resulting stage transfer function is depicted in Fig. 7.13 both during (a) the normal 1.5-bit/stage operation and (b) in the enhanced gain mode. Excluding all nonidealities, the stage output remains between the allowed voltage range of $\pm V_{ref}$ for input voltages limited to $\pm 3/4V_{ref}$, which is also the absolute maximum of the correction range. However, leaving some headroom for stage nonidealities affecting the transfer function, the allowed input range, and maximum correction range thereof,

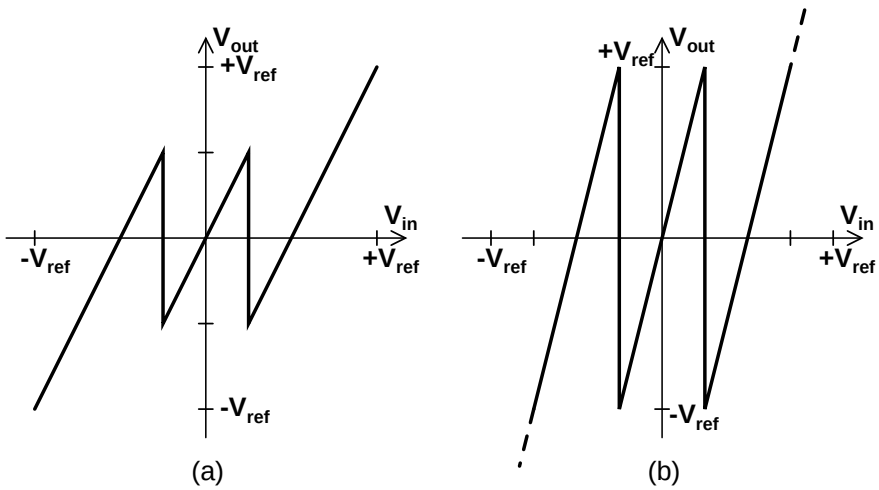

Figure 7.13 Transfer function of the enhanced gain stage (a) in the normal gain-of-two mode and (b) during the gain-of-four operation.

is given by

$$|V_{in,i}| < \delta V_{in,i} \tag{7.15}$$

and

$$|V_{in,i}| < \frac{V_{ref}}{2} + \delta V_{in,i}, \tag{7.16}$$

where the range $\delta V_{in,i}$ is determined by the combined effect of comparator offsets, capacitor mismatch, DC-gain and offset of the amplifier, charge injection, and reference voltage mismatch.

It should be noticed that the total gain error of the back-end pipeline ADC is different during the calibration measurements and normal operation because of mismatch between the feedback capacitor halves. However, the gain error is the same for all the calibration measurements and therefore does not deteriorate the calibration accuracy in case of a single-channel pipeline ADC.

7.3.4 Calculation of Calibration Coefficients

Following the switching scheme of the stage, correction coefficients for each stage output segment is cumulatively calculated from the measured capacitor errors. In Fig. 7.14, the switching scheme and principle of the coefficient calculation are shown for a 2.5-bit stage. As depicted, depending on the output of the sub-ADC none, one, two, or all three sampling capacitors are connected to the negative or positive reference voltage. By adding the measured code errors $k1-k3$ and $k5-k6$ attached to the unit capaci-

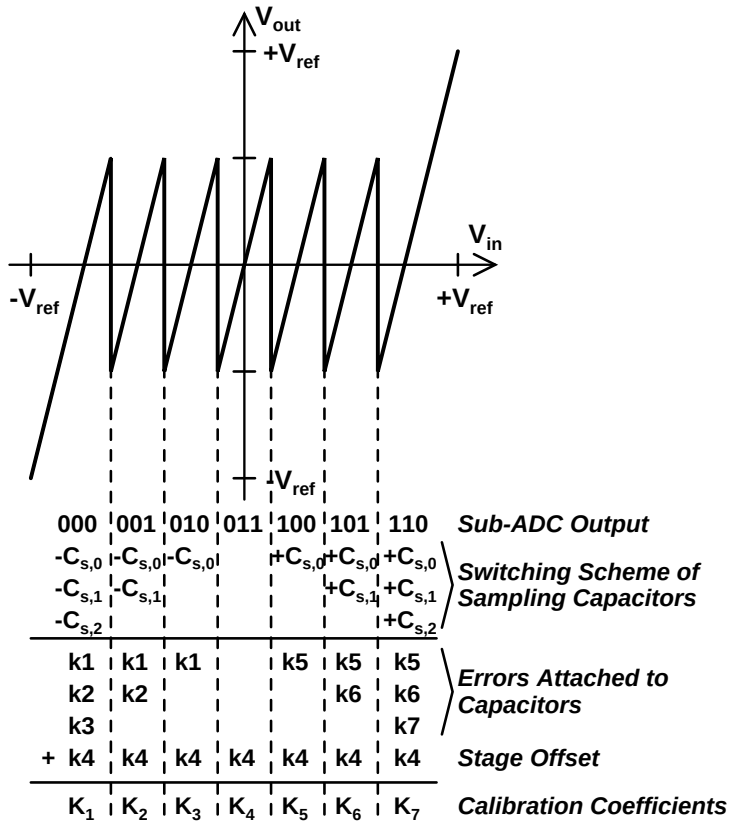

Figure 7.14 Calculation of the calibration coefficients for a 2.5-bit unit capacitor stage.

tors for negative and positive input voltages, respectively, and the offset term $k4$, the calibration coefficients $K_1 - K_7$ to be stored in a memory will result. During normal operation, the calibration coefficients are subtracted from the RSD corrected ADC output, the sub-ADC output of the calibrated stage serves as a memory address. The hardware required for calibration measurements and coefficient calculation includes a small state machine to control the MDAC switches, together with adders and logic to realize the simple calculation algorithm presented in subsection 7.3.2. During normal operation, a small memory and one adder per calibrated stage are required.

7.3.5 Gain Error Calibration

When considering calibration of a time-interleaved parallel pipeline ADC, the algorithm introduced above compensates for all the other static errors of the stage except the total gain error: the transfer function is linearized and offset removed. Reconsid-

ering the stage transfer function of a unit capacitor MDAC with capacitor mismatch, a simple gain error calibration algorithm can be derived. The erroneous transfer function rewritten from chapter 3 is given by

$$V_{out,i} = (n+\alpha)\cdot V_{in,i} - \sum_{j=0}^{n-1}(m_j\cdot(1+\alpha_j))\cdot V_{ref}, \tag{7.17}$$

where for the unit capacitor mismatches α_j hold

$$1+\alpha_j = \frac{1+\frac{\Delta C_{s,j}}{C}}{1+\frac{\Delta C_f}{C}}, \tag{7.18}$$

the total mismatch α being

$$\alpha = \sum_{j=0}^{n-1}\alpha_j. \tag{7.19}$$

From Eqs. 7.17–7.19 it can be seen that the gain error term α equals to the total capacitor mismatch error, which is also equal to the correction coefficients of the outermost sections of the transfer function. The error angle γ of the stage gain is given by

$$\gamma = \frac{\alpha}{V_{ref}}, \tag{7.20}$$

which can be graphically understood from Fig. 7.1(c) for a 1.5-bit stage ($\alpha = \alpha_1$). Using the digital ADC output codes, the gain error calibration coefficient is given by

$$K_G = \frac{K_{max} - K_{min}}{2^{N_{be}}}, \tag{7.21}$$

where K_{max} and K_{min} are the capacitor mismatch correction coefficients of the outermost code sections, and N_{be} is the resolution of the back-end pipeline ADC used to measure the errors. The combined gain error of all calibrated stages can be obtained by multiplying their individual gain errors. During normal operation, the total gain error of the converter can be corrected by multiplying the ADC output with the inversion of the combined gain error.

As one gain error calibration term per calibrated ADC channel is stored in a memory, only one extra multiplier is required for the algorithm during the normal operation. Furthermore, no extra error measurements are required and computation of the correction coefficients is very simple. However, measurement resolution enhancement cannot be accomplished with the gain-of-four stages: capacitor splitting introduces a gain error to the back-end pipeline, which is different during the calibration measurements and

normal operation.

7.3.6 Accuracy Considerations

The accuracy of the presented calibration method is limited by the accuracy of the uncalibrated back-end pipeline ADC, used to measure the calibration coefficients; the nonlinearity of the back-end must be below 0.5 LSB of its resolution N_{be}. This corresponds to the fundamental settling requirement of the stage output. Furthermore, to suppress digital truncation errors below the same level, at least one extra bit resolution has to be applied in the back-end part and the measurements, calculations, and adding of the calibration coefficients must be performed before reducing the ADC output code length to correspond its nominal resolution.

As the gain error calibration uses the same measurement results as the capacitor mismatch calibration, its accuracy has the same limitations as above. Furthermore, the total gain and offset errors of the back-end pipeline ADCs of different channels must be below 0.5 LSB of the measurement resolution. If this is not the case, one possible way of overcoming the limitation is to make additional measurements with cross-connected back-end ADC channels. From these measurements, the gain error between the back-ends can be extracted and canceled.

In principle, by adding more and more calibrated front-end stages, or by increasing the resolution of a single calibrated stage, the total resolution of a pipeline ADC can be raised well over the limit set by process matching. The calibration cycle must also proceed from less significant stages towards the most significant ones, or at least the stages joined to the measuring back-end, should be corrected with calibration before calculating the coefficient of the front-end stages. In a unit capacitor MDAC, each additional bit per stage doubles the number of capacitors, and the number of calibration measurements thereof. By applying calibration to more stages, the number of measurements and calibration coefficients are similarly doubled, while the increase in the total resolution is larger when multi-bit stages are used. That is, in the latter case with an equal increment in the complexity and duration of the calibration cycle, a larger enhancement in the total resolution results. Furthermore, the comparator offset specifications, as well as the feedback factor of the operational amplifier, are not affected. The maximal resolution that can be achieved from a pipeline ADC combined with calibration is in practice limited by the specifications of the first stage, tightening with the increasing resolution: the total capacitance must be increased because of the kT/C-noise, the opamp output settling accuracy must be better, jitter in the sampling clock has to be reduced, etc.

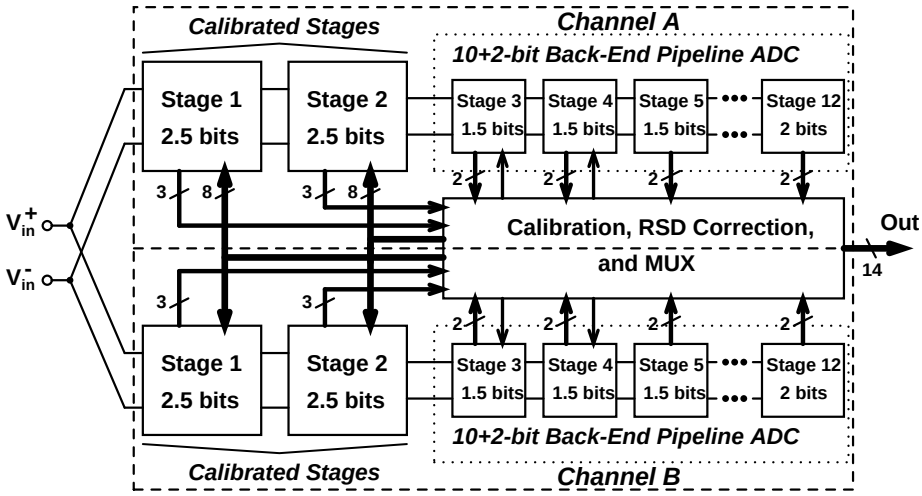

Figure 7.15 Block diagram of the parallel pipeline ADC topology used in the behavioral simulations.

7.3.7 Behavioral Model

To verify the operation of the developed digital self-calibration method, a behavioral model of pipeline A/D converters was constructed with Matlab. The non-ideal MDAC outputs follow Eq. 3.38. In addition to the static error sources of pipeline stages, including comparator offset voltages ($V_{os,c}$), capacitor mismatch ($\Delta C/C$), open loop DC-gain (A_0) and offset (v_{os}) of the operational amplifier, and reference voltage mismatch (ΔV_{ref}), the finite settling time was modeled through the amplifier gain-bandwidth (GBW) in the transfer functions. These parameters are individually set (opamp gain and bandwidth), or given as standard deviations of normal distribution (mismatches and offsets).

The topology used in the simulations is depicted in Fig. 7.15. It consists of two separately operating channels with a target resolution of 14 bits and sample rate of 80 MS/s. The ADC can also be configured as a two-channel time-interleaved pipeline ADC, which doubles the sample rate to 160 MS/s. The channel ADCs, employing RSD coding, consist of two 2.5-bit front-and stages, which can be calibrated with the proposed method, and of a back-end part of 1.5-bit stages. When the channels are separated, the two first 1.5-bit stages can be configured to gain-of-four stages and no gain calibration is performed. In the time-interleaved mode, all the back-end stages are identical and the gain error correction between the channels is activated. Two extra stages are added to get more accuracy during calibration measurements and reduce truncation errors during the calculations. The operational amplifiers of the first two

Table 7.2 Parameters used in the behavioral calibration simulations.

	2.5-bit Stages	1.5-bit Stages
A_0	95 dB	65 dB
GBW	1000 MHz	700 MHz
C	1.5 pF	1 pF
$\Delta C/C$	$\pm$0.25 %	$\pm$0.25 %
$v_{os}/2V_{ref}$	$\pm$0.5 %	
$V_{os,c}/2V_{ref}$	$\pm$2.5 %	

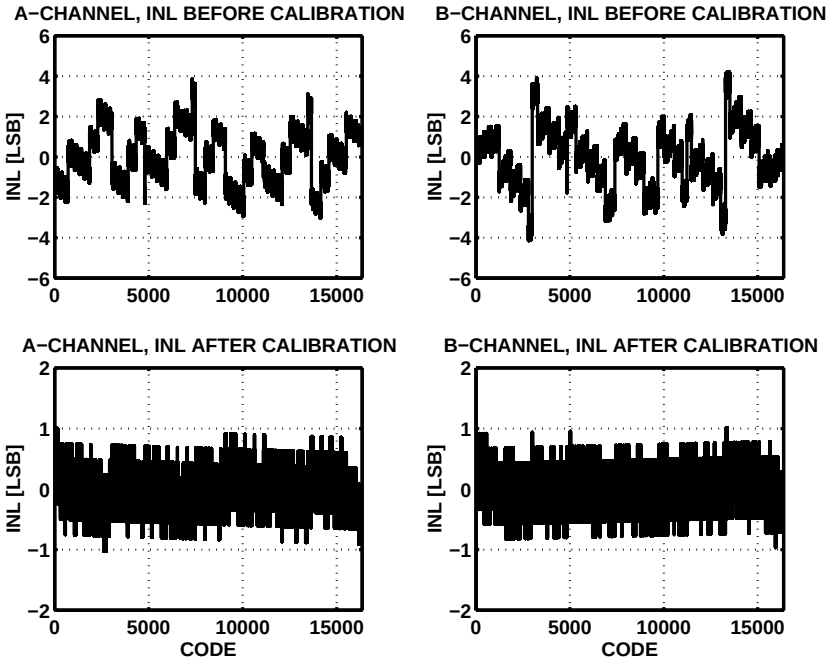

Figure 7.16 Typical INL plots of the channel pipeline ADCs before and after calibration.

stages were equal, while the opamp parameters of the back-end stages were also equal. The mismatch of the unit capacitors and offset voltages were set to values that should be easily achievable in sub-micron CMOS processes. The parameters and mismatches of the nonideal stages used in the simulations are presented in Tab. 7.2.

7.3.7.1 Simulation Results

Results from the behavioral simulations are first applied to the case when the model was applying the 14-bit 160-MS/s time-interleaved pipeline ADC architecture. Improvement in the static linearity as a result of the calibration was determined by calculating integral nonlinearity (INL) for the ADC output when a slowly increasing ramp signal,

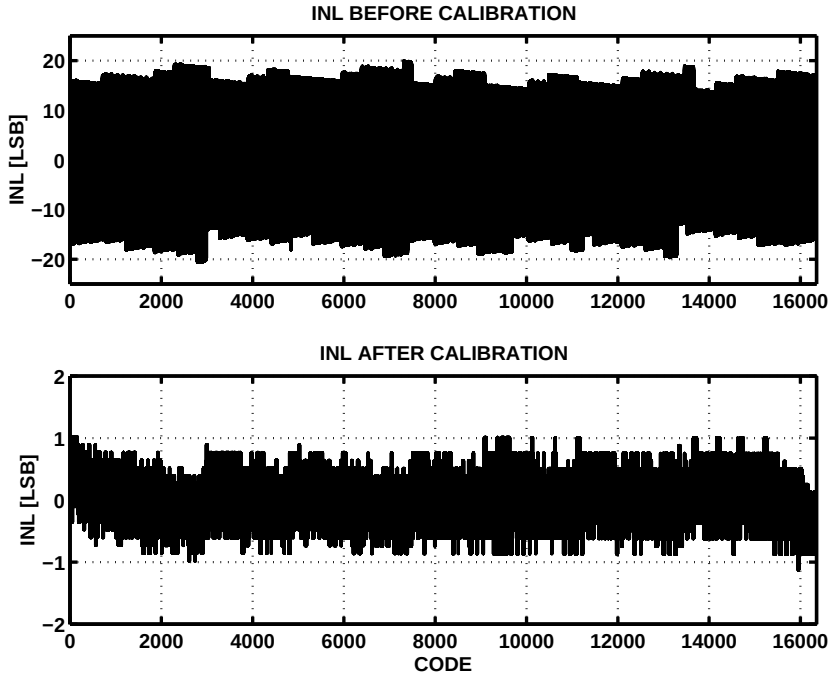

Figure 7.17 A typical INL of the total parallel pipeline ADC before and after calibration.

having ideally four samples per code in both channels, was applied at the input. In Fig. 7.16, typical INL plots of the channel ADCs are presented before and after calibration. Before calibration, the capacitor mismatch in the first and second stages is clearly visible as large steps resulting in an INL of 3.9 LSB and 4.2 LSB for the *A* and *B* channels, respectively. The calibration algorithm corrects the discontinuities, giving an INL of 1.0 LSB in both channels. The post-calibrated INL is limited by the capacitor mismatch of the back-end stages.

The INL plots of the whole parallel pipeline ADC for the same simulation as above are shown in Fig. 7.17. A relatively large offset mismatch between the channels results in very large static linearity errors, giving a post-calibrated INL of 20.5 LSB. The calibrated INL, being in the order of that of the channel ADCs, indicates that the offset and gain mismatch between the channels is sufficiently canceled.

The dynamic linearity was determined by examining spectra calculated with the Fast Fourier Transform (FFT) from the ADC output when a 74.5-MHz sinusoidal input signal with -1-dBFS amplitude is applied. The signal-to-noise and distortion (SNDR), and the effective number of bits (ENOB) thereof, are calculated using the sine wave fitting test. Typical spectra before and after calibration, for the same mismatch values

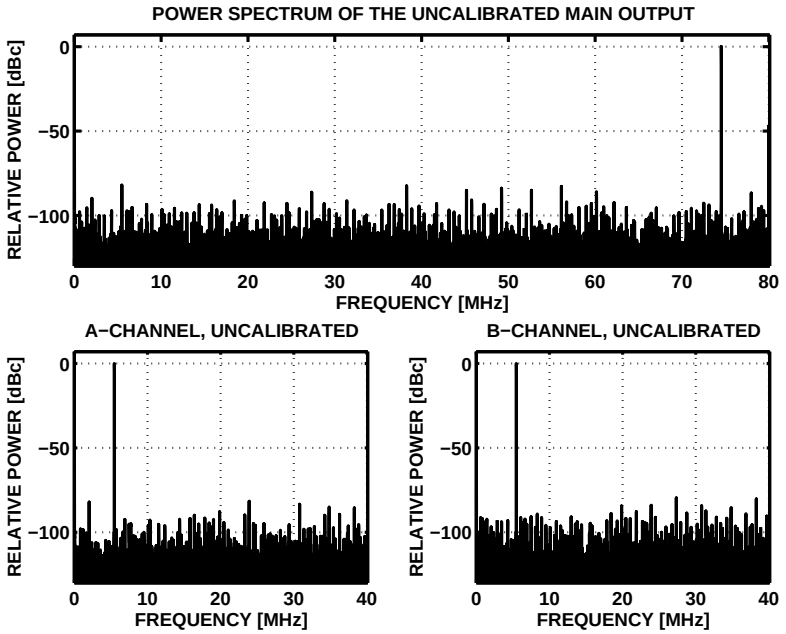

Figure 7.18 Power spectra of the parallel pipeline ADC and of its channels before calibration for a 74.5-MHz input signal at 160-MS/s.

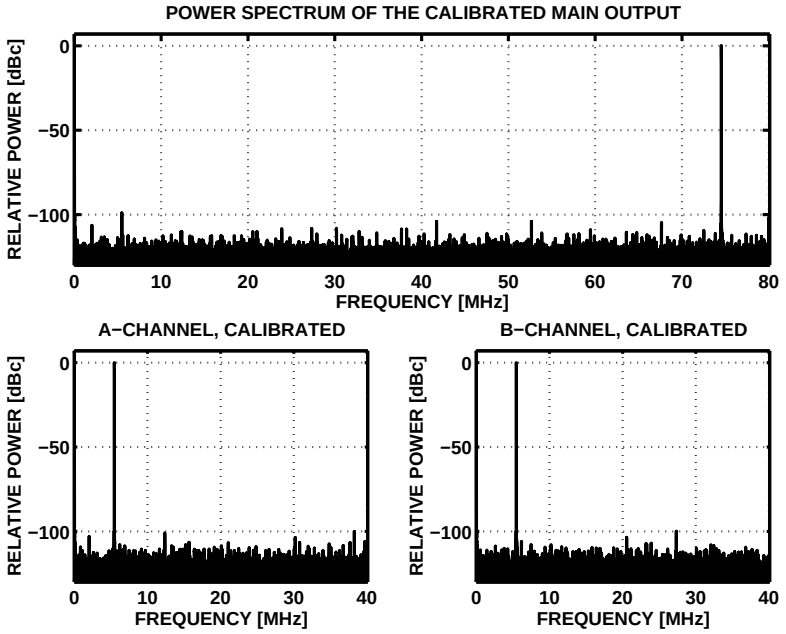

Figure 7.19 Power spectra of the parallel pipeline ADC and of its channels after calibration for the same signal as above.

Table 7.3 Summary of the behavioral simulation results.

		Uncalibrated	Calibrated
Channel ADC			
	INL	±4.2 LSB	±1.0 LSB
	SFDR	80 dB	100 dB
	SNDR	71 dB	83 dB
	ENOB	11.5 bits	13.6 bits
Parallel ADC			
	INL	±20 LSB	±1.1 LSB
	Offset	-47 dBc	-102 dBc
	Gain Mismatch	-82 dBc	-99 dBc
	SNDR	50 dB	83 dB
	ENOB	8.0 bits	13.6 bits

as the INL simulations, are shown in Figs. 7.18 and 7.19, respectively. A spurious free dynamic range (SFDR) improvement of more than 20 dB is visible in the channel ADCs and the noise floor is reduced from about 90 dB to the vicinity of 110 dB as well. Similarly, the peak at the Nyquist frequency resulting from offset mismatch and the parasitic side band at the mirror frequency are suppressed from -47 dBc and -82 dBc to -99 dBc and -102 dBc, respectively. The simultaneous enhancement of SNDR is from 50.1 dB to 83.4 dB, which corresponds to a 5.6-bit improvement in ENOB from 8.0 bits to 13.6 bits. It should be noted that the uncalibrated performance of the time-interleaved ADC has a large variation depending on the mismatch between its channels.

The simulation results are summarized in Tab. 7.3. The tabled values are typical results for the given opamp parameters and capacitor mismatch. As a conclusion, the proposed calibration method suppresses the errors resulting from 10-bit matching sufficiently to achieve 14-bit accuracy with a time-interleaved pipeline A/D converter. According to the simulations, for a single-channel pipeline ADC, in which the first two back-end stages employ the gain-of-four operation during the calibration measurements, 14-bit accuracy can be achieved with only one extra 1.5-bit stage in the back-end part. The static and dynamic linearity improvements are only a few percentage points better than for the channel ADCs of the parallel pipeline architecture but the power dissipation and area of one stage is benefited.

7.4 Application Case I: A Self-Calibrated Pipeline ADC with 200MHz IF-Sampling Front-End

7.4.1 Introduction

The increasing bit rates in both wired and wireless telecommunication systems are made possible by utilizing wider signal bandwidths. Simultaneously, there is a desire to realize an increasing portion of the receiver functions in the digital domain. These trends lead to more and more demanding specifications for A/D converters. Typically, a resolution from 12 to 15 bits is needed at input signal frequencies of dozens of megahertz and with a sampling rate of 50 MHz or higher [29]. An important application area is 3rd generation cellular base stations, where the current trend is to move the analog-digital boundary to the intermediate frequency (IF).

The requirement to sample an IF signal sets stringent specifications for the analog front-end of the ADC. Usually it is realized with a sample-and-hold (S/H) circuit that has to be able to track the high frequency input signal. One of the major challenges in implementing the S/H is the high frequency linearity of the sampling circuit, which is mainly determined by the properties of the sampling switch. In IF-sampling the signal downconversion is performed by the sampling operation and thus the jitter of the LO signal, which is used as the sampling clock, must be very low.

Typically, the matching properties of the circuit elements set the maximum attainable ADC resolution (with a reasonable yield) somewhere between 10 and 12 bits. To achieve a higher resolution with a Nyquist rate ADC, some kind of calibration or trimming has to be applied. Recently, digital self-calibration techniques, which are made feasible by the possibility of including more and more digital circuitry in the ADC, have gained in popularity [12, 15, 13, 16, 30, 31, 32].

This paper presents a 13-bit pipeline ADC [33] incorporating a digital self-calibration algorithm. The ADC has a front-end S/H circuit designed to sample signals from a 200-MHz IF. In order to cope with thermal noise, the signal range is set as high as 3.8 V_{pp} differential. Because the circuit operates on a 2.9-V supply, the large signal range has a major impact on the circuit structures used in the opamps, comparators, and switches.

7.4.2 Prototype Architecture

The block diagram of the ADC is depicted in Fig. 7.20. It consists of an IF-sampling front-end sample-and-hold circuit, a self-calibrated 13+2-bit pipeline ADC, a delay locked loop (DLL) for synchronizing the sampling of the first pipeline stages and the S/H output, and an on-chip calibration state machine for controlling the S/H circuit

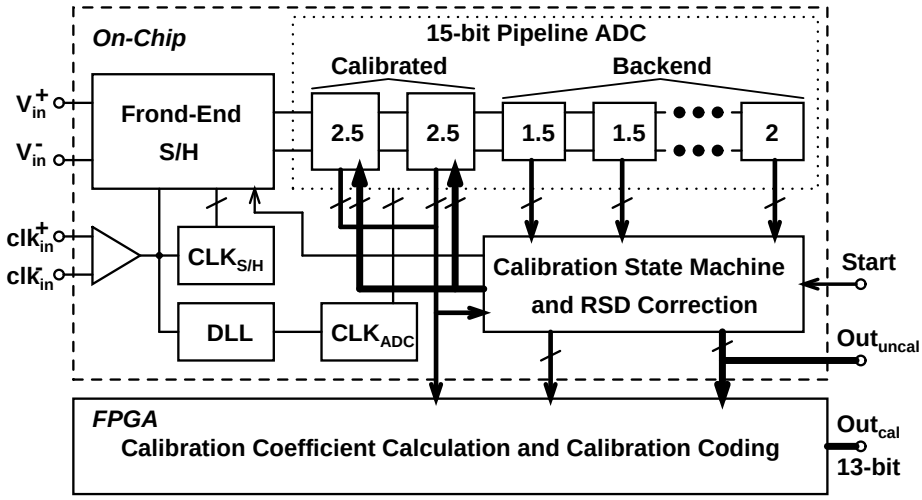

Figure 7.20 Prototype block diagram.

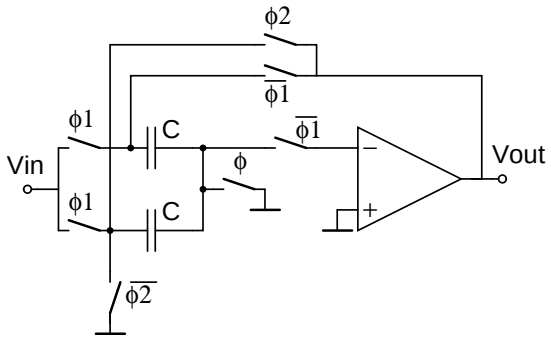

Figure 7.21 Front-end S/H circuit.

and the first four stages of the pipeline during the calibration cycle. The two extra bits are used internally for the calibration. Redundant sign digit (RSD) coding [34, 35] is exploited to relax the comparator offset specifications. Calculation of the calibration coefficients and calibration coding is realized with an external FPGA circuit.

7.4.2.1 Front-End S/H Circuit

The performance of the ADC at high signal frequencies is predominantly set by the front-end S/H circuit. Since it is in front of the signal chain, its thermal noise and distortion are not attenuated by any preceding gain stages and thus it has to fulfill the full resolution requirement.

The S/H circuit, shown in Fig. 7.21, is an SC amplifier with a programmable gain

of 1 or 2. In the unity gain mode, the circuit acts as a flip-around S/H circuit, where the input voltage is sampled into the capacitors during the sampling phase (ϕ,ϕ1=1), while in the hold phase ($\phi, \phi1 = 0$; $\phi2 = 1$) the capacitors are connected to a feedback loop around the opamp. In the gain-of-two mode, the sampling phase is unchanged, but, in the hold phase, one of the capacitors is connected to the opamp output and the other to the signal ground ($\phi, \phi1, \phi2 = 0$). Now a charge transfer occurs from the grounded capacitor to the feedback capacitor and, as a result, the sampled voltage is amplified by the ratio of the total capacitance to the feedback capacitance. The circuit utilizes the bottom-plate sampling technique [36], where the sampling switch (controlled with ϕ) is opened slightly before the input switches (controlled with $\phi1$) so to avoid signal-dependent charge injection from the input switches.

The two modes set different requirements for the opamp; the unity gain mode calls for unity gain stability, while the gain-of-two mode doubles the bandwidth requirement as a result of a smaller feedback factor. Thus, since the opamp has to fulfill both of the requirements, its specifications are more stringent than in either mode alone. The input-referred thermal noise in the sampling phase is the same in both modes, but the peak signal-to-noise ratio is 6 dB lower in the gain-of-two mode as a result of the smaller permissible signal amplitude. The total sampling capacitance (2C) is 10 pF, which leaves sufficient margin to the target resolution for the noise contribution of the opamp and the ADC.

7.4.2.2 Opamp

From the opamp, high gain, wide bandwidth, and low noise are required simultaneously. Furthermore, in order to obtain a high signal-to-noise ratio with low supply voltage, it is important to maximize the opamp output voltage swing, which makes the utilization of a rail-to-rail output stage almost a necessity.

Out of the opamps with a rail-to-rail output stage, the basic Miller topology offers only a moderate DC-gain, which is too small for this application. A higher DC-gain can be obtained with a three-stage architecture or a two-stage opamp with a high-gain first stage. The latter is chosen because of easier compensation and potentially higher speed.

Since the first stage does not need to have a large output voltage swing, it can be a cascode stage, either a telescopic or a folded cascode. The advantage of the folded cascode structure is a larger input common mode (CM) range, while the telescopic stage offers larger bandwidth and lower thermal noise. Thus, since there is no special need for a large input CM range the latter is more attractive. The designed opamp is shown in Fig. 7.22. A closely related architecture, although implemented in pure CMOS, has

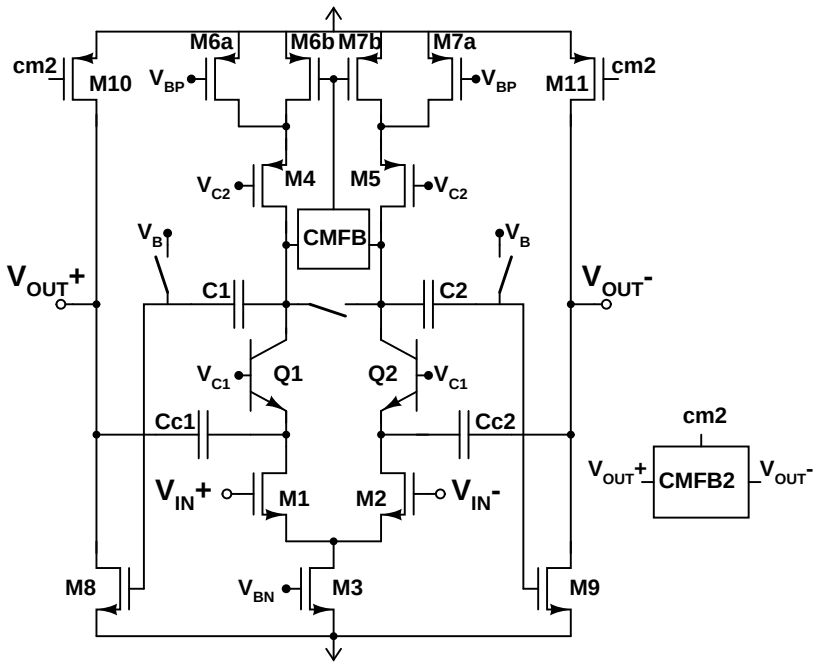

Figure 7.22 High-speed, high-swing, low-noise BiCMOS opamp.

been employed in [37].

An NMOS input pair is chosen over a PMOS one, because it offers higher bandwidth, higher frequency non-dominant pole and smaller noise. The compensation capacitors are connected to the cascode nodes in order to achieve maximal bandwidth. In this BiCMOS circuit, the large gm of the bipolar devices used as cascodes kills the unwanted gain peaking due to a high Q complex pole pair, which is normally characteristic for this type of compensation.

If PMOS devices are used as inputs of the output stage, it can be directly connected to the output of the first stage. This solution, however, suffers from low transconductance of the PMOS device and does not leave enough voltage headroom for low-noise biasing of the first stage current sources. Using a level shifter between the stages makes it possible to take the signal in from the NMOS side, eliminating both of these problems.

Since the opamp is targeted to an SC circuit, it is possible to realize the level shifting with a capacitor, which is periodically precharged to the desired DC bias voltage. In this opamp, the precharging is done during the first half of the clock period, when the opamp is not active in the circuit.

The main advantages of the capacitive level shifting are the facts that it is virtually noiseless and does not require a bias current. On the other hand, fairly large capacitors

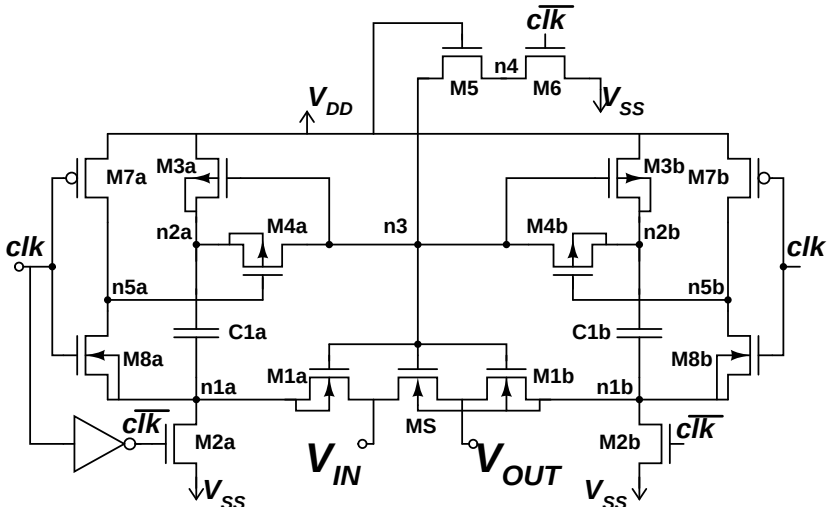

Figure 7.23 Double-side bootstrapped input switch.

are needed to prevent signal attenuation in the capacitive division with output stage parasitic capacitances. In addition, the capacitive connection also sets an upper limit for the transconductance of M9 (M8) and thus the available bandwidth. The transconductance is, however, still larger than the one obtainable with a PMOS device.

The input stage and the output stage have separate common mode feedback loops for two reasons: first, it is easier to achieve fast and accurate CMFB without a fear of instability with separate loops and, second, the first-stage CMFB is used to charge the level shift capacitor, which is not possible with a single loop, since the signal path between the stages is broken during charging. Both the CMFB circuits are realized with the standard SC circuit.

7.4.2.3 Switches

The decreasing maximum supply voltage of integrated circuits has made the driving of a MOS transistor switch with sufficient overdrive difficult. As a result, the signal-dependent switch on-resistance and parasitic capacitances generate harmonic distortion when sampling high frequency signals. A widely used method to improve the linearity is to bootstrap the switch transistor gate voltage. This makes the gate-source voltage almost constant, removing the dominant signal-dependent term from the equation of the on-resistance.

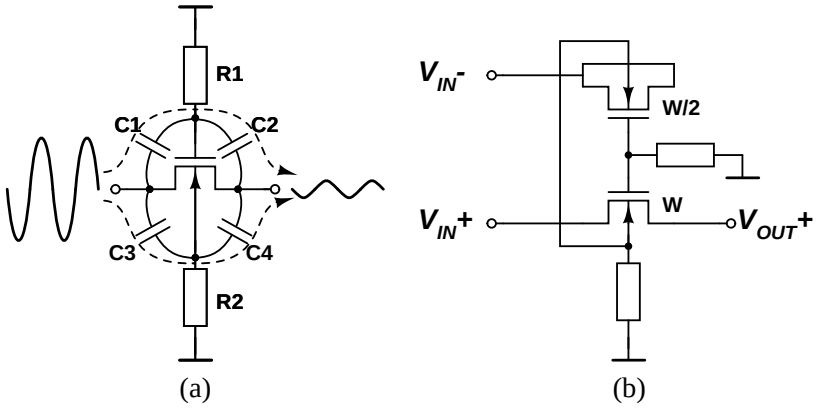

Figure 7.24 (a) High-pass feedthrough path past a closed switch and (b) a method to cancel the feedthrough.

7.4.2.4 Double-Side Bootstrapped Switch

The bootstrapped switch employed as the input switch in the S/H circuit is shown in Fig. 7.23. The circuit is based on a long-term reliable switch (Fig. 7.25) [38, 39], where the internal relative transistor terminal voltages do not exceed V_{DD}. The main difference is that the gate voltage of the switch transistor (MS) does not track the input voltage but rather an average of the input and the output voltages. This somewhat reduces distortion when the voltage drop over the switch on-resistance is significant. The averaging is accomplished by duplicating the level-shifting circuit and connecting it to the output node. Thus, a suitable name for the technique is double-side bootstrapping.

Thanks to the utilized triple well process, the voltage at the bulk node of the NMOS switch transistor can be made to track the signal. The bulks of transistors $M1a$ and $M8a$ are also connected to their sources, which improves the tracking accuracy.

7.4.2.5 Reducing Hold Mode Feedthrough

When sampling high frequency signals the switch transistor has to be large, which increases the parasitic capacitances. This may lead to a situation where the high-pass paths past an open switch cause significant input signal feedthrough to the output. This is illustrated in Fig. 7.24. There, the resistors R1 and R2 are the output resistances of the switch drivers, capacitors C1 and C2 the gate overlap capacitances to the drain and source, and capacitors C3 and C4 the drain and source junction capacitances to the bulk.

The figure also proposes a method of canceling the feedthrough in a differential circuit. There an additional transistor is used to form a matched feedthrough from the opposite signal branch. The gate and bulk nodes of both transistors are connected

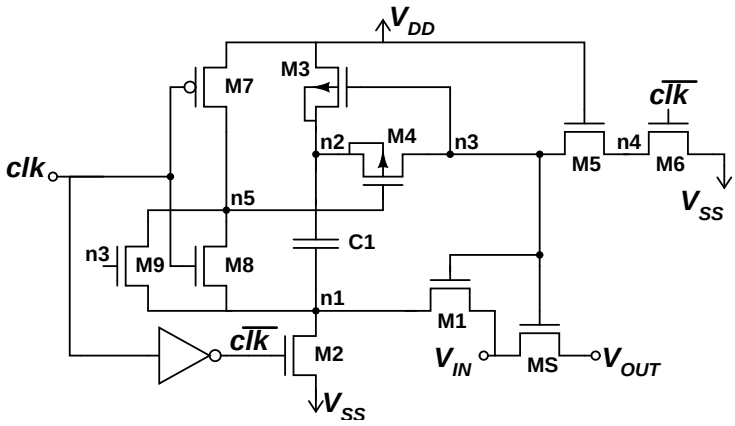

Figure 7.25 Bootstrapped switch.

together and the opposite phase input is connected to the drain and source of the added transistor, which has half the number of gate fingers of the switch transistor. The total number of diffusions (drain plus source) is also matched to the one in the input terminal of the switch transistor. The achievable cancellation is of the order of 10–20 dB and limited by the fact that especially the junction capacitances are signal-dependent. In sampling phase, the drain-source node of the added transistor is connected to the in-phase input signal. This proposed cancellation technique is utilized in the input switches of the S/H circuit.

7.4.2.6 Sampling Switch

The sampling switch ideally does not see a signal swing since it is connected to the sampling ground. In reality, due to the finite on-resistance of the switch transistor, there is some voltage drop across the switch. If this drop is small and linear, it is generally not harmful. In certain cases (large sampling capacitor and high frequency signal), the nonlinearity of the voltage drop necessitates the use of a bootstrapped switch, which provides small and constant on-resistance and signal-independent charge injection. The problem in the circuit of Fig. 7.25 is that the node n3 is pulled toward V_{SS} when the transistor M1 is still somewhat conducting, resulting in signal feedthrough to the input and output of the circuit. This is not an issue in an input switch, but, in a sampling switch, it can be a severe problem. In the utilized circuit, the problem is overcome by turning M1 off (by controlling its gate with the signal *clk*) before pulling n3 down. Now the switch M1 does not have an on-resistance that is as small and signal-independent as before, but because of the small signal swing seen by the sampling switch, this is not

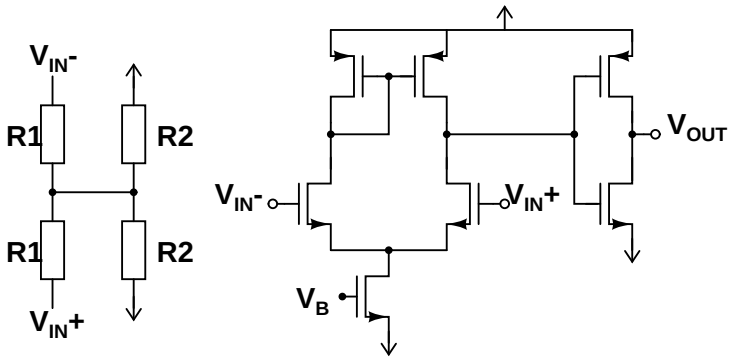

Figure 7.26 Clock buffer.

critical.

7.4.3 Clock Buffer and Clock Generator

7.4.3.1 Minimizing Sampling Clock Jitter

In IF-sampling, the signal-to-noise ratio easily becomes limited by jitter, because the SNR degradation resulting from jitter is proportional to the rate of signal change. For example, a 75-dB SNR at 200 MHz requires a jitter smaller than 141 fs.

Even if the external clock source was ideal (jitter-free), on-chip clock buffering can easily add more jitter than allowed. As is known from ring oscillators, the jitter is proportional to the total delay, without depending on the number of delay elements used [40]. Thus, in this design the target is to minimize the delay from the clock pin to the sampling switch by making the buffer chain as short and as fast as possible.

The buffer utilized is shown in Fig. 7.26. It has a differential input and internal common mode voltage biasing, which requires the clock signal to be DC decoupled on the board level. The buffer consists of two stages, a differential pair input stage and an inverter output stage. To avoid any additional delay the sampling clock (ϕ) is not generated with a non-overlapping clock generator, but taken directly from the buffer output. The signals needed to control the other switches and the opamp, though, are produced by a clock generator.

The first stage of the ADC samples output voltage of the S/H with a signal whose edge falls before the sampling clock of the S/H circuit rises. Since the sampling clock cannot be delayed, the clock edge needed by the ADC is generated with a DLL that is locked to the sampling clock.

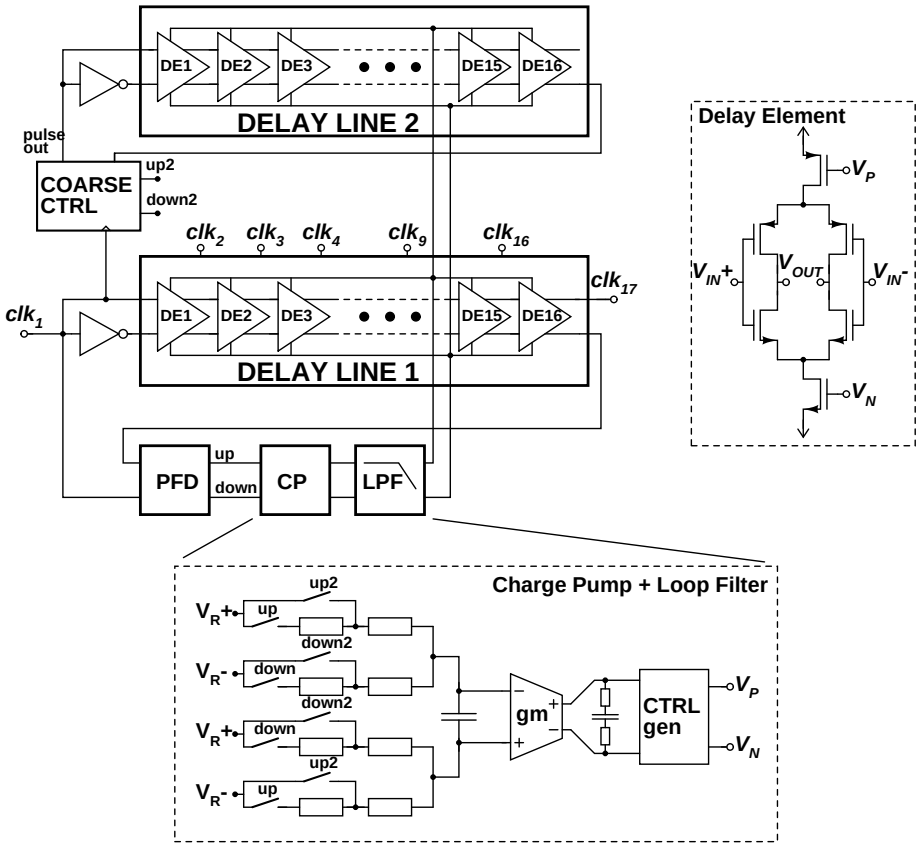

Figure 7.27 Block diagram of the DLL.

7.4.3.2 Delay Locked Loop

The architecture of the DLL is shown in Fig. 7.27. The variable delay is adjusted to be equal to a half of the clock cycle. As a result, the taps of the delay line provide evenly spaced clock edges between the falling and the rising edge of the incoming clock signal.

The circuit consists of two voltage-controlled 16-element delay lines, the first of which belongs to the primary loop, which is the only active loop in the locked state. The second delay line is used to assure locking to the correct phase. It is fed with pulses instead of a continuous clock waveform, which allows the detection of the conditions where the primary loop is outside its phase capture range and tries to lock to on a wrong clock phase. The coarse control logic generates $up2$ and $down2$ pulses, which force the primary loop into the correct range. Once there, the coarse control becomes inactive.

The differential delay element is based on a current-starved two-inverter cell, which is controlled with two voltages. The loop filter is built around a differential gm-cell.

7.4.4 Self-Calibrated Pipeline ADC

7.4.4.1 ADC Architecture

Self-calibration is applied to the first two 2.5-bit stages, while the 9+2-bit back-end pipeline ADC employs 1.5-bit stages. The 15 uncalibrated output bits, along with the raw outputs of the calibrated stages and three control signals, are brought out of the chip to the external calibration logic and coding circuitry. The ten reference voltages needed in the sub-ADCs of the stages are generated with an on-chip resistor string, while the differential reference voltage for the capacitive MDACs is supplied externally.

Partitioning of the resolution is chosen on the basis of the fact that a high-resolution stage in front of the pipeline ADC provides overall linearity improvement as well as power savings in the subsequent stages [41]. However, each additional bit in the first stage halves the opamp's feedback factor and doubles the number of comparators and their accuracy requirement. Comparable benefits are achieved by having two medium-resolution front-end stages, the amplifier and comparator specifications still being reasonable. The back-end pipeline should have the minimum stage resolution to minimize power consumption. On the basis of simulations on a behavioral pipeline ADC model, the target 13-bit linearity can be achieved with two calibrated 2.5-bit stages in front of a 1.5-bits/stage back-end.

The opamp topology used in the pipeline stages is similar to the one used in the front-end S/H circuit (Fig. 7.22). In the first two stages, the opamp differs from the one used in the S/H circuit only in having a smaller compensation capacitor. The 1.5-bit stages all have identical opamps, where the bias current and device sizes are scaled down by a factor of four from the opamps of the first two stages. The scaling is made possible by the smaller capacitive load and the relaxed accuracy requirement. In the first pipeline stage, 2.5-pF unit capacitors are used, resulting in a total sampling capacitance of 10 pF. In the second 2.5-bit stage and in the back-end pipeline stages, the unit capacitors are scaled down to 1.0 pF.

The sub-ADCs of the 2.5-bit, 2-bit, and 1.5-bit pipeline stages are of the flash type and consist of six, three, or two comparators, respectively. In the calibrated stages, a multiplexer is added to select between the normal MDAC switch control signals and the state machine-produced calibration signals. The low stage resolution, together with the RSD correction, allows the use of non-DC-power-consuming dynamic comparators.

The differential pair dynamic comparator employed in the stages is fairly insensitive to mismatches [42]. It uses two differential pairs with pulsed tail current sources to form currents proportional to the difference between the differential reference voltage and differential signal voltage. The currents are summed and fed into a latch. The

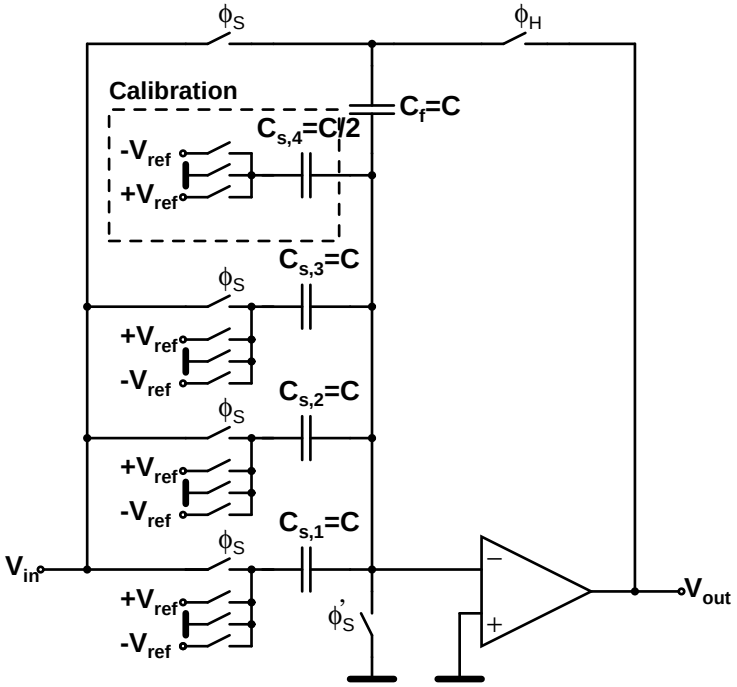

Figure 7.28 MDAC employed in calibrated 2.5-bit stages.

circuit is not sensitive to common mode voltages, even when they are not the same in the signal and in the reference, and the offset is primarily determined by the mismatch of the input devices.

7.4.4.2 Calibration Circuitry

To meet the 13-bit resolution requirement with a high yield the effects of capacitor mismatch, low opamp DC-gain, and reference voltage mismatch need to be compensated for. A widely used method in pipeline ADCs is digital self-calibration, where the discontinuities in the transfer function of each pipeline stage are serially measured using the back-end pipeline, yielding correction coefficients to be added to the ADC output during normal operation. In the calibration method employed, developed from [12], the error attached to each reference unit capacitor is measured separately with the back-end stages. The correction coefficients corresponding to different output codes of the stage can be cumulatively calculated from these measurement results.

A simplified schematic of the 2.5-bit MDAC is shown in Fig. 7.28. It differs from a conventional capacitive MDAC in that it has an extra calibration capacitor, the size of which is half of the unit capacitance. The stage under calibration samples the signal

ground voltage to all capacitors, and, in hold mode, the capacitor being measured is connected to the positive or negative reference voltage, while the extra calibration capacitor is connected to the opposite reference voltage and the remaining capacitors to the ground. The resulting deviation of the output from the ideal $\pm V_{ref}/2$ is measured with the back-end pipeline. Similarly, the error of the calibration capacitor is measured and taken into account in the calculations.

Without this extra capacitor, the stage output during the measurements would be $\pm V_{ref}$ or 0, depending on whether one capacitor or a difference between two capacitors is measured. Measuring the differential capacitor errors (using the feedback capacitor as a reference) does not take account of the error resulting from the finite opamp gain, while performing the measurement in the vicinity of $\pm V_{ref}$ easily saturates the back-end stages in the presence of even small mismatches, unless a nominal gain of radix less than two is used [15]. The extra capacitor eliminates both of these problems by shifting the measurement of the capacitor values in the same voltage range—to the vicinity of $\pm V_{ref}/2$, where the transfer function steps are in normal operation.

The principle of the coefficient calculation was depicted for a 2.5-bit stage in Fig. 7.14. In this method, the calibration order of the stages can be freely selected as well and the algorithm is very simple.

As the output of the second stage during the calibration falls in a known narrow voltage range near ± 0 or $\pm V_{ref}/2$, the first stages of the back-end pipeline are actually used as amplifiers, which makes possible the enhancement of the accuracy of the measurement by a factor of four, simply by doubling the gain of the first two 1.5-bit stages. This is accomplished by halving the MDAC feedback capacitor during the calibration, as shown in Fig. 7.11. Normally, the two halves are tied together, but during calibration, one half is connected in parallel with the reference capacitor. Two extra stages are added to the back-end to get even more resolution when measuring the calibration coefficients, as well as to reduce the truncation error in the calibration adders during normal operation. The calibrated output is fixed to 13 bits.

The calibration algorithm is implemented in VHDL. The design allows the inclusion of the calibration logic on the same chip as the ADC or its realization with an FPGA, which is combined with the ADC chip on the circuit board level. In this first silicon prototype, the latter approach is used because of its flexibility. However, to reduce the number of digital I/O pins, the signals needed to control the analog blocks (MDACs and S/H) during the calibration cycle are generated with a small on-chip state machine. As a result, the calibration cycle can be triggered with a single one-bit signal and the number of extra I/O pins is kept to a minimum.

The seven calibration coefficients per stage are calculated as an average of four

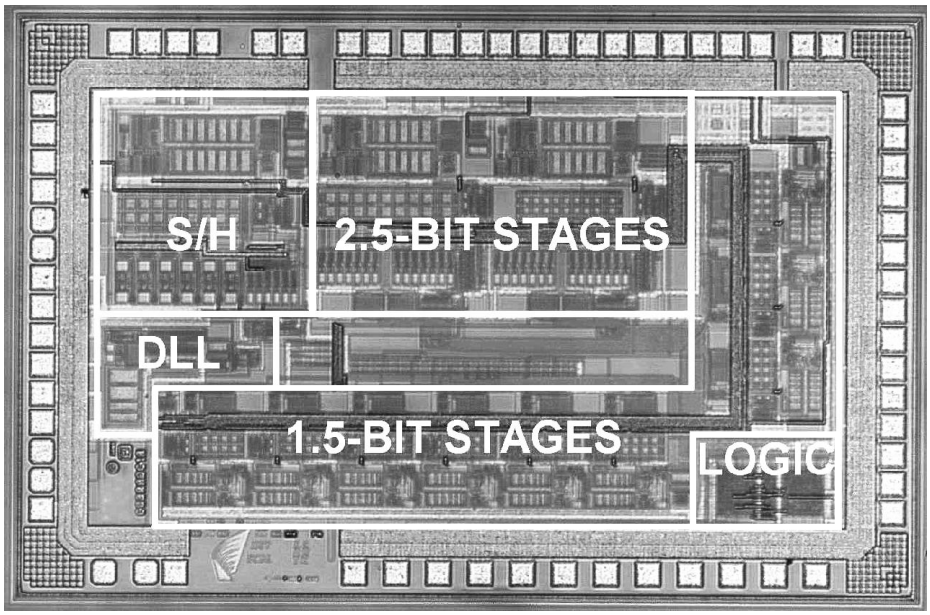

Figure 7.29 Die micrograph of the prototype.

measurements and stored in a memory. During normal operation, calibration coding is simply the addition of two coefficients, which are selected according to the raw bits of the two first stages, to each uncalibrated ADC output word.

7.4.5 Experimental Results

The circuit, a die photo of which is shown in Fig. 7.29, was fabricated with 0.35-μm BiCMOS (SiGe) technology with metal-insulator-metal capacitors and the chip was packaged in a 52-pin VFQFPN package. The benefits of this almost chip-scale package are small parasitics and also a low ground inductance and good thermal conductivity, which are thanks to the die attachment to a large pad, exposed through the package.

The prototype was measured using a 4-layer PCB, the FPGA being on a separate board. A common ground plane was used for the analog and the digital circuitry. The clock signal from an on-board 50-MHz crystal oscillator was connected to one of the differential clock inputs, while the complementary input was grounded near the oscillator. The sinusoidal input signal from a signal generator was first low-pass filtered to remove the harmonics and then transformed into a differential form using a power splitter. The signal generator was not capable of supplying the large current spikes needed to load the S/H circuit's 10-pF sampling capacitors and thus in IF measurements parallel LC resonators were put in parallel with the inputs of the prototype chip to isolate the cir-

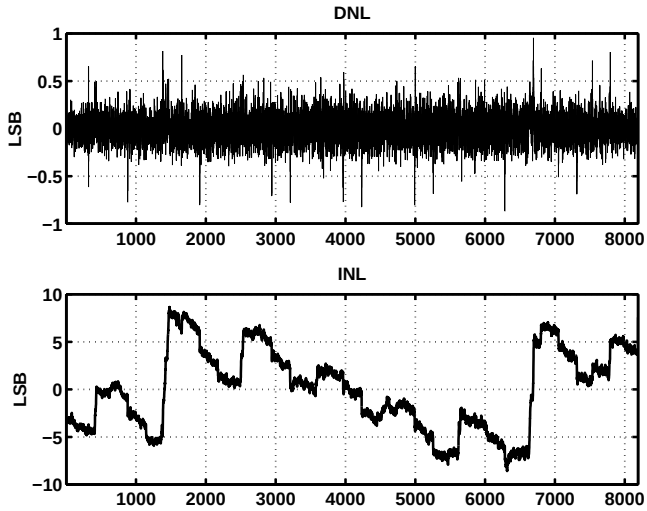

Figure 7.30 Static linearity before calibration.

cuit from the signal generator. The resonator center frequency was tuned to 195 MHz, while its measured Q was 2.6. In the baseband, an opamp-based buffer was used.

The first measurements revealed that there was a timing error in the digital delay line used for aligning the output bits of the pipeline stages. As a result, the output contained a large number of seemingly random bit errors. It was found that these errors could be minimized, but not totally eliminated, by lowering the supply voltage from the designed 3.0 V to 2.9 V and performing the testing at a temperature of $+5°$C. Due to the remaining bit errors, the noise floor was high, limiting the SNDR to 55–60 dB. On the other hand, the linearity did not seem to suffer significantly.

The static linearity was measured with a 3.9-MHz signal and calculated using the code density test. Fig. 7.30 and Fig. 7.31 show the results before and after the calibration cycle, respectively. The calibration improves the maximum INL from $\pm$8.2 LSB to $\pm$2.7 LSB, the DNL being within $\pm$1.0 LSB.

The SFDR measured with a -1-dBFS (3.4 V_{pp} differential) signal was better than 73 dB in the range from 190 to 200 MHz. Example spectra, pre and post calibration, showing an over 20-dB improvement in SFDR from 56.0 dB to 76.5 dB are plotted in Figs. 7.32–7.33. A two-tone test made with -7-dBFS signals (188.2 MHz and 192.2 MHz) and using the gain-of-two mode in the S/H circuit is presented in Fig. 7.34. The measured power consumption from the 2.9-V supply was 715 mW. Tab. 7.4 summarizes the ADC performance

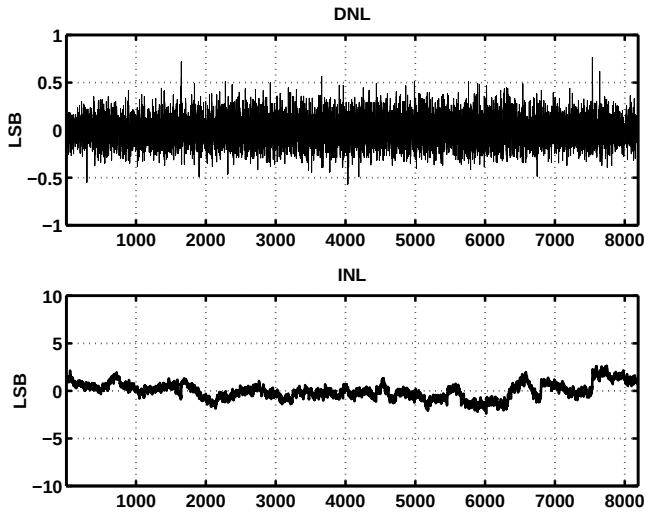

Figure 7.31 Static linearity after calibration.

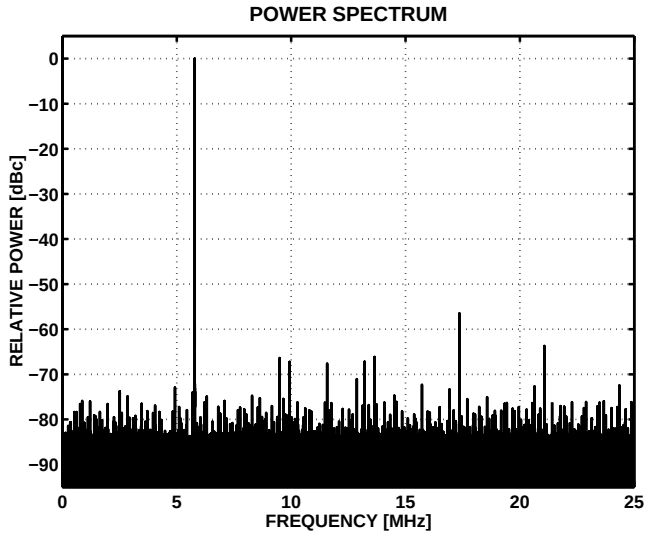

Figure 7.32 A spectrum measured with 194.2-MHz, -1-dBFS signal before calibration.

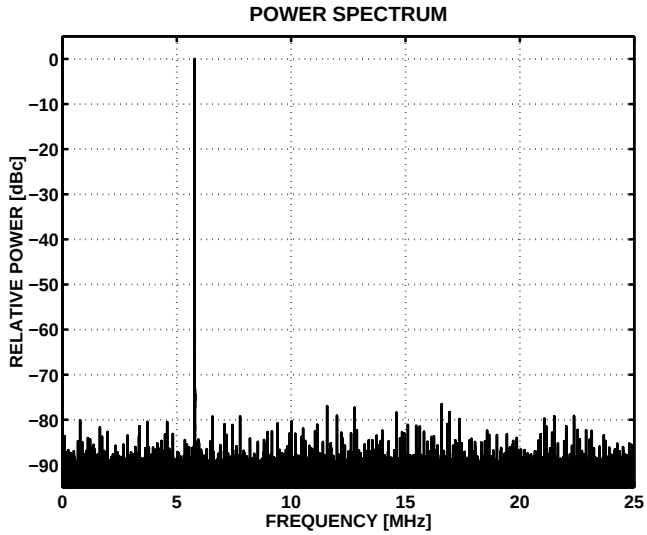

Figure 7.33 A spectrum measured with 194.2-MHz, -1-dBFS signal after calibration.

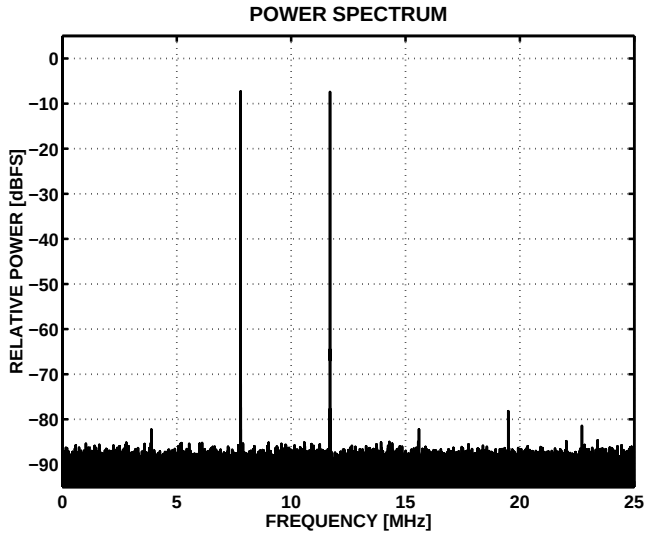

Figure 7.34 A two-tone spectrum obtained with -7-dBFS signals centered at 190 MHz. The S/H circuit is in the gain-of-two mode.

Table 7.4 Summarized ADC performance.

Resolution	13 bits
Sample Rate	50 MS/s
Input Voltage (differential)	3.8 V_{pp}
Input Bandwidth	> 200 MHz
DNL / INL (calibrated)	$\pm$0.8 / $\pm$2.7 LSB
SFDR (@ 200 MHz)	76.5 dB
SNDR	60 dB
ENOB	9.7 bits
Power Dissipation @ 2.9 V	715 mW
E_{conv}	1.7 pJ
Die Area	6.0 mm^2
Technology	0.35-μm BiCMOS (SiGe)

7.4.6 Conclusions

A self-calibrated pipeline ADC with a capability of sampling signals from 200-MHz IF has been presented. High sampling linearity is achieved with bootstrapped switches. The fully differential circuit uses rail-to-rail internal signal swing to maximize the signal-to-noise ratio. To minimize the jitter in the sampling clock, the length of the buffer chain from the clock pin to the sampling switches is minimized and the needed non-overlapping clock phase generated with DLL. Digital self-calibration with a modified capacitor-measuring scheme has been utilized to calibrate the transfer functions of the two first pipeline stages.

7.5 Application Case II: An IF-Sampling 14-bit 160-MS/s Parallel Pipeline ADC

7.5.1 Introduction

A current trend in cellular base stations is to digitize multiple channels directly from intermediate frequency (IF) with a single analog-to-digital converter (ADC). The aim for cost effectiveness and programmability creates simultaneously a need for the receivers to operate in multiple standards with only a few modifications. A/D converters with extremely wide signal bandwidth and large dynamic range are required to enable the multi-mode operation and digital channel selection capability. The time-interleaved parallel pipeline ADC architecture offers the greatest potential to achieve simultaneously a high resolution and sample rate. However, the unavoidable channel mismatch affecting the analog signal processing challenges the time-interleaved A/D converter

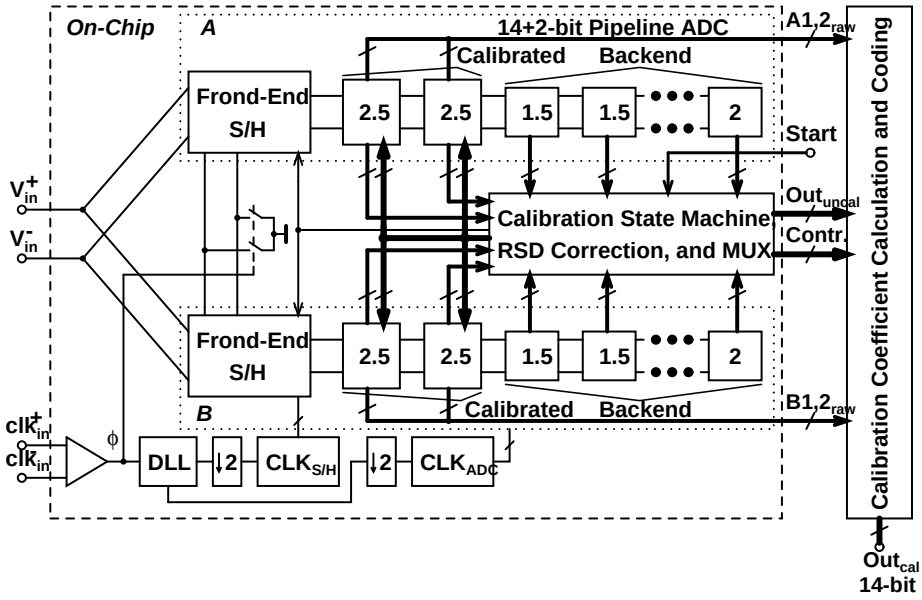

Figure 7.35 Block diagram of the IF-sampling parallel pipeline ADC.

design.

The 14-bit 160-MS/s parallel pipeline ADC presented here utilizes a front-end sample-and-hold (S/H) circuit and digital self-calibration to overcome the timing skew, gain, and offset mismatch between the ADC channels, as well as the nonlinearity resulted from capacitor mismatch. It is designed for a 0.35-μm BiCMOS process with a 3-V supply voltage to achieve a spurious free dynamic range (SFDR) greater than 72 dBc over an IF band of 140–210 MHz.

7.5.2 Circuit Description

Block diagram of the 14-bit 160-MS/s parallel pipeline ADC is depicted in Fig. 7.35. The circuit consists of two time-interleaved channels, both of which operate at 80-MS/s. Timing skew between the channels is avoided with a wide-band parallel front-end S/H circuit which feeds the pipeline ADC channels. The ADC channels consist of two calibrated 2.5-bit stages followed by ten 1-bit stages and a 2-bit flash giving 16 output bits, the two least significant of which are reserved for calibration. The raw stage outputs are first processed by a redundant sign digit (RSD) correction circuitry [34], after which the calibration coefficients are applied and the output is cut to 14 bits. The calibration algorithm is used to compensate for nonlinearity within the channels, caused by capacitor mismatch, as well as to remove the gain and offset mismatch between the channels.

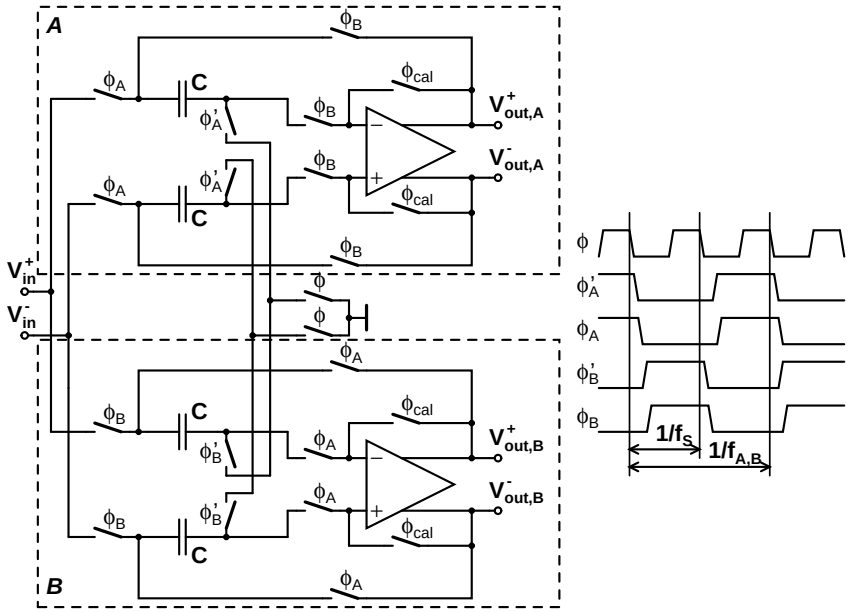

Figure 7.36 Timing skew-insensitive parallel front-end S/H circuit and its timing.

An on-chip state machine controls the ADC during the calibration cycle, while the calibration algorithm is implemented off-chip either with a field programmable gate array (FPGA) or in a PC. Synchronization between the full-speed sampling clock and half-speed clocks of the S/H and pipeline ADC channels is realized with a delay locked loop (DLL). Fully differential circuitry is used throughout the design.

7.5.2.1 Front-End

At high signal frequencies, the ADC performance is predominantly set by the front-end S/H circuit. Although a flip-around type S/H circuit theoretically achieves four times the speed of a 2.5-bit pipeline stage because of the larger feedback factor, the large sampling capacitance of 6 pF and the signal swing, set as high as 4-V_{pp} differential, force to introduce time-interleaving also into the S/H circuit, shown in Fig. 7.36. Minimization of power dissipation by using double-sampling can not be applied since the BiCMOS amplifier exploited in the circuit employs capacitive level shifting and is active only for half of the clock cycle [33]. The two-stage amplifier achieves simultaneously high gain and wide bandwidth with low noise and maximal output voltage swing.

However, applying time-interleaving in the S/H circuit makes the circuit susceptible to timing skew and therefore incapable of performing its main task of removing the skew. Sensitivity to the skew can be avoided by utilizing the timing skew-insensitive

parallel S/H circuit modification [43]. The main idea is to employ common sampling switches, clocked with a full-speed clock ϕ, for both sample-and-hold circuits, as depicted in Fig. 7.36. Bottom-plate sampling is utilized in three steps: by opening the sampling switches first, then, shortly thereafter, opening the serial switches, operating at half of the sampling speed (ϕ'_A and ϕ'_B), before the half-speed clock signals (ϕ_A and ϕ_B) of the input switches fall. Excluding the switches connected to the inputs of the amplifiers and the offset calibration switches, all the other switches are bootstrapped to achieve the target linearity at the IF frequencies.

In IF-sampling, a low clock jitter is essential. Noise coupling to the clock signal is minimized by bringing a differential clock signal to a single-stage clock buffer, after which the sampling clock is taken directly, avoiding thus the noise contribution of a clock generator. The half-speed clock signals used in the S/H circuits of the *A* and *B* channels are generated with a typical non-overlapping clock generator preceded by a divide-by-two circuit. Synchronization between the sampling clock and the other clocks used in the S/H circuit is performed with a DLL, which operates at the full sampling speed of the ADC. Similarly, the clock signals of the channel A/D converters are generated from a clock, which is taken one delay element earlier from the synchronizing DLL.

7.5.2.2 Bootstrapped Input Switch

The primary factor determining the sampling linearity is the signal-dependent on-resistance of the input switch. The problem can be overcome by making the switch on-resistance constant by applying bootstrapping to the input switch [38, 39]. In a bootstrapped switch, the linearity is limited by secondary effects including the bulk effect and nonlinear parasitic capacitances. In a triple well technology, such as the BiCMOS process used in this design, both of them can be almost completely eliminated by connecting the switch transistor bulk to the input node during the tracking phase [33]. However, in the case of an NMOS device the junction capacitance decreases, while the on-resistance increases, as the signal level rises partially canceling each other. Consequently, bootstrapping of the bulk node is sensitive to variations in the impedance level. Furthermore, the bulk forming p-well, which is now connected to the input, has a junction capacitance of its own, which can be in the same size range as the eliminated capacitance of the source and drain junctions [44].

In a 50-Ω environment, and especially if the impedance of the driving signal source is not known, a good compromise can be achieved by letting the bulk node float during the tracking phase. This can be accomplished in a triple well process with the MOS switch shown in Fig. 7.37. The floating bulk results in a parasitic structure, which is

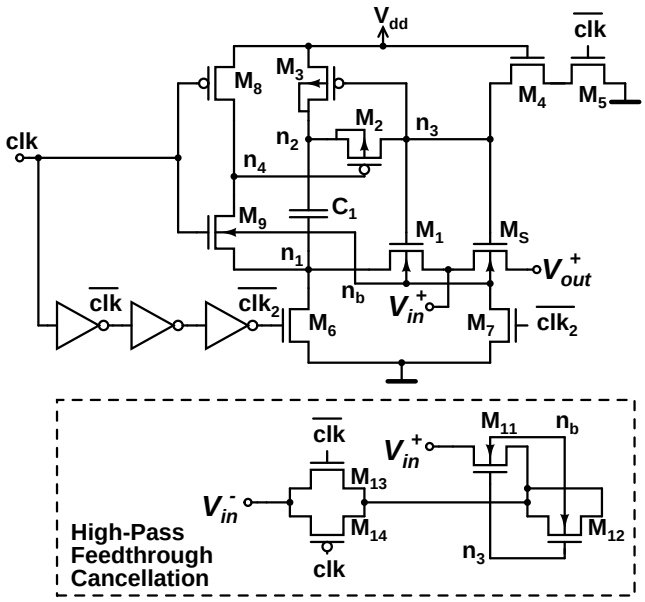

Figure 7.37 Bootstrapped switch utilizing floating bulk and high-pass feedthrough compensation.

a series connection of two diodes of opposite types. Now the capacitance is smaller and less nonlinear, but the bulk effect is only partially eliminated. In this design, bootstrapped switches with floating bulks are utilized as input switches. Additionally, a high-pass feedthrough compensation is employed using a dummy switch in the complementary input branch, as indicated in Fig. 7.37 [44].

The signal-dependent charge injection is minimized by bootstrapping also the common sampling switches in addition to the use of bottom-plate sampling. Furthermore, the bulks of the serial switches track the output voltage of the corresponding switch short-circuiting the nonlinear junction capacitances of the switch device. This results in a constant charge division of the common sampling switch after it is opened. Bootstrapped switches are also employed in the input switches of the first two pipeline stages.

7.5.2.3 Channel A/D Converters

In the pipeline channel ADCs, the two medium-resolution front-end stages reduce the noise contribution of the subsequent stages, while a fairly large amplifier feedback factor and reasonable comparator offset specifications are still maintained when aiming for high conversion rate. The low-resolution back-end stages can easily achieve the desired

speed and resolution with a small current and area consumption. Unit capacitor multiplying D/A converters (MDACs), employing the same two-stage BiCMOS amplifier as the S/H circuit, are used in the pipeline stages. The RSD correction allows the use of differential pair dynamic comparators in the sub-ADCs reducing the current consumption. Nevertheless, since the ADC is targeted to base station applications, minimization of power dissipation has not been a primary target. The unit capacitance of the first stage is 1.5 pF, which is scaled down to 1 pF in the subsequent stages.

7.5.2.4 Self-Calibration

To achieve the 14-bit resolution with high yield, a digital self-calibration is employed to correct the capacitor mismatch of the first two stages as well as the gain and offset mismatch between the parallel pipeline channels. The circuit utilizes the calibration algorithm described in section 7.3. During the calibration cycle, the error attached to each unit capacitor, including the effect of the finite gain of the operational amplifier, is measured with the back-end stages using an extra level shifting capacitor in the calibrated MDAC [33]. From these measurement results, correction coefficients for each segment of the stage transfer function are cumulatively calculated and stored in a memory. The algorithm simultaneously determines the stage offset values, which can be directly used to compensate the offset mismatch between the channel ADCs. The remaining offset between the parallel S/H circuits is measured by connecting them in a unity gain feedback and by short-circuiting the capacitor top plates during the sample phase. The resulting value is added to the offset correction coefficients of the first pipeline stages.

In a parallel pipeline ADC with two time-interleaved channels, gain mismatch between the channel ADCs result in parasitic side bands around the Nyquist frequency. Calibration of the gain error can be derived from the transfer function of the MDAC when considering the capacitor mismatch as the only error source: the gain error term is equal to the cumulative capacitor mismatch error in the outermost sections of the transfer function (000 and 110 for a 2.5-bit stage). Consequently, the gain error coefficient of each calibrated stage is equal to

$$K_G = \frac{K_{max} - K_{min}}{2^{N_{be}}}, \tag{7.22}$$

where K_{max} and K_{min} are the capacitor mismatch correction coefficients of the outermost code sections, and N_{be} is the resolution of the back-end pipeline ADC used to measure the errors. A single gain calibration coefficient, with which the channel ADC outputs must be multiplied after the capacitor and offset calibration, can be obtained as an inversion of the multiplied gain errors of the first and second stage.

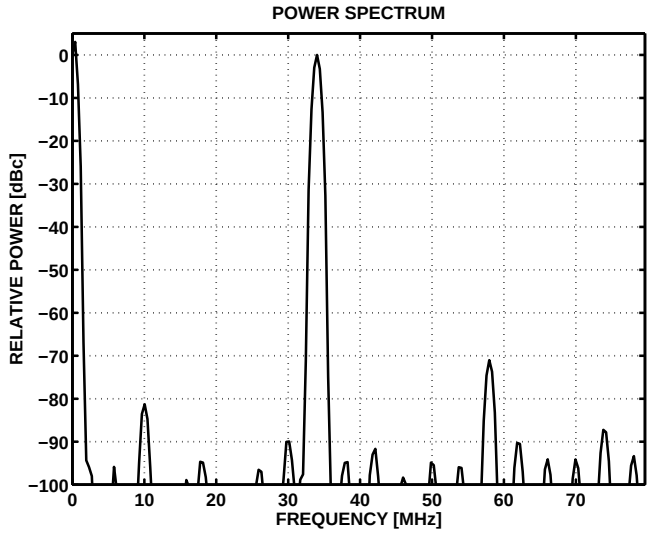

Figure 7.38 A spectrum simulated with 194-MHz, -1-dBFS signal at 160-MS/s sample rate.

Table 7.5 Simulated ADC performance.

Resolution	14 bits
Sample Rate	160 MS/s
Input Voltage (differential)	4.0 V_{pp}
Input Bandwidth	210 MHz
SFDR (140–210 MHz)	$\geq$ 72 dB
Power Dissipation @ 3.0 V	1900 mW
Die Area	10.2 mm^2
Technology	0.35-μm BiCMOS (SiGe)

7.5.3 Simulation Results

A prototype circuit of the 14-bit 160-MS/s parallel pipeline ADC has been designed and is currently being fabricated using a 0.35-μm BiCMOS (SiGe) process. According to the simulations, the circuit achieves an SFDR of 72 dB over the targeted IF-band of 140–210 MHz with ideal device matching. Based on behavioral simulations with the calibration algorithm, presented in subsection 7.3.7, the effect of capacitor, gain, and offset mismatch is suppressed below that level. An example spectrum with 194-MHz input is plotted in Fig. 7.38. The die area is 10.2 mm^2 and the circuit dissipates 1.9 W from a 3-V supply. The performance is summarized in Tab. 7.5.

7.5.4 Conclusions

A time-interleaved 14-bit 160-MS/s parallel pipeline ADC with a 210-MHz IF-sampling front-end S/H circuit was presented. A timing skew-insensitive parallel S/H circuit employing bootstrapped input switches with floating bulk was utilized to achieve a high linearity and overcome timing skew between the channels. Linearization of the pipelined channel ADCs, as well as compensation of the gain and offset mismatch between the channels, was performed by a simple digital self-calibration algorithm. According to the simulations, the circuit achieves an SFDR greater than 72 dBc over an IF band of 140–210 MHz.

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Conclusions

Wireless communications have been the driving force in analog electronics development during the last decade. Typical for the new communication standards is an ever increasing signal bandwidth, allowing more services to be provided. Simultaneously, two trends affect the design of the receivers: first, multi-mode operation according to many different standards is desired and second, the analog-to-digital conversion is pushed into high intermediate frequencies. The particularly attractive approaches to meeting these requirements include the single-chip direct conversion receiver with low-resolution and medium sample rate A/D converters, and the IF-sampling super heterodyne architecture requiring high-resolution, high sample rate, ADCs. In this thesis, the possibility of meeting the widely separated specifications of these two receiver architectures using the pipelined A/D converter architecture is examined.

Several prototype circuits of WCDMA direct conversion receivers, including quadrature low-resolution medium sample rate pipeline A/D converters, have been demonstrated, showing minimal deterioration of the overall receiver noise figure because of the digital substrate noise inherited from the ADCs. Furthermore, the embedded pipeline ADCs achieved low power dissipation and small area consumption. The configurability of the pipeline architecture was demonstrated with a dual-mode converter utilizing an adaptive sample rate, which can be applied in a multi-mode direct conversion receiver for 2G and 3G telecommunication standards.

The conversion rates of A/D converters can be extended beyond the speed of a single-channel pipeline A/D converter by employing time interleaving. Simple optimization techniques for the resolution partitioning and for the number of parallel channels in terms of power dissipation were given and the compensation of the parasitic effects, resulting timing skew, and offset and gain mismatches between the channels, were discussed.

The main focus of this thesis is on the enhancement of the resolution and attainable sample rate of an ADC by combining parallelism and calibration to allow sampling of wide-band IF signals. A digital self-calibration method that compensates the ca-

pacitor mismatch within a single ADC channel and corrects the offset and gain errors between parallel channels is presented. Extension of the resolution beyond technology-determined limits, both in the case of a stand-alone A/D channel and a time-interleaved pipeline ADC, has been demonstrated.

Development of the IC processes will bring many benefits to SC based pipeline A/D converters, like a smaller capacitor mismatch and higher bandwidth, but also many drawbacks. On the one hand, the supply voltage, decreasing with the line-width, makes the design of switches and operational amplifiers more difficult and the voltage swing lower, emphasizing the thermal kT/C-noise. Even though the resolution of all today's A/D converter architectures is finally limited by jitter in the sampling clock, in low-voltage pipeline ADCs, the practical limitation for the conversion rate and resolution comes from the amplification of the residue, which requires an opamp operating in a closed loop configuration. As a result, the design of fast and accurate pipeline ADCs will become increasingly difficult with the technology scaling. On the other hand, technology scaling allows an extensive use of digital signal processing to correct and compensate for the imperfections of the analog circuitry. Whether the evolution of the pipelined architecture has reached saturation level, or will continue to be the dominant architecture of wide-band A/D converters, depends on the balance between these pros and contras of the development of the IC processes.

Appendix A

Derivation of A/D Converter Resolution Limiting Boundaries

A.1 Thermal Noise Resolution

The spectral noise density at the A/D converter input is dominated at high resolutions by the thermal noise inherited from the sampling operation. Other noise sources include shot noise, 1/f noise, and input-referred amplifier noise. The input-referred total noise voltage is obtained by integrating these spectra over the Nyquist band $f_S/2$ and can be expressed as

$$v_n^2 = 4kTR_{eff}\frac{f_S}{2} = 2kTR_{eff}f_S, \tag{A.1}$$

where k is the Boltzmann's constant, T the temperature, and R_{eff} an effective thermal resistance, which includes the effects of all noise sources. The quantization noise voltage is shown to be

$$e_q^2 = \frac{V_{LSB}^2}{12} = \frac{V_{FS}^2}{12 \cdot 2^{2N_{thermal}}}, \tag{A.2}$$

where V_{LSB} is the quantization step for a full-scale voltage of V_{FS} and $N_{thermal}$ is the maximum number of effective bits for a given value of R_{eff}. Equating these two expressions leads to the attainable resolution of

$$N_{thermal} = \frac{1}{2}\log_2\left(\frac{V_{FS}^2}{6kTR_{eff}f_S}\right) - 1. \tag{A.3}$$

A.2 Aperture Uncertainty Resolution

The effect of the aperture uncertainty comes about because an A/D converter does not sample the input at precisely equal time-intervals $T_S = 1/f_S$. The sampling process is random-like and can be characterized by a mean and standard deviation with regard to the location in time of when sampling occurs. The mean is the average position of the sampling instant and the standard deviation is defined as the rms aperture jitter σ_a. The worst-case voltage error due to the aperture jitter corresponds to sampling a sinusoidal waveform with the Nyquist frequency, which is $f_S/2$, i.e. a full-scale signal

$$v(t) = \frac{V_{FS}}{2} \sin(\pi f_S t). \tag{A.4}$$

The maximum error will occur when attempting to sample the signal $v(t)$ at its zero-crossing, where its derivative gives the maximum slope of the signal

$$v'(0) = \frac{\pi f_S V_{FS}}{2} \cos(\pi f_S \cdot 0) = \frac{\pi f_S V_{FS}}{2}. \tag{A.5}$$

The maximum rms voltage error is given by the product of $v'(0)$ and the aperture uncertainty

$$v_{rms} = \frac{\pi f_S V_{FS} \sigma_a}{2}. \tag{A.6}$$

Equating v_{rms}^2 to the quantization noise voltage of Eq. A.2 above ($N_{thermal}$ is replaced by $N_{aperture}$), leads to the relation for $N_{aperture}$

$$N_{aperture} = \log_2 \left(\frac{2}{\sqrt{3}\pi f_S \sigma_a} \right) - 1. \tag{A.7}$$

Appendix B

Derivation of the Operational Amplifier Parameters

The DC-gain of the amplifier in a multiplying D/A converter is determined by the resolution, and the slew rate and GBW specifications can be derived from the sampling speed of the A/D converter. The MDAC topology used in the calculations below is shown in the hold mode in Fig. B.1(a) as single-ended for simplicity. However, all the calculations are performed for a fully differential topology. In this configuration, the input signal is sampled to the sampling capacitors $C_s = \sum_{j=0}^{n-1} C_{s,j}$ and feedback capacitor C_f. The analysis can easily be expanded to other topologies as well. The corresponding small-signal model is presented in Fig. B.1(b).

B.1 Open loop DC-Gain

The settling error at the output of the operational amplifier in a multiplying D/A converter, resulted from the finite open loop DC-gain $A_0 = g_m r_o$ is approximately given by

$$\varepsilon_{A_0} = \frac{1}{A_0 \cdot f}, \tag{B.1}$$

where f is the feedback factor

$$f = \frac{C_f}{C_f + \sum_{j=0}^{n-1} C_{s,j} + C_{par}}, \tag{B.2}$$

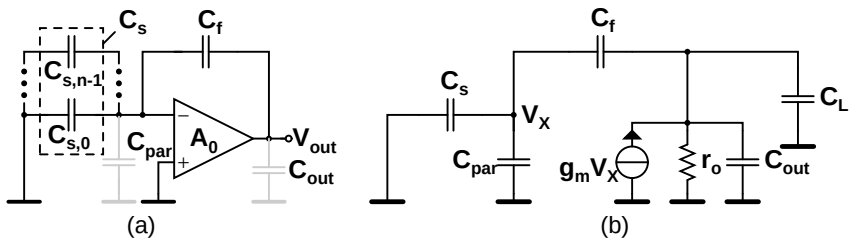

Figure B.1 A single-ended MDAC (a) in the hold mode and (b) the corresponding small-signal model.

which can be approximated in case of $C_s, C_f \gg C_{in}$ to equal

$$f \approx \frac{1}{2^{B_i}}. \tag{B.3}$$

Assuming that the errors caused by the finite DC-gain of the amplifier $\varepsilon_{A_0,i}$ in all the $m = k-1$ pipeline stages with a resolution of $B_i + r$ bits are correlated and the only error sources, the total error reduced to the input of a N-bit A/D converter is

$$\varepsilon_{tot} = \frac{\varepsilon_{A_0,1}}{2^{B_1}} + \frac{\varepsilon_{A_0,2}}{2^{B_1} \cdot 2^{B_2}} + \ldots + \frac{\varepsilon_{A_0,m}}{2^{B_1} \cdot 2^{B_2} \cdot \ldots \cdot 2^{B_m}} = \sum_{i=1}^{m} \frac{\varepsilon_{A_0,i}}{\prod_{l=1}^{i} 2^{B_l}}. \tag{B.4}$$

By substituting Eqs. B.1–B.3 into Eq. B.4, the total error reduced to the converter input can be rewritten

$$\varepsilon_{tot} = \sum_{i=1}^{m} \frac{2^{B_i}}{A_{0,i} \cdot \prod_{l=1}^{i} 2^{B_l}}, \tag{B.5}$$

where $A_{0,i}$ is the open loop DC-gain of the amplifier in the i^{th} stage. On the other hand, the total error at the ADC input must be less than LSB/2, which corresponds to $\varepsilon_{tot} < 1/2^N$ for an N-bit ADC. The inequality for the dimensioning of the amplifier open loop DC-gains becomes in general case

$$\sum_{i=1}^{m} \frac{2^{B_i}}{A_{0,i} \cdot \prod_{l=1}^{i} 2^{B_l}} < \frac{1}{2^N}. \tag{B.6}$$

There are two interesting special cases for the amplifier DC-gain dimensioning. First, the pipeline ADC consists of stages with two different stage resolutions: a front-end stages with an effective resolution of B_a bits and $b = m - a$ back-end stages with B_b effective bits. The respective amplifier DC-gains are $A_{0,a}$ and $A_{0,b}$. Eq. B.5 can be

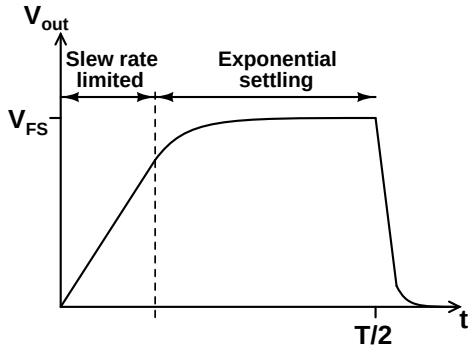

Figure B.2 Settling of the stage output.

in this case rewritten as

$$\varepsilon_{tot} = \sum_{i=1}^{a} \frac{2^{B_a}}{A_{0,a} \cdot \prod_{l=1}^{i} 2^{B_a}} + \frac{1}{2^{a \cdot B_a}} \cdot \sum_{i=1}^{m-a} \frac{2^{B_b}}{A_{0,b} \cdot \prod_{l=1}^{i} 2^{B_b}}$$

$$= \frac{2^{B_a}}{A_{0,a}} \cdot \frac{1 - \frac{1}{2^{a \cdot B_a}}}{2^{B_a} - 1} + \frac{2^{B_b}}{A_{0,b} \cdot 2^{a \cdot B_a}} \cdot \frac{1 - \frac{1}{2^{(m-a) \cdot B_b}}}{2^{B_b} - 1}. \tag{B.7}$$

If $a \cdot B_a$, $(m-a) \cdot B_b \gg 1$, the resulting inequality for an input referred error less than LSB/2 becomes

$$\frac{2^{B_a}}{A_{0,a}(2^{B_a} - 1)} + \frac{2^{B_b - aB_a}}{A_{0,b}(2^{B_b} - 1)} < \frac{1}{2^N}. \tag{B.8}$$

The second special case holds for a pipeline A/D converter with identical stages having an effective resolution of $B_i = B$ and amplifier open loop DC-gain of A_0. In this case, Eq. B.5 reduces to

$$\varepsilon_{tot} = \frac{2^B}{A_0} \cdot \frac{1 - \frac{1}{2^{m \cdot B}}}{2^B - 1}. \tag{B.9}$$

To guarantee an input referred error of LSB/2 at most, when m is large, for A_0 must hold

$$A_0 > \frac{2^{N+B}}{2^B - 1}. \tag{B.10}$$

B.2 Gain Bandwidth

The successive pipeline stages operate in opposite clock phases, which gives a settling time of a half of the clock cycle ($T/2$). The settling time is determined first by the slew rate (SR) and finally by the gain bandwidth (GBW) of the amplifier, as indicated in Fig. B.2. Again, the MDAC topology of Fig. B.1(a) is considered as fully differential.

The most commonly used OTAs can be modeled with a single-pole small-signal model of Fig. B.1(b). The GBW frequency of an OTA is related to the transconductance g_m by equation

$$GBW = \frac{g_m}{2\pi \cdot C_{L,tot}}, \tag{B.11}$$

where the total load capacitance $C_{L,tot} = C_L + C_{out}$ includes the parasitic output capacitance C_{out}. Using the symbols of Fig. B.1(b), the corner frequency for the settling in the hold mode is

$$\omega_{-3dB} = \frac{g_m}{C_{L,H}} \cdot f = \frac{g_m}{\frac{C_{L,tot}}{f} + \sum_{j=0}^{n-1} C_{s,j} + C_{par}}. \tag{B.12}$$

It is good practice to reserve one third of the settling time for the SR limited part and two thirds for the GBW limited exponential settling. The error ε_τ caused by the incomplete exponential settling during $T/3 = 1/(3f_S)$ is given by

$$\varepsilon_\tau = e^{-\omega_{-3dB} \cdot \frac{1}{3f_S}} = e^{-\frac{g_m}{\frac{C_{L,tot}}{f} + \sum_{j=0}^{n-1} C_{s,j} + C_{par}} \cdot \frac{1}{3f_S}}. \tag{B.13}$$

In order to fulfill the resolution requirement, the settling error must be less than LSB/2, this case reduced to the input of the stage i, which results in a condition

$$\varepsilon_{\tau,i} < \frac{1}{2^{N_i}}, \tag{B.14}$$

where N_i is the resolution of the remaining back-end pipeline including the i^{th} stage. By combining Eqs. B.3, B.13, and B.14, and solving the amplifier transconductance g_m yields

$$g_m > 3 \ln 2 \cdot 2^{B_i} \cdot N_i \cdot f_S \cdot k C_{L,tot}, \tag{B.15}$$

where the constant $k > 1$ is the ratio between the effective load capacitance in the feedback configuration $C_{L,H}$ and in open loop $C_{L,tot}$, resulting in

$$k = \frac{C_{L,H}}{C_{L,tot}} = 1 + \frac{C_f \left(\sum_{j=0}^{n-1} C_{s,j} + C_{par} \right)}{(C_L + C_{out}) \cdot \left(C_f + \sum_{j=0}^{n-1} C_{s,j} + C_{par} \right)}. \tag{B.16}$$

On the other hand, the transconductance is related to the width W, length L, and drain current I_D of the transistor by

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}, \tag{B.17}$$

where μ is the mobility and C_{ox} the gate oxide capacitance. By substituting Eq. B.17 into Eq. B.15, a condition for the minimum drain current of one transistor of the amplifier input differential pair I_D can be derived to be

$$I_D \cdot \frac{W}{L} > \frac{9\ln^2 2}{2\mu C_{ox}} \cdot (N_i f_S)^2 \cdot \left(2^{B_i} C_{L,tot} + \sum_{j=0}^{n-1} C_{s,j} + C_{par} \right)^2 . \tag{B.18}$$

Using Eq. B.11, this can be expressed in terms of the minimal gain bandwidth

$$GBW > \frac{3\ln 2}{2\pi} \cdot N_i f_S \cdot \left(2^{B_i} + \frac{\sum_{j=0}^{n-1} C_{s,j} + C_{par}}{C_{L,tot}} \right). \tag{B.19}$$

An interesting special case occurs when all the pipeline stages are identical, having $B_i = B$ with equal correlated settling errors $\varepsilon_{\tau,i} = \varepsilon_\tau$ being the only error sources. The total error reduced to the input of an N-bit pipeline ADC is given by

$$\varepsilon_{tot} = \varepsilon_\tau \cdot \frac{1 - \frac{1}{2^{m \cdot B}}}{2^B - 1}. \tag{B.20}$$

Again, for an N-bit ADC it must hold that $\varepsilon_{tot} < 1/2^N$. By combining this to Eqs. B.3, B.13, and B.20, for the transconductance g_m holds

$$g_m > 3\left(N\ln 2 - \ln\left(2^B - 1\right)\right) \cdot 2^B \cdot f_S \cdot kC_{L,tot}. \tag{B.21}$$

Similarly, Eq. B.18 reduces to

$$I_D \cdot \frac{W}{L} > \frac{9}{2\mu C_{ox}} \left(N\ln 2 - \ln\left(2^B - 1\right)\right)^2 \cdot f_S^2 \cdot \left(2^B C_{L,tot} + \sum_{j=0}^{n-1} C_{s,j} + C_{par} \right)^2 . \tag{B.22}$$

B.3 Slew Rate

The slew rate of a single-stage OTA, like a folded cascode amplifier, is linearly dependent on the maximal current I_{max} charging and discharging the load capacitance. To assure symmetrical slewing of the output, the currents of the output stages have to be equal to the current of the input stage, which indicates $I_{max} = 2I_D$. In a pipeline stage, the load capacitance during the slewing depends on the capacitor charging in the previous operation phase. In the worst case, the total load capacitance is $C_{L,tot} + C_f$. Using

the symbols of Fig. B.1(b), the slew rate is given in this case by

$$SR = \frac{I_{max}}{C_L + C_{out} + C_f} = \frac{2I_D}{C_{L,tot} + C_f}. \tag{B.23}$$

For a worst-case slewing of the differential full-scale voltage $V_{pp,diff}$, the SR limited part being one third of the settling time, holds the condition

$$\frac{T}{6} \cdot SR > V_{FS,diff}. \tag{B.24}$$

Substituting Eq. B.23 into the inequality of Eq. B.24, the minimum drain current set by the slew rate is given by

$$I_D > 3 \cdot f_S \cdot V_{FS,diff} \left(C_{L,tot} + C_f\right). \tag{B.25}$$