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Bandpass Delta-Sigma Modulators for Radio Receivers

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Abstract

This thesis concerns discrete-time (DT) bandpass (BP) $\Delta\Sigma$ modulators targeted for intermediate frequency (IF) analog-to-digital (A/D) conversion in radio receivers. The receiver architecture adopted has to be capable of operating with different radio frequencies, channel bandwidths, and modulation techniques. This is necessary in order to achieve an extensive operating area and the possibility of utilizing a local mobile phone standard or a standard suitable for a specific service. The digital IF receiver is a good choice for a multi-mode and multi-band mobile phone receiver, because the signal demodulation and channel filtering are performed in the digital domain. This increases the flexibility of the receiver and relieves the design of the baseband part, but an A/D conversion with high dynamic range and low power dissipation is required. BP $\Delta\Sigma$ modulators are capable of converting a high-frequency narrow band signal and are therefore suitable for signal digitization in an IF receiver.

First, the theory of BP $\Delta\Sigma$ modulators is introduced. It has been determined that resonators are the most critical circuit blocks in the implementation of a high performance BP $\Delta\Sigma$ modulator. Different DT resonator topologies are studied and a double-delay (DD) resonator is found to be the best candidate for a high quality resonator. A new DD switched-capacitor (SC) resonator structure has been designed. Furthermore, two evolution versions of the designed SC resonator are presented and their nonidealities are analyzed. The three designed DD SC resonator structures are a main point of the thesis, together with the experimental results.

Five different DT BP $\Delta\Sigma$ modulator circuit structures have been implemented and measured. All three of the designed SC resonators are used in the implemented circuits. The experimental work consists of both single-bit and multi-bit structures, as well as both single-loop and cascade architectures. The circuits have been implemented with a 0.35μm (Bi)CMOS technology and operate with a 3.0V supply. The measured maximum signal-to-noise-and-distortion ratios (SNDRs) are 78dB over 270kHz (GSM), 75dB over 1.25MHz (IS-95), 69dB over 1.762MHz (DECT), and

48dB over 3.84MHz (WCDMA) bandwidths using a 60MHz IF signal.

Keywords: analog integrated circuits, analog-digital conversion, bandpass delta-sigma modulation, CMOS, discrete-time systems, double-sampling, IF systems, radio receivers, sampled data circuits, subsampling, switched-capacitor circuits, resonators

Preface

I started my university studies in 1995 and my sole target was to graduate as a Master of Science in Engineering. Such matters as my main subject were as yet unclear but my answers were formed step by step. My first choice, and quite a decisive, one as regards this book, was to start my master's thesis at the Electronic Circuit Laboratory at HUT in 1999. The good working atmosphere and the culture of the university formed my opinions in such a way that postgraduate studies seemed a good option as I approached my graduation. Hence, I decided to continue my studies and to take a couple of years to take a licentiate degree, which I thought would be enough for me. However, the research work soon yielded good results and a doctor's thesis started to appear as a possible choice. Furthermore, when a postgraduation position in the GETA graduate school became achievable, I became determined to pursue the goal of doctoral degree, despite my earlier thoughts on the matter, and this book is a consequence.

There is always too little positive feedback but here it is possible to say something. I want to thank my supervisor, Professor Kari Halonen, for the opportunity I have had to work in his laboratory on an interesting research topic with modern equipment and for the encouragement he gave me during the work. Saska Lindfors deserves my special thanks for his valuable co-operation at the beginning of the project and for his teamwork with publications. Special thanks are due to Mika Länsirinne, for his valuable practical advice, and to Jere Järvinen for assisting in the circuit testing during the work. I would like to thank Jarkko Jussila, Marko Kosunen, Lauri Sumanen, and Mikko Waltari for their advice and instructions. Thanks are also due to all my colleagues at the laboratory for creating a pleasant working atmosphere, especially to Lauri Koskinen, Asko Haapamäki, and Tuomas Hollman. I would like to thank our secretary, Helena Yllö, for her help in making arrangements during my studies.

The reviewers of this thesis, Professor Gabor C. Temes (Oregon State University, Oregon, USA) and Professor W. Martin Snelgrove (Soma Networks, Toronto,

Canada), deserve my special thanks for their valuable comments and suggestions.

My wife Johanna has borne great responsibility on the home front and she, together with our son Valtteri (born in 2001), deserves thanks for providing me with a more colorful life outside the research work. Finally, I wish to thank my mother Maija for the strong support she provided through my student days.

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Contents

Symbols and Abbreviations

α	filter bandwidth parameter of DQPSK
β	feedback factor
Δf	frequency error
Δ	quantization step
δ	relative part of bottom plate parasitic capacitance, mismatch term
$\Delta\Sigma$	Delta-Sigma
ε	error term
γ	noise excess factor, error term
λ	quantization gain
μ_0	carrier mobility of the channel
ω	angular frequency
ϕ	signal phase
σ_j	standard deviation of timing error
σ_x	standard deviation of the error of the sampled voltage
τ	time constant
A	signal amplitude
A_b	interference (blocker) amplitude
A_{DC}	DC gain
A_{max}	maximum signal amplitude
B	internal resolution, number of bits, value of feedback bit
BT	GMSK parameter, determines the 3dB point of the Gaussian filter and the bit duration

C_b	bottom plate parasitic capacitance
C_c	compensation capacitance
C_{DAC}	DAC feedback capacitance
C_{eq}	equivalent load capacitance
C_i	integration capacitance
C_L	load capacitance
C_{min}	minimum usable capacitance
C_{op}	parasitic capacitance of opamp output
C_{ox}	gate oxide capacitance
C_p	parasitic capacitance
C_{slew}	slewing capacitance
C_s	sampling capacitance
C_u	unit capacitor
D	distortion noise of the DAC in z-domain
E	quantization noise in z-domain
e_A	noise of AGC
e_L	noise of LNA
e_M	noise of mixer
e_{Op_f}	standard deviation of the flicker noise
e_{Op_kT}	standard deviation of the thermal noise
e_{RF}	noise of input RF signal
e_{rms}	standard deviation of the quantization noise
e_R	resistor thermal noise
f_0	resonance frequency
f_{BW}	desired signal band
f_b	interference (blocker) frequency
f_{Nyq}	Nyquist frequency
f_{sig}	signal frequency
F_s	sampling frequency

f_s	sampling frequency
g_0	gain of resonator
G_A	gain of AGC
g_{ds}	drain-source (channel) conductance
G_L	gain of LNA
G_M	gain of mixer
g_m	transconductance
g_mC	transconductor Capacitor
I_{SR}	slewing current
I_{SS}	tail current of the opamp input pair
$I_{V_{dd}}$	total supply current
k	Boltzmann's constant 1.380658E-23 J/K, scaling ratio of signal levels
KF	flicker noise coefficient
L	effective channel length of the transistor, the order of BP ΔΣM loop filter
n_0	standard deviation of the in-band noise
N_{cap}	number of capacitors
N_{clk}	number of clock signals
N_{opa}	number of opamps
N_q	quantization noise density
N_{switch}	number of switches
$NPSD$	noise power spectral density
R	resistance
r	pole radius in z-domain
R_{ON}	switch on-resistance
T	absolute temperature, clock period
t_j	absolute clock jitter
U	ΔΣM input signal in z-domain
V	ΔΣM output signal in z-domain

V_{cb}	bias voltage of CMFB circuit
V_{cmo}	common mode voltage (output)
V_{dd}	power supply
v_{dsat}	drain-source saturation voltage
v_{ds}	drain-source voltage
v_{gd}	gate-drain voltage
v_{gs}	gate-source voltage
v_{incmr}	input common-mode range
V_{off}	offset voltage
V_{PP}	peak-to-peak voltage
V_{ref}	reference voltage
V_T	threshold voltage
W	effective channel width of the transistor
X	input signal in z-domain
Y	output signal in z-domain
2.5G	enhanced 2G, usually GSM EDGE
2G	the Second Generation
3G	the Third Generation
AD, A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
AMPS	Advanced Mobile Phone System, 1G analog system in USA
b	bit
BB	BaseBand
BiCMOS	Bipolar CMOS
BP	BandPass
BPF	BandPass Filter
BPSK	Binary PSK
BW	BandWidth

CAP	CAPacitor(s)
CDMA	Code Division Multiple Access
cdma2000	the 3G IS-95 technology
CLA	CLocked Averaging, a DEM technique
CLKG	CLocK signal Generator
CMFB	Common Mode FeedBack
CMOS	Complementary Metal Oxide Semiconductor
COMP	COMParator
CQFP	Ceramic Quad Flat Pack
CT	Continuous-Time
DA, D/A	Digital-to-Analog
dBr	difference in decibels between input signal peak amplitude and reference voltage
DC	Direct Current
DD	Double-Delay
DECT	Digital Enhanced Cordless Telecommunications
DEM	Dynamic Element Matching
DLL	Delay Locked Loop
DQPSK	Differential QPSK
DR	Dynamic Range
DS	Double-Sampling
DSP	Digital Signal Processing
DT	Discrete-Time
DWA	Data Weighted Averaging, a DEM technique
EDGE	Enhanced Data rate for Global Evolution
ENOB	Effective Number Of Bits
FB	FeedBack
FDD	Frequency Division Duplexing
FDMA	Frequency Division Multiple Access
FE	Forward Euler

FF	FeedForward (ΔΣM topology)
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FM	Frequency Modulation
FOM	Figure Of Merit
G	Gain (amplifier block)
GBW	Gain-BandWidth product
GMSK	Gaussian-filtered Minimum Shift Keying
GSM	Global System for Mobile Communications, the first European digital standard
HBT	Heterojunction Bipolar Transistor
HDx	the xth order Harmonic Distortion component
HPSK	Hybrid PSK, equal to OCQPSK
I	In-phase
IC	Integrated Circuit
IF	Intermediate Frequency
IIPx	Input IPx
ILA	Individual Level Averaging, a DEM technique
IMDx	the xth order Intermodulation Distortion component
IPx	the xth order Intermodulation intercept Point
IS-136	2G TDMA-based technology (NA-TDMA)
IS-54	2G TDMA-based technology (NA-TDMA)
IS-95	CDMA-based technology, based on EIA/TIA-95 standard
L	inductor
LA	Logic Analyzer
LC	inductor Capacitor
LDI	Lossless Discrete Integrator
LNA	Low-Noise Amplifier
LO	Local Oscillator
LP	LowPass

LPF	LowPass Filter
MASH	cascade ΔΣM architecture
MDAC	Multiplying Digital-to-Analog Converter
MFB	Multiple FeedBack (ΔΣM topology)
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NA-TDMA	North American TDMA
NAND	Not AND logical operation
nMOS	n-channel Metal Oxide Semiconductor
NMT	Nordic Mobile Telephone, 1G analog system in the Nordic Countries
NOR	Not OR logical operation
NPSD	Noise Power Spectral Density
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OCQPSK	Orthogonal-Complex Quadrature PSK, equal to HPSK
OIPx	Output IPx
OPA	OPerational Amplifier
opamp	operational amplifier
OQPSK	Offset QPSK
OSC	OSCillator (crystal)
OSR	OverSampling Ratio
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PDC	Personal Digital Cellular, TDMA-based Japanese standard
PM	Phase Margin
pMOS	p-channel Metal Oxide Semiconductor
PSK	Phase Shift Keying
Q	Quality factor of the resonator, Quadrature-phase
QPSK	Quadrature PSK

RC	Resistor Capacitor
RDA	RanDom Averaging, a DEM technique
RF	Radio Frequency
RFG	Radio Frequency signal Generator
S/H	Sample-and-Hold
SAW	Surface Acoustic Wave
SC	Switched-Capacitor
SDR	Software Defined Radio
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization Noise Ratio
SR	Slew-Rate
STF	Signal Transfer Function
TB	Bit of Thermometer code
TDMA	Time Division Multiple Access
THD	Total Harmonic Distortion
TIA	Telecommunications Industry Association
UMTS	Universal Mobile Telecommunications System
VFQFPN	Very thin Fine pitch Quad Flat Non-leaded package
VGA	Variable Gain Amplifier
WCDMA	Wide-band CDMA technology

Chapter 1

Introduction

Different wireless applications have been a driving force in the development of integrated circuit technologies and vice versa. The demands for small size, low power, and low price require a high level of integration. At the same time, the increased use of digital signal processing makes possible the use of more effective modulation techniques and narrower channel spacings. Due to the lack of suitable radio spectra, this is a necessary development in the growing area of mobile communications.

The physical size of radio receiver electronics is no longer significant in contemporary cellular phones. Instead, the sizes of batteries and displays are the limiting factors. Battery technology has evolved considerably, but further development work is still needed. The size of displays cannot be decreased without reducing visual clarity. In fact, at the moment there is a need to increase the size of displays and to improve their quality in order to meet the requirements for displaying a moving video. The further development of the receiver part can decrease the power consumption and in that way smaller batteries can be utilized or, alternatively, the charging interval can be pro-longed. Increasing the integration level reduces the price of the receiver part because this renders some of the passive components unnecessary and consequently reduces component and assembly costs.

The various existing 2G mobile phone standards in different countries and the new 3G standards call for multi-mode mobile phones. The implementation of multi-mode functionality requires new architectural and circuit level features in radio receivers. The receiver architectures that are currently used are not well suited to multi-mode mobile phones because most of the analog circuitry has to be doubled. Low-frequency operations, such as the second mixing and channel filtering, can be performed more efficiently in the digital domain, utilizing so-called digital IF receiver architecture

[1]. The increased use of digital signal processing affords more flexibility for the implementation of multi-mode functionality. The size of the digital part of the receiver is also directly affected by technological developments, unlike the analog parts. This will lead to a decrease in the physical size and power dissipation of radio receivers in future. The architecture requires analog-to-digital conversion from a high frequency, which yields to stringent dynamic range requirements. The bandpass $\Delta\Sigma$ modulator appears to be a suitable architecture for this purpose but the circuits that have been reported do not have an adequate performance. In this book, BP $\Delta\Sigma$ modulators for the digital IF receiver architecture are studied and new circuits implemented.

1.1 Digital Wireless Systems for Mobile Communication

The first mobile phones were based on several analog technologies, such as NMT in the Nordic countries and AMPS in the USA. There was a lack of suitable radio frequencies when the number of users increased. Second generation mobile phones are based on digital modulation schemes and employ radio frequencies more effectively. Furthermore, voice quality has been improved considerably, as has security. Different industrial and political interests have led to several 2G cellular systems (Table 1.1). In Europe the GSM standard was adopted and nowadays it is the most widely used 2G system. However, in the USA the 2G TDMA systems, IS-54 and later IS-136, were designed to utilize the same spectrum as the analog AMPS technology. On the other hand, after IS-54 the higher-capacity CDMA-based technology (IS-95) was developed. The PDC system was developed in Japan, where it is widely used, but it has not spread elsewhere. Several different systems and spectra prevent the use of the same basic mobile phone everywhere. Even effective utilization of the GSM networks in Europe and the USA requires tri-band or quad-band mobile phones, but a real 2G universal mobile phone should operate at least in GSM, IS-95, and PDC systems with a multi-band capability. Tri-band GSM cellular phones are available, but real 2G multi-mode mobile phones have not been offered.

There has been a great effort to develop a 3G standard which would make possible a real universal mobile phone. The final solution includes cdma2000 and WCDMA technologies with a channel bit rate of 3.84 Mchip/s, using QPSK modulation. At least in Europe and Japan, the system will operate on radio frequencies around 2-gigahertz (downlink 2110-2170 MHz, uplink 1920-1980 MHz) with a 5 MHz channel spacing. Furthermore, backward compatibility with the 2G systems, GSM and IS-

Table 1.1 The 2G digital cellular systems [2] [3].

System	GSM	IS-95	IS-54/136	PDC
Region	Europe[1], USA[2], Asia	USA[1], Japan[2], Korea[3]	USA	Japan
Downlink Frequency [MHz]	869-894[2] 925-960[1] 1805-1880[1] 1930-1990[2]	832-846[2] 869-894[1] 1840-1870[3] 1930-1990[1]	869-894 1930-1990	810-826 1429-1453
Uplink Frequency [MHz]	824-849[2] 890-915[1] 1710-1785[1] 1850-1910[2]	887-901[2] 824-849[1] 1750-1780[3] 1850-1910[1]	824-849 1850-1910	940-956 1477-1501
Multiple access	TDMA/ FDMA	CDMA/ FDMA	TDMA/ FDMA	TDMA/ FDMA
Channel spacing	200 kHz	1250 kHz	30 kHz	25 kHz
Users per channel	8	-	3	3
Duplex method	FDD	FDD	FDD	FDD
Modulation (*) GSM EDGE)	GMSK, BT=0.3 $3\pi/8$ 8-PSK*)	BPSK QPSK/OQPSK	$\pi/4$-DQPSK ($\alpha = 0.35$)	$\pi/4$-DQPSK ($\alpha = 0.5$)
Channel bit rate	270.833 kb/s 812.5 kb/s*)	1.2288 Mchip/s	48.6 kb/s	42 kb/s
Speech bit rate	13 kb/s	-9.6 kb/s	8 kb/s	6.7 kb/s

95, is a target. The 3G will make possible new types of services, such as real video and Internet access, which will be usable with the GSM EDGE (2.5G) as well. The spreading and mushrooming of the new standard depends on the desire of customers to adopt the new services offered by operators. Naturally, the price of services and terminals affects the behavior of end users.

There is a growing demand for real multi-mode mobile phones which will operate in existing 2G networks and in the new 3G networks. It seems that at least rural areas will be covered by the 2G network in the near future, because of the existing infrastructure, and it is reasonable to utilize the capacity of the 2G network for speech services. Furthermore, customers travel more and more between different countries and continents and thus they will require their mobile phones to operate everywhere.

1.2 Receiver Architectures

There are a few receiver architectures suitable for mobile phone receivers. RF signal down-conversion can either be performed in one phase or a couple of down-conversion stages can be utilized. One difference is in the placing of the quadrature mixers re-

quired for demodulation and the partitioning of the signal filtering in the receiver path. The signal digitization can be performed at the baseband frequencies or with higher IF, before or after the demodulation stage. Direct RF digitization would be attractive, but it is not feasible with contemporary technology. At the present the development trend is to increase the integration level of the receiver and to minimize the expensive external passive components, usually selective BP filters. On the other hand, a target that exists is to move the analog-digital boundary to higher frequencies so as to increase the flexibility of the receiver. A final target is often referred to as software-defined radio (SDR), in which the desired radio system(s) can even be programmed afterwards. Signal digitization at higher frequencies is one way ahead, but the total power dissipation of DSP and ADC has to be carefully considered before the transition.

1.2.1 Superheterodyne Receiver

The superheterodyne receiver is a traditional receiver architecture, and the one most often used. The heterodyne receiver is depicted in Figure 1.1. The large dynamic range is achieved using mediocre mixers and amplifiers. However, passive filters and amplifiers with an automatic gain control are required. As there are several external passive components, the architecture is not suitable for full integration [4].

At first, the RF band is selected and the out-off band signals are attenuated using a passive band selection filter. The signal is amplified by means of a low-noise amplifier and the image signal is filtered with a passive bandpass filter. Then the signal is mixed to the first fixed intermediate frequency and the desired channel is selected by means of a passive filter. Before a quadrature down-conversion, the signal is again amplified, usually with variable gain. The channel selection is finalized with analog baseband filters and the signal is converted to the digital domain. The trade-off between sensitivity and selectivity can be improved using two or more IFs, with the added expense of extra mixer stages and extra passive image filters. Multi-mode implementation of the superheterodyne receiver would require separate analog baseband channel selection filters for different modes, in addition to a low integration level.

1.2.2 Direct Conversion Receiver

A direct conversion or homodyne receiver [5] is shown in Figure 1.2. The RF band is selected by an external passive filter and the signal is amplified by an LNA, as in the superheterodyne architecture. After that, the signal is mixed directly to DC by a quadrature RF mixer; hence, the rest of the passive filters and mixing stages are

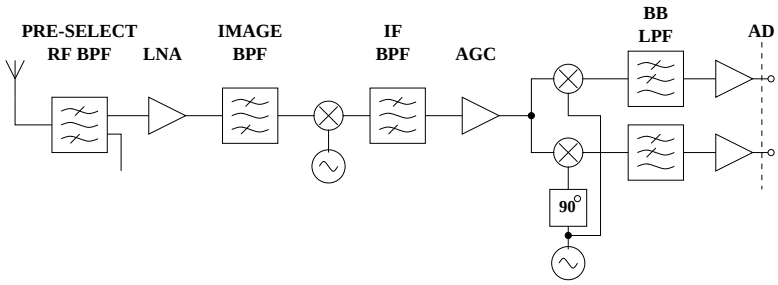

Figure 1.1 Superheterodyne receiver architecture.

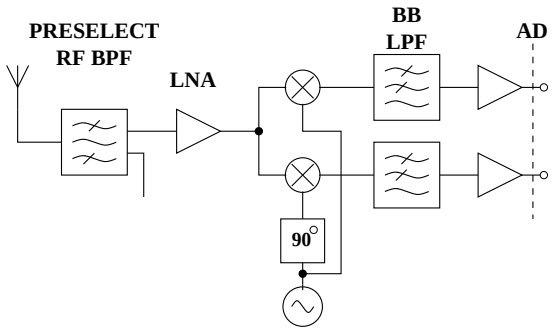

Figure 1.2 Direct conversion or homodyne receiver architecture.

unnecessary. The channel selection is performed by analog baseband filters before the AD conversion.

There are several problems in the implementation of the direct conversion receiver, such as DC offset, local oscillator leakage, I/Q mismatch, even-order distortion, and flicker noise. However, there are many techniques to overcome these shortcomings and the architecture is already in use. The separate analog baseband filters are required to implement the multi-mode functionality, as in the superheterodyne receiver. The considerably higher integration level, as compared to the superheterodyne receiver, is the driving force in the development and utilization of the direct conversion receiver.

1.2.3 Low-IF Receiver

The RF front-end of the low-IF receiver [6] is similar to the direct conversion in Figure 1.2. A difference is that the RF signal is down-converted using quadrature RF down-conversion to an IF of around a few hundred kilo-hertz, instead of the DC frequency, and hence DC problems are avoided. The IF BB LP filters are replaced with complex BP filters or with real filters, but then four mixers are needed at the final stage for

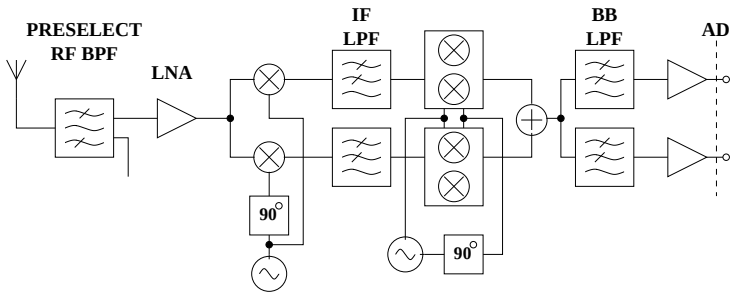

Figure 1.3 Wide-Band IF receiver architecture.

image rejection. It is possible to integrate these filters, because of the low IF, and the advantages of the direct conversion are maintained, but a higher-performance ADC is usually needed to meet the image rejection requirements. After AD conversion the signal is digitally down-converted to DC before digital filtering.

1.2.4 Wide-Band IF Receiver

In a wide-band IF receiver architecture [7] [8], signal down-conversion is performed in multiple phases, as in the superheterodyne receiver, but the discrete image and IF filters are avoided. The wide signal band is first down-converted to the fixed IF frequency, using a quadrature RF mixer, and, after that, the high-frequency components are filtered using a simple LP filter. Due to a higher IF, when compared to a low IF receiver, the image band is more attenuated at the preselection filter. The second mixer stage is tunable to perform the channel selection and furthermore it is a quadrature type to accomplish the image rejection. The channel filtering is performed at the baseband and a VGA may be required before AD conversion.

1.2.5 Digital IF Receiver

In the dual IF heterodyne receiver architecture, low-frequency operations, such as the quadrature mixing and channel filtering, can be performed more efficiently in the digital domain [1] [9]. The so-called digital IF receiver or IF sampling receiver is depicted in Figure 1.4. The digital quadrature mixer eliminates the I/Q mismatch problems of the last mixer stage. Furthermore, the digital filtering makes possible greater flexibility, which is a preferred property in multi-mode mobile phones.

The front end of the receiver is similar to the heterodyne receiver. After the passive channel filter, the signal is digitized to the second digital IF. The rest of the signal processing is completely digital. In a conventional superheterodyne radio receiver

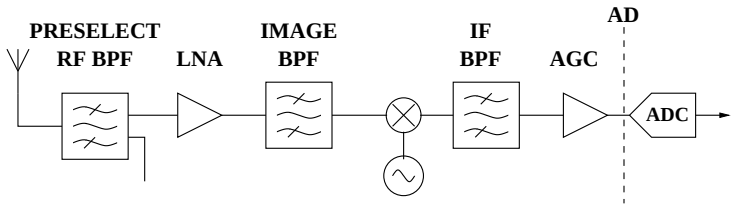

Figure 1.4 Digital IF receiver architecture without DSP part.

an image filter is required after the LNA. However, if the down-conversion mixer is an image reject type, this filter can be avoided, leaving mode-dependent filtering only to RF pre-select and DSP. Digital IF architecture has not been used in portable devices because of the limitations of ADC performance. The linearity and dynamic range requirements for the ADC are very stringent as a result of possible large adjacent interferers. The variations in signal level resulting from path loss and multipath fading also increase the dynamic range requirements [1].

1.3 Research Contribution and Publications

The material contained in the journal articles [L1] [L2] [L3] is included in this book and the contents are further presented in the publications [S1]- [S7]. The author bears the main responsibility for the publications but Dr. Saska Lindfors participated in the writing of the manuscripts and Prof. Kari Halonen gave valuable advice.

The basis for the work is the switched-capacitor resonator structures that were designed. At the beginning of the project Dr. Lindfors made clear the main imperfections and problems of earlier published SC resonators. In order to remove the main limitations a new SC resonator structure was designed by the author and Dr. Lindfors in co-operation [S1]. The author has designed two improved versions of the original circuit, which significantly reduce power dissipation when compared to the first version [S1] [S3].

The first implemented BP $\Delta\Sigma$ modulator utilizes the original SC resonator structure [L1]. The author has performed all the design work and measurements. The second circuit implementation is based on the further improved SC resonator structure [S5]. The author has carried out the design work and measurements of the implemented BP $\Delta\Sigma$ modulator but the internal A/D converter used is based on other work performed by Tuomas Hollman. This circuit and an 8th-order cascaded BP $\Delta\Sigma$ modulator designed by the author [S6] are presented in more detail in the paper [L3]. Jere Järvinen participated in the testing of the circuit. The paper [L2] includes a theoretical

study of discrete-time resonators and an analysis of the proposed SC resonator [S3]. A multi-bit BP ΔΣ modulator merged with an analog DT BP decimation filter [S7] has been implemented using the double-sampling version of the designed SC resonator. The circuit measurements are presented in this book.

1.4 Organization of the Thesis

The book is divided into seven chapters. Chapter 1 has been an introduction to the work, including an overview of digital wireless systems for mobile communications and a short summary of the most important receiver architectures. Chapter 2 introduces the basic theory of BP ΔΣ modulators, including the principle of quantization noise shaping and different architectures of BP ΔΣ modulators. Furthermore, different nonidealities on the BP ΔΣ modulator level are adduced and the most important design aspects are introduced.

In Chapter 3 a BP ΔΣ modulator is studied as a part of the digital radio receiver. Subsampling, noise, and clock jitter theory are considered. Furthermore, the principle of the DT BP decimation sampler is presented. The structure is utilized in the last circuit implementation.

Chapter 4 concerns resonators and their implementation with the SC technique. First, the theory and different topologies of discrete-time resonators are studied. After that, the SC implementations of the double-delay resonator published earlier are introduced. Next, the three designed SC resonator versions are presented and compared to the earlier structures. At the end, different nonidealities are analyzed.

Chapter 5 includes four implemented prototype chips. The measurement results of five different BP ΔΣ modulator circuit structures are presented.

In Chapter 6 the most widely-published monolithic BP ΔΣ modulators and their performances are listed in tables. The circuits presented in this book have been designed for IF digitization and, in order to achieve a comprehensive comparison to earlier work, some published LP ΔΣ modulators used for the same purpose are briefly introduced. At the end the measured circuits are compared to the published circuits. Chapter 7 concludes the thesis.

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Chapter 2

BP ΔΣ Modulators

The exploitation of digital signal processing is increasing all the time. Its benefits are flexibility and insensitivity to nonidealities. However, information is usually transferred, collected, and/or used in analog form. Therefore high-performance A/D and D/A converters are the basis for the generation. The imperfections of analog circuitry and different noise sources limit the achievable conversion resolution and dynamic range. Technology scaling does not improve the situation and the demand for lower supply voltages actually makes the designing more difficult and calls for new analog circuit structures.

Flash AD converters are the fastest ADC topology and are suitable for a low resolution (below 6 bits). For example, interpolation can be used to increase the resolution to 10 bits with a lower conversion rate. The pipeline topology has a long latency time but it can achieve as much as a 15-bit resolution utilizing calibration techniques. In the pipeline structure the resolution is traded against conversion time. In ΔΣ modulators, instead of this, the resolution is traded against the sampling frequency vs. signal band ratio or oversampling ratio (OSR). The quantization noise spectrum is shaped by the feedback loop and the internal quantization can be very coarse (often 1b), which makes high-performance ΔΣ modulators more insensitive to analog circuit nonidealities than their traditional Nyquist rate ADC counterparts. The achieved resolution can be over 14 bits in a narrow signal band, but ΔΣ modulators are not suitable for the high-resolution AD conversion of wide-band signals because of the high OSR required.

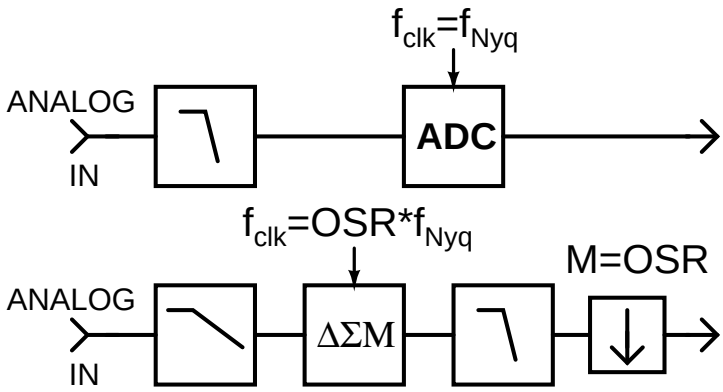


Figure 2.1 A/D conversion by Nyquist rate ADC or ΔΣM.

2.1 Basic Theory

The system level differences between the Nyquist rate A/D converter and ΔΣ modulator are shown in Figure 2.1. The traditional ADC requires a high-performance analog LP filter before the signal sampling occurs. In the case of ΔΣ modulators a loose LP filter, for example an RC loop, is usually adequate, because of the higher sampling rate. The ΔΣM is quite a simple circuit structure and, compared to Nyquist rate converters, is insensitive to analog circuit nonidealities, despite the higher clock rate. However, the required digital filter and decimation stage have to be considered in the total power budget when the A/D topology is selected.

2.1.1 Quantization

If the quantization step of the ADC is Δ and the quantization error is evenly distributed in the range $\pm\Delta/2$, we obtain the quantization noise power as

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2\, de = \frac{\Delta^2}{12}. \tag{2.1}$$

Due to the sampling, the quantization noise power folds in the frequency range $[0,\ f_s/2]$. By the assumption of a white quantization noise, we may write the quantization noise density as

$$N_q = \frac{2}{f_s}\cdot e_{rms}^2. \tag{2.2}$$

If the desired signal band ($f_{BW} = f_2 - f_1$) is ideally filtered by a digital filter (H_d) the in-band noise power is

$$n_0^2 = \int_{f_1}^{f_2} |H_d(f)|^2 N_q \, df = \frac{e_{rms}^2}{f_s} 2 f_{BW} = \frac{e_{rms}^2}{OSR}, \tag{2.3}$$

where the oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{2 f_{BW}} = \frac{f_s}{f_{Nyq}}. \tag{2.4}$$

We see that by doubling the sampling frequency the quantization noise power can be reduced by 3dB or that the resolution is improved by half a bit. This is valid for all ADCs but further noise reduction is possible by quantization noise shaping, which is utilized in ΔΣ modulators.

2.1.2 Noise Shaping

The efficiency of the oversampling can be improved by the ΔΣ modulator, in which the feedback signal is used to shape the quantization noise spectrum. In LP ΔΣMs (Figure 2.2) the basic building blocks are an integrator and an A/D and D/A converter. By linearizing the loop the output signal may be written in the z-domain as

$$Y_{LP}(z) = z^{-1} X(z) + (1 - z^{-1}) E(z). \tag{2.5}$$

We see that the noise transfer function (NTF) has a zero at the DC frequency and hence the quantization noise is high-pass filtered. The signal transfer function (STF) causes only one clock period delay between input and output.

The zeros of the NTF can also be designed to a non-zero frequency [1]. This can be done by replacing the integrators in the LP ΔΣM by resonators, which is equivalent to the $z^{-1} \rightarrow -z^{-2}$ transformation. This leads to the BP ΔΣM structure (Figure 2.3) and we obtain

$$Y_{BP}(z) = z^{-2} X(z) + (1 + z^{-2}) E(z). \tag{2.6}$$

Now the NTF has zeros at the frequencies $\pm f_s/4$ instead of the DC frequency and the quantization noise is shaped away from the frequencies around $f_s/4$. The differences between LP and BP ΔΣMs are further clarified in Figures 2.4 and 2.5.

A more effective quantization noise shaping can be achieved by increasing the order of the loop filter or adding resonators to the loop. It can be shown (Appendix A)

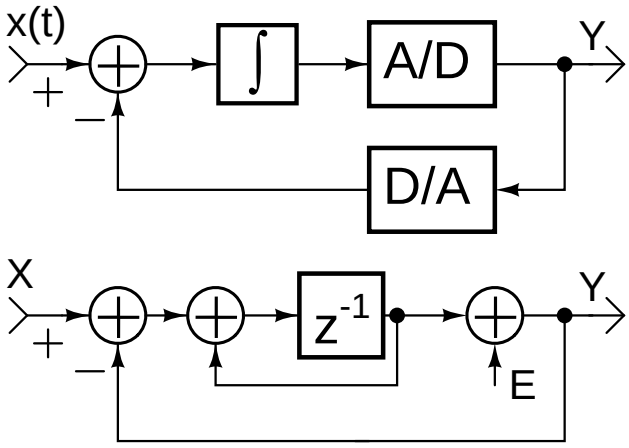


Figure 2.2 LP ΔΣ quantizer and its discrete-time equivalent model.

that the in-band noise power of a 2N-order $f_s/4$ BP ΔΣ modulator is

$$n_0^2 \approx \frac{\pi^{2N}}{2N+1} \frac{e_{rms}^2}{OSR^{(2N+1)}}. \tag{2.7}$$

If the OSR is doubled the in-band quantization noise power of 2nd-, 4th-, 6th- and 8th-order BP ΔΣMs can be reduced by 9dB, 15dB, 21dB, and 27dB, respectively. This is a significant improvement compared to Equation (2.3) and it enables the use of a low resolution internal quantizer (even 1-bit) in the loop if the OSR is high enough.

The LP ΔΣMs and their properties are well-known and therefore the easiest way to design BP ΔΣMs is to select a suitable LP ΔΣM prototype and perform the LP-to-BP transformation. The earlier mentioned $z^{-1} \rightarrow -z^{-2}$ transformation is attractive because the properties of the LP prototype, such as stability and dynamics, are preserved. The disadvantage is that the notch of the NTF is fixed at the $\pm f_s/4$. The general discrete-time LP-to-BP transformation is

$$z \rightarrow -z\frac{z+a}{az+1}, -1 < a < 1 \tag{2.8}$$

and it enables full control of the notch frequency through the parameter a. However, the dynamic properties of the LP prototype are not preserved [2]. The third possibility is to use a filter optimizer to design a suitable NTF for the specific purpose.

The LP-to-BP transformation doubles the order of the loop filter and hence, in principle, the number of required active components is also duplicated. However, for example in a radio receiver, one BP ΔΣM replaces two LP ΔΣMs and no extra

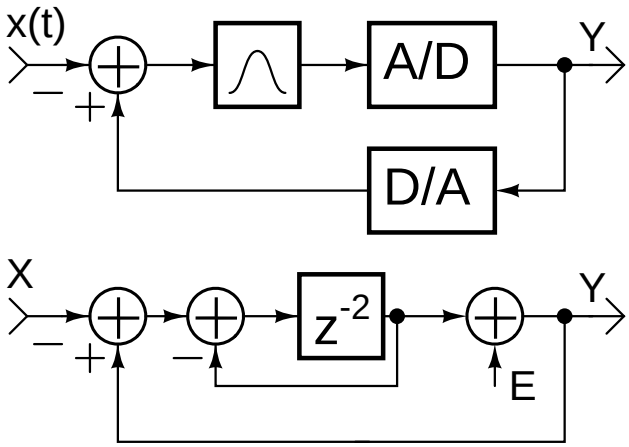


Figure 2.3 BP ΔΣ quantizer and its discrete-time equivalent model.

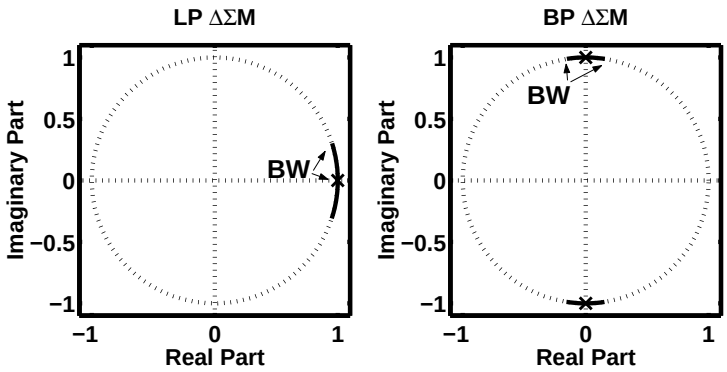


Figure 2.4 Poles and signal band locations in LP and BP ΔΣ modulators.

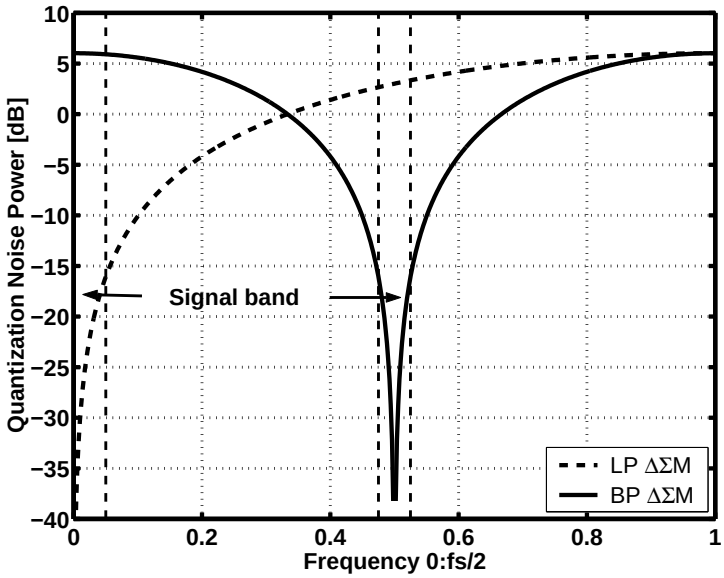


Figure 2.5 The principle of quantization noise shaping in ΔΣ modulators.

active components are needed. Actually, the BP ΔΣM can be used to reduce active components by using the resonator structures presented later in this book.

2.1.3 Discrete-Time vs. Continuous-Time

ΔΣ modulators can be designed as discrete-time (DT) or continuous-time (CT) circuits (Figure 2.6). With DT circuits an S/H stage is required at the input of the ΔΣM to convert a continuous-time analog signal to a discrete-time signal. This block can limit the linearity and noise floor of the whole ΔΣM and, furthermore, an anti-alias filter is needed prior to the sampler. With CT circuits the sampling occurs only in the ADC and possible sampling errors are attenuated by the loop. The loop filter also operates as an anti-alias filter and therefore the analog pre-filter may be eliminated. The power dissipation of CT ΔΣMs is usually lower than that of DT SC circuits and they are suitable for high-speed and low-power applications. However, the linearity requirements are harder to achieve, for example with the RC or g_mC techniques, than with the SC technique.

Despite the many advantages of the CT design, DT ΔΣMs are considered in this book. The main reason is clock jitter, which is a serious problem in the DAC of CT ΔΣMs because the discrete-time feedback signal is added to the high-speed continuous-time analog signal [3]. Time uncertainty in the feedback raises the noise floor at the

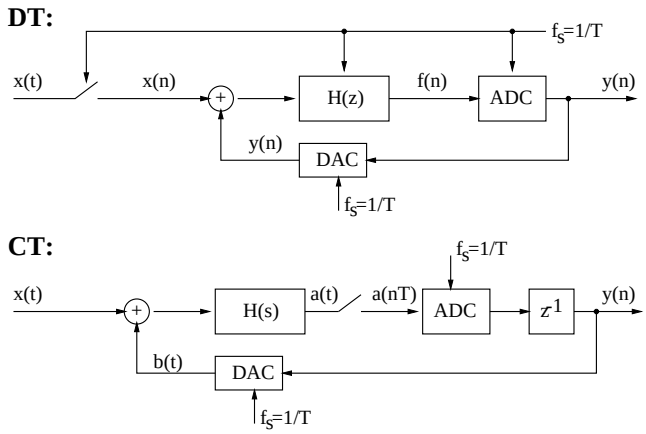


Figure 2.6 A model for DT and CT ΔΣ modulators.

notch frequency and the effect can be reduced a little by using a non-return-to-zero (NRZ) DAC. A time-variant feedback waveform DAC, called an SCR-DAC, is also proposed in order to reduce the effect of clock jitter [4]. The jitter specifications are always more stringent in CT designs than in their DT counterparts. With high input frequencies clock jitter starts to limit the performance of DT ΔΣMs as well and this will be a more and more serious problem.

2.1.4 Performance Parameters

The most significant specifications for ΔΣ modulators are the dynamic range, signal-to-noise-and-distortion ratio, and power dissipation. When different circuits are compared, the speed of ΔΣM as terms of the input signal frequency and the sampling frequency has to be considered. Next, the usual performance parameters are introduced.

2.1.4.1 Dynamic Range

The dynamic range (DR) is the ratio between the maximum input signal and the minimum input signal level, which is detectable at the output, within a specified band. Assuming that the quantization noise does not limit the dynamic range, the main noise sources are the input sampling switch, the DAC switch, and the first amplifier. Com-

bining these noise sources the dynamic range is given by

$$DR = 10log_{10}\left(\frac{1}{2}\frac{A_{max}\sqrt{OSR}}{\sqrt{d\frac{kT}{C_s}+\frac{1}{2}e_{Op1}^2}}\right), \tag{2.9}$$

where A_{max} is the maximum input signal amplitude, C_s is the sampling capacitor, and e_{Op1}^2 the amplifier input-referred total noise. The term d is 1 if the feedback DAC capacitor is shared between the sampling capacitors, but if a separate DAC capacitor is required the switch noise is doubled and hence a term d of 2 has to be used. The separate DAC capacitor is needed if a single-ended reference voltage is used. From Equation (2.9) we see that the DR is directly proportional to the input signal amplitude but proportional to the square root of the sampling capacitor and OSR. Therefore the input voltage level should be maximized and the size of C_s minimized when the power dissipation is minimized with a fixed OSR. However, low power supplies reduce the usable reference voltage range and larger capacitors have to be used, which leads to a higher current consumption.

The signal-to-noise ratio (SNR) is the ratio between signal power and noise power within a specified band. The SNR is usually shown as a function of the input signal level and the measured *peak SNR* or the achieved maximum SNR is announced. The DR and SNR should be designed to be thermal noise-limited rather than quantization noise-limited when low power dissipation is a target.

The signal-to-quantization noise ratio (SQNR) is the ratio between signal power and quantization noise power within a specified band. The SQNR is a useful figure in the design phase and for a 2N-order BP ΔΣM (see Appendix A), we have

$$SQNR_{max} \approx 10log_{10}\left(\frac{3}{2}\frac{(2N+1)OSR^{(2N+1)}}{\pi^{2N}}\right) + 6.02\cdot(B-1), \tag{2.10}$$

where B is the number of bits in the internal ADC. One should be very cautious about using Equation (2.10) for high order (N>2) or multi-bit (B>2) ΔΣMs because the selected circuit structure and different nonidealities affect the achievable SQNR quite considerably. Therefore system level simulation, with a specific circuit structure, has to be used to obtain more realistic results.

2.1.4.2 Linearity

The signal-to-noise-and-distortion ratio (SNDR) is the ratio between signal power and noise and distortion power within a specified band or the ratio between signal power

and all error power. The SNDR is usually reported in the same way as the SNR.

Spurious-free dynamic range (SFDR) is the ratio between signal power and the largest in-band spurious/distortion frequency component.

Harmonic distortion (HD) is the ratio between signal power and the specific harmonic distortion component. The most important is third-order harmonic distortion (HD3). *The total harmonic distortion (THD)* is the ratio between signal power and the sum of total distortion power at harmonic frequencies.

Intermodulation distortion (IMD) is the ratio between signal (tone carrier) power and the distortion component, which two signal components at different frequencies cause as a result of circuit non-linearity. The most important is the third-order intermodulation distortion (IMD3) component, which will appear at the output at frequencies $(2f_1 - f_2)$ and $(2f_2 - f_1)$ when the two input signal tones are at the frequencies f_1 and f_2.

Intermodulation intercept point (IP) is the theoretical signal power which would cause the intermodulation power to be equal to the carrier power. It can be reported as input-referred IP (IIP) or output-referred IP (OIP), in which the gain of the circuit has to be considered. The most important is the third-order intermodulation intercept point (IP3).

Effective number of bits (ENOB), or sometimes only resolution, is the maximum SNDR expressed as bits ((SNDR-1.76)/6.02). The word "resolution" is sometimes used to express DR or SNR as bits, which can cause misunderstanding.

2.1.4.3 Speed, Power Dissipation and Area

Both the sampling frequency and OSR have to be known in order to define the real conversion speed of the $\Delta\Sigma$ modulator which, in the case of Nyquist ADCs, is usually expressed as the number of samples per second. When different circuits are compared the input signal frequency has to be taken into account because high linearity is harder to achieve at high frequencies and clock jitter can start to reduce the circuit dynamic range.

Power dissipation is a very important issue in battery-operated devices, but because of heating problems, has to be considered in other applications too. The technology scaling, together with low power supplies, helps to reduce the power dissipation of digital circuits, but low power consumption and a low power supply in analog circuits are challenges that need to be solved.

The circuit area can be an important figure of merits in some applications, but usually the area of $\Delta\Sigma$ modulators is considered to be small compared to other ADC

topologies. However, in multi-bit ΔΣ modulators the circuit area can be a significant issue.

2.1.5 Design Parameters

The basic design parameters of ΔΣ modulators are the oversampling ratio, the order of the loop filter, and the internal resolution. A higher OSR can be used to increase SNR until the circuit implementation begins to consume too much power as a result of the settling requirements of the amplifiers. Ideally, SNR increases quite sharply when the order of the loop filter is increased. However, the third- and higher-order single-loop LP ΔΣ modulators, equivalent to the sixth- and higher-order BP ΔΣ modulators, may be unstable and therefore cascaded architectures are a possible choice in high-order ΔΣ modulators [5] [6]. Furthermore, SNR can ideally be increased by 6dB by adding one bit to the quantization. In multi-bit ΔΣ modulators the performance can be limited by the non-linearity of the DAC and the loading of the amplifiers is a problem, especially in high-frequency applications [7].

2.2 Architectures

2.2.1 Single-Loop

The multiple feedback (MFB) and the feedforward (FF) topologies shown in Figure 2.7 are the basic single-loop ΔΣM structures. It is also possible to add local resonator feedbacks or combine different structures [2]. It is well known that the third- and higher-order single-loop LP ΔΣ modulators, equivalent to the sixth- and higher-order BP ΔΣ modulators, may be unstable and therefore, in addition to noise-shaping properties, stability issues also have to be carefully considered in the design phase.

The NTF of the FF topology can be derived from Figure 2.7 and we obtain, for a 2N order BP ΔΣM with a center frequency of $f_s/4$

$$NTF_{FF}(z) = \frac{1}{1 - \sum_{i=1}^{N} \frac{a_i z^{-2\cdot i}}{(1+z^{-2})^i}}. \tag{2.11}$$

Similarly, the STF can be found to be

$$STF_{FF}(z) = \frac{\sum_{i=1}^{N} \frac{a_i z^{-2\cdot i}}{(1+z^{-2})^i}}{1 - \sum_{i=1}^{N} \frac{a_i z^{-2\cdot i}}{(1+z^{-2})^i}}. \tag{2.12}$$

There are some restrictions in the use of the FF topology. Firstly, the structure is not suitable for resonator topologies which have only one feedforward delay, because the free arrangement of delays on analog signal paths is not possible. On the other hand, the optimized NTF will cause a fixed STF, which will have some out-of-band gain and hence a prefilter prior to ΔΣM may be required to prevent overloading due to the out-of-band signals. It is of course possible to design a flatter STF but then the quantization noise shaping will be less effective. One drawback is that the analog output signals of the resonators have to be summed prior to the ADC, for example using an SC amplifier, which will consume a good deal of power. An advantage compared to the MFB structure is that only one linear DAC is required, which will help in multi-bit applications.

If a LP MFB ΔΣM with one feedforward delay integrators is used as a prototype we have for the MFB topology (Figure 2.7)

$$NTF_{MFB}(z) = \frac{1}{1-\sum_{i=1}^{N}\left(\frac{(-1)^{(i+1)}z^{-2\cdot i}}{(1+z^{-2})^{i}}\prod_{j=(N+1-i)}^{N}a_j\right)} \tag{2.13}$$

and

$$STF_{MFB}(z) = \frac{\left(\frac{z^{-1}}{1+z^{-2}}\right)^{N}\cdot\prod_{j=1}^{N}a_j}{1-\sum_{i=1}^{N}\left(\frac{(-1)^{(i+1)}z^{-2\cdot i}}{(1+z^{-2})^{i}}\prod_{j=(N+1-i)}^{N}a_j\right)}. \tag{2.14}$$

Feedback delays are different (see Section 5.1.1) if a prototype LP MFB ΔΣM with a delay free integrator is used. Now it is possible to use a resonator topology which has a feedforward delay order of one or two by arranging the delays to the DAC branches. Hence, single-opamp resonator structures can also be utilized. The NTFs of the FF and MFB topology are quite similar and can be designed to be identical (Equations (2.11) and (2.13)). In both cases the designed NTF will also cause a fixed STF. However, the STF of the MFB topology can have a flat response, unlike in the FF structure. A disadvantage compared to the FF topology is the linear DACs needed in each feedback branch. Naturally, the problem is avoided if one-bit feedback is adopted.

2.2.1.1 Stability

In the stability analysis a single-bit ΔΣ modulator is divided into two parts, which are a linear loop filter and a nonlinear quantizer. The nonlinearity is usually modeled by a variable gain factor λ and its value can vary between 0 and infinity [8] [9] [10]. In multi-bit ΔΣ modulators the gain over the quantizer has been defined and the λ is equal to unity if the ADC is not overloaded. Using the notation we may write Equation

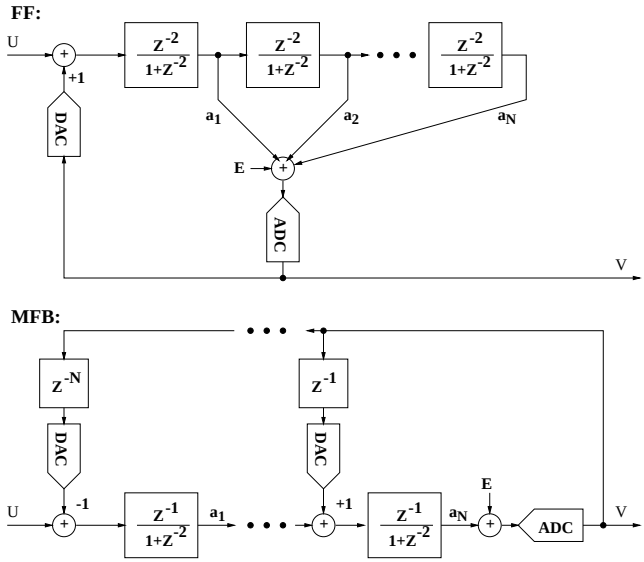


Figure 2.7 Feedforward and multiple feedback BP ΔΣ modulator structures.

(2.13) in the form

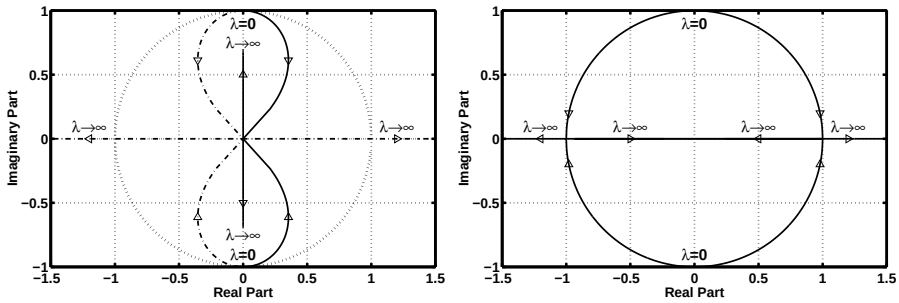
$$NTF_{MFB}(z) = \frac{(1+z^{-2})^N}{(1+z^{-2})^N - \lambda \sum_{i=1}^{N} \left((-1)^{(i+1)} z^{-2\cdot i} (1+z^{-2})^{N-i} \prod_{j=(N+1-i)}^{N} a_j \right)}. \tag{2.15}$$

For stability the system poles have to lie inside the unit circle. However, one pole pair of the BP ΔΣ modulator loop filter can move outside the unit circle and despite the fact, the loop is said to be stable. The oscillation is tolerated in the loop, because the temporary instability increases signal swings at the resonator outputs, which decreases the quantizer gain λ and hence moves the poles inside the unit circle again. If some of the other pole pairs move outside the unit circle, instability occurs.

For an MFB 4th-order (N=2) BP ΔΣ modulator we have

$$NTF^4_{MFB}(z) = \frac{(1+z^{-2})^2}{1+(2-\lambda a_2)z^{-2}+(1-\lambda a_2(1-a_1))z^{-4}}. \tag{2.16}$$

We see that the gain coefficient of the 2nd resonator (a_2) is insignificant in single-bit ΔΣ modulators because the term appears with the indefinite gain of the quantizer. Hence, the loop coefficient a_1 is the only free design parameter. The pole locations are plotted in Figure 2.8 with different values of λ and a_1. We can see that the second pole pair stays inside the unit circle if a_1 is sufficiently low (below one) and hence the ΔΣM is stable even if the other pole pair is temporarily outside the unit circle.



(a) (b)

Figure 2.8 The root locus of the 4th-order BP ΔΣ modulator with (a) $a_1 = 0.5$ or (b) $a_1 = 1$.

The ΔΣ modulator is considered to be higher-order if N is 3 or higher. For an MFB 6th-order (N=3) BP ΔΣ modulator we have

$$NTF^6_{MFB}(z) = \frac{(1+z^{-2})^3}{1+(3-\lambda a_3)z^{-2}+(3-\lambda a_3(2-a_2))z^{-4}+(1-\lambda a_3(1-a_2+a_1a_2))z^{-6}}. \quad (2.17)$$

An example of the root locus is shown in Figure 2.9. When λ increases the one pole pair spreads along the real axis outside the unit circle, as was the case with the 4th-order BP ΔΣM. This increases signal swings at the quantizer input and the gain λ decreases. With some values of λ two pole pairs move outside the unit circle and cause instability. Regardless of the coefficients a_1 and a_2 the loop cannot tolerate the instability, because the further lower values of λ keep the poles outside the unit circle (Figure 2.9). Therefore there is a certain input signal range in which a high-order single-loop ΔΣM is stable and hence usable. If the upper limit of the input is exceeded, the signal swings at the ΔΣM increase too much and λ decreases outside the stability range. The usable input signal range relative to the reference voltages is reduced when the ΔΣM order is increased, which makes it difficult to design an input stage which has a noise level below the quantization noise [9].

The possible instability of the higher-order ΔΣM has to be prevented or at least detected [2]. This is possible by, for example, limiting the output signal level of the last resonator (integrator), which keeps λ high enough. Detection is possible from the input signal level or from the output samples. When the possible instability has been detected the resonators have to be reset so as to enable stable operation once more.

The quantizer gain λ is fixed to the unity if the internal resolution of the ΔΣM is increased (>1bit). Hence a higher-order single-loop multi-bit ΔΣM is stable as a

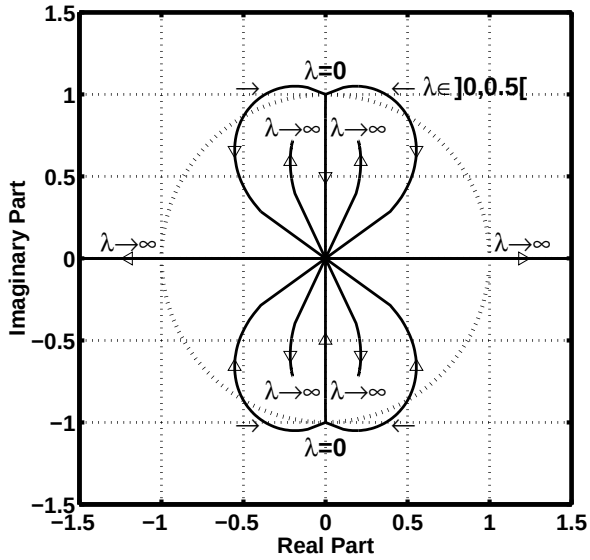


Figure 2.9 The root locus of the 6th-order BP $\Delta\Sigma$ modulator with $a_1 = 1/3$ and $a_2 = 1$ ($a_3 = 3$).

result of proper loop coefficient selection when quantizer overloading is prevented. However, nonlinearity and the loading of the DACs will generate new problems for the design.

2.2.1.2 Loop Filter Design

Depending on the architecture selected, a signal transfer function (STF) and noise transfer function (NTF) can be designed separately or the one can be determined by the other, as in the structures shown in Figure 2.7. The STF is designed to have a flat response, at least over the passband, but the out-of-band signals may be attenuated (Figure 2.10). This would be a preferred property in, for example, radio receivers where the out-of-band blockers decrease the dynamic range. The NTF is designed to minimize the in-band quantization noise, but stability issues also have to be considered. A high SNDR or DR is usually the main target and it is not improved by more effective noise shaping if the usable input range is decreased by the same amount. The degree of freedom in the loop filter design can be augmented by increasing the order of the $\Delta\Sigma$ modulator and by adding local feedback or feedforward paths. However, the selection of the loop coefficients is always an iterative process and long behavioral level simulations are required to ensure loop stability.

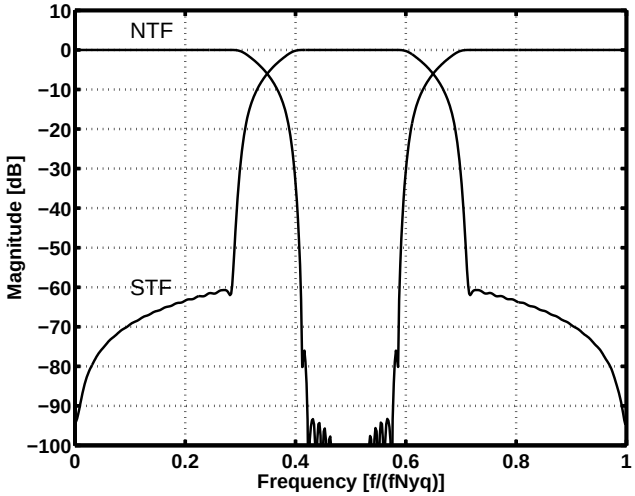


Figure 2.10 Principle of the target STF and NTF in a $f_s/4$ BP ΔΣM.

2.2.2 Cascaded ΔΣ Modulators

A method for designing higher-order ΔΣ modulators and, at the same time, avoiding instability problems is to use cascaded or MASH ΔΣM architectures. The fact that 2nd- and 4th-order BP ΔΣMs are inherently stable can be exploited by cascading lower-order stages, as shown in Figures 2.11 and 2.12. In these structures the quantization error of the preceding stage is used as an input signal for the next stage and after a digital post DSP the output ideally contains only the quantization noise of the last cascade stage.

The block diagram of a 4-4 cascade ΔΣM is shown in Figure 2.11, in which the quantization error of the 1st 4th-order stage is still shaped by the 2nd stage, which is similar to the first one. Using the terms in Figure 2.11 we can write the transfer functions of the stages as

$$V_{1,2}(z) = \frac{a_1 a_2 z^{-2} U_{1,2}(z) + (1+z^{-2})^2 E_{1,2}(z)}{1+(2-a_2)z^{-2}+(1-a_2(1-a_1))z^{-4}}, \tag{2.18}$$

where U is the z-transform of the input signal and E the z-transform of the ADC quantization noise. Typically, the values

$$\begin{cases} a_1 = 0.5 \\ a_2 = 2 \end{cases} \tag{2.19}$$

are selected. The choice cancels the poles of the transfer function and leads to a flat

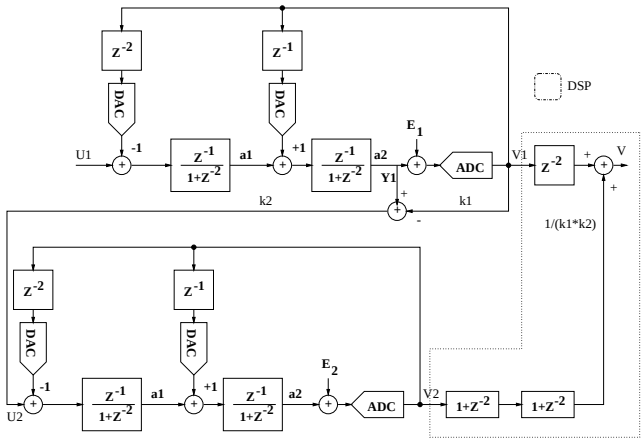


Figure 2.11 A 4-4 (8th-order) cascade BP ΔΣ modulator.

STF. When E_1 is the desired input to the 2nd stage, the value k_1 of 1 has to be selected if the gain a_2 is realized in a resonator, while the value of k_1 should be equal to a_1 if the gain a_2 is realized by scaling the ADC reference voltages. Using these values we obtain the output signal as

$$V_{44}(z) = z^{-4}U_1(z) + \frac{1}{k_1 k_2}(1+z^{-2})^4 E_2(z), \tag{2.20}$$

where k_2 is the scaling factor of the 2nd stage input. Now the quantization noise of the 1st stage is fully canceled and the output contains the 8th-order shaped noise of the 2nd stage multiplied by the term $1/(k_1k_2)$. The input signal of the 2nd stage usually has to be scaled down ($k_2 < 1$) in order to prevent overloading, which decreases the advantage of higher order noise shaping.

8th-order noise shaping can also be implemented by a 4-2-2 cascade BP ΔΣ modulator, as shown in Figure 2.12, and we obtain

$$V_{422}(z) = z^{-4}U_1(z) + \frac{1}{k_1 k_2 k_4}(1+z^{-2})^4 E_3(z). \tag{2.21}$$

If the 6th-order noise shaping is adequate, the last resonator stage can be removed.

Effective quantization noise shaping in the cascade ΔΣ modulators is based on matching between analog and digital transfer functions. This is a prerequisite for the proper cancellation of the preceding stage's quantization noise. If there is some mismatch between the analog and digital side the low-order shaped noise will leak to the output and will rapidly reduce the dynamic range. The accuracy required for the capacitor ratios and the properties of the amplifier set the upper limit for the rational

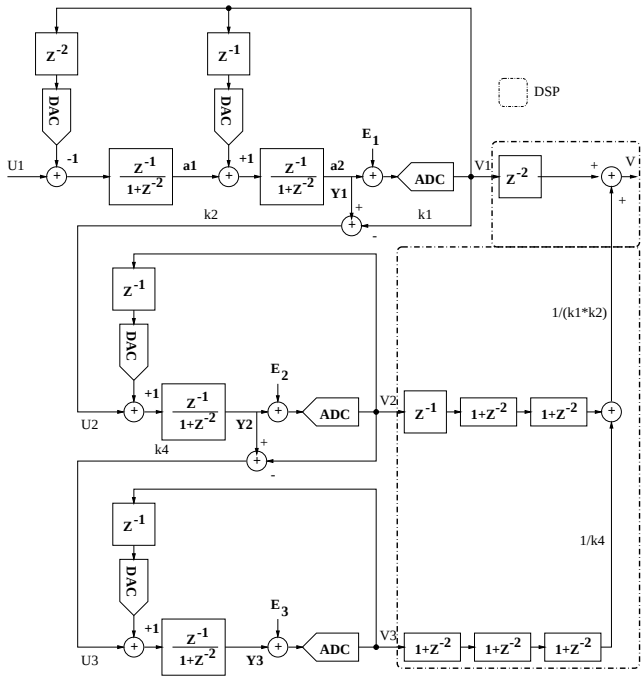


Figure 2.12 A 4-2-2 (8th-order) cascade BP ΔΣ modulator.

order of the cascaded ΔΣM with a fixed OSR.

The first cascade stage could also be a second-order one instead of a 4th-order one. But then the possible leakage power of the first stage is shaped only by the second-order transfer function $(1+z^{-2})$ and the properties of the first resonator are more stringent. Therefore the natural choice is to use the highest-order and stable BP ΔΣM in the first stage and shape its quantization by extra stages if necessary.

1-bit or multi-bit ADCs/DACs can be used in the cascade ΔΣMs. According to Equations (2.20) and (2.21), only the quantization noise of the last stage ADC is relevant. In this sense it is reasonable to implement only the last ADC as a multi-bit structure, because only its quantization noise is visible at the output and the linearity of the DAC is not as critical as in the first stage, because the DAC error will be shaped by the digital filter. However, the use of a multi-bit ADC at the first stage would decrease the possible leakage noise at the output. Furthermore, the input error signal for the next stage becomes smaller and hence the input scaling factor (k_2) can be increased, which directly improves the resolution. Therefore, the use of multi-bit ADCs in all stages may be reasonable.

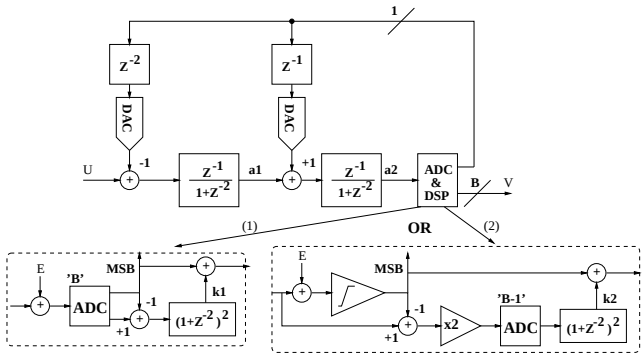


Figure 2.13 A 4-0 (4th-order) cascade BP ΔΣ modulator using two alternative circuit structures for the 2nd stage.

2.2.2.1 Leslie-Singh Topology

It is possible to implement a cascade stage without noise shaping [11]. Then only a multi-bit ADC realizes the 2nd stage and the extra bits are used to cancel the coarse quantization noise of the first stage (Figure 2.13). The DAC utilizes only 1-bit or the MSB of the ADC and, hence, DAC nonlinearity is not an issue. Of course, it is possible to use a moderate resolution (2b-3b) in the DAC and higher resolution in the ADC (>3b). The output signal can be written as

$$V_{40}(z) = z^{-2}U(z) + k_{1,2}(1+z^{-2})^2 E_q(z), \tag{2.22}$$

where E_q is the quantization noise of the B-bit ADC. Hence, the output signal ideally includes only the quantization noise of the B-bit ADC shaped by the 4th-order transfer function and multiplied by the term k. The quantization can be performed directly by means of a B-bit ADC and, after that, the remaining signal processing is fully digital. This is the alternative (1) shown in Figure 2.13 for which we should select

$$k_1 = \frac{1}{a_1 a_2}. \tag{2.23}$$

The loading of the ΔΣ modulator can be reduced by performing the quantization in two stages. The disadvantage is that the MDAC is needed to perform the MSB subtraction but the resolution of the fine quantization is reduced by one bit. The alternative (2) is shown in Figure 2.13 for which we require

$$k_2 = \frac{1}{2a_1 a_2}. \tag{2.24}$$

We can see that the theoretical resolution can be decreased as a result of the signal scaling, as it was earlier with other cascaded structures. The term k can be quite large in ΔΣ modulators with a 1b feedback, in particular because quite a small coefficient a_2 is required to attenuate signal swings at the 2nd resonator output. The problem can be solved by using a 2b (or >2b) DAC, because then the signal scaling requirements are relaxed and the gain of the ΔΣM loop is usually fixed to $a_1 a_2 = 1$.

The mismatch between the analog ΔΣM loop filter and the digital filter can easily increase the noise at the signal band, because the first stage noise leaks to the output, as in the other cascade topologies. A method is to use an adaptive digital filter in the 2nd stage [12].

2.2.3 Internal Resolution

The main motivation for adding more bits to the loop is the direct reduction of quantization noise and the improvement in the dynamic range (Equation (2.10)). Furthermore, the stability constraints are much easier to achieve than with single-bit structures and the internal signal swings of the loop are decreased, which relieves the amplifier design in the sense of the slewing requirements that are placed on it. On the other hand, the loading of the amplifiers is a problem, especially in the case of high-frequency applications [7], and more analog circuit components are needed to implement internal ADCs and DACs. The possibility of using higher gain on the part of the resonators (integrators) than in a single-bit loop can improve the SNR by even more than 6dB per added bit [13]. In multi-bit ΔΣ modulators the out-of-band quantization noise is also reduced, which relieves the digital post filtering.

Despite the advantages of multi-bit structures, single-bit ΔΣ modulators are the most frequently used. The reason is the nonlinearity of the required multi-bit feedback DAC, which sets the upper limit for ΔΣM performance. The possible distortion noise in the DAC is not shaped in the loop of the ΔΣM but is directly added to the input, as shown in Figure 2.14. Therefore the output signal of the ΔΣM is

$$V(z) = STF(z) \cdot [U(z) + D(z)] + NTF(z) \cdot E(z), \tag{2.25}$$

where the distortion noise of the DAC (D) is only shaped by the STF. Hence, the linearity of the whole ΔΣM cannot be better than the linearity of the internal DAC. DAC linearity can be improved by element trimming, but this is expensive and not a suitable method for mass-produced products. Calibration techniques may be utilized, but extra hardware and calibration time are needed [14] [15]. Nowadays, different dynamic element matching (DEM) techniques, which randomize and/or shape the distortion noise

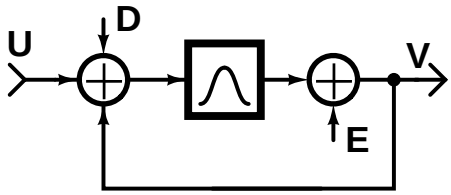


Figure 2.14 A simplified model of the BP ΔΣM with a nonlinear DAC.

of the DAC to improve the linearity over the signal band [16]- [32], are widely used. This is possible with oversampling converters because the out-of-band noise is filtered afterwards. The DEM technique can also be used for error correction in the internal ADC of the ΔΣM [33] or utilized together with a calibration technique [34]. Next, the most common DEM techniques are briefly reviewed.

2.2.3.1 DEM Overview

A single-bit DAC is inherently linear because the output varies only between two values. If the levels are added the mismatch between the DAC elements causes a gain variation from the ideal curve (Figure 2.15). An absolute DAC error is of no consequence in the sense of DAC noise but the gain variation between DAC levels increases the nonlinearity. For example, if the full-scale output signal of a three-level DAC is normalized to one, the input signal '1' produces the output signal

$$DAC_o = 0.5 + \frac{\varepsilon}{2} \vee DAC_o = 0.5 - \frac{\varepsilon}{2}, \tag{2.26}$$

where ε is the relative mismatch term between the DAC elements. The nonlinearity causes harmonic distortion components at the output, which the different DEM techniques try to move in the frequency domain or convert to white noise. Furthermore, the effect may be boosted by first- or higher-order noise shaping characteristics.

Clocked Averaging The clocked averaging (CLA) technique changes the unit elements of the DAC in a periodic manner [35]. For example, if the input signal to the DAC in Figure 2.15 is equal to one, the output is produced by either of the two DAC unit elements and the elements are changed by a periodic frequency f_{clk}. Hence, the DC error of the output will be zero. In fact, the harmonic distortion components are moved to the surrounding frequencies, which are multiples of the switching clock frequency. The method can be extended to a DAC with more than two elements using a stack of CLA blocks [35] or a flipping algorithm [17]. To avoid distortion components

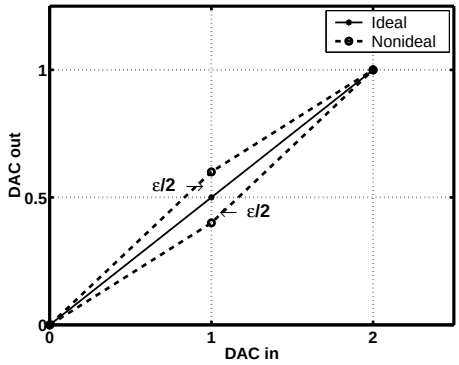


Figure 2.15 A transfer function of the 3-level (1.5-bit) DAC.

falling back into the signal band, the OSR has to be high enough and the requirements of the antialias filtering may be tightened [17].

Random Averaging The random averaging (RDA) technique connects the M inputs of the DAC to the M outputs by changing the connections in a random manner, unlike in the CLA technique [16]. The method attempts to convert the DAC distortion components to white noise, whereas the CLA tries to move the distortion components away from the signal band. A butterfly network [16] or a less complex tree-structured encoder [31] may be used for the implementation when the DAC has many elements.

Individual Level Averaging The problem with CLA is the tones whose frequency depends on the input signal and on the CLA clock frequency. The main reason is the correlation between the periodic averaging method of the DEM and the interpolating loop of the $\Delta\Sigma$ modulator [17]. In individual level averaging (ILA), each output code of the DAC is alternately generated using all the DAC elements [17]. The advantages of the ILA are low tones and a lower noise floor at the DC frequency than is the case with the RDA, but the disadvantage is the complexity of the system when the DAC resolution is increased [32].

Data Weighted Averaging To average the DAC mismatch error near the DC frequency, all the elements should be used equally often. Furthermore, the averaging time should be small because then the distortion noise is moved to higher frequencies. If the CLA technique is used it can take a (very) long time before the condition is met and, furthermore, the operation depends on the signal. With ILA the averaging time can also be quite long, because all the DAC levels with a different configuration of

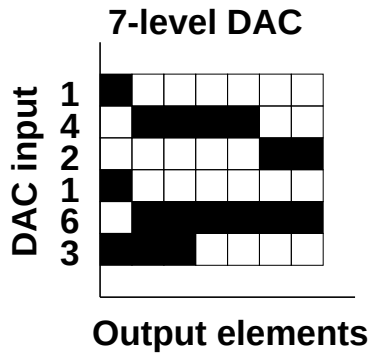


Figure 2.16 An example of the DAC element selection in a DWA DEM with the $(1-z^{-1})$ noise shaping characteristic.

elements have to be trawled through. In principle, the RDA uses all the DAC elements equally often, but the passing-through time of the element array varies randomly.

The data weighted averaging (DWA) technique maximizes the use of each DAC element and ensures that each element is used the same number of times [19]. The DAC elements are selected from the element array so that the output code is generated by starting from the next unused element (Figure 2.16). The selection method actually has a first-order noise shaping characteristic but an arbitrary noise shaping function is feasible with a different selection algorithm [20]. Hence, LP second-order noise shaping or BP noise shaping functions can be realized with the DWA technique.

2.2.3.2 DEM for BP ΔΣM

The published discrete-time BP ΔΣ modulators (ADCs) have been realized with a single-bit feedback, except the circuits in [29] and [30], where a 9-level or 33-level DAC and a BP DWA DEM are utilized (Table 2.1). There are experimental results of DWA DEMs in DAC BP ΔΣ modulators in [23] [26] [28], but otherwise little research has been performed regarding bandstop noise-shaping DEMs [18] [20] [22]. All the published BP DEM methods are based on DWA, but of course the RDA can be utilized if the DAC distortion components and the noise floor are sufficiently low for the application.

A bandstop DWA DEM has to be of second or higher order. A simple method to realize the transfer function is to use the N-path structure of a suitable LP DWA DEM [22] [23]. However, the in-band noise power will be 6dB higher (N=4) than it would be with a transfer function $H(z) = (1+z^{-2})$, but the advantage is the simple circuit structure [22]. One method is to utilize a general error feedback system DEM

Table 2.1 An overview of DEM techniques.

	CLA	RDA	ILA	DWA
Noise shaping	none	none	1st order	1st-, 2nd-, (higher-) order
Advantage	low tones	low tones	low tones	noise shaping
Disadvantage	sig.dependence	high noise	complexity	(complexity)
+/- for ΔΣMs	-	+	++	+++
LP ΔΣM	T: [17]E: [35]	T,E: [16]	T: [17]E: [32]	T: [19]- [21]E: [24]- [27]
BP ΔΣM DAC	N/A	N/A	N/A	T: [20] E: [23] [26] [28]
BP ΔΣM ADC	N/A	N/A	N/A	T: [22] E: [29] [30]

('T'=theoretical paper; 'E'=experimental paper)

[18] [26] [29] or divide the filtering into a network as a butterfly shuffler [28].

2.3 Nonidealities in Noise Shaping

BP ΔΣ modulators consist of resonators, instead of the integrators of their LP counterparts. The properties of the resonators directly affect the noise-shaping performance of the BP ΔΣ modulator and, furthermore, a high-quality resonator is hard to implement. Next, the effect of nonidealities is analyzed on the ΔΣM level; analysis at the resonator level will be presented in Chapter 4.

2.3.1 Single-Loop ΔΣ Modulators

If we assume a basic single-loop BP ΔΣ modulator structure (Figure 2.7) and eliminate the possible poles of the noise transfer function, the NTF of a 2N-order BP ΔΣ modulator is

$$NTF(z) = \left(1 - p_1 z^{-1} + p_2 z^{-2}\right)^N, \tag{2.27}$$

where p_1 (ideally zero) and p_2 (ideally one) for $\pi/2$-resonator describe the effects of nonidealities.

The preferred BP ΔΣ modulator topology is usually a 4th-order or cascaded structure if higher-order noise shaping is needed. Therefore, it is reasonable to calculate the noise power for a 4th-order(N=2) modulator for the sake of simplicity. Assuming that the band of interest is around $\pi/2$, we have (see Appendix B)

$$n_0^2 \approx N_q f_s \left[\frac{h_1}{OSR} + \frac{h_2\pi^2}{OSR^3} + \frac{h_3\pi^4}{OSR^5}\right], \tag{2.28}$$

where the terms h_i are functions of the parameters p_i according to Equations (B.4) and (B.6). By comparing Equations (2.7) and (2.28) we can see that the additional

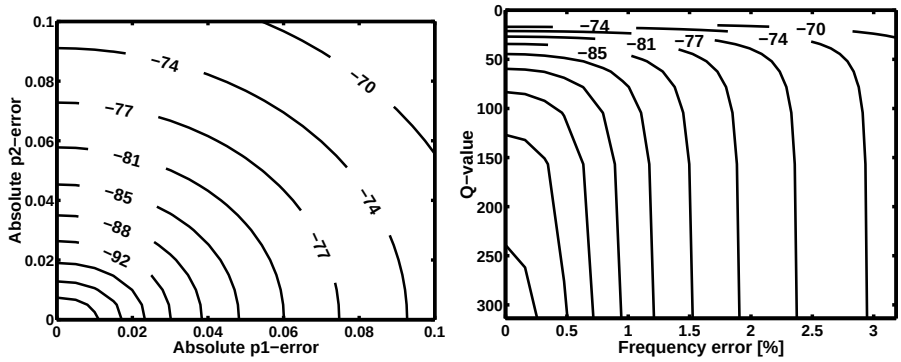


Figure 2.17 The effect of error in p_1- and p_2-terms on in-band noise power [dB] in a 4th-order BP $\Delta\Sigma$ modulator with two identical resonators (OSR=150, $\Delta = 1.0$) and the result as a function of the Q-value and the frequency error of the resonators.

terms, which are proportional to OSR^{-1} and OSR^{-3} instead of OSR^{-5}, appear in the last equation and therefore the in-band noise power will increase quite rapidly with h_1 and h_2.

With a narrow bandwidth (high OSR) the error in both terms (p_1,p_2) increases the noise power greatly and almost equally (Figure 2.17). If we allow the noise power to increase by 1dB as a result of mismatch terms separately, the error in p_1 should be below 3.3e-3 and in p_2 below 5.6e-3. In Chapter 4 the values for the relative notch frequency error and for the required Q-value of the resonator will be derived (Figure 2.17). The corresponding error in the notch frequency should be below 0.1% and a Q-value of over 280 is required. It is obvious that the requirements are relaxed with large bandwidths (low OSR), and so inferior resonators can be utilized.

As shown by the previous discussion, the performance of the whole BP $\Delta\Sigma$ modulator is very sensitive to the properties of the resonator used. In particular, even small errors in the resonance frequency will degrade the SNR, as, for example, in a published BP $\Delta\Sigma$ modulator [36]. The performance is not equally sensitive to the changes in the Q-value but it has to be sufficiently high for the relevant OSR.

2.3.2 MASH $\Delta\Sigma$ Modulators

In cascaded architectures the main problem is the leakage noise power of the first stage to the output of the BP $\Delta\Sigma M$, which is caused by mismatch between a digital and an analog transfer function. It is reasonable to implement the first cascade stage as a 4th-order one, as discussed earlier in Section 2.2.2. The leakage quantization power

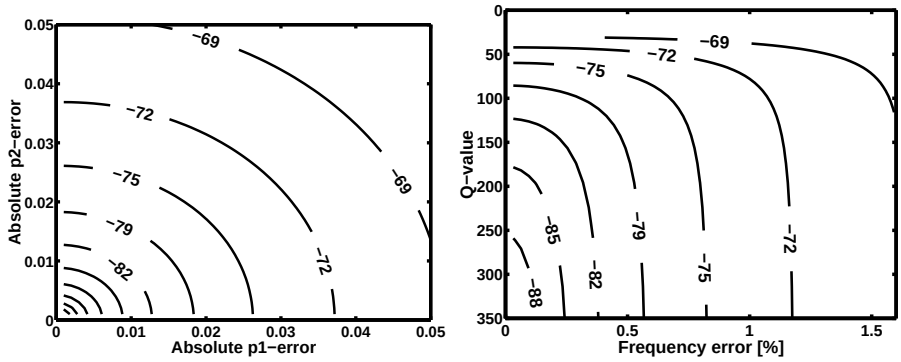


Figure 2.18 The first stage (4th-order, $f_s/4$) leakage noise power to the output in a cascaded architecture as a function of resonator characteristics (OSR=30, $\Delta = 1$).

of the first cascaded stage (a 4th-order $f_s/4$ BP $\Delta\Sigma M$) at the output can be written (see Appendix B) as

$$n_{0le}^2 \approx e_{rms1}^2 \left(\frac{c}{OSR} + \frac{\pi^2}{3} \frac{b}{OSR^3} \right), \tag{2.29}$$

where e_{rms1}^2 is the quantization noise power of the first cascade stage and the terms c and b are functions of the parameters p_i according to Equations (B.12) and (B.10). We can see that the leakage noise has first-order dependence on the OSR and hence the leakage is sensitive to the growth of the term c or errors in the resonator terms p_1 and p_2. From Equation (2.29) we can also see that the multi-bit quantizer in the first stage will directly decrease the leakage noise power at the output. Hence, the first cascade stage may be implemented using a multi-level ADC and DAC, though ideally the noise is not visible at the output.

From Figure 2.18 we can see how the resonator characteristics affect the leakage noise power and set an upper limit for the achievable dynamic range. According to Equation (2.7) the ideal in-band noise power of the 6th- and 8th-order BP $\Delta\Sigma M$ is -92dB and -113dB, respectively (OSR=30, $\Delta = 1$). If, for example, a 6th-order BP $\Delta\Sigma$ modulator (OSR=30) is implemented using a cascade architecture, the resonator Q-value should be over 400 and the frequency error below 0.12%. If these limits are exceeded, the leakage noise power starts to limit the performance and the second stage increases power dissipation too much. With an 8th-order cascade BP $\Delta\Sigma$ modulator the requirements for the resonators are yet more stringent. Because of these limitations a higher order cascade architecture may be used when the OSR is in the order of several dozens. If 4th-order noise shaping is not adequate and the OSR is high, a single-

loop higher order BP ΔΣ modulator may be used. However, the properties of the resonators limit the performance of single-loop structures as well (Equation (2.28)). Instead, multi-bit structures are the best choice for very low OSRs, because higher ΔΣ modulator orders improve the resolution precious little.

Because the leakage noise is caused by mismatch between the analog and digital filters, a straightforward method to reduce the leakage would be to change the coefficients of the digital filter so as to match the analog. However, the problem is that the analog transfer function is not constant due to the process variations, temperature variations or amplifier properties. Therefore the digital filter should be able to adapt to changes in the analog circuitry [12].

2.4 Design Aspects

There are many open questions when starting the design procedure of a BP ΔΣ modulator. Usually, at least the signal bandwidth, target resolution, power supply, technology, and maximum power dissipation are determined by the system specifications. When designing ΔΣ modulators to achieve a specified signal-to-noise ratio (SNR) and dynamic range (DR), the design parameters are the oversampling ratio (OSR), the order of the loop filter (n), and the internal resolution (B). First, a higher OSR is used to increase the SQNR until the circuit implementation begins to consume too much power as a result of the settling requirements of the amplifiers. On the other hand, the sampling frequency can be fixed on the system level, leading to a fixed OSR or, for example, the clock jitter can determine the minimum OSR. Secondly, the SQNR ideally increases quite sharply when the order of the loop filter is increased. However, third- and higher-order single-loop LP ΔΣ modulators, equivalent to sixth- and higher order BP ΔΣ modulators [37] [38], may be unstable and therefore cascaded architectures are a good choice for higher-order BP ΔΣ modulators [5] [39]. However, in cascaded structures the performance is usually limited by the leakage of the integrators or by the mismatch between the analog and the digital transfer functions. Thirdly, the SQNR can be ideally increased by 6dB by adding one bit to the quantization. In multi-bit ΔΣ modulators the performance is limited by the non-linearity of the DAC and therefore different error averaging techniques are usually required. Furthermore, the loading of the amplifiers is a problem, especially in high-frequency applications.

As the previous discussion shows, the design procedure of BP ΔΣ modulators is an iterative process and hence there is no direct answer to the questions of what is the correct architecture, the optimized sampling frequency, or the quantizer resolution. Regardless of the selections adopted, however, there are common design aspects,

which are discussed next.

2.4.1 Dynamic Range and Power Dissipation

If we want to increase the circuit's noise power limited dynamic range, it will lead to higher power dissipation, according to Equation (2.9). A higher OSR calls for a higher sampling frequency, which reduces the available settling time of the amplifier. On the other hand, the slewing capacitance is directly proportional to the sampling capacitance, or a larger sampling capacitor increases the required slewing current. The equivalent load of the opamp will also increase, which calls for a larger bias current. Also if opamp noise limits the noise floor, more bias current is required. The maximum usable input signal amplitude can be determined by the stability constraints in higher-order single-loop structures, and then a re-design of the loop filter or a different circuit architecture may improve the dynamic range without a power penalty. If the operation of the transistor switches limits the voltage levels used, the higher reference voltages will also lead to higher power dissipation as a result of the required clock signal boosting circuits. The output signal levels of integrators and some SC resonators can be scaled down abruptly without increasing the amplifier load. However, the signal levels have to be re-scaled in the next stage of the $\Delta\Sigma$ modulator, which increases the capacitive load of both the previous stage and the next stage. Impedance level scaling facilitates the situation but it is limited by the smallest usable capacitance determined by the process parameters. Slightly higher reference voltages can be used if an amplifier with a large output signal swing capability is adopted, which again leads to a higher current consumption. In summary, when a higher dynamic range is targeted, the current consumption will almost invariably increase, but the design task is to minimize the accretion of the power dissipation.

2.4.2 Signal Level Scaling

The total noise in a $\Delta\Sigma$ modulator consists of the quantization noise and electrical noise from the circuitry. The circuit noise is mainly determined by the thermal noise of the switched sampling and DAC capacitors (switches) in the first stage, together with the noise sources of the first amplifier. Assuming that the quantization noise does not dominate, the achieved dynamic range is proportional to the square root of the sampling capacitor but directly proportional to the input signal amplitude (Equation (2.9)). Therefore the modulator should be designed for as high an input signal (reference) level as possible so as to achieve the required dynamic range when a low power dissipation is required.

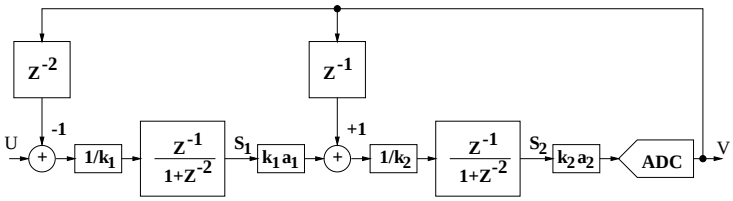


Figure 2.19 A block diagram of the 4th-order BP ΔΣ modulator.

For example, a block diagram of the 4th-order MFB BP ΔΣ modulator is shown in Figure 2.19, where the terms k_1 and k_2 are signal level scaling coefficients. The output signal levels of the resonators (S_1 and S_2) are simulated by setting the gain coefficients of the resonators to the values $a_1 = 0.5$ and $a_2 = 2$ (not valid in a 1b-loop). These are the most commonly used values and the selection also eliminates the poles of the NTF and makes possible a flat STF. On the other hand, the performance of the 4th-order BP ΔΣM is not very sensitive to the values of the gain coefficients [40]. A simulation result of the resonator output swings, when the internal resolution of the loop is 1b, 2b or 3b, is shown in Figure 2.20. We can see that the internal signal swings of the 1b BP ΔΣ modulator are several times higher than the input signal amplitude. When the resolution of the ADC and DAC is increased, the largest voltage swings are roughly halved, because the loop operates more like a linear filter. It is obvious that the resonator output signals need to be scaled down if the supply voltage is low, and the required scaling factors are quite large, especially if the internal resolution is only 1b. This has been a serious problem in previously published single-opamp SC resonators, because the load of the amplifiers increases as a function of the scaling coefficient. The SC resonator structures which solve the problem will be presented in Chapter 4.

A 1b loop filter can have a range of behavior with some input frequencies (Figure 2.21), which has to be considered in wide-band applications. We can see that the resonator swings increase very rapidly with some input frequencies (input 0.045-0.1 f_{Nyq} offset from the resonance frequency). The signal levels grow when the quantization noise interacts with the input signal over a certain frequency range as a result of the nonlinear ΔΣ modulator feedback loop [41]. The problem is eliminated by adding more bits to the loop (Figure 2.21), and it also becomes less severe in a 1b-loop when the input signal level is reduced. A possible solution is to decrease the gain (a_1) of the first resonator below 0.5, which has a stabilizing effect on the feedback loop and eliminates the undesired operation of the loop [10] [41].

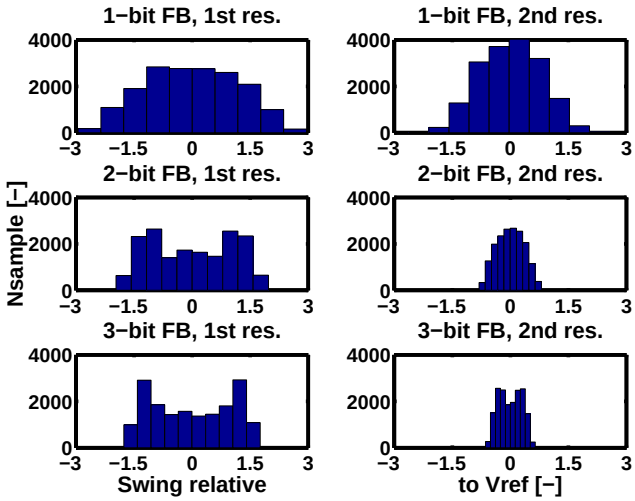


Figure 2.20 Simulated resonator output swings in a BP ΔΣM (Figure 2.19, a_1=0.5, a_2=2, $k_1 = k_2 = 1$, input 0.502 f_{Nyq} -3dB below V_{ref}).

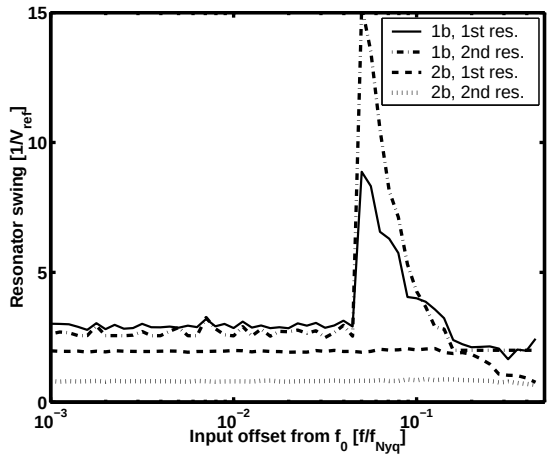


Figure 2.21 Simulated maximum output swings of the resonators in a 4th-order BP ΔΣ modulator (input -3dB below V_{ref}).

2.4.3 Amplifiers

An operational amplifier is a basic building block of active analog circuits [45] [46]. The properties of the amplifier often set the upper limit for the achievable performance of the whole analog circuit in terms of dynamic range, noise, distortion, speed, and power dissipation. Therefore, a basic task in analog circuit design is to optimize the power dissipation and the required performance of the opamp with the usable technology. In textbooks and in other publications, there are several opamp circuit topologies and their different variations and hence this section gives only an overview of the opamps used in this work.

2.4.3.1 Opamp Requirements in BP ΔΣMs

The input impedance of the opamp in SC circuits has to be purely capacitive, which limits the exploitation of the BiCMOS technology because the input pair has to be implemented using MOSFET transistors. Furthermore, the load of opamps is fully capacitive and hence the opamp can have a large output impedance, enabling the utilization of operational transconductance amplifiers (OTAs).

The DC gain of the opamp affects the precision of the feedback system. In BP ΔΣMs the opamp is used to realize a resonator and hence the DC gain has an impact on the Q-value of the resonator and on the accuracy of the resonance frequency. Typically, a DC gain of the order of $10^3 - 10^5$ (60-100dB) is adequate.

Because of the gain-bandwidth product (GBW) or the unity-gain frequency of the opamp, the accuracy of the feedback loop depends on the clock frequency. A low GBW has a similar influence on the resonator properties to a finite DC gain, but, instead of the static dependence, the small-signal output-input relation of the opamp is

$$\frac{V_{out}(t)}{V_{in}(t)} = 1 - e^{-(\frac{t}{\tau})}, \tag{2.30}$$

where τ is the time constant of the feedback and it is inversely proportional to the value of the GBW. Hence, the finite GBW of the opamp can cause a charge transfer error in SC circuits as a result of incomplete settling. The available linear settling time is below half of the clock period in normal circuit structures and the required settling accuracy also depends on the large signal behavior of the opamp. Usually, in discrete-time BP ΔΣ modulators the GBW should be adequate to confirm the settling accuracy between 0.001-0.1% ($7\tau - 10\tau$) and this calls for a unity-gain bandwidth of four to six times the clock frequency used. This makes also possible the adequate high loop gain to settle the disturbance noise of the clock generator and the digital parts.

The output voltage of the opamp has a rate of change limited by time and therefore a large input signal will cause nonlinear settling behavior. The nonlinear settling characteristic of the opamp is described by the slew-rate (SR), which depends on the maximum output current of the opamp (I_{SR}) and the capacitive loading during slewing (C_{slew})

$$SR = \frac{I_{SR}}{C_{slew}}. \tag{2.31}$$

Opamp slewing is undesirable in ΔΣ modulators, because the nonlinear settling will cause harmonic distortion [42] [43]. However, in ΔΣ modulators it requires the use of a great deal of power, or it may even be impossible, to prevent opamp slewing, because of the large signal steps. Therefore, long circuit simulations are required to find out the required SR and GBW of the opamp, which ensures an adequate low distortion level and high settling accuracy. As a design starting point, a rough rule is to allocate a third of the available settling time to the slewing and the latter two-thirds to the linear settling.

In ΔΣ modulators differential opamps are used and therefore the common-mode voltage levels of the output and the input are not directly fixed. The output common-mode level is set to a designed value (usually near $V_{dd}/2$) using a common-mode feedback circuit, which can have a continuous-time or a discrete-time topology. A target in ΔΣ modulators is to maximize the output voltage swing of the opamp. When the SC circuit technique is adopted, the input common-mode level can be selected freely, regardless of the output common-mode level. Therefore, for example in the folded cascode opamp topology, the input common level is designed to be higher than $V_{dd}/2$ if a nMOS and lower than $V_{dd}/2$ if a pMOS input pair is employed.

The noise of the opamp contains the flicker noise (1/f noise) and the thermal noise. The input referred 1/f noise power density of a MOSFET is

$$e^2_{Op\_f} = \frac{KF}{2\mu_0 C^2_{ox} WL} \cdot \frac{1}{f}, \tag{2.32}$$

where KF is the flicker noise coefficient, μ_0 the carrier mobility, and C_{ox} the gate oxide capacitance. KF is a process-dependent parameter and it is considerably lower for pMOS transistors than for nMOS transistors. Instead, the nMOS transistors are faster (higher μ_0) than the pMOS transistors. However, in conclusion, the flicker noise of the pMOS transistor is lower than with nMOS transistors, and therefore they are preferred in LP ΔΣ modulators. An important remark is that the area of the input transistors should be enlarged until the 1/f noise is low enough (Equation (2.32)). In BP ΔΣ modulators the 1/f noise is not of consequence and hence a nMOS input pair

may be used, because of the inherently higher transconductance. The gate-referred thermal noise power density of a MOSFET is given by

$$e^2_{Op\_kT} = \frac{4\gamma kT}{g_m}, \tag{2.33}$$

where g_m is the transistor small signal transconductance and γ is a process-dependent noise excess factor, which is 2/3 for long channel devices (L>1.7μm) but can be considerably larger for short channel devices because of hot carrier effects [44]. Furthermore, γ increases when the gate-source (v_{gs}) or the drain-source (v_{ds}) voltage of the transistor increases [44]. The thermal noise of the opamp input transistors is given directly by Equation (2.33). The noise contribution of the other transistors will be divided by the input gain and hence the total thermal noise of the opamp is reduced by increasing the g_m of the input pair. This can be done by using a nMOS input pair, by increasing the bias current, or by enlarging the gate width of the input transistors.

2.4.3.2 Basic Topologies

The cascode opamp topologies are a natural choice for $\Delta\Sigma$ modulators because the high output impedance is no of consequence. The telescopic OTA depicted in Figure 2.22a is a very fast opamp topology. The GBW is determined by the transconductance of the input transistor and the load capacitance, while the non-dominant pole depends on the transconductance of the cascode transistor and the parasitic capacitances on the nodes n1 and n2. Now, if a nMOS input pair is used the GBW is maximized and at the same time the non-dominant pole depends on nMOS transconductance, which also improves the phase margin. The disadvantage of the topology is a narrow output swing, which is limited below $V_{dd} - 5v_{dsat}$. Furthermore, the input common mode level has to be set quite accurately and the allocated margin further reduces the output voltage range. Due to the many cascode devices it requires, the topology is not suitable for $\Delta\Sigma$ modulators if the power supply is reduced below 3 V.

The output voltage swing can be increased a little using a folded cascode OTA, as shown in Figure 2.22b, but the power dissipation increases. In this topology the output voltage swing is limited below $V_{dd} - 4v_{dsat}$ and the improvement, compared to the telescopic topology, is quite marginal, and the power supply cannot be decreased below 2.5 V. In principle, the topology is as fast as the telescopic OTA. However, if the GBW is maximized using a nMOS input pair the phase margin is decreased because of the pMOS cascode transistors. On the other hand, if a pMOS input pair is utilized, the 1/f noise is minimized and the phase margin is increased, but the GBW decreases.

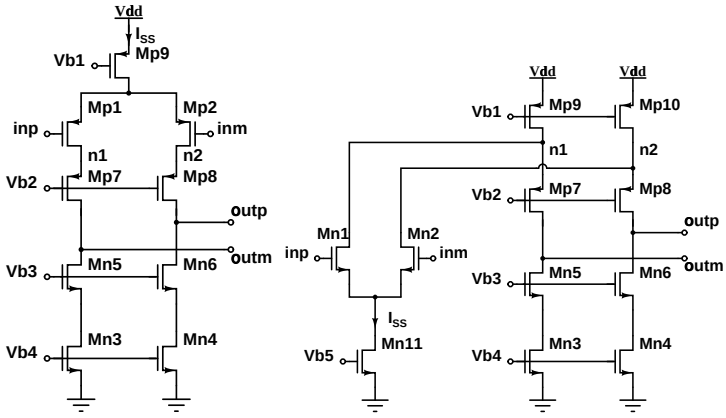


Figure 2.22 a) A telescopic OTA with pMOS input pair and b) a folded cascode OTA with nMOS input pair.

The evident advantage of the topology is the possibility it provides to select the input common mode level quite freely. If, for example, a pMOS input pair is adopted, the input common mode level can be set almost to a negative power supply, which again improves the operation of the nMOS transistor switches.

There is a continuous trend to decrease the power supply of analog circuits, along with their digital counterparts. When the power supply is reduced below 2.5 V, the basic cascode opamp topologies in Figure 2.22 are not feasible. Two-stage opamps enable a high DC gain and a large output signal swing even when the power supply

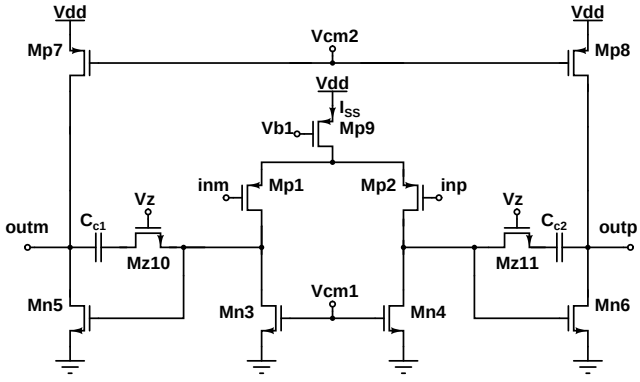


Figure 2.23 A Miller compensated opamp with pMOS input pair.

Table 2.2 A comparison of opamps.

	Telescopic OTA	Folded cascode OTA	Miller compensated
Stages	1	1	2
DC gain	$\frac{g_{m1}}{\frac{g_{ds3}\cdot g_{ds5}}{g_{m5}}+\frac{g_{ds7}\cdot g_{ds1}}{g_{m7}}} \sim \frac{g_m^2}{2g_{ds}^2}$	$\frac{g_{m1}}{\frac{g_{ds3}\cdot g_{ds5}}{g_{m5}}+\frac{g_{ds7}\cdot(g_{ds2}+g_{ds9}))}{g_{m7}}} \sim \frac{g_m^2}{3g_{ds}^2}$	$\frac{g_{m1}}{g_{ds1}+g_{ds3}}\cdot\frac{g_{m5}}{g_{ds5}+g_{ds7}} \sim \frac{g_m^2}{4g_{ds}^2}$
GBW	$\frac{g_{m1}}{C_L}$	$\frac{g_{m1}}{C_L}$	$\frac{g_{m1}}{C_c}$
2nd pole	$\frac{g_{m7}}{C_{pn1}}$	$\frac{g_{m7}}{C_{pn2}}$	$\frac{g_{m5}}{C_L}$
Speed	+++	++	+
I_{SR}	I_{SS}	I_{SS}	I_{SS}
$I_{V_{dd}}$	I_{SS}	$\approx 2I_{SS}$	$\approx 3I_{SS}$
Output swing	$V_{dd}-5v_{dsat}-v_{incmr}$	$V_{dd}-4v_{dsat}$	$V_{dd}-2v_{dsat}$
Noise $\frac{8kT}{g_{m1}}*$	$\left(\gamma_1+\gamma_3\frac{g_{m3}}{g_{m1}}\right)$	$\left(\gamma_1+\gamma_3\frac{g_{m3}}{g_{m1}}+\gamma_9\frac{g_{m9}}{g_{m1}}\right)$	$\left(\gamma_1+\gamma_3\frac{g_{m3}}{g_{m1}}\right)$

is decreased (Figure 2.23). The disadvantages are the higher power dissipation and degraded speed properties compared to the cascode topologies, because the load capacitance affects the place of the non-dominant pole. Furthermore, separate CMFB circuits are needed for the first and the second stage.

The preceding opamp topologies are briefly compared in Table 2.2. The main properties were mentioned earlier, but worth mentioning further is the higher noise of the folded cascode OTA compared to the other topologies.

2.4.4 Clock Signal Generation and Switches

SC circuits require two nonoverlapping clock signals for the switch control. A simple method for the clock generation is shown in Figure 2.24. The nonoverlapping time can be increased by adding an even number of inverters to the paths of the loop. The last inverters outside the loop operate like buffers and can be designed to be larger than the other cells. Furthermore, they may be switched to the analog supply so as to isolate digital noise from the analog circuitry.

A slightly more complicated clock generator, depicted in Figure 2.25, has to be used when the bottom plate sampling technique is adopted. The clock signals for the bottom plate control (ϕ_{1b} and ϕ_{2b}) rise almost at the same time as the basic clock signals ϕ_1 and ϕ_2. However, inverters and an NOR gate are used to delay the falling edge of the bottom plate clock signals by a certain time (t_2) . The nonoverlapping time (t_1) consumes a larger relative part of the clock period when the sampling frequency increases. This wastes power and makes amplifier design harder, due to the narrow settling time. A solution is to utilize a delay locked loop based (DLL) clock generator, but then the circuit complexity increases [47].

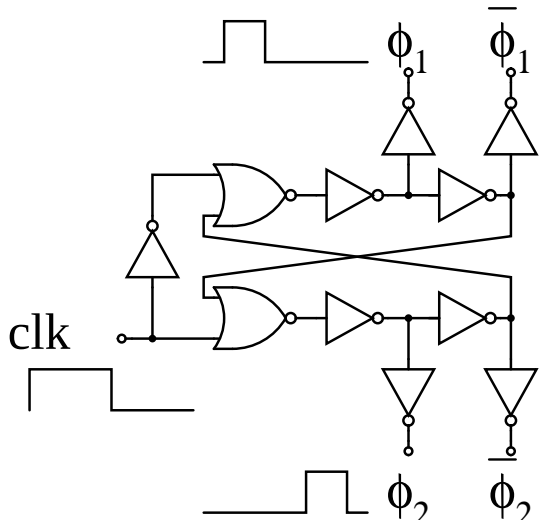


Figure 2.24 A basic nonoverlapping clock signal generator.

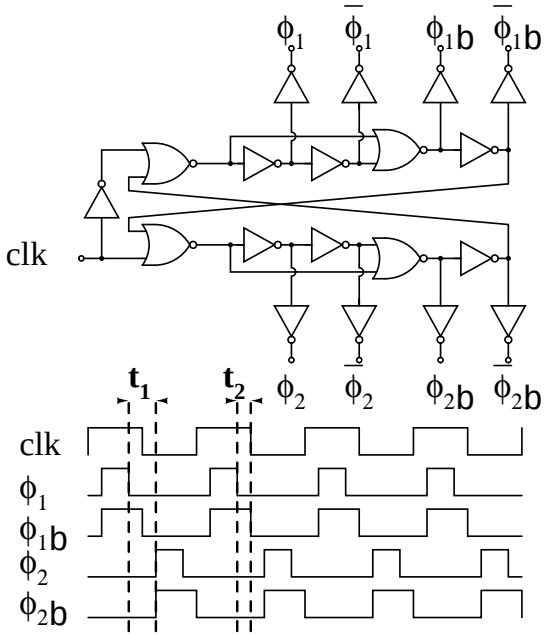


Figure 2.25 A clock signal generator for the bottom plate sampling.

The switches required in SC circuits are implemented using one transistor (usually a nMOS) or using a complementary switch with both nMOS and pMOS devices (CMOS switch). The on-resistance of a single transistor switch can be written as

$$R_{ON} \approx \frac{1}{\mu C_{ox} \frac{W}{L} (v_{gs} - V_T)}, \tag{2.34}$$

which is valid when $v_{gs} \geq V_T$. According to Equation (2.34) the on-resistance can be decreased by increasing W or gate-to-source voltage. Actually, an absolute on-resistance is not as important as the time constant of the RC loop formed by the channel resistance and the switched capacitors. To keep this value low enough the transistor width (W) can be increased. However, the drawbacks are increased parasitic capacitances, clock feedthrough, and a higher load on the clock buffers. The threshold voltage is determined by process parameters and it is not scaled down to the same extent as the supply. Therefore, there is a need to increase the v_{gs} voltage somehow so as to keep the on-resistance low enough. The operation range of the switch can extend over a range from a negative to positive supply when a CMOS switch is utilized. However, the minimum supply voltage is limited well above $2V_T$. Another problem is the nonlinearity of the channel resistance. When a continuous-time signal is sampled, this causes harmonic distortion. Furthermore, the charge injection can cause an error voltage at the sampling capacitor.

There are three different methods to decrease channel resistance when the W cannot be increased any more and the use of CMOS switches does not relax the situation. In some processes there are special transistors with lower threshold voltages. These can be used in switches to lower the on-resistance, but the complexity and costs of the process increase. The second way is to increase the transistor gate voltage by using a higher supply voltage for clock signals or boosting the gate voltage locally. If a high external supply voltage is not available [48], charge pumps [49] can be used to produce a high supply voltage for clock buffers or the gate voltage can be increased locally, using clock multipliers [50]. The method is best suited to circuits which are used below the nominal supply voltage of the process. If the nominal supply level is exceeded the reliability has to be considered, because of the mechanisms of device breakdown. The third way is to control the gate-to-source voltage rather than the gate voltage, using different bootstrap circuits. The gate voltage may exceed the supply voltage only marginally but keeps the v_{gs} constant if the supply is high enough to keep the time constant low, however, the nonlinearity of the switches is a problem. The bootstrap circuit can both increase the gate voltage over the supply voltage and keep the v_{gs} independent of the signal. However, the voltage differences between transistor

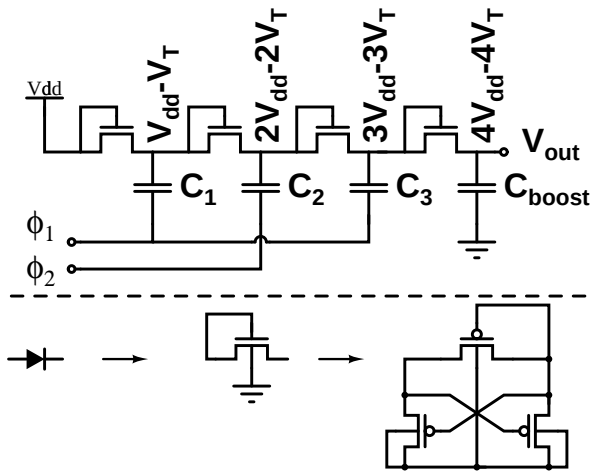


Figure 2.26 Dickson charge pump and a method to adjust the body voltage [49] [53].

terminals (like v_{gs}, v_{gd}, v_{ds}) are usually kept below the supply level in order to avoid reliability problems.

Alternative methods to allow the use of low supply voltages is to use a switched opamp [51] or an unity-gain-reset opamp technique [52]. These can be used to replace critical switches with opamps, but the input stage requires another solution, e.g. an RC circuit.

A Dickson charge pump, depicted in Figure 2.26, can be used to produce a high supply voltage for clock buffers and we ideally have

$$V_{out} = N \cdot (V_{dd} - V_T), \tag{2.35}$$

where N is the number of stages in the diode chain [49]. The threshold voltage of a diode-connected transistor increases due to a body effect, which decreases the achievable output voltage, or the efficiency decreases when the number of stages increases. The effect can be eliminated, for example by adjusting the body voltage, as shown in Figure 2.26, proposed in [53].

Dynamic clock multipliers can be used to locally boost a transmission gate or a set of gates (Figure 2.27). In the clock booster depicted in Figure 2.27a the capacitor C_1 is charged to $V_{dd} - V_T$ through the diode-connected transistor M_1 when the input clock signal is high [54]. When the clock signal is low the switch gate voltage is ideally boosted to $2V_{dd} - V_T$. A capacitance of the clock bus (c_{bus}) and a gate capacitance of

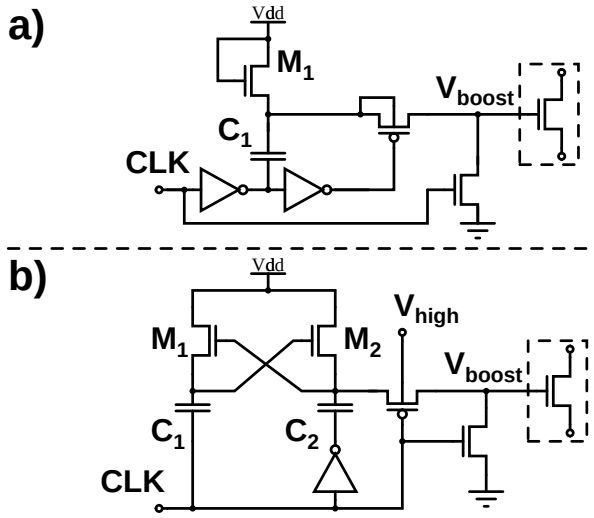


Figure 2.27 Dynamic clock voltage multipliers for a gate boosting [54] [55].

the switch (c_g) decrease the output voltage and we have

$$V_{boost} = \frac{C_1}{C_1 + c_{bus} + c_g}(2V_{dd} - V_T). \tag{2.36}$$

According to Equation (2.36) the C_1 has to be designed to be large enough to minimize the effect of the parasitic. In the circuit shown in Figure 2.27b the feedback technique is utilized to charge C_1 to V_{dd} instead of $V_{dd} - V_T$ [50] [55]. To prevent latch-up during the initial power-up transient the well bias (V_{high}) for the pMOS switch is generated using another charge pump [55]. Now we have

$$V_{boost} = \frac{C_2}{C_2 + c_{bus} + c_g} 2V_{dd}, \tag{2.37}$$

which can be considerably higher with a low supply voltage than in Equation (2.36).

The reliability of the switch transistor can be increased by using a constant voltage source between the gate and source of the switch transistor (Figure 2.28). Thus the gate voltage is ideally a sum of the sampled signal and the used bias voltage (V_O), but the gate-to-source voltage does not exceed the value of V_O, which is kept below V_{dd}. A basic circuit implementation is shown in Figure 2.28 [2]. During clock phase ϕ_2 the capacitor C_1 is charged to V_{dd} or $V_{dd} - V_T$ and during clock phase ϕ_1 C_1 is connected between the input port and the switch gate. If the gate voltage of the transistor M_4 is not boosted the charged bias voltage of C_1 is limited to $V_{dd} - V_T$ because the switch

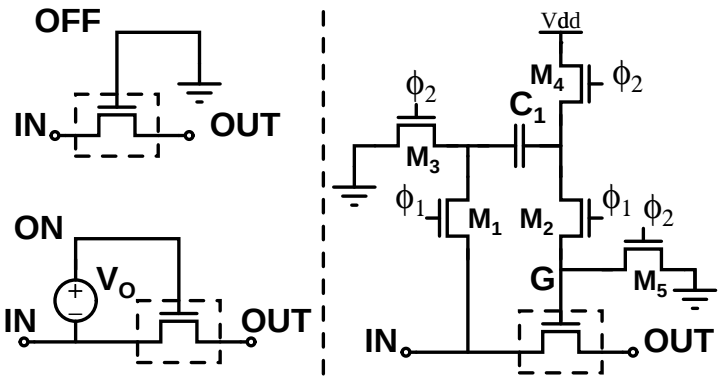


Figure 2.28 Principle of a bootstrapped switch and a basic circuit implementation [2].

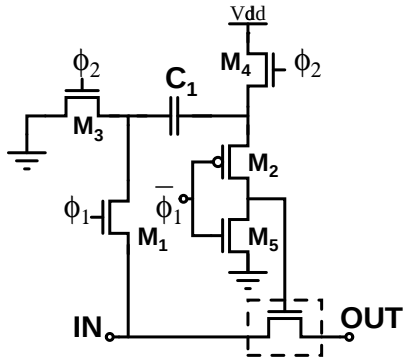


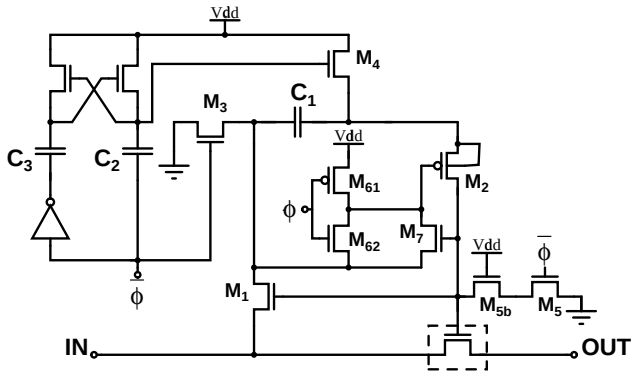
Figure 2.29 A bootstrapped switch [57].

turns off when its v_{gs} voltage is below V_T. Hence, the gate voltage (V_G) is a function of the input signal (V_{IN}) and can be approximated as

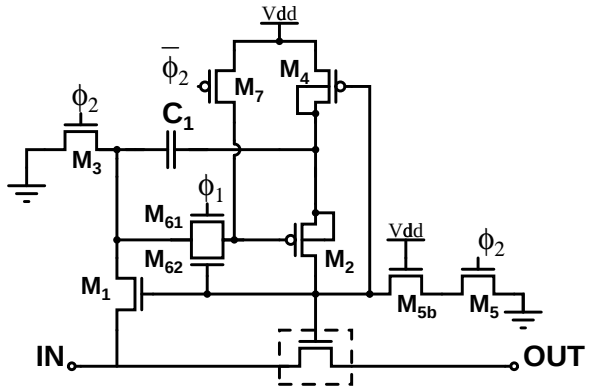
$$V_G \approx V_O + V_{IN}(t) = V_{dd} - V_T + V_{IN}(t). \tag{2.38}$$

The parasitic capacitors connected to node G should be minimized and the C_1 should be quite large because otherwise the parasitics can cause harmonic distortion because of their memory effect [47]. If the oversampling ratio between a sampling clock and an input signal frequency is high, the input signal may be charged to the capacitor C_1 in the previous clock phase and then, during the sampling phase, the C_1 is connected between V_{dd} and the gate [56].

Another implementation of the bootstrapped switch is shown in Figure 2.29 [57]. Transistors M_1-M_5 correspond to those used in Figure 2.28. Again, during clock phase ϕ_2 the capacitor C_1 is charged to $V_{dd} - V_T$ and during clock phase ϕ_1 C_1 is connected



(a)



(b)

Figure 2.30 Long time reliable bootstrapped switches [58] [59].

between the input port and the switch gate through transistors M_1 and M_2. Hence, the gate voltage of the switch follows the input signal according to Equation (2.38). The supply voltage used (V_{dd}) has to be sufficiently high, because the overdrive voltage of the switch is only $V_{dd} - V_T$. The circuit guarantees that the voltage difference between the terminals of the switch transistor does not exceed the V_{dd} but the V_{gs} of M_2 and the V_{ds} of M_5 will exceed the V_{dd} by the value of $V_{IN}(t) - V_T$. Hence, the input common mode level and the amplitude of the input signal should be low enough to ensure the reliability of the transistors.

In Figure 2.30 two-long time reliable bootstrapped switches are shown which are capable of sampling a rail-to-rail input signal with a switch overdrive voltage of V_{dd} [58] [59]. Again, the operation of the transistors M_1-M_5 is the same as in the circuits presented earlier, and the extra hardware is needed to improve reliability and to enable a rail-to-rail input signal. In the first circuit (Figure 2.30a) the C_1 is charged to V_{dd} by boosting the gate of M_4 by a dynamic clock multiplier. In the second circuit (Figure 2.30b) the same function is achieved using a pMOS switch (M_4), whose gate voltage in the off-state is controlled by the boosted voltage. In both the circuits the gate of M_1 is also controlled by the boosted voltage so as to ensure its conductivity with amplitudes of the input signal near V_{dd}. The transistor M_{5b} is needed to limit the v_{ds} and v_{gd} voltage of M_5 below V_{dd}. The transistors M_{61}, M_{62} and M_7 are used to control M_2 and to improve its reliability.

The on-resistance of transistor switches has a second-order dependence on the voltages between the bulk and the terminals of the transistor. This is emphasized with very low supply voltages and some bootstrapped switches to reduce the effect have been published [60] [61] [62]. Furthermore, the drain-to-source (v_{ds}) voltage has an effect on the on-resistance, especially when the size of the sampling capacitor increases and the switch on-resistance is large. A circuit in [63] uses an average voltage of drain and source terminals in the gate tracking to overcome the problem.

2.4.5 Internal ADC and DAC

An internal ADC of $\Delta\Sigma$ modulators is not a very critical circuit block in terms of noise and distortion because of the preceding loop gain. A flash ADC is a natural choice because the A/D conversion has to performed during one clock period. The area and power dissipation constraints limit the usable resolution to below 6 bits.

The internal DAC is a more critical circuit block for the achievable overall performance and a low-resolution DAC does not mean low accuracy. Feedback DACs can produce distortion (Section 2.2.3.1); they increase thermal noise (Equation (2.9))

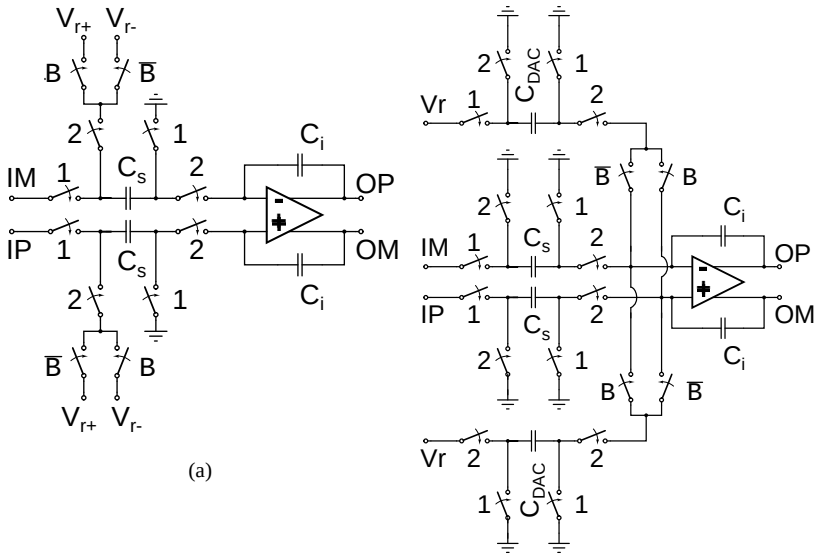


Figure 2.31 Two alternative SC DAC topologies.

and furthermore load the opamps. The output of the DAC is a product of the voltage references and digital output, which again is the sum of an A/D converted input signal and quantization noise. Hence, if either the analog input signal or digital output signal couple to reference voltage lines, the reference noise can fold to the desired signal band and increase second-order harmonic distortion [2]. Two alternative SC input stages of $\Delta\Sigma$ modulators including a feedback DAC are shown in Figure 2.31 [2]. The first topology (Figure 2.31a) shares a sampling and DAC feedback capacitor and therefore the DAC increases neither the thermal noise nor the capacitive load of the opamp. However, a positive and negative voltage reference is needed. The second topology (Figure 2.31b) utilizes separate DAC capacitors and hence the thermal noise and capacitive load of the opamp are larger than in the first topology. The main advantage is that only one reference voltage level is needed. Furthermore, the loading of references is signal-independent, unlike in the first topology, in which the charge loaded from the reference voltage source with a non-zero output impedance depends on the input signal and hence can cause a second-order harmonic distortion.

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Chapter 3

Bandpass ΔΣ Modulators in an IF Receiver

In a digital IF receiver the RF front-end amplifies and down-converts the signal to an IF, where it is first filtered to prevent aliasing and then A/D converted (Figures 3.1 and 3.2). A BP ΔΣ modulator performs a high-resolution A/D conversion of a high frequency narrow band signal, which makes it optimally suited for the purpose. The sampling operation in the BP ΔΣ modulator is often used for performing a second down-conversion. This has the effect of relaxing the BP ΔΣ modulator clock frequency, which otherwise has to be at least three to four times higher than the IF. After A/D conversion the signal is digitally down-converted to the baseband and demodulated.

The main motivation for performing the early A/D conversion is to shift more signal processing to digital circuitry, thus allowing greater flexibility. If the IF filtering is wide-band, the final channel selection is postponed to DSP, which makes the architec-

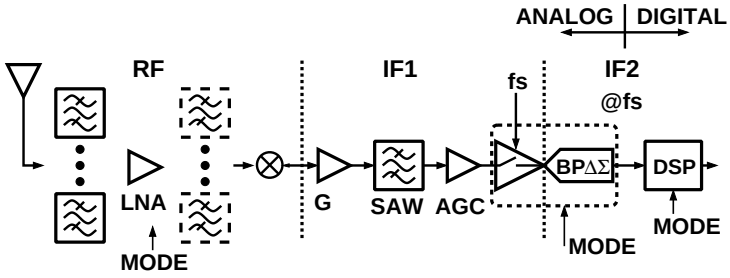

Figure 3.1 A multi-mode digital IF receiver.

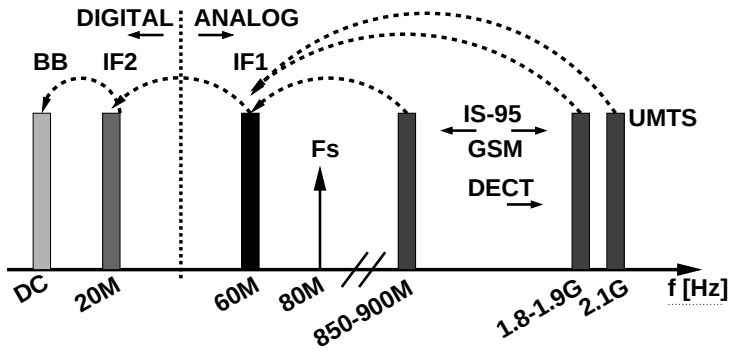

Figure 3.2 Principle of the frequency down-conversion in a multi-mode receiver.

ture suitable for multi-mode applications. A separate RF pre-select filter is required for each mode, but the LNA and mixer can be shared [1]. In a conventional super-heterodyne radio receiver an image filter is required after the LNA. However, if the down-conversion mixer is of the image reject type, this filter can be avoided, leaving mode-dependent filtering only to RF pre-select and DSP.

3.1 Specification

3.1.1 System Overview

The selection of IF frequencies is not straightforward. The choice of frequencies is a compromise between the RF filtering and front-end linearity requirements, the IF filtering requirements, the sampling clock jitter [2], and ADC clock frequency. If the first IF frequency is high, the requirements for the first passive image filter are relaxed but the sampling frequency of the BP $\Delta\Sigma$ modulator, as well as the clock jitter requirements, rapidly increase to an impractical level. The subsampling technique can be used at the input of the BP $\Delta\Sigma$ modulator to relax the clock frequency of the $\Delta\Sigma$ modulator. However, the subsampling ratio has to be low, because otherwise the implementation of the image/antialias filtering before the ADC ceases to be feasible. As a good compromise the first IF should be between 60-120MHz so as to enable the implementation of both the image filter and the ADC. The sampling frequency should be selected as an integer multiple of the highest chip rate included (WCDMA), and hence in the other possible operation modes fractional decimation with interpolation filters can be utilized. The sampling frequency should be around 80MHz, because the lower sampling frequency tightens the jitter requirements in narrow band applications (GSM) too much and the higher sampling frequency increases unnecessarily the power

dissipation of the BP ΔΣM.

The demodulation is performed in the digital domain by multiplying the output of the modulator by $exp(-j\omega_0 n)$, where ω_0 is the notch (IF_2) frequency. If a notch frequency of $f_s/4$ is selected, we have

$$\begin{aligned} exp(-j\omega_o n) &= cos(\omega_0 n) - jsin(\omega_0 n) \\ &= (+1,\ 0,\ -1,\ 0,\ ...) + (0,\ -1,\ 0,\ +1,\ ...) \end{aligned}, \tag{3.1}$$

where n=0, 1, 2, ... and the multiplication can be performed simply by inversion and the hardware complexity of the filters is reduced [3]. The filtering of the quantization noise and decimation are usually effectively carried out in two phases [3] [4].

3.1.2 BP ΔΣ Modulator

In a multi-mode digital IF receiver, the selectivity of the analog IF filter is determined by the widest bandwidth operating mode. As a limiting case, the filter can perform the full channel selection of the widest bandwidth mode, leaving the filtering in the narrower bandwidth modes to DSP. However, the filtering has an impact on the dynamic range requirements of the BP ΔΣ modulator. A full channel selection eliminates interfering signals from neighboring channels, leaving only the detection SNR requirement and some implementation margin for the automatic gain control and DSP to be covered by the BP ΔΣ modulator. In modes with a narrower bandwidth the interfering signals are, in absolute terms, closer to the IF, which diminishes the advantage resulting from the fixed IF filter.

The theoretical signal-to-quantization noise ratio (SQNR) of a 1b BP ΔΣ modulator is given by

$$SQNR \approx 10log_{10}\left(\frac{3}{2\pi^L}(1+L)\cdot OSR^{L+1}\right), \tag{3.2}$$

where L is the order of the loop filter. From Equation 3.2 we note that the SQNR of a BP ΔΣ modulator improves rapidly with an increasing OSR, which helps in meeting the higher dynamic range requirement with the same hardware. The interfering signals can be, for example, 40 to 70dB above the desired signal. From Equation 3.2 we find that obtaining an SQNR improvement in that range for $L = 4$ requires increasing the OSR by a factor of 4 to 5. Consequently, the SQNR improvement resulting from noise shaping is adequate only in modes where the signal bandwidth is significantly narrower than in the mode with the widest bandwidth. In intermediate cases either the order of the loop filter or the internal resolution has to be increased.

As an example, we may consider a multi-mode digital IF receiver supporting

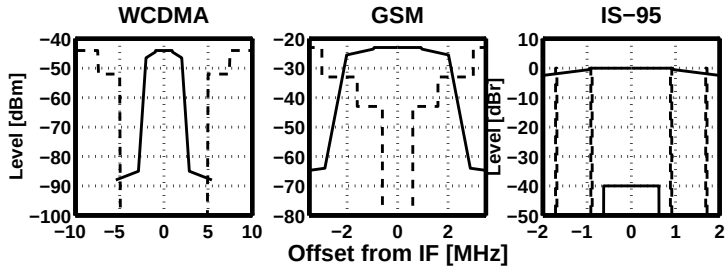

Figure 3.3 A model of the IF filter (SAW) magnitude response and blockers.

WCDMA (cdma2000), IS-95, and GSM a combination of 2G and 3G systems on two continents. From Figure 3.3 we can see that for WCDMA the IF filter effectively eliminates the interfering signals, leaving only the desired channel to be A/D converted [5]. For IS-95, the situation is somewhat different. The nearest interfering signals pass the IF filter unattenuated, remaining some 40 decibels higher than the desired signal, which leads to a correspondingly increased SNR requirement [6]. The ratio of the OSRs in IS-95 and WCDMA modes is only 3.2, which does not provide enough SQNR improvement in the case of a 4th-order loop filter. In GSM mode the worst-case interfering signal [7] is only marginally attenuated (Figure 3.3), but the SQNR improvement compared to WCDMA mode is around 57dB, which is more than adequate. The intermediate modes, which in this case are represented by IS-95, are clearly a problem in this architecture. Instead of designing the BP $\Delta\Sigma$ modulator for the most demanding case it can be made reconfigurable, thus minimizing the power consumption in each mode.

A 1b 4th-order BP $\Delta\Sigma$ modulator attenuates the quantization noise very effectively for large oversampling ratios. At a sampling rate of 80MHz the OSR for a GSM channel is 148, giving an SQNR of 97dB (Figure 3.4), which is sufficient to meet the GSM dynamic range requirements. Although a higher-order loop filter would shape the noise more, allowing a lower sampling rate, it would, in practice, only waste power, since the minimum sampling frequency is limited by the sampling jitter. Furthermore, a 4th-order loop filter is unconditionally stable, which is not the case for higher orders. The single-bit internal quantization leads to a very simple quantizer and to an inherently linear DAC implementation. Furthermore, the loading of amplifiers resulting from DACs and the quantizer is much lower than in multi-bit structures [8]. The capacitive loading is a problem, especially in narrow-band applications, where the thermal noise does not require large sampling capacitors.

Multi-mode applications, for example the IS-95 and DECT standards, require

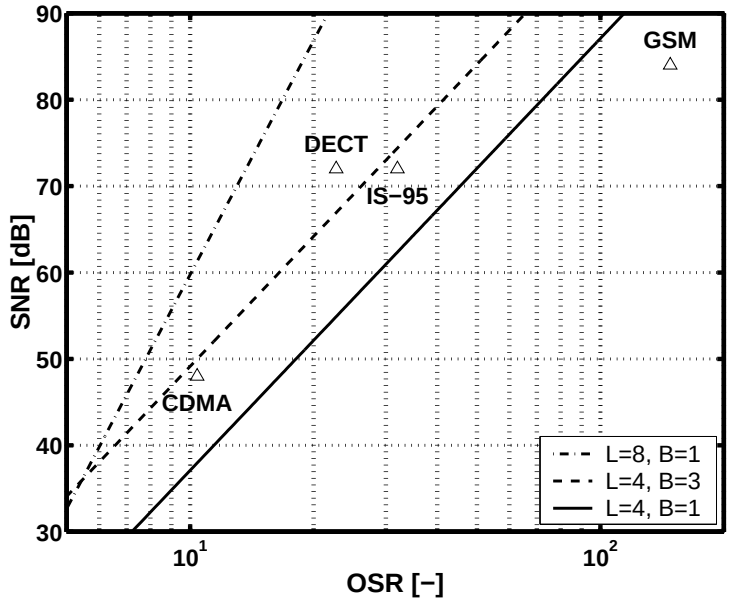

Figure 3.4 The theoretical SNR as a function of OSR (L=the order of BP ΔΣM and B=internal resolution [bit]).

more quantization noise shaping than a 1b 4th-order loop filter with an 80MHz sampling frequency (Figure 3.4). As discussed earlier, the OSR is not sufficiently increased and there is not much benefit from the anti-alias filter. Of course, a higher-order loop filter would improve the noise shaping, but it would require major modifications to the 4th-order BP ΔΣM. The same applies for a multi-bit feedback. It would require changes in the opamps as a result of increased loading, as well as different signal level scaling at the opamp outputs. An approach adopted in this book is to use the 4th-order BP ΔΣM as a module and to try to improve the noise shaping by cascading. This will allow the same input ΔΣM to be used in all modes, while turning on the cascade stages only when they are required.

3.2 Subsampling

A continuous-time signal has to be sampled when discrete-time analog signal processing is utilized. The sampling causes noise and unwanted signal aliasing over the desired signal band if the sampling frequency (f_s) violates the Nyquist criterion

$$f_s \geq 2 f_{BW}, \tag{3.3}$$

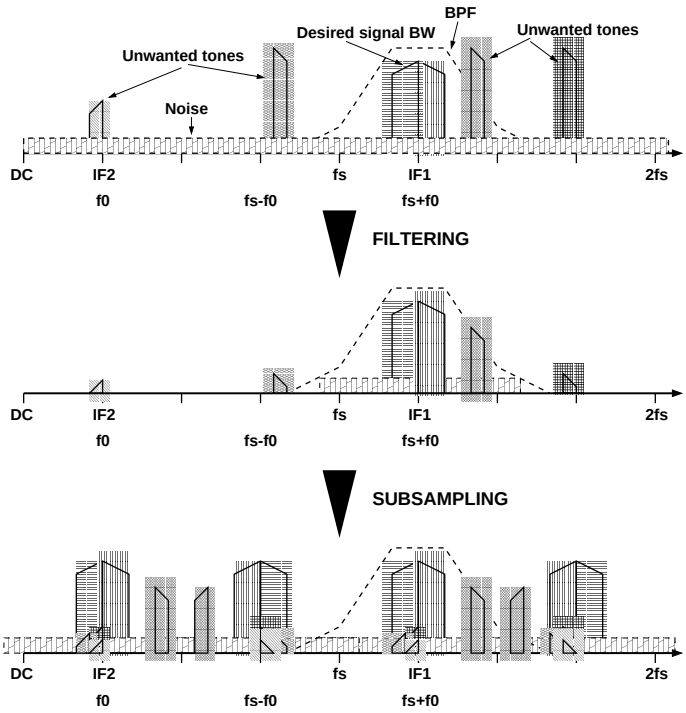

Figure 3.5 Subsampling and IF filtering.

where f_{BW} is the bandwidth of the sampled continuous-time signal. In an IF receiver [9] the RF signal is down-converted to the first intermediate frequency (IF_1) using an analog mixer. After that the BP $\Delta\Sigma$ modulator performs the signal digitization. The $IF_1$is usually in the range of 50-200MHz because the RF filtering before the down-conversion would be either impossible or too expensive if the lower IF_1 were used. If the whole frequency band from DC to IF_1 were digitized an f_s of 100-400MHz with LP filtering would be required, according to Equation (3.3). However, the required information is in a narrow signal band around IF_1 and, performing BP filtering before the sampling, the f_s can be lowered significantly, leading to a subsampling (Figure 3.5). This is desired because the power dissipation of the $\Delta\Sigma$ modulator is decreased and the implementation becomes, on the whole, feasible. In the subsampling the desired signal aliasing is utilized to down-convert the signal from IF_1 to IF_2. If LP $\Delta\Sigma$ modulators are used the IF_2=DC and IF_1 is a multiple of f_s [10], but in the case of BP $\Delta\Sigma$ modulators [11]

$$IF_2 = f_0 \; or \; IF_2 = f_s - f_0, \tag{3.4}$$

where f_0 is the resonance frequency of the BP ΔΣM loop filter and

$$IF_1 = nf_s \pm f_0,\ n = 1,2,3,\ldots. \tag{3.5}$$

The selection of f_0 (IF_2) affects the filtering requirements before the subsampling and therefore the f_0 should be high enough, as well as f_s, which is related to f_0 in the BP ΔΣM implementation. In a low-IF receiver the resonance frequency f_0 near DC is used by utilizing a complex BP ΔΣM architecture.

3.2.1 Noise

The MOS sampler produces thermal noise as a result of the finite on-resistance of the MOS switch (Figure 3.6). The noise is also known as kT/C noise, because we can write, for an RC circuit the mean square noise voltage as

$$n^2 = \int_0^\infty \frac{4kTR}{1+4\pi^2R^2C_s^2f^2}df = \frac{kT}{C_s}, \tag{3.6}$$

where k is the Boltzmann constant, T is the absolute temperature, R is the on-resistance of the MOS switch, and C_s is the sampling capacitor. Hence, the thermal noise power is only dependent on the size of the sampling capacitor as a result of an RC lowpass-shaped noise power. Because all noise aliases into the Nyquist band we can write the sampler noise power spectral density as

$$e_R^2 = \frac{kT}{C_s}\cdot\frac{1}{f_{Nyq}}. \tag{3.7}$$

When designing high-speed samplers we want to keep the time constant of the sampler as small as possible, but because of kT/C noise the size of the sampling capacitor is fixed by the noise specifications. Hence, the time constant can only be reduced by using larger MOS switches, which causes other problems because of the larger parasitics. To achieve a high dynamic range using low supply voltages requires large sampling capacitors, which easily leads to high power dissipation in analog circuits.

In Figure 3.6 the term e_{RF}^2 is the noise power spectral density of the RF input signal and e_L^2, e_M^2, and e_A^2 are the input-referred noise power spectral densities of each block. The corresponding gains of LNA, mixer, and AGC are G_L, G_M, and G_A. The equivalent noise bandwidth of the IF filter and that of the AGC are marked by BW_{BPF} and BW_{AGC}, respectively. Now we can write the receiver input referred equivalent

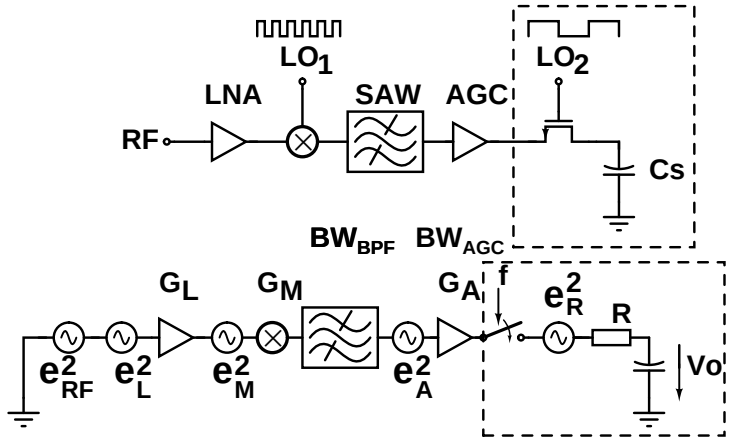

Figure 3.6 The front-end of the IF sampling receiver and an equivalent noise model.

noise power spectral density as

$$e_{eq}^2 = \frac{BW_{BPF}}{f_{Nyq}}\left(e_{RF}^2 + e_L^2 + \frac{e_M^2}{G_L^2}\right) + \frac{BW_{AGC}}{f_{Nyq}}\frac{e_A^2}{(G_L G_M)^2} + \frac{e_R^2}{(G_L G_M G_A)^2} \tag{3.8}$$

and the total in-band noise power referred to the receiver input as

$$n_{BW}^2 = \frac{BW_{BPF}}{OSR}\left(e_{RF}^2 + e_L^2 + \frac{e_M^2}{G_L^2}\right) + \frac{BW_{AGC}}{OSR}\frac{e_A^2}{(G_L G_M)^2} + \frac{1}{OSR}\frac{kT/C}{(G_L G_M G_A)^2}. \tag{3.9}$$

It can be seen that by increasing the sampling frequency or the OSR the effect of the noise sources can be reduced. The noise power spectral density of the AGC and its equivalent noise bandwidth have a great impact on the total noise budget, because the noise is not filtered and hence it aliases over the desired frequency band as a result of the sampling. It is clear that to prevent noise aliasing the bandwidth of the BPF has to be below the sampler Nyquist frequency. The narrower BW_{BPF} of the passive IF filter (SAW) is used more the noise of the preceding blocks has been decreased. The narrow IF filter also decreases the dynamic range requirements of the ADC and relaxes the channel filtering caused by attenuated blocker levels. The clock jitter requirements of the sampling clock are also reduced, as will be shown in the next section. The MOS sampler has a much higher noise figure than a conventional analog mixer but in the IF sampling receiver the noise can be effectively reduced by the preceding gain, according to Equations (3.8) and (3.9).

3.2.2 Clock Jitter

The timing uncertainty in the sampling clock causes an amplitude error in the discrete-time signal, as shown in Figure 3.7 [2] [12]. If a sampled sinusoidal signal without clock jitter is

$$x(nT) = Asin(2\pi f_{sig} nT + \phi) \tag{3.10}$$

then the sampled signal with clock jitter (t_j) is

$$x_j(nT) = Asin(2\pi f_{sig}(nT + t_j) + \phi), \tag{3.11}$$

where A, ϕ and f_{sig} are the signal amplitude, phase, and frequency, respectively. The amplitude error is

$$\varepsilon_A = x(nT) - x_j(nT) \approx t_j 2\pi f_{sig} A cos(2\pi f_{sig} nT + \phi). \tag{3.12}$$

Hence, the magnitude of error is dependent on the phase difference between the sampling clock and the signal. The maximum error

$$\varepsilon_{Amax} = t_j 2\pi f_{sig} A \tag{3.13}$$

occurs if the sinusoidal signal is sampled at the zero crossing points, where the derivative of the signal achieves its maximum value.

The timing error (t_j) can be assumed to be normally distributed with a standard deviation of σ_j. Then the standard deviation of the error of the sampled voltage (rms value) is

$$\sigma_x = \sigma_j \sqrt{\frac{1}{T}\int_0^T \left(\frac{dx(t)}{dt}\right)^2 dt}, \tag{3.14}$$

where T is the signal period and for a sinusoidal signal

$$\sigma_x = \frac{A}{\sqrt{2}} 2\pi f_{sig} \sigma_j. \tag{3.15}$$

Assuming a white jitter noise and that it is evenly spread over the frequency band, we obtain the maximum available signal-to-noise ratio (SNR_{max}) resulting from the clock jitter as

$$SNR_{max} = 10log_{10}\left(\frac{\left(\frac{1}{\sqrt{2}}A\right)^2}{\int_{f_1}^{f_2}\left(\frac{A}{\sqrt{2}}2\pi f_{sig}\sigma_j\right)^2 \frac{2}{f_s} df}\right), \tag{3.16}$$

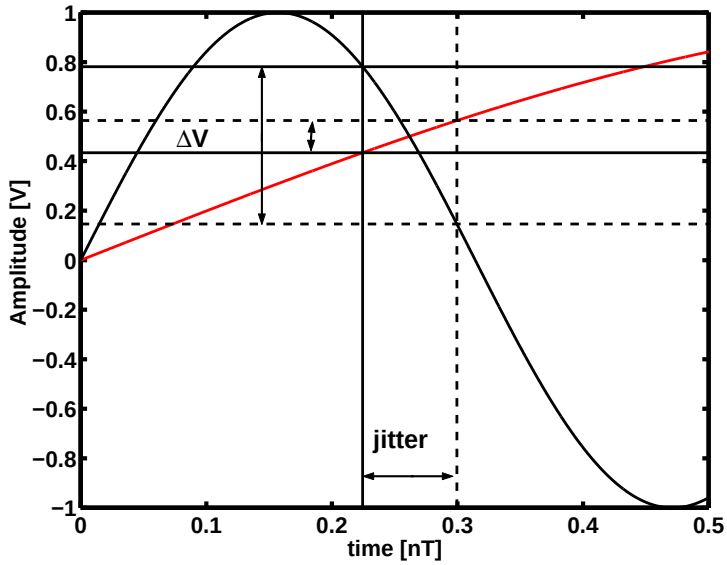

Figure 3.7 An amplitude error in the signal sampling due to the clock jitter T=1/f_s ($f_{sig} = f_s/4$ or $f_{sig} = 5f_s/4$).

where $f_2 - f_1$ is the band of interest. The oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{2(f_2 - f_1)} \tag{3.17}$$

and we obtain

$$SNR_{max} = 10log_{10}\left(\frac{OSR}{\sigma_j^2 4\pi^2 f_{sig}^2}\right). \tag{3.18}$$

We can see that the only way to relax the jitter requirements is to increase the OSR with a fixed input signal frequency.

In radio receivers the sampled signal consists of the desired signal and nearby blocker signals. The blockers increase the dynamic range requirements of the receiver and tighten the jitter requirements. If the blocker signals are assumed to be sinusoidal Equation 3.18 may be rewritten as

$$SNR_{max} = 10log_{10}\left(\frac{OSR}{\sigma_j^2 4\pi^2\left(f_{sig}^2 + \Sigma_i\left(\frac{A_{bi}}{A_{sig}} f_{bi}\right)^2\right)}\right), \tag{3.19}$$

where A_{bi} and f_{bi} are the amplitude and frequency of the i:th blocker.

In the previous equations, the white noise assumption was made for the clock jitter. If the phase noise of the sampling clock dominates the noise floor, we have [13]

$$SNR_{max} = \left(\frac{f_s}{f_{sig}}\right)^2 \cdot SNR_{clk}, \tag{3.20}$$

where SNR_{clk} is the signal-to-noise ratio of the sampling clock signal. Hence, in this case the SNR can be improved only by decreasing the subsampling ratio. However, in the IF subsampling the clock jitter noise is dominated by the flat noise floor of the oscillator and by the noise generated in clock buffers as a result of the low phase noise. This is because the phase noise is directly proportional to the square of the clock frequency and inversely proportional to the square of the oscillator Q-value, which is large at frequencies of the order of 100MHz [13] [14]. Therefore, the assumption of the white jitter noise is valid here.

If we have a 100MHz IF sampling receiver and an OSR of 150 we can plot the maximum achievable SNR as a function of the clock jitter according to Equation (3.18) by assuming that the jitter noise of the desired signal dominates (Figure 3.8). This is valid with large input signals and we can see that if, for example, an SNR of 84dB is targeted the jitter should be below 1.2ps. If we have a small desired signal and large blockers the jitter caused by the blockers starts to dominate the SNR (Equation (3.19)). The blocker levels in the GSM specifications can be 56dB above a signal level offset 0.6-1.4MHz, 65dB above a signal level offset 1.6-2.8MHz, and 75dB above a signal level offset over 3.0MHz from the desired channel (Figure 3.3) [7]. If we model these blockers with sinusoidal signals with 200kHz spacing and assume that an IF filter attenuates blockers offset over 4MHz from the desired channel to an insignificant level, we can plot the worst-case SNR as a function of the clock jitter (Figure 3.9). An SNR of 10dB can be kept as a minimum requirement so as to get some margin for the signal detection and other noise sources. We notice that the blocker specifications set much more stringent requirements for the clock jitter than the jitter noise of the desired signal. If the IF filter attenuates the blockers between 3-4MHz by at least 5dB, a clock jitter below 0.48ps is required, which is a very stringent requirement. It is clear that the clock jitter is the most serious problem in the implementation of IF receivers.

3.3 BP Decimation Sampler

In the IF sampling receiver a subsampling is utilized to lower the operation frequency of the ADC and, at the same time, to make possible a fairly high IF_1 frequency. How-

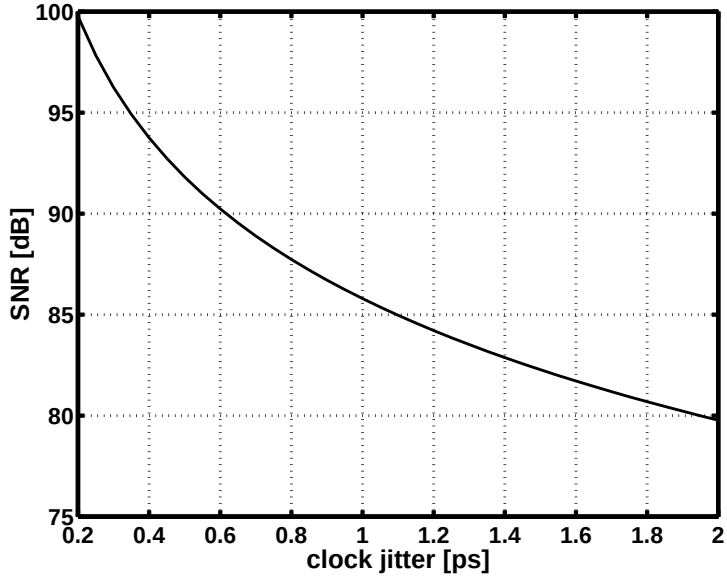

Figure 3.8 The maximum SNR as a function of the clock jitter (OSR=150 and IF=f_{sig}=100MHz).

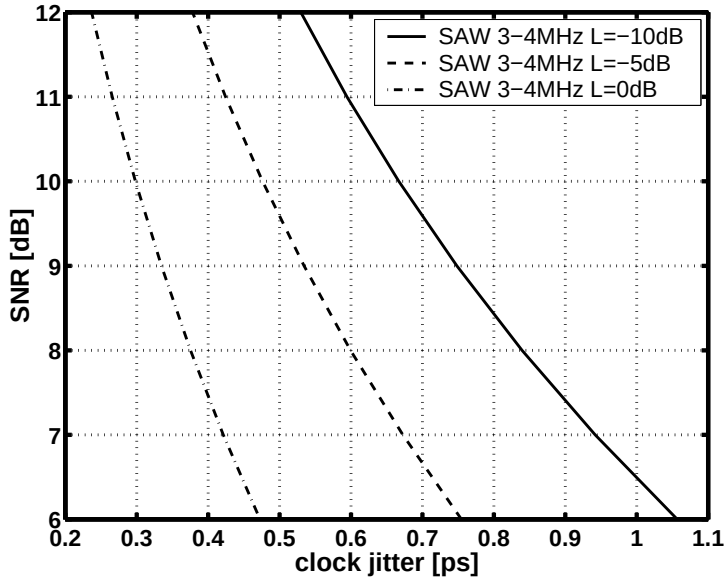

Figure 3.9 Clock jitter requirements in IF sampling receiver with a minimum desired signal, OSR=150, and IF=100MHz using GSM blocker specifications.

ever, quite a high sampling frequency is still required to relax the IF filtering requirements before subsampling and, furthermore, to enable the sufficiently high OSR required as a result of the clock jitter noise. This can lead to an unnecessarily high ADC operating frequency when the quantization noise vs. power dissipation is optimized. Therefore, there is a need to decrease the ADC operating frequency without tightening the IF filtering and clock jitter specifications. This is made possible by the subsampling mixer, which prevents noise aliasing when the sampling frequency is decreased [15] [16]. The LP decimation principle [15], which performs RF/IF_1 to DC mixing, can be modified to BP decimation or RF/IF_1 to IF_2 mixing [17].

3.3.1 Theory

In the analog LP decimator N samples are taken to N hold capacitors and then they are connected in parallel and buffered out at the frequency of f_s/N, in which N is the decimating factor (Figure 3.10). A minimum of $3N/2$ samplers are needed because new samples are taken when the others are buffered out. The decimator transfer function in the z-domain is

$$H(z) = 1 + z^{-1} + \ldots + z^{-(N-1)}, \tag{3.21}$$

which is an FIR with N-taps. The transmission zeros of the FIR prevent noise aliasing to DC in the decimation (Figure 3.11). In the LP decimation the (N-1) zeros are placed in the frequency (z-plane) plane with the spacing

$$\Delta f_{zeros}^{N-1} = \frac{2 f_{Nyq}}{N} \tag{3.22}$$

starting at $2f_{Nyq}/N$, where f_{Nyq} is the sampler Nyquist frequency before the decimation. Of course, the new Nyquist frequency has to be high enough compared to the desired signal band near DC.

In the BP decimator the desired signal from IF_1 has to be subsampled to the IF_2 frequency. Let us consider a case where the notch frequency (f_0) of $f_{Nyq}/(2N)$ or a so-called $f_s/4$ resonator is selected. To prevent noise aliasing over the desired signal the 2(N-1) zeros should be placed in the frequency (z-plane) plane with the spacing

$$\Delta f_{zeros}^{2(N-1)} = \frac{f_{Nyq}}{N} \tag{3.23}$$

starting at $3f_{Nyq}/(2N)$. The requirement of 2(N-1) zeros leads to a more complicated FIR filter than in the LP decimator. Some samples have to be taken to memory and not all the FIR coefficients are equal to one, or sampling capacitors of different sizes

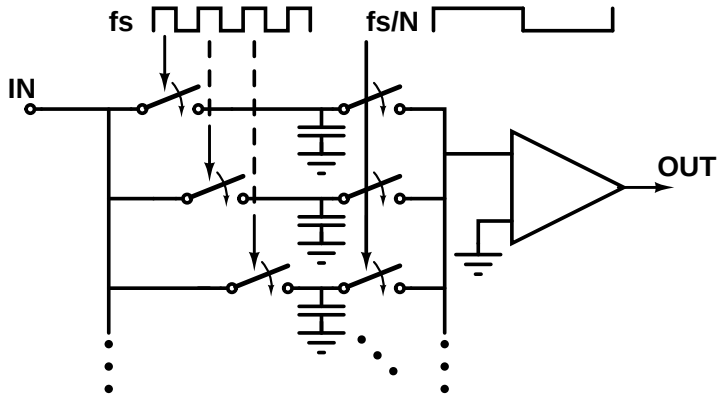

Figure 3.10 Principle of the analog decimator [15].

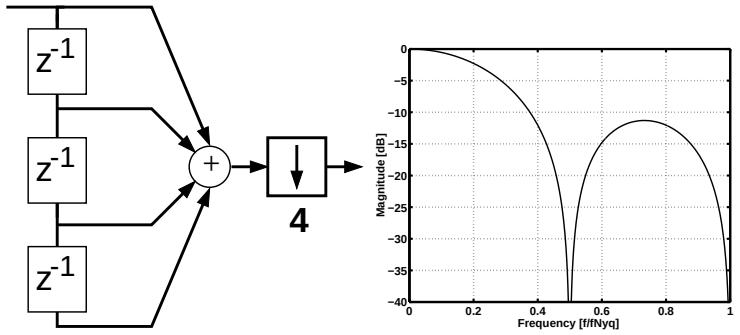

Figure 3.11 Block diagram and frequency domain presentation of the LP decimator N=4 [15].

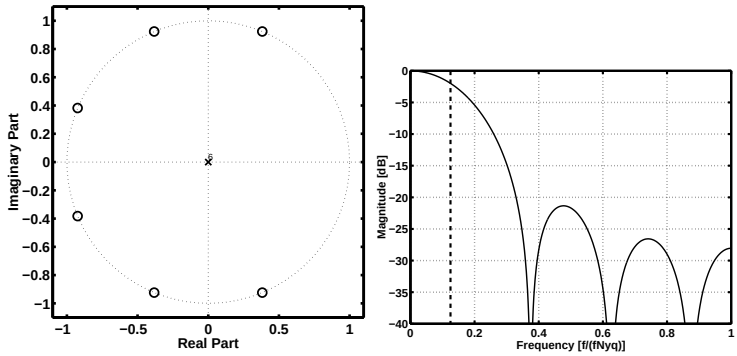

Figure 3.12 Z-plane and frequency domain presentation of the BP decimator N=4 (dashed line=IF_2).

are needed. For example, decimation by 4 (Figure 3.12) demands a FIR filter given by

$$H(z) = 1 + 1.85z^{-1} + 2.41z^{-2} + 2.61z^{-3} + 2.41z^{-4} + 1.85z^{-5} + z^{-6}. \qquad (3.24)$$

Hence, three samples have to be saved for the next summation and unit capacitors of four different sizes are required. We can see that the full cancellation of the aliasing noise by the zero placement leads to too-complicated an equation when N increases. Decimation by two is still quite simple and feasible (Figures 3.13 and 3.14). Only one sample has to be saved for the next summation and capacitors of two different sizes have to be used. If a decimation factor higher than two is realized the noise aliasing requirements should be analyzed separately in each case in order to find a less aggressive FIR filter for the purpose.

The magnitude response of the FIR is not exactly flat over the signal band around IF_2 and furthermore causes a slight attenuation, which, in the case of N=2, is -1.65 dB at the IF_2 frequency. If the desired signal band is wide there may be a need to correct the gain variation over the signal band by a digital post filter after digitization.

3.3.2 Noise

In a decimation sampler the kT/C noise consists of the noise of M-sampling capacitors buffered to the output at the same time. The noise between unit samplers (C_u) is not

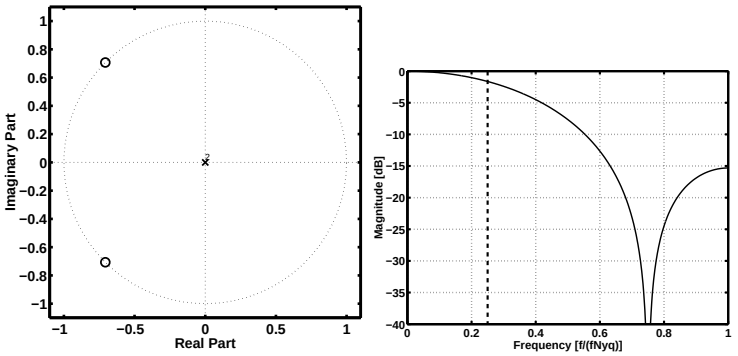

Figure 3.13 Z-plane and frequency domain presentation of the BP decimator N=2 (dashed line=IF_2).

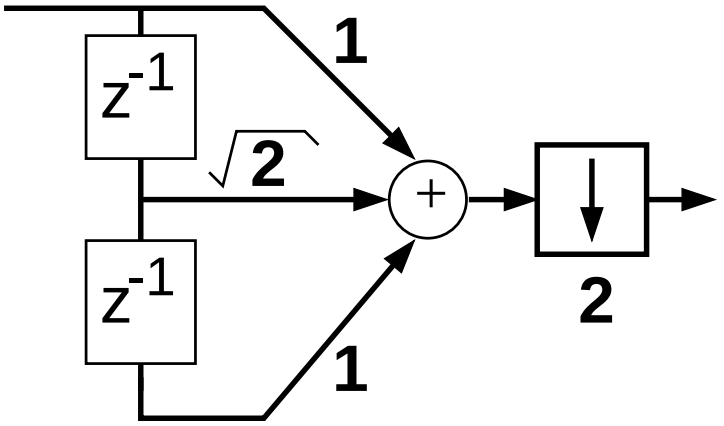

Figure 3.14 Block diagram of the BP decimator N=2.

correlated and we obtain

$$n_{tot}^2 = \frac{Q_{noise}^2}{C_{tot}^2} = \frac{\sum_{m=1}^{M}\left(C_{um}^2 \frac{kT}{C_{um}}\right)}{\left(\sum_{m=1}^{M} C_{um}\right)^2} = \frac{kT}{\sum_{m=1}^{M} C_{um}}. \tag{3.25}$$

Hence, the size of the unit samplers can be selected so that the sum of the capacitances is equal to the size of one large capacitor, which would be used in a normal sampling to one capacitor by the frequency of f_s/N. Therefore the power dissipation is almost the same as it would be in a normal circuit structure operating with a sampling frequency of f_s/N. The power dissipation can increase a little as a result of the more complicated clocking generator but, on the other hand, the unit clock buffers can be smaller than would be needed to drive a wide switch of one large sampling capacitor.

Because a BP decimation sampler attenuates the signal ($\sim$1-2dB), this will decrease the SNR with a fixed input level. To achieve the same SNR as would be achieved without decimation a slightly higher input level has to be used, which tightens the linearity requirements of the input sampler.

3.3.3 Clock Jitter

The clock jitter noise sets the maximum available SNR in a BP decimation sampler, as well as in conventional samplers. In the jitter study the jitter noise has to be separated into two parts; one is the jitter noise in the full-speed clock before clock division to separate sampling paths and the second is the jitter noise generated in each sampling path after the clock division. The jitter noise model in the first case is shown in Figure 3.15a. The samples are taken by the full sampling frequency and the jitter noise is filtered by the ideal FIR filter and decimated, like the other noise sources. Hence, the zeros of the FIR filter cancel the aliasing part of the jitter noise and, as a result of the narrower Nyquist frequency, we obtain Equation (3.18) to form

$$SNR_{max} = 10log_{10}\left(N\frac{OSR}{\sigma_j^2 4\pi^2 f_{sig}^2}\right). \tag{3.26}$$

Hence, when the BP decimation sampler is used to increase the sampling frequency, the jitter noise of the main clock is reduced and the reduction is directly proportional to the decimation factor (N). Now, if the jitter noise increases in separate clock paths after the clock division, the jitter noise of the separate paths has to be summed and multiplied by the FIR coefficients (c_m). This jitter noise is not filtered and the noise model is shown in Figure 3.15b. Assuming the same jitter standard deviation of σ_{jm}

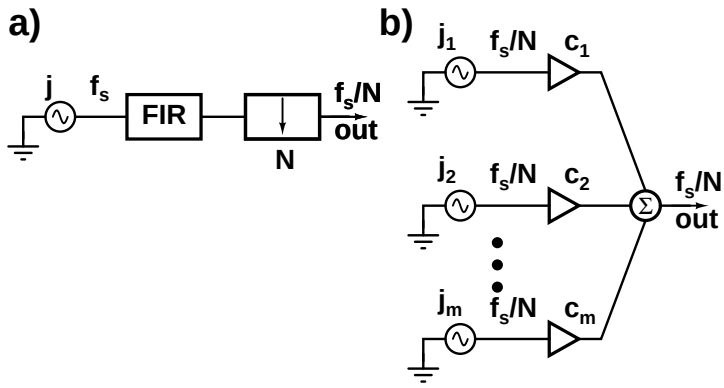

Figure 3.15 Clock jitter noise model: a) jitter before clock division and b) separate clock jitter for each sampler.

in each sampling path, we may write

$$SNR_{max} = 10log_{10}\left(\frac{OSR}{\sigma_{jm}^2 4\pi^2 f_{sig}^2 \frac{1}{M}\sum_{m=1}^{M} c_m^2}\right). \tag{3.27}$$

We notice that this jitter noise is not reduced as a function of the decimation factor N. However, it is possible to design the clock generator so that the σ_{jm} is determined by the noise contribution of one transistor, which is driven by a rail-to-rail signal, and therefore the noise is insignificant. Hence, using the BP decimation sampler the jitter specifications are unchanged if the operating frequency of the ADC or OSR is decreased.

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Chapter 4

Resonators

In the realization of BP ΔΣ modulators the integrators of LP ΔΣ modulators are replaced with resonators. A high-performance resonator is more difficult to implement than a high-quality integrator. Therefore, poor resonator structures usually limit the performance of the whole BP ΔΣ modulator.

In this chapter, a resonator is at first studied in the z-domain. After that, different discrete-time (DT) resonator topologies are discussed. The double-delay (DD) topology is found to have the highest potential for a high-quality resonator and the published switched-capacitor (SC) implementations of the DD resonator are briefly introduced. Next, the different versions of the designed SC resonator are presented and the designed SC resonator is compared to earlier published structures. Finally, nonidealities are analyzed.

4.1 Resonator in z-domain

In resonators the figures of merit are the Q-value and accuracy of the resonance frequency. In the z-domain a resonator ideally has two poles on the unit circle, but because of different nonidealities the location of the poles on the circle changes and the radius (r) differs from its ideal value of one (Figure 4.1); the complex pole pair can be written as

$$z_{p1,2} = r(\cos(\phi) \pm j\sin(\phi)) = re^{\pm j\phi}, \tag{4.1}$$

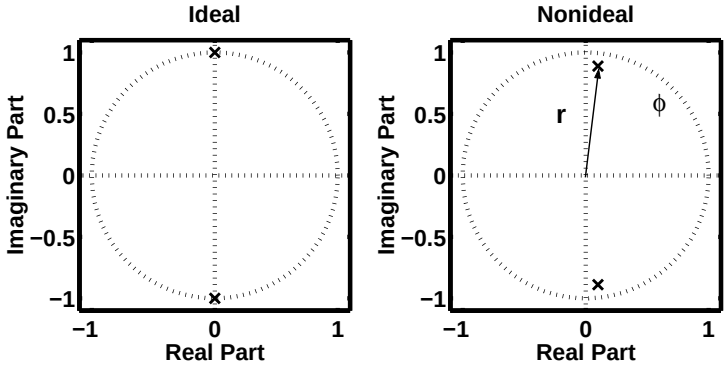

Figure 4.1 Pole location in a $\pi/2$ resonator.

where $\phi = 2\pi f_0/f_s$ is the resonance frequency in radians. The transfer function of the resonator is

$$H_{res}(z) = \frac{1}{(z-z_{p1})(z-z_{p2})} = \frac{z^{-2}}{1-2r\cos(\phi)z^{-1}+r^2z^{-2}}. \tag{4.2}$$

If the gain of the resonator is g_0, we can write the transfer function as follows:

$$H_{res}(z) = \frac{g_0 z^{-2}}{1-p_1z^{-1}+p_2z^{-2}}. \tag{4.3}$$

By comparison with Equation (4.2), we have the relationships

$$\begin{cases} r = \sqrt{p_2} \\ \phi = \arccos\left(\frac{p_1}{2\sqrt{p_2}}\right) \end{cases}. \tag{4.4}$$

There is particular interest in resonators with a resonance frequency of $f_s/4 = \pi/2$, because this relaxes the design of the high-frequency digital part in radio receivers [1]. Then the term p_1 is ideally zero and p_2 should be one, so as to guarantee the maximum Q-value, which is ideally infinite, or the pole lies on the $j\omega$-axis in the s-domain.

For the $f_s/4$-resonator the relative frequency error is

$$\begin{array}{c} \frac{\Delta f}{f_0} = \frac{|\pi/2-\phi|}{\pi/2} = \left|1-\frac{2}{\pi}\arccos\left(\frac{p_1}{2\sqrt{p_2}}\right)\right| \\ \Rightarrow \frac{\Delta f}{f_0} \approx \left|\frac{p_1}{\pi}\right| \end{array}. \tag{4.5}$$

We note that the possible frequency error is caused by the p_1 term (near zero) and the effect of the error in the p_2 term (near one) is negligible.

When we have the pole $s_p = \sigma_p + j\omega_p$ in the s-domain, the Q-value is determined

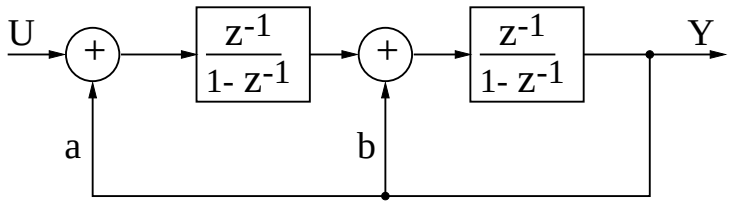

Figure 4.2 Forward Euler resonator.

by

$$Q_s = \frac{\sqrt{\sigma_p^2 + \omega_p^2}}{2\,|\sigma_p|}. \tag{4.6}$$

The s_p mapped to the z-domain is

$$z_{sp} = e^{(\sigma_p + j\omega_p)T} = e^{\sigma_p T} e^{j\omega_p T} = re^{j\phi} \tag{4.7}$$

and we get the relationships

$$\Rightarrow \begin{cases} \omega_p = \phi/T \\ \sigma_p = \ln(r)/T \end{cases}. \tag{4.8}$$

Now the Q-value can be written in the z-domain as

$$Q_z = \frac{\sqrt{(\ln(r))^2 + \phi^2}}{2\,|\ln(r)|} \tag{4.9}$$

and using the terms p_1 and p_2

$$\begin{aligned} Q_z &= \frac{\sqrt{(\ln(\sqrt{p_2}))^2 + \left(\arccos\left(\frac{p_1}{2\sqrt{p_2}}\right)\right)^2}}{2\left|\ln(\sqrt{p_2})\right|} \\ &\Rightarrow Q_z \approx \frac{\pi}{4\left(1-\sqrt{p_2}\right)} \end{aligned}. \tag{4.10}$$

Hence, the Q-value is mainly determined by the term p_2 (near one) and the error in p_1 (near zero) has a negligible effect on the magnitude of Q.

4.2 Discrete-Time Resonator Topologies

A discrete-time resonator can be implemented with different structures [2], such as Forward Euler (FE), lossless discrete integrator (LDI), or double-delay (DD). The FE resonator (Figure 4.2) consists of two identical integrators with the feedback terms a

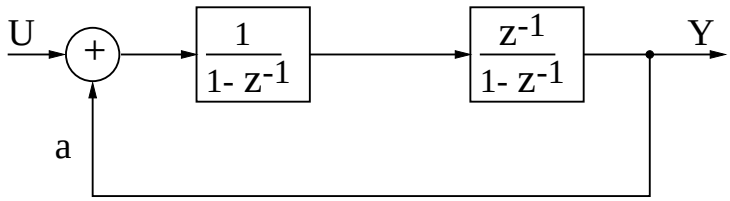

Figure 4.3 Lossless Discrete Integrator(LDI).

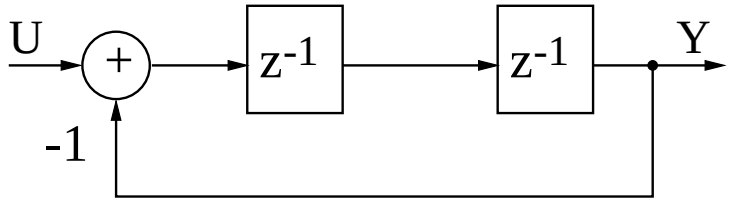

Figure 4.4 Double Delay resonator(DD).

and b. In SC implementations of resonators capacitor mismatch is one of error sources. For the sake of simplicity we assume the same gain error resulting from capacitor mismatch (ε_c) for the signal path and feedback. This simple study gives an adequate view of the sensitivity of topologies to capacitor mismatches, but ultimately the nonidealities have to be analyzed with a specific SC structure. The transfer function of the FE resonator is

$$H_{FE}(z) = \frac{(1+\varepsilon_c)^2 z^{-2} U(z)}{1-(2+b(1+\varepsilon_c))z^{-1}+(1-a(1+\varepsilon_c)^2+b(1+\varepsilon_c))z^{-2}}. \tag{4.11}$$

The notch place can be moved by the parameter a. If we select a=b=-2 the notch is fixed ideally at $f_s/4$. We notice that both the notch frequency and the notch depth (Q-value) are dependent on the gain error. Therefore this structure is not favored.

The LDI resonator (Figure 4.3) also consists of two integrators, but one is delay-free and the loop has only one feedback coefficient a. The transfer function can be found to be

$$H_{LDI}(z) = \frac{(1+\varepsilon_c)^2 z^{-1} U(z)}{1-(2+(1+\varepsilon_c)^2 a)z^{-1}+z^{-2}}. \tag{4.12}$$

Now the notch frequency can be changed by the parameter a and with a=-2 it is ideally fixed at $f_s/4$. Here we note that the poles remain on the unit circle, and hence notch is maximally deep, yet its place is dependent on the integrator gain errors. In this sense it could be regarded as better than FE, but the gain error affects the notch frequency more than in FE and the inaccurate resonance frequency decreases the performance.

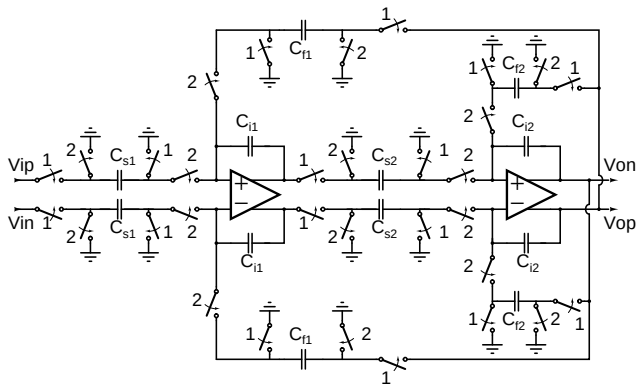

Figure 4.5 An SC implementation of the FE resonator in Figure 4.2.

The DD resonator (Figure 4.4) consists of two delay elements in series, with a feedback term of one. The feedback loop can be implemented without a gain error using pseudo-two-path SC structures [3] [4] [5] and we have

$$H_{DD}(z) = \frac{(1+\varepsilon_c)z^{-2}U(z)}{1+z^{-2}}. \tag{4.13}$$

Now the notch frequency is directly fixed at $f_s/4$ and therefore other choices cannot be made. We see that the notch frequency is guaranteed and the notch is maximally deep (high Q), regardless of the capacitor mismatch. Consequently, the DD resonator has the highest potential for the realization of high-performance BP $\Delta\Sigma$ modulators and should be used if the center frequency of $f_s/4$ is suitable. However, the finite DC gain and GBW of the amplifier affect the transfer function and have to be considered separately. The different DD resonator implementations are studied in Section 4.4.

4.3 SC Implementation of the FE or LDI Topology

The FE and LDI topology offer the possibility of changing or programming the resonance frequency, unlike the DD resonator. However, in the last section their performance was found to be sensitive to capacitor mismatch, and this is further studied using SC macromodels in the ELDO simulation program. An SC implementation of the FE resonator is depicted in Figure 4.5. The ideal amplitude responses of the structure using resonance frequencies of $\pi/3$ and $3\pi/4$ are shown in Figure 4.6a. We can see that the center frequency can be freely selected by changing the sizes of the feedback capacitors (C_{f1}, C_{f2}) or coefficients a and b in Figure 4.2. Next, an ideal

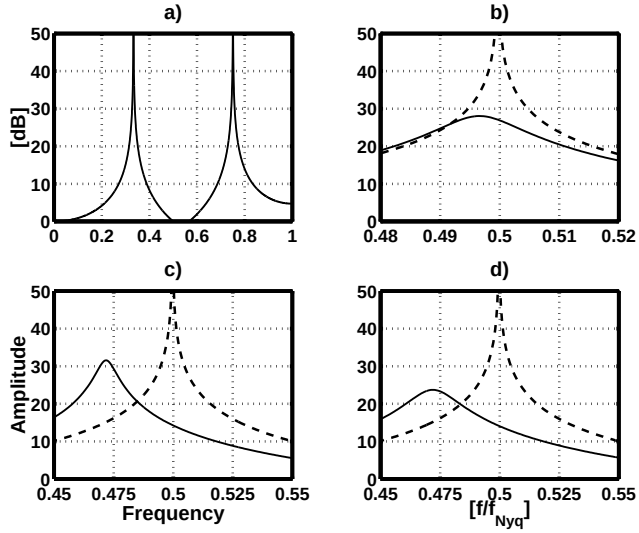

Figure 4.6 Simulations of the FE SC resonator (Figure 4.5; C_{s1}=C_{s2}=C_{i1}=C_{i2}=0.5pF). a) Ideal $\pi/3$ resonator (C_f=0.5pF) and ideal $3\pi/4$ resonator (C_f=1.71pF), b) $\pi/2$ resonator with a capacitor mismatch of 1.0% (C_{f1}=1.01pF, C_{f2}=0.99pF), c) with a finite DC gain of 40dB and an input parasitic capacitance of 0.2pF and d) additionally, a capacitor mismatch of 2.0% (C_{f1}=0.98pF).

response of the $\pi/2$ resonator (dashed line) and the response with a capacitor mismatch of $\pm$1.0% in the feedback capacitors (solid line) is shown in Figure 4.6b. We see that the notch frequency moves (0.7%) and the Q-value decreases, as Equation (4.11) indicates. When the opamp DC gains are set to 40dB and opamp input parasitic capacitances of 0.2pF are added, the notch frequency error is as great as 5.6% (Figure 4.6c) and the performance is further degraded if the capacitor ratios are inaccurate (Figure 4.6d). According to this general review, the FE structure is not suitable for high-performance BP $\Delta\Sigma$ modulators, although the programmable resonance frequency would be an attractive option.

An LDI SC resonator where the first integrator is delay-free and there is only one feedback path is presented in Figure 4.7. Also, in this topology the center frequency can be freely selected and an ideal simulation example of a $\pi/6$ resonator is depicted in Figure 4.8a. Capacitor mismatch does not affect the Q-value but a 1.4% center frequency error is caused by an error of 2.0% in the feedback capacitance (Figure 4.8b). According to Figures 4.8c and d the finite DC gain and input parasitic of the opamps affect the center frequency (5.1%) in quite a similar way as in the FE topology but the Q-value is degraded more than in the FE structure.

It is worth mentioning that both the FE and LDI structure require two amplifiers

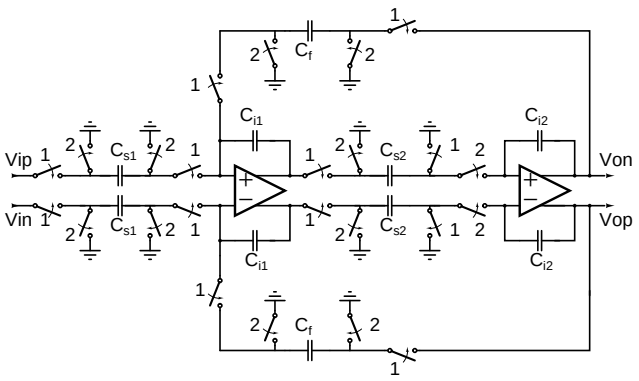

Figure 4.7 An SC implementation of the LDI resonator in Figure 4.3.

to implement a resonator, instead of only one amplifier in some DD SC structures. Furthermore, these two amplifiers have to have a high DC gain and a large GBW, which leads to unnecessarily high power dissipation.

4.4 Implementation of DD Resonator

A DD resonator can be implemented using two analog delay elements in series [7] [8] or utilizing a pseudo-two-path architecture [3] [4] [5] [6]. The most important attributes of an SC resonator implementation are the number of opamps, the total capacitive loading, and the settling time available per sample. Furthermore, the number of switches, the complexity of the clocking signals, and insensitivity towards different nonidealities, such as capacitance mismatch, finite opamp DC gain, and GBW, are also important properties.

The number of opamps can be reduced to one by implementing the delay with two parallel signal paths [3] [4] [5] [6]. A single-opamp SC implementation is shown in Figure 4.9. More time to settle is obtained by employing double-sampling SC techniques [4] [7] [6]. Path mismatch gives rise to a mirror signal. However, the mirror signal is small and it is the image of the received channel itself and is, therefore, of minor consequence in a radio receiver. It appears that the best efficiency is achieved when these two techniques are combined, as in [4] (Figure 4.10). However, the actual capacitive loading still has to be considered in order to provide a fair comparison of the power consumption. Typically, the feedback capacitors have to be designed to be several times larger than the input capacitors so as to accommodate the large internal signal swings of the $\Delta\Sigma$ modulator. However, in all of the previously-reported structures a large feedback capacitor is at some time connected to load the opamp

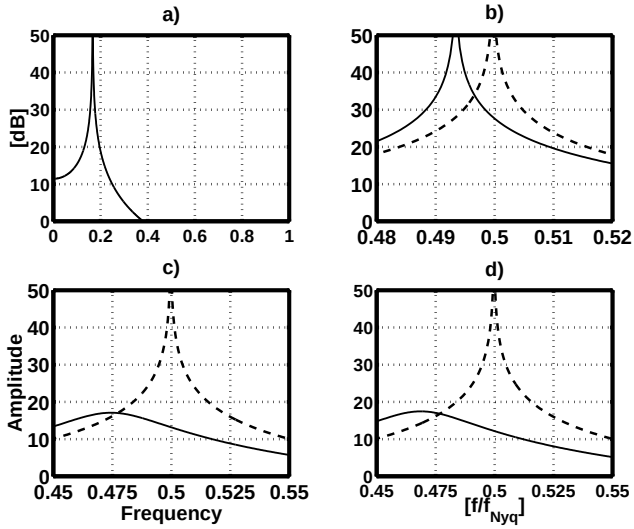

Figure 4.8 Simulations of the LDI SC resonator (Figure 4.7; C_{s1}=C_{s2}=C_{i1}=C_{i2}=0.5pF). a) Ideal $\pi/6$ resonator (C_f=0.134pF), b) $\pi/2$ resonator with a capacitor mismatch of 2.0% (C_f=0.98pF), c) with a finite DC gain of 40dB and an input parasitic capacitance C_p of 0.2pF and d) additionally, a capacitor mismatch of 2.0% (C_f=0.98pF).

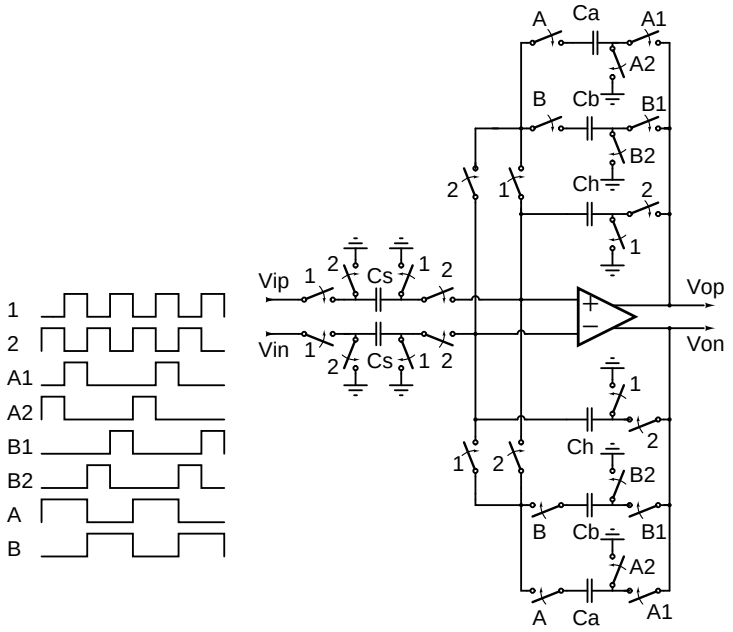

Figure 4.9 Single-opamp DD SC resonator in [3].

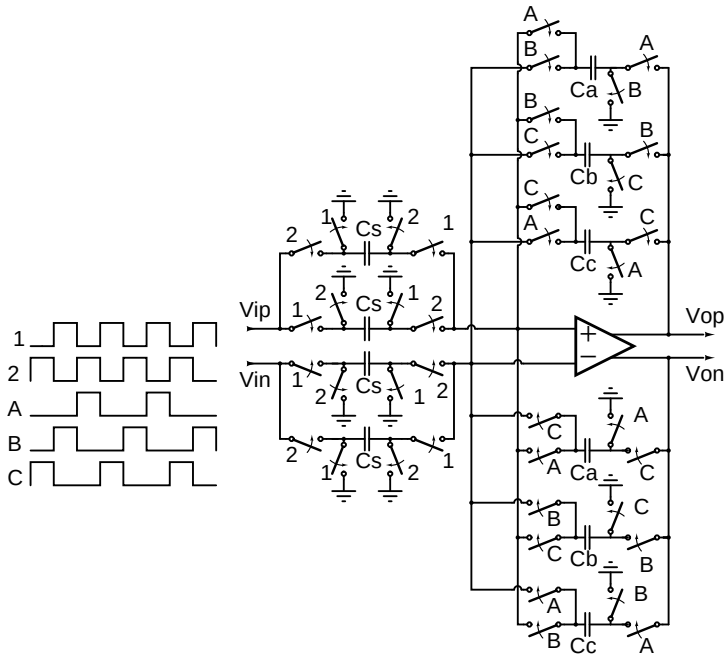

Figure 4.10 Double-sampling single-opamp DD SC resonator in [4].

(Figure 4.11). Let us denote the signal scaling ratio by k, the ratio of the bottom plate parasitic capacitance to the main capacitance by δ, and the minimum usable capacitor specified by process parameters by C_{min}.

$$\begin{cases} k = \frac{C_i}{C_s} \\ C_{bi} = \delta \cdot C_i \\ C_{bs2} = \delta \cdot C_{s2} \\ C_{s2} = \frac{k}{2} C_{DAC} = \frac{k}{2} C_{min} \end{cases} \tag{4.14}$$

The equivalent load capacitance C_{eq} of the opamp in feedback (Appendix C) is then given by

$$\Rightarrow \begin{array}{c} C_{eq}(k) = (k+1+2\delta k+\delta)C_s + \left(2+\frac{C_p}{kC_s}+\frac{1}{k}\right)C_{op} \\ +(1+\delta)C_p + \left[(1+\delta)\left(2k+\frac{C_p}{C_s}+1\right)\right]\frac{C_{min}}{2} \end{array} . \tag{4.15}$$

C_{s2} also increases as a function of k as a result of the C_{DAC} of the next stage, which is fixed to C_{min}. This is valid when the thermal noise of the second resonator is insignificant. We note from Equation (4.15) that the equivalent capacitive load increases more or less linearly as a function of the scaling ratio k. Structures exhibiting such an

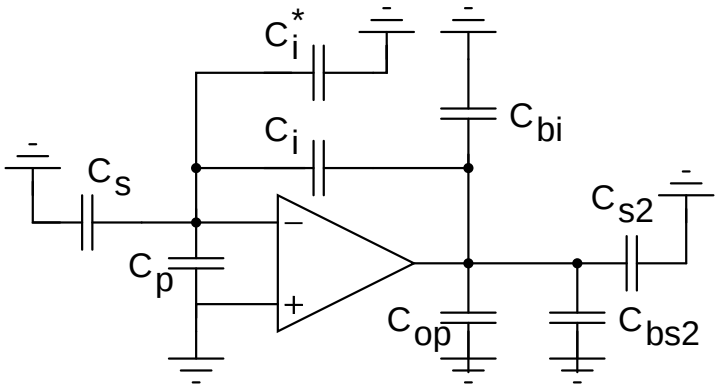

Figure 4.11 The loading of the opamp in reported single-opamp resonators [3] [4].

unfavorable trade-off are not well suited for low supply voltage operation.

4.5 DD SC Resonator Design

In the design of BP ΔΣ modulators, the first task was to select or to design a suitable resonator structure. Among discrete-time resonator topologies, the DD resonator was found to have the highest potential for a high-performance resonator such as was mentioned earlier. To keep power dissipation low enough it was clear that only a single-opamp DD SC resonator could be used. Therefore, the SC resonator structures in Figures 4.9 and 4.10 were the starting point for design. However, the capacitive loading of the amplifier proved to be a problem in these structures when the internal signal swings of the BP ΔΣ modulator were scaled down. Therefore, a new single-opamp DD SC resonator without the loading problem was designed.

During the work the originally-designed SC resonator, known as Version I, was further improved, leading to Versions II and III. These structures are closely based on Version I but the power dissipation has been significantly reduced by using the amplifier more effectively. Because all the resonator versions have been used to implement BP ΔΣ modulators, they are presented separately in the following sections.

4.5.1 Version I

The operation of the developed DD SC resonator can be seen in Figures 4.12 and 4.13a-d. In clock phase 2, the charge in the sampling capacitor C_s is summed with the charge in either of the integration capacitors C_{iA} or C_{iB}. In the clock phase 1, a new sample is taken from the input and the output of the resonator may be sampled by the

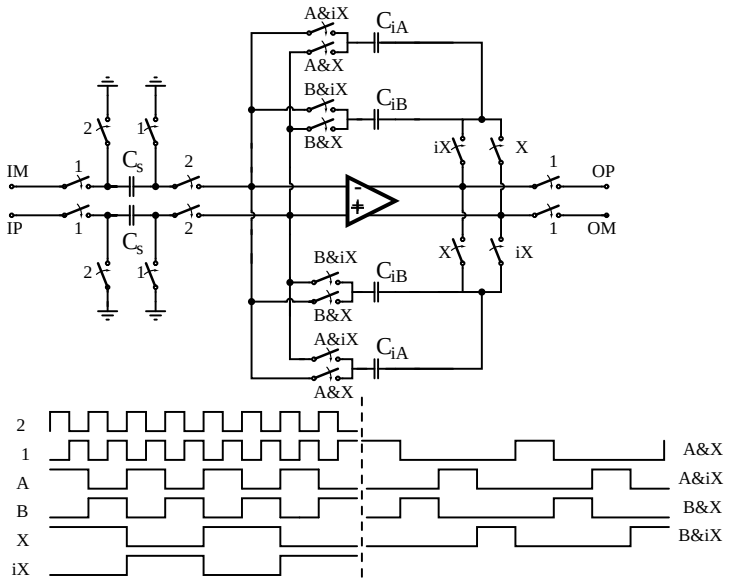

Figure 4.12 The designed single-opamp DD SC resonator (Version I).

following circuit. The delay of two clock periods is implemented using two branches (A & B), in which the signal value is alternately integrated. The sample integrated two clock periods earlier is stored in the integration capacitor of the respective branch. The DD resonator feedback factor of minus one is realized by switching integration capacitors alternately on the opposite nodes of the opamp.

Using differential signals and assuming no component mismatches, we can write the output signal in the z-domain as

$$V_{od}(z) = \frac{-\frac{C_s}{C_i}z^{-1}}{1+z^{-2}}V_{id}(z), \tag{4.16}$$

which is a resonator with a center frequency at $f_s/4$.

The resonator is implemented with only one opamp, so it is, in that sense, comparable to the approaches in Figures 4.9 and 4.10. However, the improvement is that the large feedback capacitor (Figure 4.11: C_i^* between ground and opamp input) is never connected to load the opamp. Figure 4.14 illustrates the loading of the designed resonator during different clock phases. Using the terms in Equation (4.14), the equivalent load of the resonator during the integration phase (I) is given by

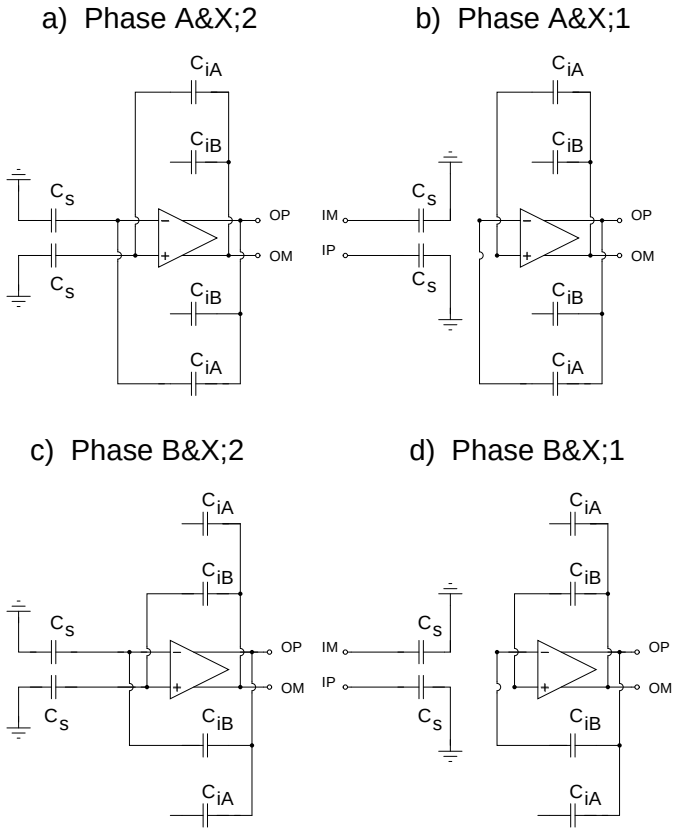

Figure 4.13 The designed resonator circuit during the X clock phase.

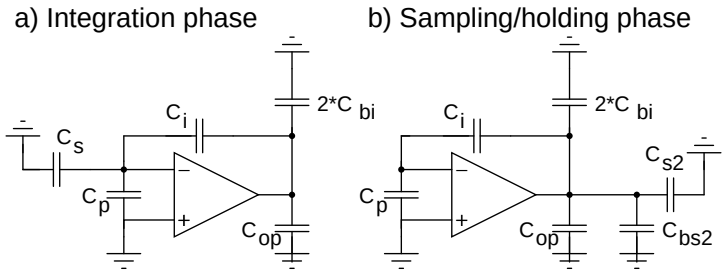

Figure 4.14 The loading of the opamp in the designed SC resonator (Version I).

$$C_{eq}(k) = (1+2\delta k+2\delta)C_s + \left(1+\frac{C_p}{kC_s}+\frac{1}{k}\right)C_{op} + (1+2\delta)C_p \tag{4.17}$$

and during the sampling/holding phase (S) by

$$\begin{aligned} C_{eq}(k) &= 2\delta k \cdot C_s + \left(1+\tfrac{C_p}{kC_s}\right)C_{op} \\ &+ (1+2\delta)C_p + \left[(1+\delta)\left(k+\tfrac{C_p}{C_s}\right)\right]\tfrac{C_{min}}{2} \end{aligned} . \tag{4.18}$$

we can see that the equivalent capacitive load of the proposed resonator remains rather constant with large scaling ratios.

4.5.2 Version II

If the operation of the resonator in Figure 4.12 is considered in detail, it can be noted that during clock period 1 the charge is only carried forward to the next circuit. The charge transfer can already be performed in the integration phase, when the opamp is active only during clock period 2 (Figure 4.15). The same opamp may be shared between two resonators, which means that using the resonator structure in Figure 4.15 it is possible to realize a 4th-order BP $\Delta\Sigma$ modulator with only one opamp. The only consequence of sharing the opamp between the resonators is that the sampling capacitors of the second resonator have to be separate for signal branches A and B. The generation of the clock signals is not more complicated than in the two-opamp implementation. A disadvantage is the bottom plate parasitics of the integration capacitors and switch parasitics, which load the opamp. The memory effect of the opamp input and output parasitics also has to be considered more carefully. Figure 4.11 illustrates the loading of the resonator by removing C_i^* from the opamp input and by adding three bottom plate parasitics of C_i (two resonators) to the opamp output. The equivalent load of the resonator is given by

$$\begin{aligned} C_{eq}(k) &= (1+4\delta k+4\delta)C_s + \left(1+\tfrac{C_p}{kC_s}+\tfrac{1}{k}\right)C_{op} \\ &+ (1+4\delta)C_p + \left[(1+\delta)\left(k+\tfrac{C_p}{C_s}+1\right)\right]\tfrac{C_{min}}{2} \end{aligned} . \tag{4.19}$$

4.5.3 Version III

The power efficiency of the Version I resonator can also be improved by applying the double-sampling SC technique, which also relieves the amplifier design, compared to Version II (Figure 4.16). The operation of the double-sampling resonator is quite

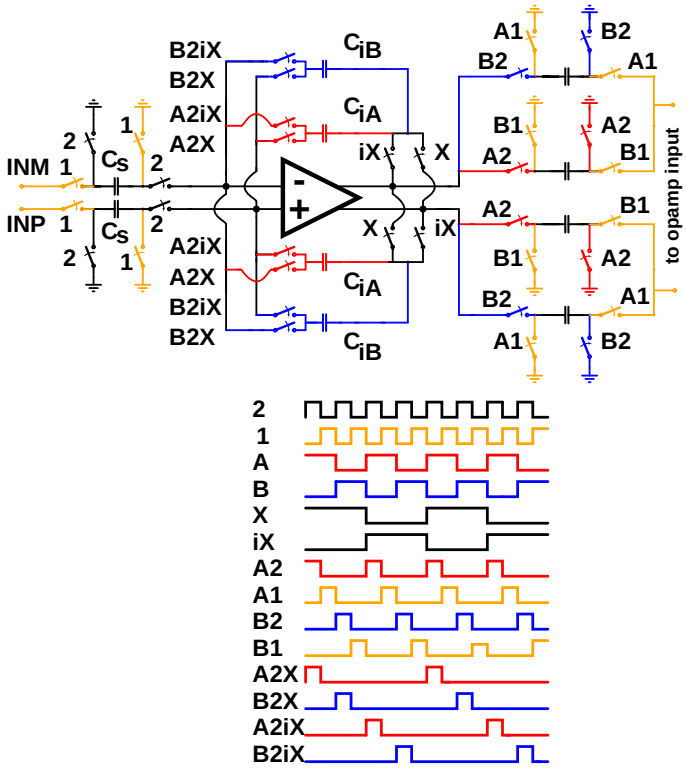

Figure 4.15 The circuit configuration to realize the DD resonator during a half clock period (Version II).

similar to the earlier versions and can be seen in Figures 4.16 and 4.17a-d. The input signal is sampled alternately by paths 1 or 2; when one path is in a sampling phase the other is in an integration phase, which doubles the effective sampling rate or the opamp settling time. In the integration phase, the charge in the sampling capacitor C_s is summed with the charge in the integration capacitor C_i of the respective branch. During integration the output of the resonator is also sampled by the following circuit. The delay of two clock periods is achieved using two integration branches(1&2), in which the signal value is alternately integrated at a frequency which is half of the effective sampling rate. The sample integrated two clock periods earlier is stored in the integration capacitor. The DD resonator feedback factor of minus one is realized by switching integration capacitors alternately on the opposite nodes of the opamp.

In the discrete-time domain the output signals of the resonator can be written as

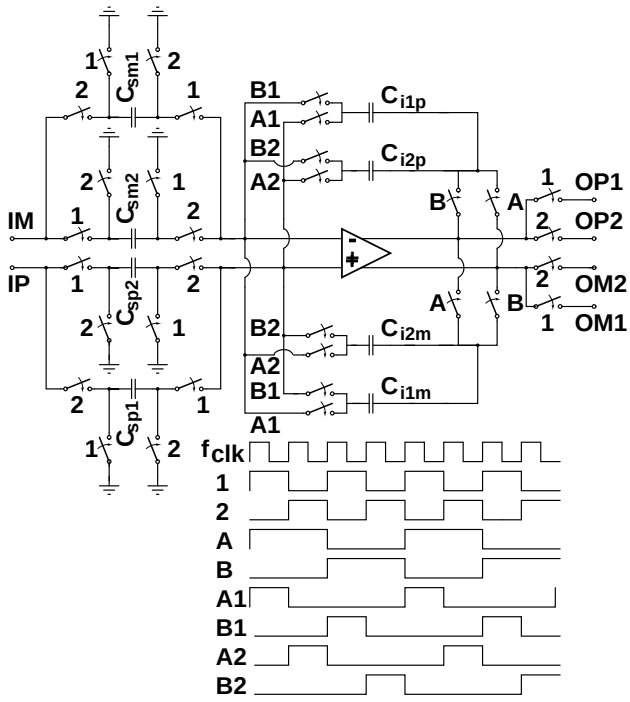

Figure 4.16 The designed double-sampling DD SC resonator (Version III).

$$\begin{aligned}
v_{op}(n-4)C_{i1p} &= v_{om}(n-6)C_{i1p} + v_{im}(n-5)C_{sm1} \\
v_{op}(n-3)C_{i2p} &= v_{om}(n-5)C_{i2p} + v_{im}(n-4)C_{sm2} \\
v_{op}(n-2)C_{i1m} &= v_{om}(n-4)C_{i1m} + v_{im}(n-3)C_{sm1} \\
v_{op}(n-1)C_{i2m} &= v_{om}(n-3)C_{i2m} + v_{im}(n-2)C_{sm2} \\
v_{op}(n)C_{i1p} &= v_{om}(n-2)C_{i1p} + v_{im}(n-1)C_{sm1}
\end{aligned} \tag{4.20}$$

etc. The v_{om} can be obtained correspondingly by interchanging subscripts m and p with each other in the equations. Using differential signals and assuming no component mismatches, the output signal in the z-domain is similar to that in Equation (4.16). Figure 4.11 illustrates the loading of the proposed resonator by removing C_i^* from the opamp input and by adding another bottom plate parasitic of C_i to the opamp output. The equivalent load of the proposed resonator is given by

$$\begin{aligned}
C_{eq}(k) = (1+2\delta k+2\delta)C_s + \left(1+\tfrac{C_p}{kC_s}+\tfrac{1}{k}\right)C_{op} \\
+(1+2\delta)C_p + \left[(1+\delta)\left(k+\tfrac{C_p}{C_s}+1\right)\right]\tfrac{C_{min}}{2}
\end{aligned} \quad . \tag{4.21}$$

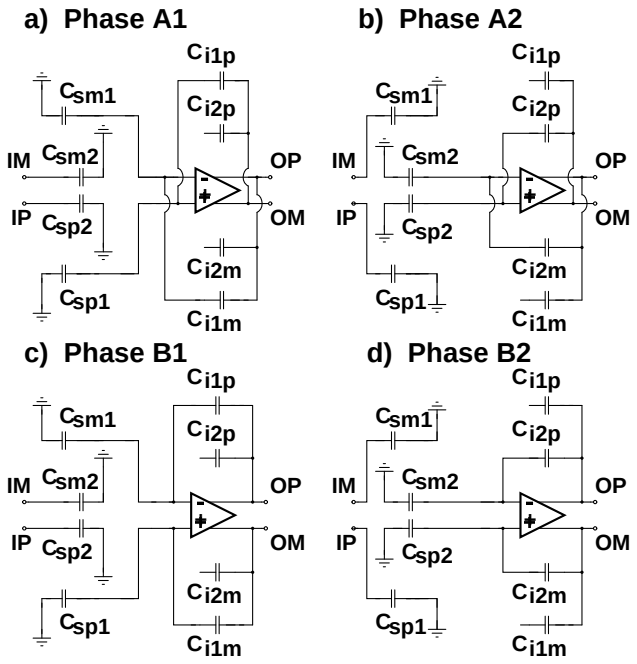

Figure 4.17 The double-sampling resonator circuit during different clock phases.

4.6 Comparison

Comparing Equation (4.15) to Equations (4.18), (4.19), and (4.21), we see that, unlike in the earlier single-opamp structures (Figures 4.9 and 4.10), the equivalent capacitive load of the designed resonators remains rather constant with large scaling ratios. Instead, in [4] the load starts to increase as a result of the large capacitive load connected to the opamp input. The equivalent capacitive load, multiplied by the number of amplifiers needed per resonator and divided by the available settling time as clock periods, gives a fair estimation of the power efficiency. The loading of the designed resonators and that in [4] are plotted in Figure 4.18 as a function of the signal level scaling ratio k. The parasitic capacitances were estimated from an opamp designed for a 2.7V 85MHz BP $\Delta\Sigma$M in a 0.35μm CMOS process.

At first the equivalent load capacitance of the designed resonators decreases, because the effects of the opamp input and output capacitances are reduced by an increasing feedback factor. With a very large scaling ratio, C_{eq} begins to increase slowly, because the sampling capacitance of the next stage starts to dominate. The equivalent load of the resonator in [4] initially decreases for the same reason, but the effect is soon offset by the increase in the total capacitive loading at the input.

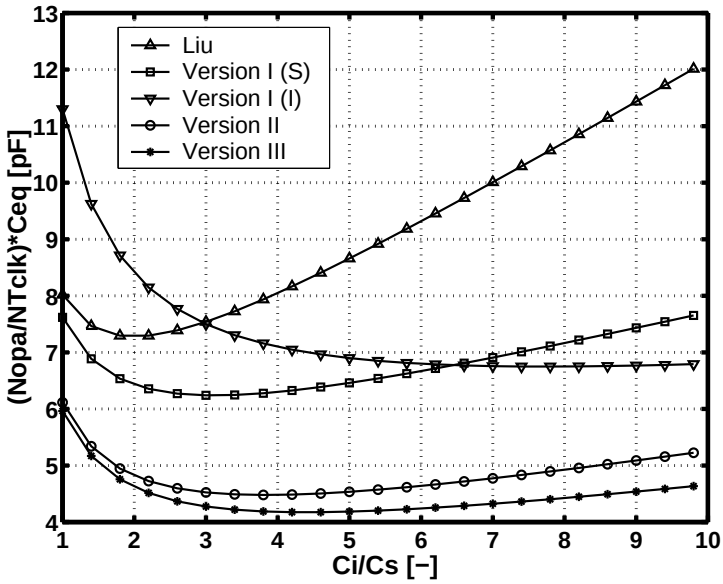

Figure 4.18 Loading during linear settling. Parameters: C_s=0.5pF, C_{min}=0.2pF, input parasitic C_p=0.5pF, opamp output capacitance C_{op}=1.5pF and 5% bottom plate capacitance of C_i and C_{s2}.

Some properties of previously-reported double-delay SC resonators are summarized in Table 4.1. We can see from the table and from Figure 4.18 that power savings are achieved, compared to the SC resonator in [4], using the Version I resonator. A theoretical paper on a similar structure has also been published in [12], which has been done as work parallel to ours [5] [10] [11]. The other structures published earlier are inferior to that in [4] in the sense of the most important properties (N_{opa}, $t_{settling}$ or signal scaling). Therefore they are not considered in more detail. The designed Version II and III resonators are superior to the others, according to Figure 4.18 and Table 4.1. Consequently, the power dissipation can be roughly halved compared to the

Table 4.1 Characteristics of different DD SC resonators.

Reference	[14]	[13]	[11] [12]	[9]	[4]	[7]	[3]	[8]
Version	III	II	I					
N_{opa}	1	0.5	1	4	1	2	1	2
N_{cap}	8	6-8	6	12	10	12	8	14
N_{switch}	28	20(22)	20	40	40	48	28	44
$t_{settling}$	T_{clk}	$T_{clk}/2$	$T_{clk}/2$	T_{clk}	T_{clk}	T_{clk}	$T_{clk}/2$	$T_{clk}/2$
N_{clk}	8	12	8	4	5	2	8	2
scaling	good	good	good	good	poor	poor	poor	poor

resonator structure in [4], with only a more complicated clocking scheme. Version III gives small power savings, together with easier implementation compared to Version II. Different nonidealities can significantly reduce the performance of analog circuitry and their effect is analyzed in the following section.

4.7 Nonidealities

4.7.1 Capacitor Mismatch and Image

Capacitor mismatch is one error source in SC structures. If we first assume that the A and B paths in Versions I/II (1 and 2 paths in Version III) are identical but that there is mismatch between differential branches, we can mark

$$\begin{cases} C_{ip} = (1+\varepsilon_i)C_{im} = (1+\varepsilon_i)C_i \\ C_{sp} = (1+\varepsilon_s)C_{sm} = (1+\varepsilon_s)C_s \end{cases}, \tag{4.22}$$

where ε is the relative mismatch between differential nodes. Assuming that there is mismatch in both capacitor ratios the differential gain of the resonator will vary at the frequency of $f_s/4$, because the integrating capacitors are connected alternately on the opposite nodes of the opamp. The effect of the gain variation can be modeled by an $f_s/4$-multiplier before the resonator. The possible DC offset or the 1/f noise at the resonator (modulator) input will be partly transferred to the notch frequency as a result of the $f_s/4$ multiplication and the differential error voltage at the resonator output can be written as

$$v_{od}^{noise} \approx \left(\frac{\varepsilon_s \cdot \varepsilon_i}{1+\varepsilon_i} \right) \frac{C_s}{C_i} v_{dc,in}^{noise}, \tag{4.23}$$

where the term $v_{dc,in}^{noise}$ includes the DC offset and the 1/f noise at the resonator input. The error magnitude will not be significant until the ratio errors are in the order of a few percent and the $v_{dc,in}^{noise}$ is a few dozen millivolts.

Some behavioral level transient simulations have been performed in the ELDO program for a 1b 2nd-order BP ΔΣM structure (MFB in Figure 2.7 with N=1), which consists of the designed DS SC resonator, a comparator, and a feedback logic. The FFT has been calculated from 16384 windowed (Kaiser β=13) samples using MATLAB. The opamp model was a folded-cascode amplifier with a GBW of 8 times the sampling frequency and a DC gain of 80dB to eliminate the effect of the finite DC gain and GBW. A DC offset as large as 100mV was added to the opamp model to verify Equation (4.23). The switches were modeled with an on-resistance of 10Ω and parasitic capacitors of 1fF between the switch terminals. In Figures 4.19a and b there

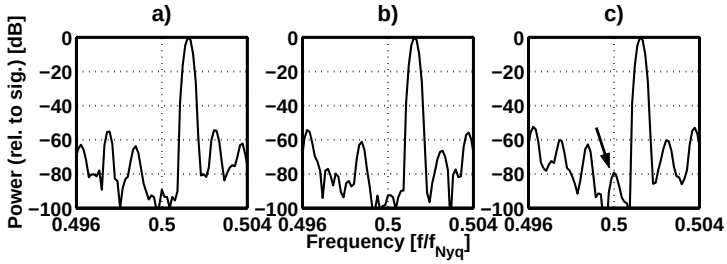

Figure 4.19 Simulation results with mismatches in capacitor ratios; a) ε_s=-0.05, b) ε_i=-0.05 and c) ε_s=-0.05 and ε_i=-0.05. Nominal parameters: C_s=0.5pF, C_i=2.5pF, opamp input parasitic C_p=0.5pF, f_s=80MHz and a -9dBr input signal.

is no clear frequency component at the notch frequency when a capacitor mismatch of 5% was separately set between the differential branches. Instead, in Figure 4.19c a clear frequency component at a notch frequency 79dB below the signal level appears in the output when there is a 5% capacitor mismatch in both capacitor ratios (ε_s and ε_i in Equations (4.22) and (4.23)). According to Equation (4.23) the noise component (v_{od}^{noise}) is 47.6μV or 92dB below the reference level ($\pm$1.0V reference voltages). Hence, the simulated result of 88dB below the reference level (79dB below -9dBr input signal) corresponds quite well to the theory.

In double-sampling structures the output can be written as [7]

$$V_{od}(z) = H(z)\left[V_{id}(z) + \gamma V_{id1}(z)\right], \tag{4.24}$$

where γ is the gain error between paths. The term γV_{id1} will cause an attenuated copy of the signal at the $\Delta\Sigma$ modulator output. If there is a ratio error of capacitances between paths in Versions I/II

$$\gamma = \frac{C_{iA}}{C_{iB}} - 1 \tag{4.25}$$

and in Version III

$$\gamma = \frac{(C_{i1}/C_{s1})}{(C_{i2}/C_{s2})} - 1. \tag{4.26}$$

Assuming opamp settling behavior to be linear, the difference between the on-times of the integration clock signal creates a similar gain error between paths in all the versions and, furthermore in Version III a difference between the sampling clocks. Hence, for Version III

$$\gamma \approx \frac{t_{A1}}{t_{A2}} - 1 \; or \; \gamma \approx \frac{t_{B1}}{t_{B2}} - 1 \; or \; \gamma \approx \frac{t_1}{t_2} - 1. \tag{4.27}$$

4.7.2 Amplifier DC Gain and GBW

The amplifier characteristics affect each of the resonator versions somewhat differently. To simplify the analysis, Version III is first studied in detail and after that the special characteristics of Versions I and II are discussed. Finally, the results of the analysis of all versions are collected.

4.7.2.1 Version III

The finite DC gain(A_{DC}) and non-zero input capacitance(C_p) of the opamp have an effect on resonator performance. We have [15]

$$v_{op,m}(n) = v_{Ci}(n) - \frac{1}{A_{DC}} v_{op,m}(n) \tag{4.28}$$

and

$$\beta = \frac{C_i}{C_s + C_p + C_i}, \tag{4.29}$$

where v_{Ci} is the voltage over the C_i and β the feedback factor of the opamp. Here C_{DAC} has been shared with C_s. Using the z-transform and by simplification, we get, for Version III

$$V_{od}(z) = \frac{-\frac{C_s}{C_i}\left(\frac{1}{1+\frac{1}{\beta A_{DC}}}\right) z^{-1}}{1 + \frac{C_p}{C_i}\left(\frac{1}{A_{DC}+\frac{1}{\beta}}\right) z^{-1} + \left(\frac{1+\frac{1}{A_{DC}}}{1+\frac{1}{\beta A_{DC}}}\right) z^{-2}} V_{id}(z), \tag{4.30}$$

where the z^{-1} term is insignificant, with a typical C_p/C_i ratio of the order of ˜0.2 (Figure 4.20). We notice that the notch frequency moves very slightly as a result of the low DC gain. The notch depth (Q-value) decreases as a result of low A_{DC} when β is smaller than one. The effect of the error in the p_2 term (Equation (4.3)) on the Q-value resulting from low DC gain is plotted in Figure 4.20 with different feedback factor values. Naturally, the required DC gain depends on the band of interest or on the oversampling ratio.

The same BP $\Delta\Sigma$M as was used in Section 4.7.1 was simulated using opamp DC gains of 80dB, 55dB, and 30dB and the output spectra are shown in Figure 4.21. When the opamp DC gain is as low as 30dB (Figure 4.21d) the notch frequency moves slightly (below 0.2%) and the Q-value decreases, according to Equation (4.30). A small resonance frequency error may also be detected in the simulated spectrum but ultimately, the finite DC gain has only a minor impact on the performance of the

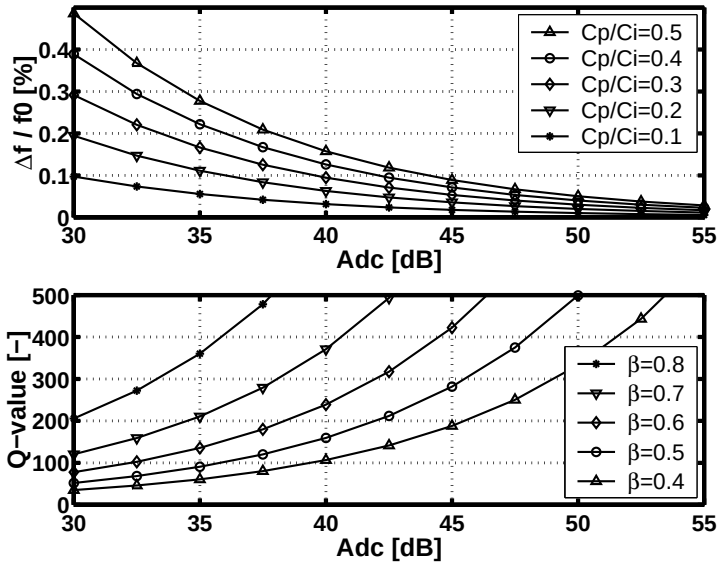

Figure 4.20 The performance degradation of the resonator (Version III) resulting from the finite DC gain of the opamp.

resonator.

The finite GBW of the opamp can cause charge transfer error because of incomplete settling. The opamp output voltage (Figure 4.22) can be written as

$$v_o(t) = v_o(t=0) + \frac{1}{\beta}\left(v_a(t) - v_a(t=0)\right). \tag{4.31}$$

Assuming linear settling of the folded-cascode opamp we have

$$v_a(t) = v_a(t=0)\exp\left(-\beta \cdot GBW \cdot t\right). \tag{4.32}$$

The initial conditions can be calculated from the capacitor voltages at the switching action using the charge conservation principle. By writing the charge equations for each node we can solve

$$\begin{array}{c} v_a(t=0) = \frac{\beta}{(1-\beta)C_i + C_{Ltot}}\left[(C_{Lp} \mp C_{Lbb})\,v_o(n-1)\right. \\ \left. + C_{Ltot}v_o(n-2) + \frac{C_s}{C_i}(C_i + C_{Ltot})v_{in}(n-1)\right] \end{array} \tag{4.33}$$

and

$$\begin{array}{c} v_o(t=0) = \frac{1}{(1-\beta)C_i + C_{Ltot}}\left[\right. \\ \left.(C_{Lp} \mp C_{Lbb})\,v_o(n-1) + C_i(\beta-1)v_o(n-2) + \beta C_s v_{in}(n-1)\right] \end{array}, \tag{4.34}$$

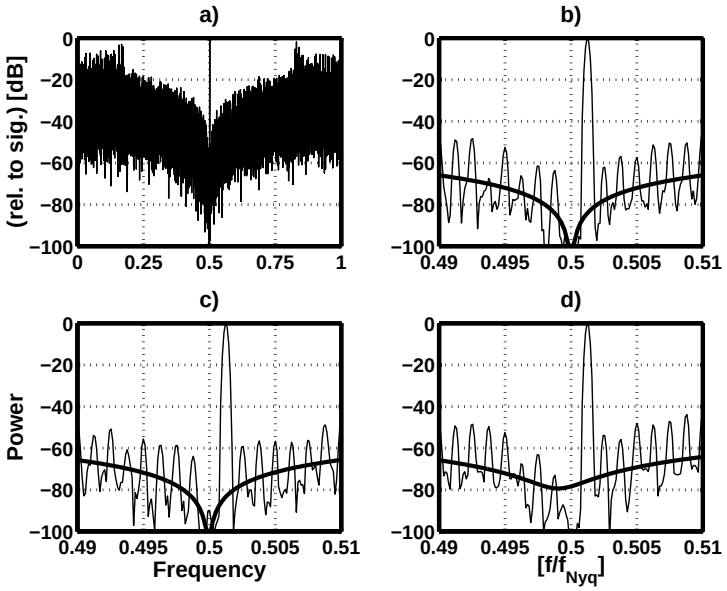

Figure 4.21 Simulated output spectra of a 1b 2nd-order BP ΔΣM using the designed DS SC resonator structure compared to the nonideal model in Equation (4.30). a,b) A_{DC}=80dB, c)A_{DC}=55dB and d)A_{DC}=30dB.

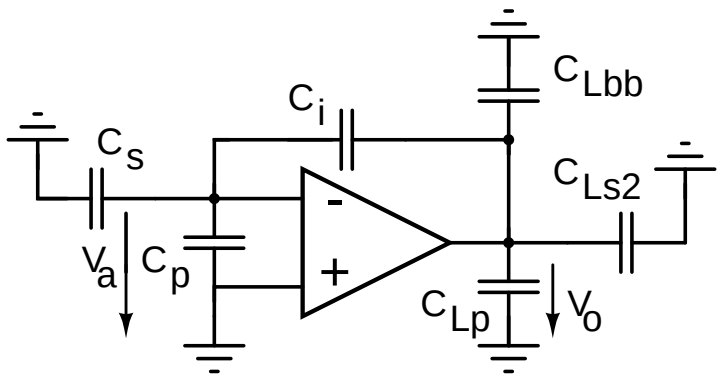

Figure 4.22 A simplified schematic of opamp loading during settling.

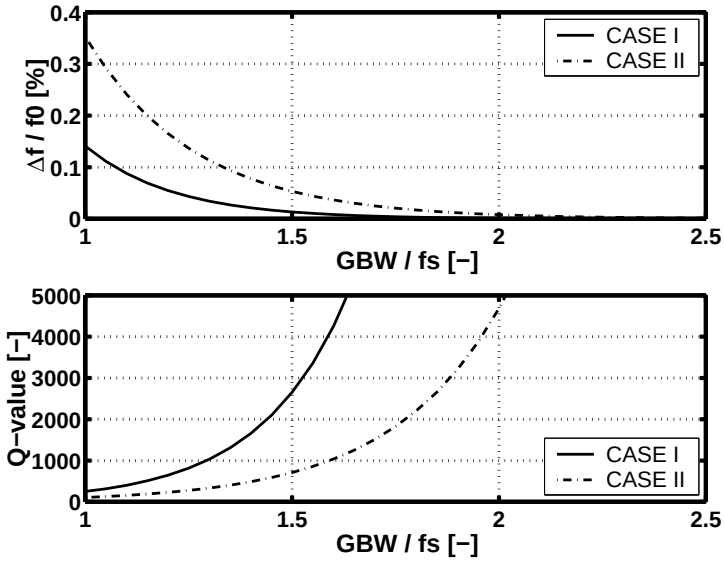

Figure 4.23 The performance degradation of the resonator (Version III) resulting from the finite GBW of the opamp (f_s=the effective sampling rate). C_s=0.6pF, C_i=kC_s, C_{Lp}=1.0pF, C_{Lbb}=2*0.05C_i; CASE I: k=5.5, C_p=0.5pF, C_{Ls2}=0.55pF $\Rightarrow \beta = 0.75$ and CASE II: k=4, C_p=1.0pF, C_{Ls2}=0.4pF $\Rightarrow \beta = 0.6$.

where

$$C_{Ltot} = C_{Ls2} + C_{Lp} + C_{Lbb}. \tag{4.35}$$

The C_{Ls2} is the load of the next stage, the C_{Lp} is the total parasitic of the opamp output, and C_{Lbb} is the bottom plate parasitics of the two integration capacitors. In the previous calculations it is assumed that the voltage over C_i is equal to the output voltage or that the effect of the finite DC gain has not been observed. In Version III the available settling time of the opamp $t_{sett} \sim 1/f_s = T$. Solving Equation (4.31) in the discrete time domain we get the following terms in Equation (4.3)

$$\begin{cases} g_0 = -\frac{C_s}{C_i}\frac{\beta-(1+C_{Ltot}/C_i)(1-\exp(-\beta\cdot GBW\cdot t_{sett}))}{\beta-(1+C_{Ltot}/C_i)} \\ p_1 = \frac{(C_{Lp}\pm C_{Lbb})\exp(-\beta\cdot GBW\cdot t_{sett})}{(1-\beta)C_i+C_{Ltot}} \\ p_2 = \frac{(1-\beta)C_i+C_{Ltot}(1-\exp(-\beta\cdot GBW\cdot t_{sett}))}{(1-\beta)C_i+C_{Ltot}} \end{cases}. \tag{4.36}$$

We can see that the finite GBW causes error in the notch frequency (p_1-term) as a result of the memory effect of the parasitic capacitors. However, the effect is, in any case, negligible, with β in the order of 0.7 (Figure 4.23). The Q-value also decreases slightly with a very low gain bandwidth of the opamp (Figure 4.23).

Behavioral level transient simulations of the 2nd-order 1b BP $\Delta\Sigma$M were per-

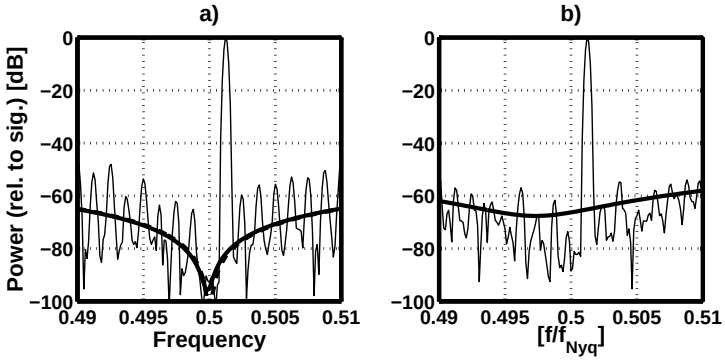

Figure 4.24 Simulated output spectra compared to the nonideal model in Equation (4.36). a) GBW=1.5· f_s b) GBW=0.75· f_s (parameters equivalent to Figure 4.19, 5% bottom plate parasitics of C_is have been added).

formed using an opamp DC gain of 80dB and by setting the opamp input transconductance to values of 1.5mS and 0.75mS (Figure 4.24). These are equivalent to GBWs of 1.5 times and 0.75 times the sampling frequency. In Figure 4.24a a GBW of $1.5\,f_s$ does not degrade the performance of the resonator and the simulated output spectrum corresponds well to the model. A GBW of $0.75\,f_s$ quite clearly decreases the Q-value but it is hard to detect a resonance frequency error from the simulated output spectrum (Figure 4.24b). Instead, the model indicates a small frequency error of 0.5% and a larger degradation in the Q-value than in the simulation.

4.7.2.2 Version II

In Version II an opamp is shared between two resonators, which causes coupling between the outputs of the resonators, which has to be analyzed on a BP ΔΣ modulator level (Figure 4.25). In a 1b ΔΣ modulator the gain over the quantizer is not defined and we may assume it to be $2k_2$. By ignoring the denominator (poles), we obtain

$$STF(z) = g_{01}\left(g_{02} + d_2\frac{2k_2}{k_1}\right)z^{-2} \tag{4.37}$$

and

$$NTF(z) = 1 + \left(p_{21} + p_{22} - d_1\frac{g_{02}k_1}{2k_2} - d_1d_2\right)z^{-2} + p_{21}p_{22}z^{-4}, \tag{4.38}$$

where the g-terms describe the gain and the p-terms the errors (ideally one) in the Q-value of the resonators. The k-terms are signal level scaling coefficients and the

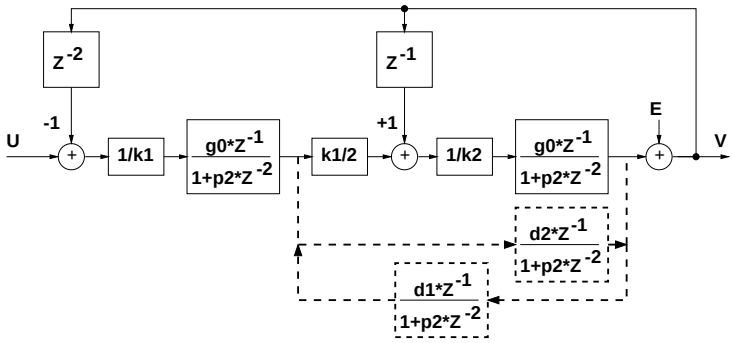

Figure 4.25 Nonidealities resulting from opamp properties and sharing between two resonators (Version II).

Table 4.2 Coefficients in Figure 4.25 as a function of A_{DC} and GBW of the opamp (subscript m refers to 1st and 2nd resonator).

	A_{DC}	GBW
$g_{0m=1,2}$	$-\frac{C_{DACm}}{C_{im}}\left(\frac{1}{1+\frac{1}{\beta_m A_{DC}}}\right)$	$-\frac{C_{DACm}}{C_{im}}\frac{\beta_m-(1+C_{Ltotm}/C_{im})(1-\exp(-\beta_m\cdot GBW\cdot t_{sett}))}{\beta_m-(1+C_{Ltotm}/C_{im})}$
$p_{2m=1,2}$	$\left(\frac{1+\frac{1}{A_{DC}}}{1+\frac{1}{\beta_m A_{DC}}}\right)$	$\frac{(1-\beta_m)C_{im}+C_{Ltotm}(1-\exp(-\beta_m\cdot GBW\cdot t_{sett}))}{(1-\beta_m)C_{im}+C_{Ltotm}}$
$d_{m=1,2}$	$\frac{C_p}{C_{im}}\left(\frac{1}{A_{DC}+\frac{1}{\beta_m}}\right)$	$\frac{\left(C_{Lp}\ \begin{matrix}(\pm)_1\\(+)_2\end{matrix}\ C_{Lbb}\right)\exp(-\beta_m\cdot GBW\cdot t_{sett})}{(1-\beta_m)C_{im}+C_{Ltotm}}$

d-terms are the coupling coefficients between resonators. The terms as a function of opamp characteristics are listed in Table 4.2 and the parameters used in the equations are described in Table 4.3. We can see that opamp nonidealities cause a gain error for the STF and slightly move the zeros of the NTF from their ideal value of $f_s/4$ to $f_s/4\pm\Delta f$ and decrease the Q-value.

Assuming a white quantization noise and a notch frequency of $f_s/4$, the in-band noise power of a 4th-order BP ΔΣM is

$$n_0^2=\frac{\Delta^2}{6}\left(\frac{a}{OSR}-\frac{b}{\pi}sin(\frac{\pi}{OSR})+\frac{c}{2\pi}sin(\frac{2\pi}{OSR})\right), \tag{4.39}$$

where Δ is a quantization step, OSR an oversampling ratio, and

$$\begin{cases} a=0.5\left(1+\left(p_{21}+p_{22}-d_1\frac{g_{02}k_1}{2k_2}-d_1d_2\right)^2+p_{21}^2p_{22}^2\right)\\ b=(1+p_{21}p_{22})\left(p_{21}+p_{22}-d_1\frac{g_{02}k_1}{2k_2}-d_1d_2\right)\\ c=p_{21}p_{22}\end{cases}. \tag{4.40}$$

Table 4.3 Parameters and capacitances used in the equations in Table 4.2.

Parameter	Description
C_s	sampling capacitance
C_{DAC}	DAC capacitance
C_i	integration capacitance
C_p	opamp input parasitic capacitance
C_{Lp}	opamp output parasitic capacitance
C_{Lbb}	total bottom plate parasitics of C_is
C_{ADC}	total ADC input capacitance
C_{Ltot1}	$C_{Lp}+C_{Lbb}+C_{s2}$
C_{Ltot2}	$C_{Lp}+C_{Lbb}+C_{ADC}$
β_1	$C_{i1}/(C_{DAC1}+C_p+C_{i1})$
β_2	$C_{i2}/(C_{s2}+C_{DAC2}+C_p+C_{i2})$
$k_{m=1,2}$	C_{im}/C_{DACm}

Table 4.4 The effect of the finite GBW in Version I.

g_0	$-\frac{C_{DAC}}{C_i}\left(1+\frac{1}{\beta_S}\exp\left(-\beta_S\cdot GBW_S\cdot t_{sett}\right)\right)\frac{\beta_I-(1+C_{LtotI}/C_i)(1-\exp(-\beta_I\cdot GBW_I\cdot t_{sett}))}{\beta_I-(1+C_{LtotI}/C_i)}$
p_1	$\left(1+\frac{1}{\beta_S}\exp\left(-\beta_S\cdot GBW_S\cdot t_{sett}\right)\right)\frac{(C_{Lp}\pm C_{Lbb})\exp(-\beta_I\cdot GBW_I\cdot t_{sett})}{(1-\beta_I)C_i+C_{LtotI}}$
p_2	$\left(1+\frac{1}{\beta_S}\exp\left(-\beta_S\cdot GBW_S\cdot t_{sett}\right)\right)\frac{(1-\beta_I)C_i+C_{LtotI}(1-\exp(-\beta_I\cdot GBW_I\cdot t_{sett}))}{(1-\beta_I)C_i+C_{LtotI}}$
C_{LtotI}	$C_{Lp}+C_{Lbb}$
β_I	$C_i/(C_{DAC}+C_p+C_i)$
β_S	$C_i/(C_p+C_i)$

4.7.2.3 Version I

In Version I the integration is performed during clock phase 2 (I) and the charge is only transferred forward during clock phase 1 (S). Therefore, during clock phase 2 the amplifier operates in a similar way to in Version III. Only the available settling time and capacitive load differ from Version III. Hence, the finite DC gain of the opamp has an effect on the transfer function, as in Version III (Equation (4.30)). The finite GBW of the opamp leads to extra terms in Equation (4.36) as a result of settling during clock phase 1 (Table 4.4).

4.7.2.4 DC Gain and GBW Summary

The requirements of an amplifier have to be estimated by considering the quantization noise shaping of the BP ΔΣ modulator. The in-band noise power of a 4th-order BP ΔΣM was studied in Chapter 2 (Equation (2.28)) and the special characteristics of opamp sharing between two resonators in Equation (4.39). Using these equations and the resonator nonidealities that were earlier calculated we can plot opamp require-

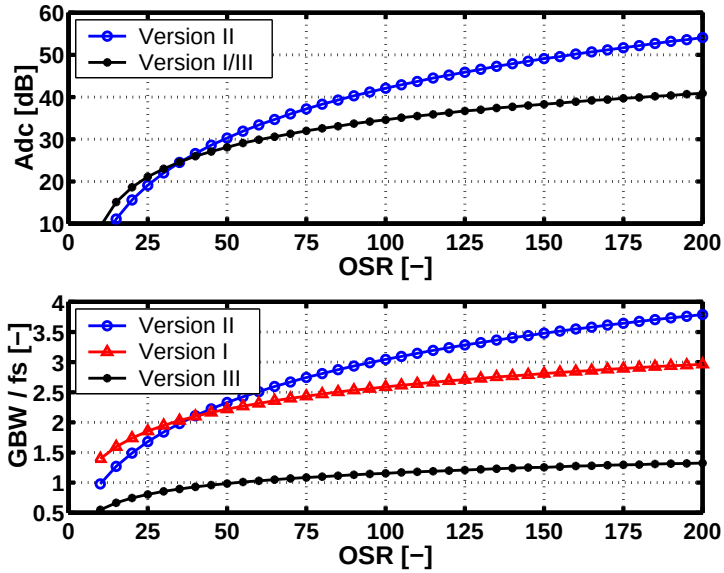

Figure 4.26 The required characteristics of the opamp, if the in-band noise is allowed to increase by 1dB with two identical resonators in a 4th-order BP ΔΣ modulator ($t_{settling} = 0.4/f_s$ for Versions I/II, $0.9/f_s$ for Version III, C_s=0.6pF, C_i=3.3pF, C_{Lp}=1.0pF, C_{Lbb}=(2;4)*0.04C_i, C_p=0.6pF, C_{Ls2}=0.55pF).

ments if we allow the in-band noise power to increase by 1dB as a result of opamp DC gain and gain bandwidth separately (Figure 4.26). For the sake of simplicity the capacitance values and GBW of the opamp in both resonators are assumed to be equal. We can see that a DC gain about 10dB higher is required in Version II, compared to Version I and II with high OSRs. This is due to the signal coupling mechanism (Section 4.7.2.2). Version II also requires a higher opamp GBW than Version I, regardless of the equal settling times, because of higher capacitive loading during the integration phase and also the signal coupling mechanism. The GBW requirements in Version III are relaxed considerably compared to Versions I and II because of the available settling time enabled by the double-sampling technique. Naturally, the requirements are relaxed with a lower OSR and an inferior amplifier can be used.

4.7.3 Amplifier DC Offset

The possible DC offset of the amplifier causes error at the DC frequency; the output error voltage is

$$V_{out} = \left(2 + \frac{C_s}{C_i}\right) V_{off}. \tag{4.41}$$

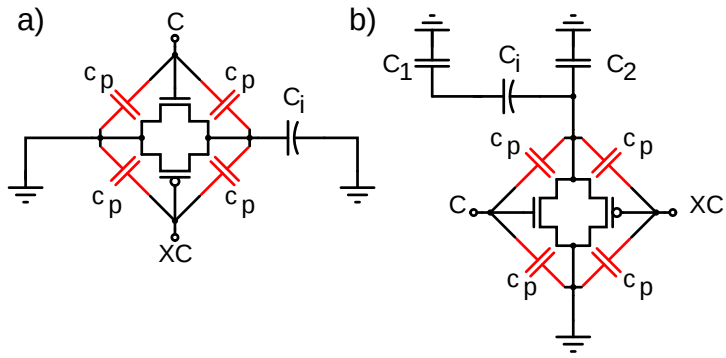

Figure 4.27 Circuit schematics for clock feedthrough calculations.

Because the band of interest is around $\pi/2$ the component is of no consequence. As a second-order effect, the largely attenuated DC offset will be shifted to the notch frequency because of $f_s/4$ clock signals at the opamp input and, if necessary, can be removed using a digital DC calibration. The 1/f noise can be thought of as behaving in a way similar to that of the offset voltage and it is of no consequence.

4.7.4 Switches

Possible mismatch between the switches connected to the resonator input will cause a clock feedthrough component at the notch frequency ($f_s/4$) (Figure 4.27a). We shall denote the mismatch error between the pMOS and nMOS transistors of CMOS switches in the positive node ε_p and in the negative node ε_m, respectively. Furthermore, there can be mismatch (δ) between switches in the differential nodes. By terming the nominal total parasitic capacitances of the switches between the gate and the channel (signal path) c_p, we can derive the clock noise (f=$f_s/4$) at the resonator output as

$$v_{od,noise}^{clk} \approx \frac{c_p}{C_i}\left[(1+\delta)\varepsilon_m - \varepsilon_p\right]V_{dd}, \tag{4.42}$$

where V_{dd} is the positive supply (negative equal to 0). This is a first-order approximation but it gives an adequate estimate of the magnitude of error. The difference between the on/off times of the switches can also cause clock feedthrough as a result of incomplete cancellation, regardless of the switch matching.

The 1b 2nd-order BP $\Delta\Sigma$M used earlier was again simulated in ELDO using a near-ideal opamp model (A_{DC}=80dB and GBW>8f_s). The f_s/4 switches connected to the opamp input and output were modeled by a CMOS switch using an on-resistance of 10Ω (near-ideal) and parasitic capacitors of 10fF between the switch terminals.

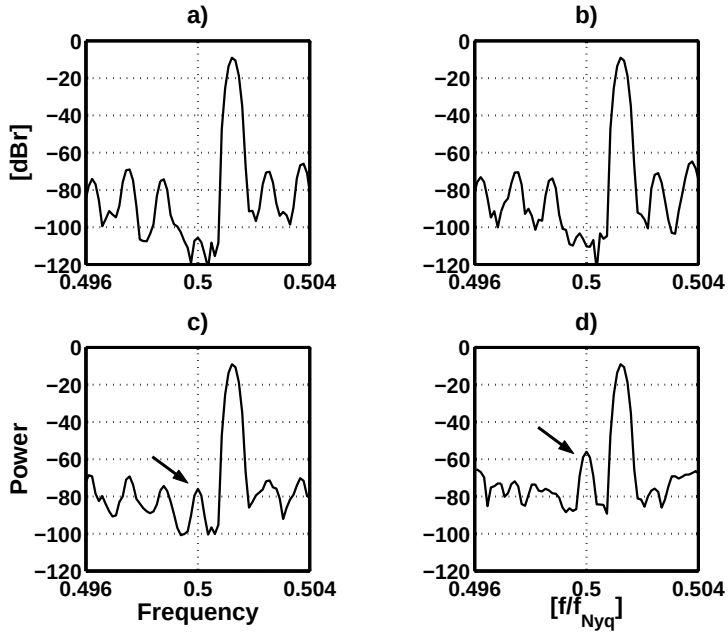

Figure 4.28 Simulated output spectra using nonideal switch models driven by $f_s/4$ clock signals ($c_p = 10fF$, V_{dd}=3.0V). a) ε_p=ε_m=δ=0, b) ε_p=ε_m=-0.05 and δ=0, c) ε_p=ε_m=0 and δ=-0.05, d) ε_p=-0.05, ε_m=0.03 and δ=0.

A simulated output spectrum without switch mismatches is shown in Figure 4.28a. Then a 5% mismatch between parasitic gate-to-channel capacitors in both differential branches is added to a CMOS switch model driven by the A1 clock signal. In Figure 4.28b the simulated output spectrum does not contain any frequency component at the notch frequency, as Equation (4.42) predicts. However, if the size of the switch parasitic capacitors in one input switch is changed by 5%, a frequency component appears at the notch frequency 76dB below references (Figure 4.28c). This corresponds a differential error (δ) of 5% and the other error terms in Equation (4.42) are zero. Hence, the frequency component should not be visible according to Equation (4.42) and the first-order approximation does not work correctly in this example. Next, different mismatch errors of 5% and 3% in differential nodes are added to a CMOS switch model driven by the A1 clock signal. In Figure 4.28 this causes a frequency component at the notch frequency 56dB below the reference level, which is near the value of -60dBr predicted by Equation (4.42). When the previous mismatch errors had been set to values of 2% and 1% a -74dBr clock feedthrough component was simulated. The component level decreased 18dB, corresponding to Equation (4.42). As a conclusion, the calculated first-order approximation for the clock feedthrough in Equation (4.42)

does not give a good estimate of the level of the $f_s/4$ clock feedthrough component at the output when there is only differential mismatch (δ) between input switches. However, it illustrates well the importance of switch matching for the clock feedthrough level, as even a 1% mismatch in one input switch will cause a clock feedthrough component of the order of -78dBr. Therefore, it is evident that the component has to be removed using a digital DC calibration after a digital down-conversion.

The switches at the resonator output are also driven by the clock signals at a frequency of $f_s/4$ (Figure 4.27b). Assuming the same relation between these switches, we obtain

$$v_{od,noise}^{clk} \approx \frac{c_p}{C_i + \left(1 + \frac{C_i}{C_1}\right) C_2} [(1+\delta)\varepsilon_m - \varepsilon_p] V_{dd}, \tag{4.43}$$

where C_1 is the total parasitic capacitance resulting from the switches connected to the input side of C_i and C_2 is the total parasitic capacitance connected to the output side node of C_i at the switching moment. In the previous equations it is assumed that the switches driven by the clock signals of X(A) or iX(B) are always turned on before, and off after, the other switches. In the implementation of the 4th-order BP $\Delta\Sigma$ modulator the generated clock noise of the switches is caused mainly by the first resonator, because the noise of the second stage is shaped in the loop by the second-order transfer function and will be negligible. The parasitic capacitances C_1 and C_2 include voltage-dependent parts, because of the switch transistors. However, the voltage over C_1 is relatively constant between clock periods and C_2 will be dominated by the bottom plate parasitics of the integration capacitors. Furthermore, in an 80MHz circuit implementation, Equation (4.43) parameter C_1 may be of the order of 10^{-14}, C_i of the order of 10^{-12}, and C_2 of the order of 10^{-13}. This leads to a denominator over 10 times larger than in Equation (4.42) and therefore the clock feedthrough noise is dominated by the $f_s/4$ switches connected to the opamp input.

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Chapter 5

Implemented BP ΔΣ Modulators

All the designed and implemented BP ΔΣ modulators are targeted for the digital IF receiver architecture and are implemented with a 0.35μm (Bi)CMOS technology and operate with a 3.0V supply. They combine frequency down-conversion with analog-to-digital conversion by directly sampling an input signal from an intermediate frequency of 60-100MHz to a digital intermediate frequency of 10-20MHz. The circuits operate at a sampling frequency of 80MHz, for example, in order to keep the clock jitter requirements low enough.

The first implemented BP ΔΣM is based on Version I of the designed SC resonator. Hence, two opamps operating at full sampling frequency are required in order to realize a 4th-order transfer function. The second implemented 4th-order BP ΔΣM utilizes Version II of the designed SC resonator and therefore only a single opamp is needed, to implement two DD resonators. The two implemented cascade architectures are also based on the Version II resonator. The fourth implemented BP ΔΣM circuit (the fifth architecture) is preceded by a decimation sampler which decreases the effective operation frequency of the ΔΣM to 40MHz but remains at a sampling frequency of 80MHz. Utilizing the double-sampling SC resonator, called Version III, the operating frequency is further reduced to 20MHz.

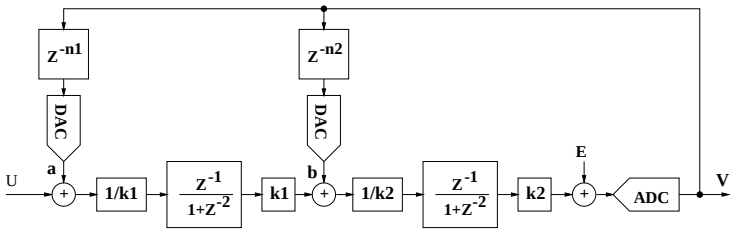


Figure 5.1 A block diagram of the 4th-order BP ΔΣ modulator with scaling coefficients (k_1, k_2).

5.1 Single-Bit 4th-order BP ΔΣMs

5.1.1 Loop Filter

A block diagram of the 4th-order (2-stage) BP ΔΣ modulator is presented in Figure 5.1 with the loop coefficients a and b. The n_1 and n_2 determine the feedback loop delays. The resonators have only one feedforward delay because such structures can be implemented with one amplifier. The signal transfer function and quantization noise are given by

$$V(z) = \frac{z^{-2} \cdot U(z) + (1+z^{-2})^2 \cdot E(z)}{1 + 2z^{-2} + z^{-4} - az^{-(n_1+2)} - b\left(z^{-(n_2+1)} + z^{-(n_2+3)}\right)}, \tag{5.1}$$

where U is the z-transform of the input signal and E the z-transform of the ADC quantization noise. If we require the denominator to be ideally equal to one, then we have two possibilities for the coefficients and delays,

$$n_1 = 0; n_2 = 1; a = 1; b = 1 \tag{5.2}$$

or

$$n_1 = 2; n_2 = 1; a = -1; b = 2. \tag{5.3}$$

5.1.2 Two-Amplifier Circuit

The 4th-order BP ΔΣ modulator was implemented as a fully-differential switched capacitor circuit [1]. The block diagram of the implemented modulator is equivalent to that in Figure 5.1 (Equation (5.2)) and the corresponding circuit schematic is shown in Figure 5.2. The input sampling capacitances were set to 0.5pF and the same capacitors were shared in the feedback DAC in order to minimize kT/C noise. The reference voltage levels were selected as $\pm 0.7V$; hence the maximum differential input is $2.0V_{PP}$.

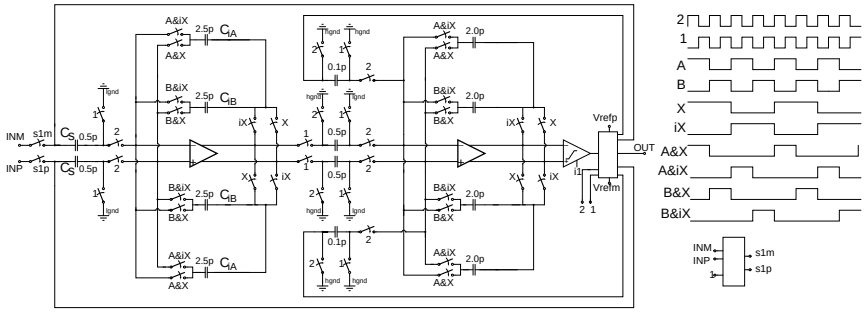


Figure 5.2 The implemented BP ΔΣ modulator (lgnd=1.1V and hgnd=1.8V).

The thermal noise of the input stage integrated over 270kHz was estimated to be over 90dB below the full-scale signal. The kT/C noise of the second stage is divided by the gain of the 1st stage and therefore the DAC capacitances of the 2nd stage were selected as 0.1pF so as to minimize the loading of the 1st stage.

The two resonators were implemented using Version I of the DD SC resonator structure introduced in Section 4.5.1. The internal signal swings at the output of the first resonator were scaled down by a factor of five, setting the integrating capacitances to 2.5pF. This is high enough with the V_{ref}/V_{dd} ratio of 0.23, which is depicted in Figure 5.3 (see also Section 2.4.2). The size of the integrating capacitors at the second resonator was optimized according to the load and the phase margin of the opamp, which led to 2.0pF capacitors. The scaling ratio is higher than needed to accommodate the signal swings but the small output swing is of no consequence, because of the 1-bit quantization.

5.1.2.1 Clock Signals and Switches

The resonator structure requires 8 non-overlapping clock signals and two extra clock signals to the bottom plate sampling. Furthermore, the inversions are needed to drive the CMOS switches. The non-overlapping clock signals '1' and '2' were generated with a conventional clock generator for SC circuits (Figure 5.4). The bottom plate sampling clocks were also obtained from the same circuit. The clock signals of $f_s/4$ were generated by dividing the full-speed clock by 4 using registers and, to ensure correct timing, they were triggered by the selected signal (dclk1) of the basic clock chain. The clocks have to be generated in such a way that the rising order of the clocks is (X; iX), (A&X; A&iX; B&X; B&iX) and finally (1;2). Naturally, the falling edges should be in the reverse order. The clock signals connected to the opamp input were generated by dividing the full-speed clock by two, after which the correct rise

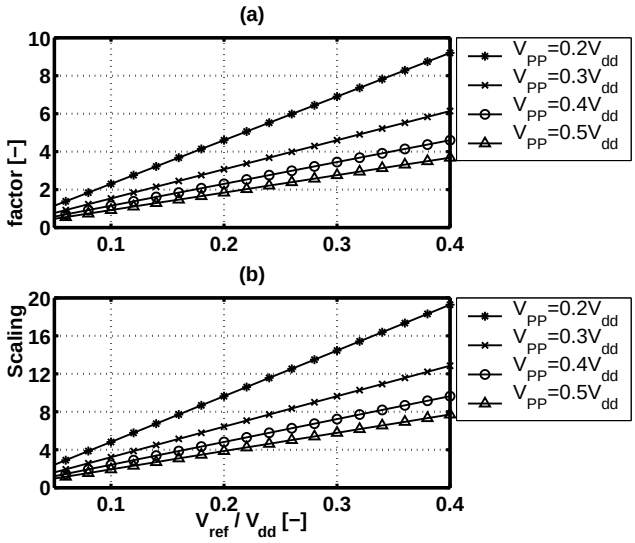


Figure 5.3 The required scaling factors of the signal swings (k_1, k_2) in the 1b 4th-order BP ΔΣM using the coefficients in Equation (5.2) (the maximum output peak-to-peak voltage of the opamp V_{PP} and V_{ref} as single-ended, a simulation with $f_{sig} = 0.502\,f_{Nyq}$@-3dBr). (a) First resonator. (b) Second resonator.

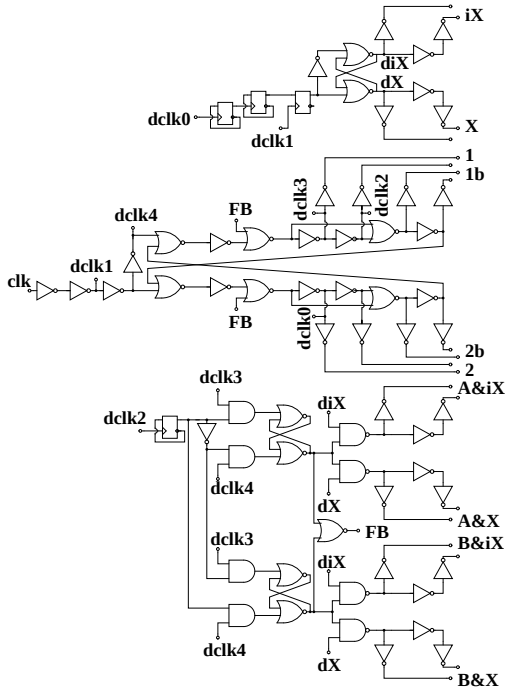


Figure 5.4 The simplified schematic of the clock circuit.

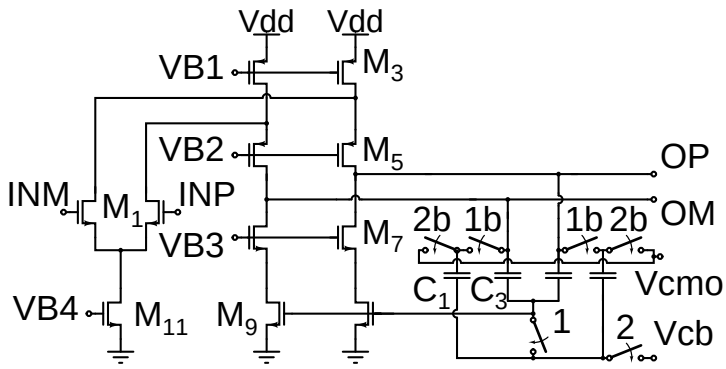


Figure 5.5 The CMOS folded-cascode OTA.

and falling times were formed using the clocks dclk3 and dclk4 from the basic clock chain, and finally the signals were gated with the X clocks. The feedback signal (FB) ensures that the feedback path of the opamp has been connected before any voltage is connected to the opamp input, because this would slow the settling. The FB signal is only an extra check and it does not have any effect on clock generation during normal operation.

The clock circuit uses a separate digital power supply. To ensure that the digital noise did not couple to the analog parts via clock signals, a separate power supply was used for the last inverters in the clock generator. These inverters also operate as buffers and are larger than the other cells.

In the IF sampling receiver a high-speed input signal (100MHz) has to be sampled without introducing too much distortion. However, the on-resistance of an nMOS switch at the input is signal-dependent, increasing the nonlinearity of the modulator. To keep the on-resistance of the input switches signal-independent, a bootstrap circuit similar to that in Figure 2.29 was used in the sampling stage.

The other switches at the modulator were implemented as CMOS switches. The switches driven by the X clock were larger than the others so as to reduce the time constant of the feedback.

5.1.2.2 Operational Amplifier, Comparator, and DAC

The operational amplifiers in the resonators were implemented using a folded-cascode topology (Figure 5.5 and Table 5.1). The amplifier has an nMOS input pair in order to increase the transconductance and, therefore, the drive capability of the amplifier. The nMOS differential pair has to be biased at a high input common-mode voltage but, on the other hand, a low common-mode level is required in the sampling stage.

Table 5.1 Component dimensions in the OTA.

Transistor	Dimensions
M_1	220/0.55
M_3	780/0.5
M_5	800/0.4
M_7	770/0.6
M_9	1800/1.3
M_{11}	700/2
C_1	0.2pF
C_3	0.4pF

Table 5.2 Simulated characteristics of OTA.

GBW	456MHz
SR	$370V/\mu s$
PM	62.5^o
A_{DC}	62.5dB
Output swing	$1.8V_{PPdiff}$
I_{supply}	9.4mA

Therefore, a low common-mode level of 1.1V was used at the modulator input in the sampling phase but in the integration phase the level was raised to 1.8V. The common-mode feedback was implemented by a switched-capacitor technique. The simulated performance of the designed OTA is summarized in Table 5.2.

The quantizer was implemented as a regenerative type comparator (Figure 5.6) followed by an SR flip-flop. After latching, the DC path between positive and negative power supply is switched off using the pMOS transistors M3 & M4.

The feedback voltages were generated using logic gates and switches (Figure 5.7). The output bit of the comparator is delayed using registers. The correctly delayed bit and the feedback clock signal drive the NAND gate and the output is used to control the feedback switches after buffering.

5.1.2.3 Experimental Results

The implemented chip was packed in a 44-pin CQFP, which was directly mounted on a 2-level PCB. The ground plane was divided into separate analog and digital parts. The simplified measurement arrangement is shown in Figure 5.8. Three separate supplies, analog, digital, and one for the clock buffers, were stabilized with 100nF surface mount capacitors, which were placed on the other side of the board immediately below the chip pins. 1μF capacitors were added on to the PCB further away from the chip.

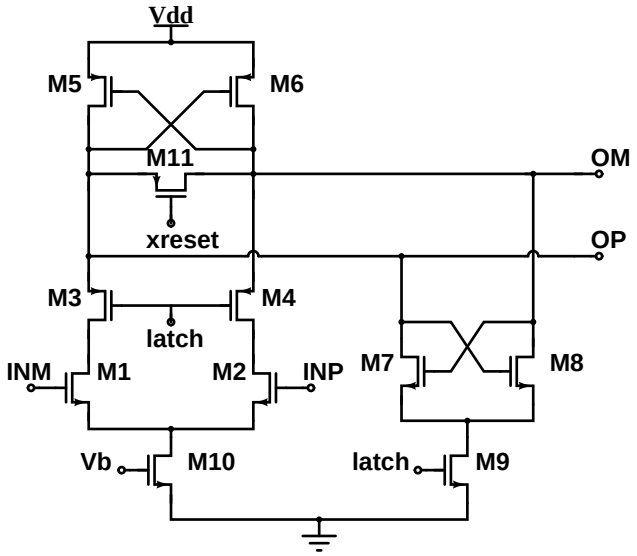


Figure 5.6 The regenerative comparator used.

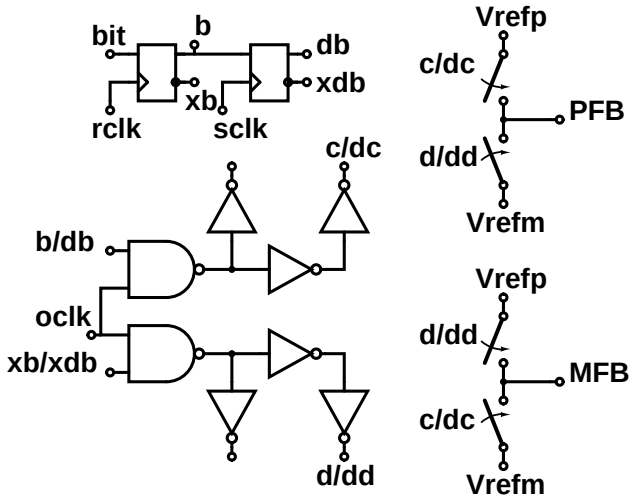


Figure 5.7 Generation of the feedback signals.

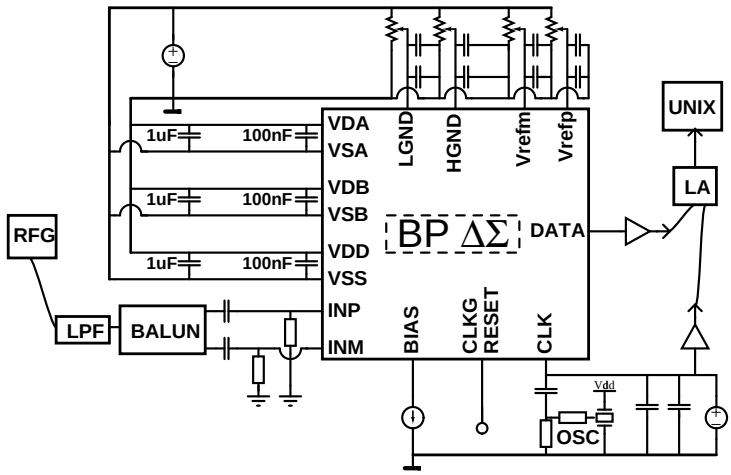


Figure 5.8 The measurement setup.

Reference voltages and ground levels were generated on the board with trimmers and stabilized in the same manner as the supplies.

The 80MHz clock was obtained from a crystal oscillator, which was placed on the external board. The 5V clock signal was resistively divided to a 2.5V peak-to-peak signal. The 100MHz input signal was generated using an RF signal generator (RFG) and low-pass filtered by a 150MHz passive LP filter before its conversion to differential form by means of a passive balun. The output signal was buffered on the board and the 1-bit data were collected with a logic analyzer (LA). A 65536-sample FFT was calculated from the windowed (Kaiser β=13) measurement data using MATLAB.

The measured output spectrum with a 100.03MHz input signal is shown in Figure 5.9a-d. In the resonator structure the clock signal is directly at the notch frequency and the feedthrough component can be seen 65dB below the signal level (Figure 5.9c). However, this feedthrough component is near-constant with all input signal levels (Figure 5.11) and will be transferred to DC in the down-sampling and can be almost entirely removed using digital DC calibration. The resonator has two integration paths and the mismatch between them causes an image signal, which is as low as 63dB below the signal in Figure 5.9c. The path mismatch can be caused by the ratio error between the integration capacitances and/or by the different on-times of the integration clocks. The very low image signal will cause only marginal I/Q mismatch and has no impact on the system performance. The third harmonic distortion component can also be observed in Figure 5.9c and it is 73dB below the signal level.

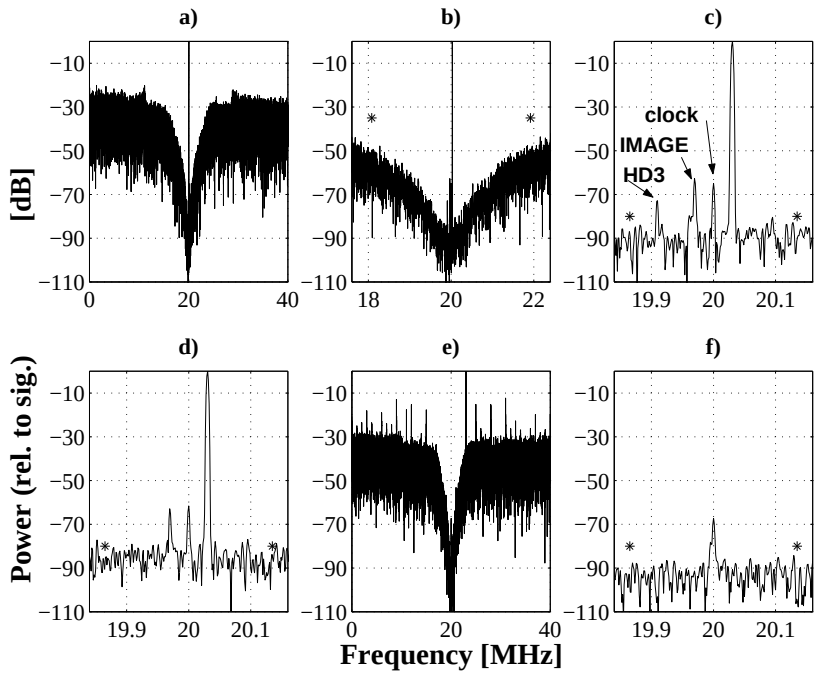


Figure 5.9 The measured frequency response of the modulator with 100.03MHz (a-c) -7.1dBr (d) -11.5dBr and (e-f) blocker test with 103MHz@-7.1dBr input signal ('*' f_{BW}=3.84MHz or 270kHz).

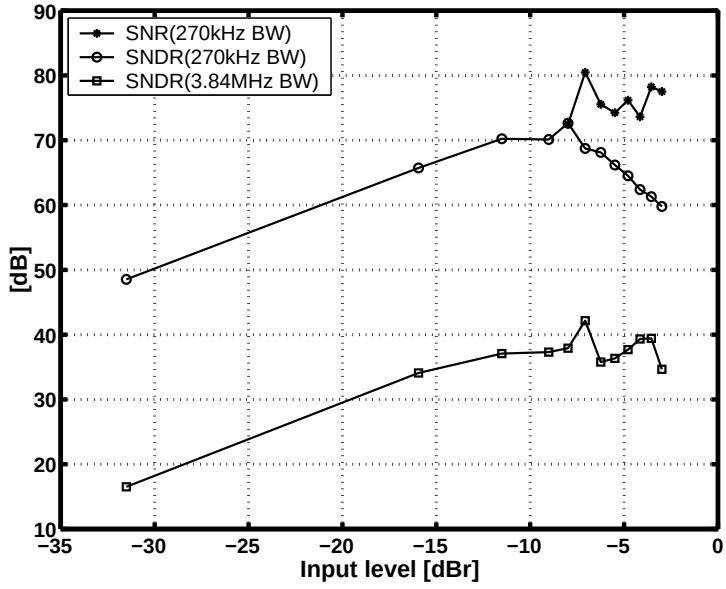


Figure 5.10 The measured SNR/SNDR curves with 100.03MHz input signal.

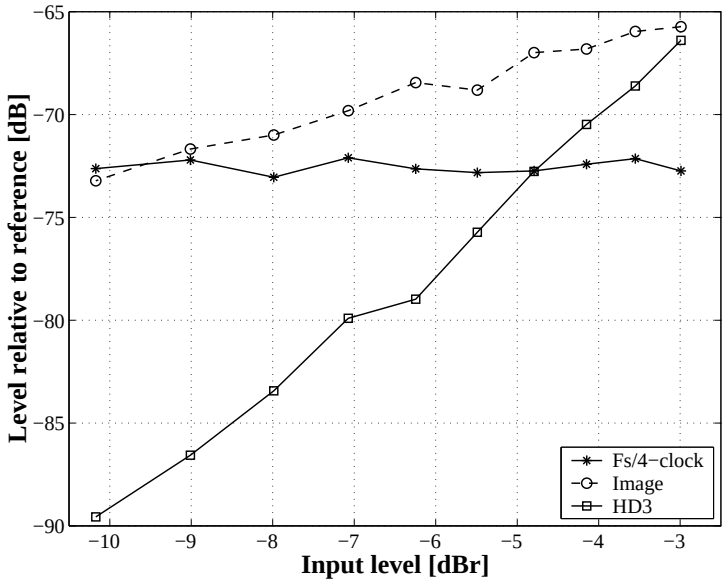


Figure 5.11 Levels of clock feedthrough and image component in the measurement of the SNR/SNDR curves together with the third harmonic.

The measured SNR and SNDR curves over a 270kHz(GSM) signal band are shown in Figure 5.10. The SNDR is calculated without the $f_s/4$ clock feedthrough and image components, because the former can be corrected digitally and the latter is sufficiently low as not to cause any performance degradation. The measured peak SNR and SNDR are 80dB and 72dB, respectively. The SNDR curve over a 3.84MHz (WCDMA) band is also plotted in Figure 5.10 and a peak value of 42dB, including all spectrum components, is achieved. The levels of $f_s/4$ clock feedthrough, image, and HD3 during the SNR measurement with higher input signals are shown in Figure 5.11.

The noise floor was about 10dB higher than expected and the degradation was probably due to clock jitter noise and/or coupling on the PCB. A dynamic range of 84dB was estimated with a 103MHz blocking test to eliminate the effect of the close-in phase noise of the signal generator (Figure 5.9e-f). The total noise can be separated into the quantization noise, the thermal noise ($\frac{kT}{C}$), the opamp noise, the clock jitter noise, and the disturbance/coupling noise on the PCB or on the chip. We may estimate the in-band noise of the different noise sources over the GSM bandwidth. We can calculate that the quantization noise power should be -106dB and the thermal noise power -102dB, normalized to references. According to the opamp simulation, the noise power of the first opamp is -113dB and hence insignificant. The crystal oscillator should have a timing jitter below 1.0ps. If we estimate the jitter noise power using a

Table 5.3 Performance summary.

Technology	0.35μm CMOS
Power Supply	3.0V
Power Consumption	56mW
Core Area	0.58sqmm
OSR	148 / 10
Signal Frequency	100MHz
Sampling Frequency	80MHz
Bandwidth	270kHz / 3.84MHz
SFDR	62dB
Peak SNDR	72dB / 42dB
Peak SNR	80dB / 42dB
IIP3[1)]	+30dBV
Dynamic Range	84dB / 46dB
Image rejection	62dB
Clock feedthrough level	-72dBr

[1)] calculated from HD3

100MHz signal frequency and a timing jitter standard deviation of 0.5ps or 1.0ps, the corresponding noise powers are -97dB and -91dB. These results are very close to the measured noise floor in Figure 5.9f when the signal level of -7.1dBr is considered and hence the clock jitter noise can be a limiting factor in the noise floor. On the other hand, the noise floor rises when an in-band signal frequency is used (Figure 5.9c) and this can be caused by the coupling mechanisms or by impurities in the input signal. Hence the coupling and disturbance noise, rather than the timing jitter, are probably what limits the measured maximum SNR. This was ascertained by using 20MHz and 60MHz input signals, which do not lead to better maximum SNRs.

The measured total power dissipation was 56mW, of which 85% was consumed by the opamps. A microphotograph of the circuit is shown in Figure 5.12 and the performance is summarized in Table 5.3.

5.1.3 Single-Amplifier Circuit

As mentioned earlier in Section 4.5.2, the same opamp can be shared between two resonators, which means that it is possible to realize a 4th-order BP $\Delta\Sigma$ modulator with only one opamp (Figure 5.13) [2]. The only consequence of sharing the opamp between the resonators is that the sampling capacitors of the second resonator have to be separate for the A and B signal branches. The generation of the clock signals is not more complicated than in the two-opamp implementation. A disadvantage is the bottom plate parasitics of the integration capacitors and switch parasitics, which

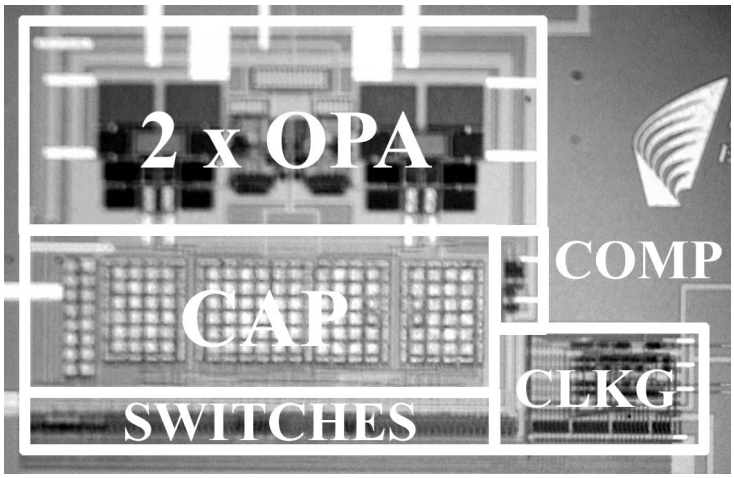


Figure 5.12 A chip microphotograph.

load the opamp. The sampling capacitors of the second resonator load the amplifier during the integration phase, unlike in the original structure in Figure 5.2, but this is not a problem when signal scaling ratios are not much over 10 (C_i/C_s-ratio). In the structure, the memory effect of the opamp input and output parasitics has to be considered carefully.

The BP $\Delta\Sigma$ modulator was implemented as a fully-differential switched-capacitor circuit (Figure 5.13) and the corresponding block diagram is equivalent to that in Figure 5.1 (Equation (5.3)) [3]. The input sampling capacitances of the first stage were set to 0.6pF and the same capacitors were shared in the feedback DAC so as to minimize kT/C noise. The reference voltage levels were selected as $\pm 0.9V$; hence, the maximum differential input is $2.5V_{PP}$. The kT/C noise of the second resonator is divided by the gain of the first resonator and therefore the DAC capacitances of the second resonator were selected as 0.2pF so as to minimize the loading of the first resonator.

The signal level scaling requirements of the first stage are quite similar to those shown in Figure 5.3, but the signal swings of the second resonator are roughly halved as a result of the coefficients selected. The selection of the coefficients in Equation (5.3) reduces the capacitive load of the first (and the second) opamp compared to the second alternative (Equation (5.2)) because, in both cases, the DAC capacitances of the second resonator are fixed by noise issues or technology constraints and now the sampling capacitance of the second stage can be halved (b=2). By increasing the integration capacitances the signal swings are scaled down by a factor of 5.5 and 11 at the outputs of the first and second resonator, respectively. The signal scaling factor

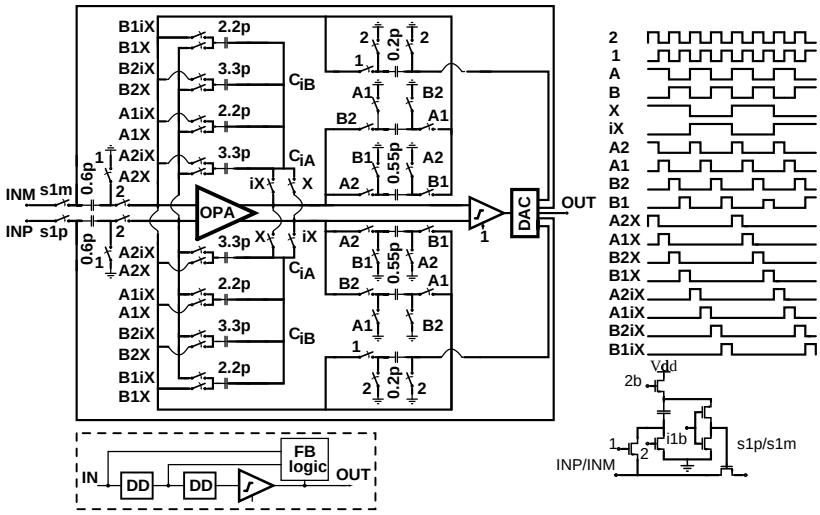


Figure 5.13 A single-opamp 4th-order BP ΔΣM.

Table 5.4 Component dimensions in the OTA.

Transistor	Dimensions
M_1	500/0.55
M_3	500/0.5
M_5	500/0.35
M_7	300/0.6
M_9	1300/1.3
M_{11}	480/2
C_1	0.2pF
C_3	0.4pF

of the second resonator is again optimized according to the phase margin and settling time constant of the opamp and is higher than needed for signal scaling.

5.1.3.1 Circuit Blocks

The resonator structure requires several clock signals (Figure 5.13) and they are generated in quite a similar way, as shown in Figure 5.4. The switches connected to the ground terminal are implemented as nMOS and the others as CMOS switches.

The operational amplifier in the resonators is implemented using a folded-cascode topology (Figure 5.5) with the component values shown in Table 5.4. The simulated GBW, DC gain, and phase margin are 430MHz, 61dB, and 61°, respectively. The comparator in Figure 5.6 is used in the 1b quantizer.

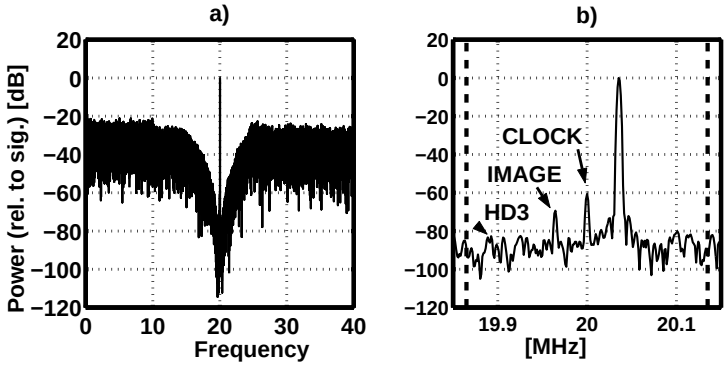


Figure 5.14 The measured output spectrum with a 59.965MHz -8.4dBr input signal (dashed line GSM BW).

5.1.3.2 Experimental Results

The test setup was similar to that depicted in the previous section. In these measurements a 60MHz input signal was used and it was low-pass filtered by a 100MHz passive LP filter. The measured output spectrum of the 1b 4th-order BP $\Delta\Sigma$ modulator is shown in Figures 5.14a and b. The image signal is 69dB and the third harmonic 83dB below the signal level, respectively (Figure 5.14b). The $\Delta\Sigma$ modulator has clock signals at a frequency of $f_s/4$=20MHz and the clock feedthrough component is 61dB below the signal level (Figure 5.14b).

From Figure 5.14 we may see that the quantization noise does not limit the noise floor. Instead, the resolution is limited by the clock jitter. This was ascertained by lowering the input frequency from 60MHz to 20MHz, which clearly decreased the noise at the notch frequency (about 5dB). The measured peak SNRs over GSM BW were 85, 80, and 75dB using 20, 60, and 100MHz IF and out-off band input signals, respectively. A further noise floor about 5dB lower was measured using a 40MHz sampling frequency and 10MHz input signal. These results indicate a standard deviation of the timing jitter over three picoseconds, which cannot be dominated by the crystal oscillator. On the other hand the jitter noise was not sensitive to the crystal oscillator used and therefore the clock noise has to be generated in the internal clock circuit. This may be reduced by adding more digital supply pins or by using the input clock signal for the sampling directly after buffering [4]. However, a high dynamic range (86dB) and SNDR (78dB) were achieved over the GSM bandwidth (270kHz) using a 60MHz input signal. More results, the SNDR curve, and a chip micrograph, are presented, together with the results of the cascaded structures, in the next section.

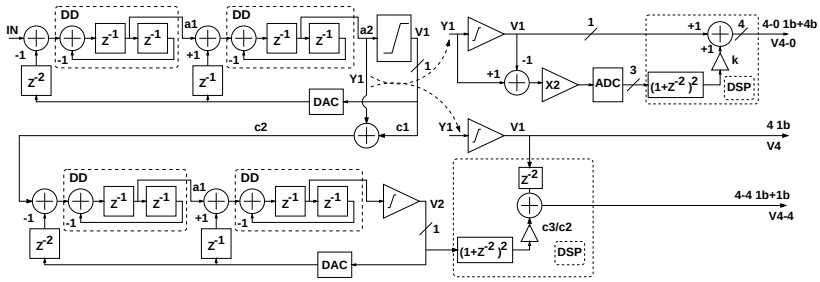


Figure 5.15 The architectures of the BP ΔΣ modulators.

5.2 Cascaded BP ΔΣMs

One way to improve the resolution of the ΔΣM is to utilize cascade architectures. In the following sections two cascade topologies (4-0 and 4-4) providing different levels of SQNR improvement are studied as a way to add multi-mode functionality to the 4th-order BP ΔΣM presented in the last section (Figure 5.15). In both circuits a single-opamp 4th-order BP ΔΣM is used as a design block.

5.2.1 4-0 BP ΔΣM

One implemented prototype was a 4-0 cascade structure in which the output signal of the first 4th-order stage was quantized by 4b resolution and processed by a post DSP but only 1b was connected to the feedback. The architecture can be expected to lead to the same resolution as a pure 3b structure [5] and therefore it is especially suitable for WCDMA/cdma2000.

In the block diagram (Figure 5.15) the terms a_1 and a_2 are the gains of the resonators and k a multiplier in the DSP. In the loop an internal resolution of 1b was used and therefore the gain over the comparator is not fixed. For the analysis we may use a linearized model for the quantizer and assume that the gain is $1/(a_1a_2)$ and, if we mark the ratio of voltage references in the 4b ADC and in the ΔΣM by r, we have, for the 4-0 structure,

$$V_{4-0}(z) = z^{-2}U(z) + (1+z^{-2})^2\left(\left(1-\frac{2k}{r}a_1a_2\right)E_1(z) + kE_q(z)\right), \qquad (5.4)$$

where U is the z-transform of the input signal, E_1 is the z-transform of the 1b, and E_q that of the 4b ADC quantization noise. If we require the 1b quantization noise to be

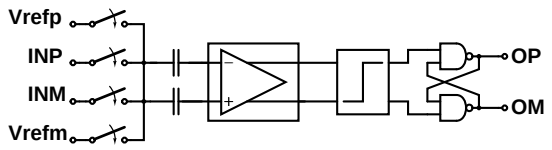


Figure 5.16 Principle of the comparators in the 3b ADC.

canceled ($k = r/(2a_1a_2)$), we obtain

$$V_{4-0}(z) = z^{-2}U(z) + k(1+z^{-2})^2 E_q(z). \tag{5.5}$$

Hence, ideally the output signal includes only the quantization noise of the 4b ADC shaped by the 4th-order transfer function and multiplied by the term k. The resolution achieved can decrease as a result of mismatches between the analog and digital transfer functions and/or a leakage of the multiplier in the ADC. The ADC is implemented in two stages (1b+3b) in order to decrease the loading of the ΔΣM (Figure 5.15). The output of the multiplier DAC (MDAC) performing the required MSB subtraction is sampled to the input capacitors of the 3b flash ADC (Figure 5.16). The flash ADC includes pre-amplifiers followed by analog and digital latches. The digital signal post-processing of the ADC output is realized in MATLAB.

In theory, the structure is capable of decreasing the quantization noise by 3 bits. However, the output of the ADC has to be multiplied by the term k (Equation (5.5)), thus amplifying its quantization noise. In order to retain some of the advantage, different reference voltages (r=±0.25V/±0.9V) are used in the ADC and DAC, which lead to an eventual reduction of 13dB in the quantization noise power compared to 1-bit quantization in the pure 4th-order structure.

5.2.2 4-4 BP ΔΣM

The 8th-order loop filter is realized by cascading two single-opamp 4th-order BP ΔΣM circuits. In the block diagram (Figure 5.15) the term c_2 is the scaling factor of the 2nd-stage input. If we require the 1st-stage quantization noise shaped by the 4th-order transfer function to be canceled ($a_2 = 1$), we obtain

$$c_1 = a_1 = \frac{1}{c_3} = \frac{1}{2} \tag{5.6}$$

and we have

$$V_{4-4}(z) = z^{-4}U_1(z) + \frac{c_3}{c_2}(1+z^{-2})^4 E_2(z). \tag{5.7}$$

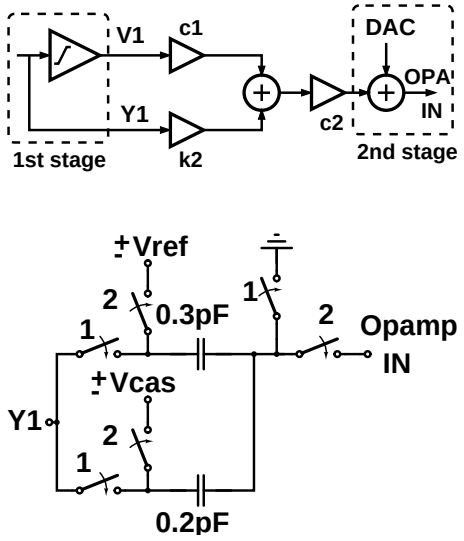


Figure 5.17 The implementation (single-ended) of the combined summing and input circuit in the 2nd stage of the 8th-order BP ΔΣM.

Hence, ideally the output signal includes only the quantization noise of the 2nd stage shaped by the 8th-order transfer function and multiplied by the term c_3/c_2.

At the input of the 2nd cascading stage, the analog (Y1) and digital output signal (V1) of the 1st stage have to be summed and scaled down by the term c_2 to accommodate the result into the input range of the 2nd stage (Figure 5.15). The block diagram and the simplified circuit of the input stage are shown in Figure 5.17. The chosen parameters are

$$\begin{cases} c_1 = 0.5 \\ k_2 = \frac{1}{a_2} = \frac{2.2pF}{0.2pF} = 11 \\ c_2 = \frac{1}{6.6} = 0.15 \\ \pm V_{cas} = \pm c_1 c_2 \frac{0.3pF}{0.2pF} V_{ref} = \pm 0.1 V_{ref} \end{cases}, \tag{5.8}$$

where k_2 is the output swing scaling factor of the second resonator in the 1st stage. The input sampling capacitances of the 2nd stage were set to 0.5pF and part (0.3pF) of the capacitance was shared in the feedback DAC (Figure 5.17). The integration capacitances of the first resonator in the 2nd stage were scaled down from 3.3pF to 1.65pF, respectively. The other capacitors in the 2nd stage are similar to those in the 1st stage (Figure 5.13). The DSP required for the post-processing of the 2nd-stage output and to combine the outputs from different stages is realized in MATLAB.

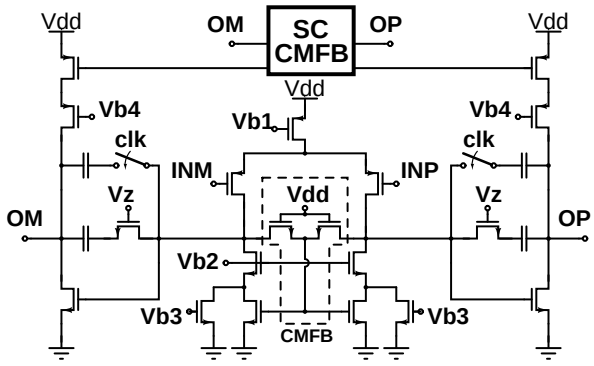


Figure 5.18 The Miller-compensated opamp with alternating C_c.

5.2.3 Circuit Blocks

Most of the circuit blocks were introduced in the previous section. The current of the 1st-stage opamp in the 4-4 cascaded structure is reduced by 20% compared to the 4th-order structure and the current of the 2nd stage by a further 12%.

The amplifier in the MDAC was implemented using a Miller-compensated opamp (Figure 5.18)[1]. Because the load of the opamp is very different during the sampling and multiplication phases, the size of the compensation capacitor is replaceable between phases. A pMOS input pair is used and hence a lower common-mode level of 1.1V can be used at the input and output.

5.2.4 Experimental Results

The prototypes were implemented as two different circuits on the same chip, a 1b 4th-order BP ΔΣM including a 4b quantizer [3] and a 1b 8th-order BP ΔΣM [6]. The implemented chip was packed in a 44-pin CQFP and a similar measurement setup to that used to achieve the earlier measurements was used.

The measured output spectrum of the 1b 8th-order BP ΔΣ modulator (4-4 cascade) is shown in Figures 5.19a-d. The image signal is 45dB and the third harmonic 75dB below the signal level, respectively (Figure 5.19d). The measured image level is 24dB higher than in the 4th-order structure but still adequately low. Instead, the measured clock feedthrough component is lower and hardly visible 78dB below the signal level in Figures 5.19b and c. The second-stage input level was scaled down by the term 6.6 (Equation (5.8)) when a scaling factor of 3 would be high enough to ensure the proper function of the 2nd stage. Hence, the measured SNDRs would be about 3.5dB better

[1] Designed by Jarkko Jussila and Lauri Sumanen

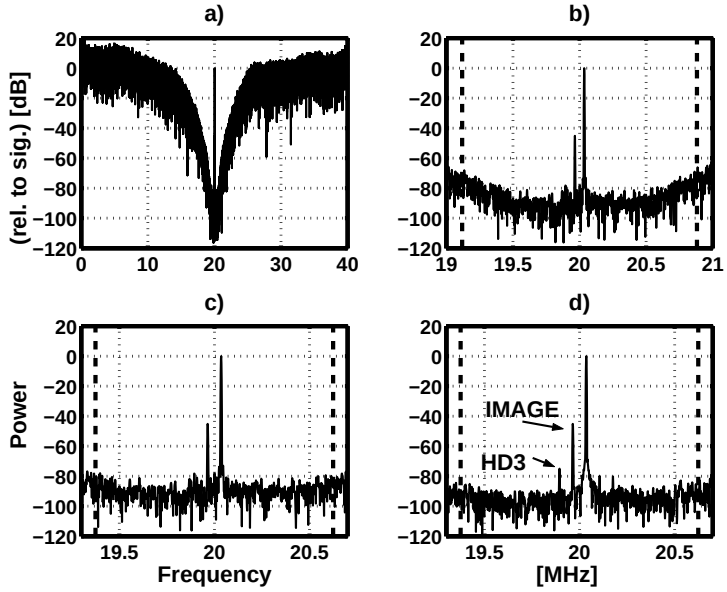


Figure 5.19 a,b,c) The measured output spectrum with 59.965MHz -12.3dBr and d) -5.2dBr input signal (dashed line b: DECT BW; c,d: IS-95 BW).

over the DECT and WCDMA bandwidths with the correct scaling factor.

The measured output spectrum of the 1b/4b 4th-order BP ΔΣM (4-0 cascade) is shown in Figures 5.20a and b. The image signal is 61dB, the third harmonic 65dB, and the $f_s/4$ clock component 70dB below the signal level, respectively. The measured image level is 8dB higher and the $f_s/4$ clock level 9dB lower than those measured with the 1b structure. The noise floor at the notch frequency clearly rises compared to the other structures. This is probably due to the increased substrate and/or supply noise, which can be explained by the high-speed MDAC, the comparators, and the 4b output buffers. However, the quantization noise at the band edges limits the performance over the CDMA bandwidth (3.84MHz).

The 4-0 structure was found to be the most suitable for the WCDMA/cdma2000 bandwidth (3.84MHz) and the 4-4 cascade structure for the IS-95 (1.25MHz) and DECT (1.762MHz) bandwidths. The 8th-order BP ΔΣM is over-designed for the GSM bandwidth (270kHz) and hence the pure 1b 4th-order ΔΣM is the best choice for the GSM. The SNDR curves measured using the most suitable structure for different OSRs (bandwidths) are shown in Figure 5.21. The SNDR is calculated without $f_s/4$ clock feedthrough and image, because the former can be corrected digitally and the latter is too low to cause performance degradation. The SNDR achieved is almost the same over the GSM BW, using 4th-order, and over the IS-95 BW, using 8th-order

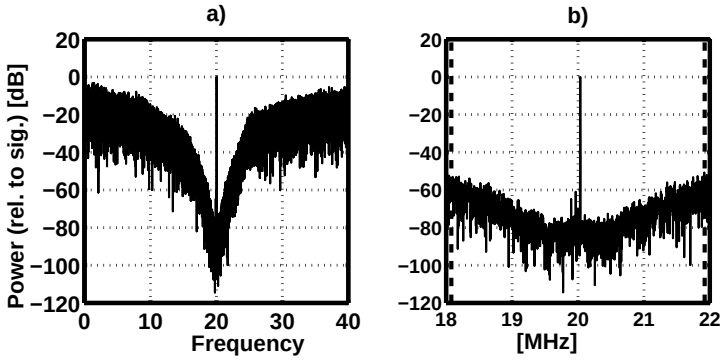


Figure 5.20 The measured output spectrum with 59.965MHz -9.3dBr input signal (dashed line CDMA BW).

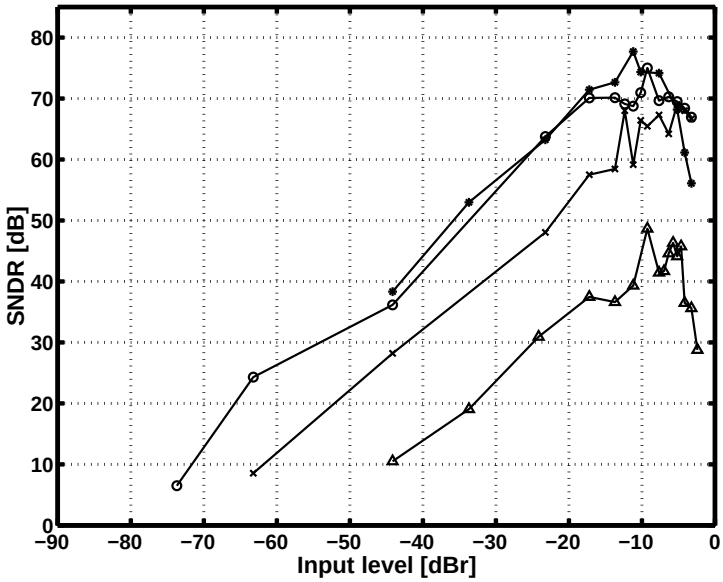


Figure 5.21 Measured SNDR curves over different bandwidths ('*'=GSM, 'o'=IS-95, 'x'=DECT, 'Δ'=CDMA).

Table 5.5 The performance summary.

Standard	GSM	IS-95	DECT	CDMA
Technology		$0.35\mu m$ CMOS		
Power Supply [V]		3.0		
Power Consumption [mW]	24	37	37	38
Core Area [sqmm]	0.52	1.0	1.0	0.79
(-“- one circuit [sqmm]		˜1.27)		
Bandwidth [MHz]	0.27	1.25	1.762	3.84
OSR [-]	148	32	23	10
BP ΔΣM order [-]	4	8	8	4
quantizer / feedback [bit/bit]	1/1	1/1	1/1	4/1
Signal Frequency [MHz]		60		
Sampling Frequency [MHz]		80		
Peak SNDR [dB]	78	75	69	48
Peak SNR [dB]	80	75	70	48
IIP3[1)] [dBV]	+30	+30	+30	-
Dynamic Range [dB]	86	82	72	50
Image rejection [dB]	70	45	45	61
Clock feedthrough level [dBr]	-69	-82	-82	-77

[1)] calculated from HD3

quantization noise shaping. Over the DECT BW and CDMA BW the quantization noise limits the resolutions achieved. Over the CDMA BW, the measured maximum and average improvement of the 4b ADC compared to the 1b quantizer are 12dB and 6dB, respectively. However, the peak SNDRs differ by only 2dB and the SNDR/power ratio of the 4-0 structure was much lower than expected. The main reason is probably the mismatch between the 1b ΔΣM loop filter and the digital filter.

The performance in the different standards using the best implementation based on the single-opamp BP ΔΣM structure is summarized in Table 5.5. In the 4-0 structure the DSP accumulates the errors between paths, lowering the image rejection a little. The lower image rejection in the cascaded structure can be explained by the doubled two-path structure and by the higher loading of the clock generator, which possibly causes more mismatch between the signal paths. The clock feedthrough level was found to be sensitive to the PCB and different levels were measured. It is possible that the clock feedthroughs of the 1st and 2nd stages in the cascaded structure partly cancel each other, leading to a very low clock feedthrough level. However, the measured clock component was always quite constant in different measurements, which means that it can be removed using a digital DC calibration after a digital down-conversion. A micrograph of the chip is shown in Figure 5.22.

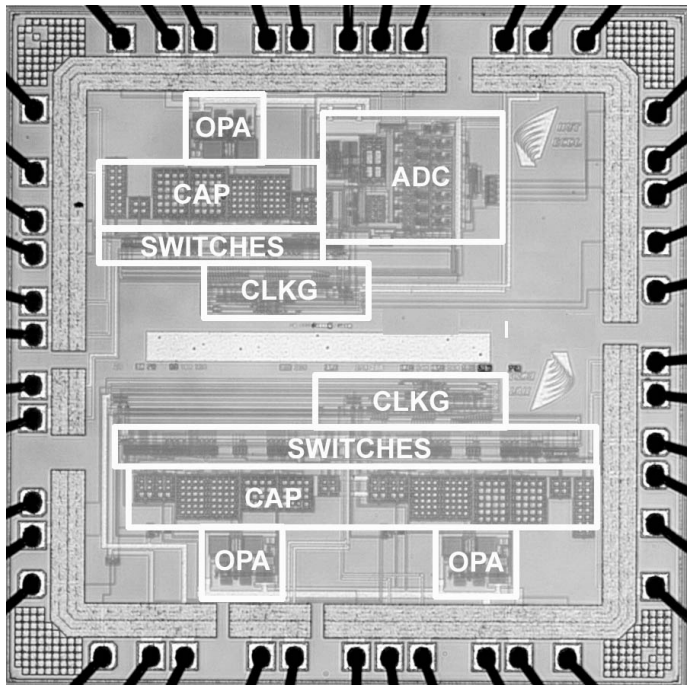


Figure 5.22 A micrograph of the chip (upper part the 1b/4b 4th-order and lower part the 1b 8th-order BP ΔΣM).

5.3 Multi-Bit BP ΔΣM

In theory, a multi-bit BP ΔΣM achieves the same resolution with a lower sampling frequency as a pure single-bit structure. However, in a digital IF receiver a high sampling frequency has to be selected because of the clock jitter and IF filtering. This can lead to unnecessarily high power dissipation in the BP ΔΣM, and a solution to the problem is to utilize a BP decimation sampler (see Section 3.3) to decrease the sampling frequency of the BP ΔΣM without tightening the system specifications. In this section an implementation of the analog DT BP decimation filter, which makes possible a lower BP ΔΣ-modulator clock frequency, is presented [7]. The designed decimator is combined with a 2b/4b 4th-order double-sampling BP ΔΣ modulator targeted for an IF receiver. The circuit can be used in an IF receiver to combine frequency down-conversion with analog-to-digital conversion by directly sampling an input signal from an intermediate frequency of 90MHz to a digital intermediate frequency of 10MHz.

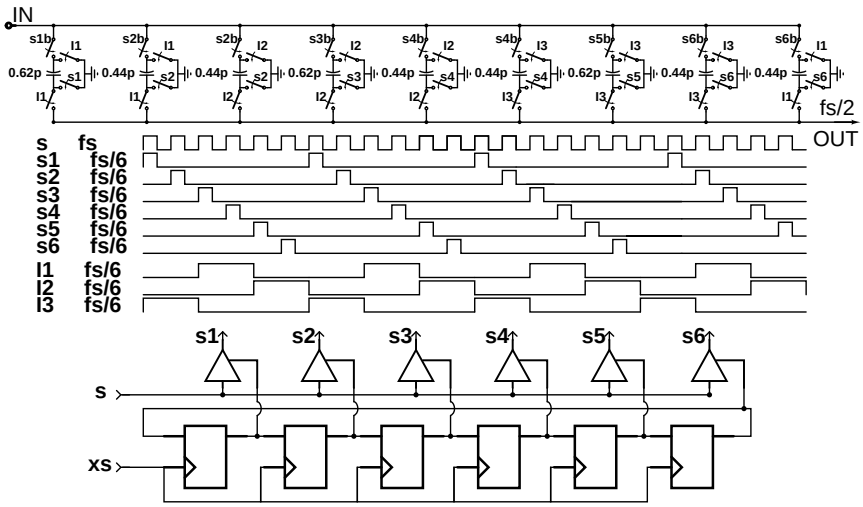


Figure 5.23 BP decimation sampler with N=2 for double-sampling $\pi/2$ BP $\Delta\Sigma$Ms.

5.3.1 BP Decimation Sampler

BP decimation by two (Figure 3.14) can be implemented by the SC network depicted in Figure 5.23. Six separate sampling clocks are needed, because three samples are switched to the output concurrently. The input is sampled alternately either to two 0.44pF capacitors or to one 0.62pF capacitor to store the batch of input samples required for each output sample. Three output clock signals at the $f_s/6$ frequency select the correct capacitor batch and generate an output data rate of $f_s/2$. Because the decimator is followed by a double-sampling circuit, the output has to be in the hold phase all the time. The input switches are implemented using nMOS transistors and they are driven by a bootstrap circuit (Figure 5.24). The structure is quite similar to those in earlier implementations but now the same capacitor (C_1) is used to drive all 9 gates of the input switches. The basic clock signals of the decimation sampler are generated by a conventional clock generator, which operates with a full sampling frequency (using the principle shown in Figure 2.25). The clock signals s_1-s_6 and their delayed equivalents for the bottom plate sampling are generated by delay chains, as shown in Figure 5.23. The output clock signals (I_1-I_3) at the $f_s/6$ frequency are generated using suitable clock signals from the full-speed clock chain of the decimator and from the other clock generator used to produce the basic clock signals for the BP $\Delta\Sigma$ modulator. These clock signals are at a frequency of $f_s/4$ and hence their on-time is suitable for I_1-I_3. A suitable clock signal at the $f_s/4$ frequency is selected using SR flip-flops, different logic gates, and CMOS switches to produce clock signals (I_1-I_3) at the $f_s/6$

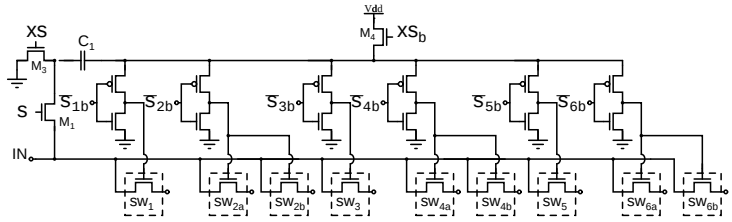


Figure 5.24 Driving arrangement of the nMOS input switches in the BP decimation sampler.

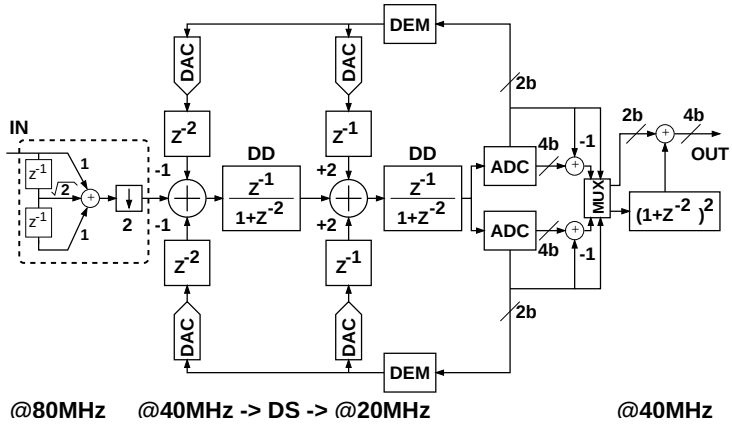


Figure 5.25 A block diagram of the implemented 2b/4b BP ΔΣM.

frequency with a duty cycle of 1/3.

5.3.2 2b/4b 4th-order Double-Sampling BP ΔΣM

The combined signal down-conversion and A/D conversion stage for a digital IF receiver is shown in Figure 5.25. The IF_1 signal is sampled by an 80MHz sampling frequency and the decimation stage drops the sampling frequency to 40MHz without tightening the antialias filtering and clock jitter specifications. The ADC is realized with a 40MHz 4th-order $f_s/4$ double-sampling BP ΔΣ modulator, which operates at 20MHz because of the two-path structure. The resolution of the internal ADC is 4b but only 2b are connected to the feedback, or the architecture can be called a 4-0 cascade. Two ADCs are used to implement the separate signal paths of the DS structure. The two-bit DACs load the amplifiers less than a 3b-4b feedback DAC and make easier to realize a linearized DAC.

The simplified circuit schematic of the designed BP ΔΣ modulator is shown in Figure 5.26. The resonators in the ΔΣ modulator loop filter were implemented using the double-delay double-sampling SC resonator structure or Version III presented in

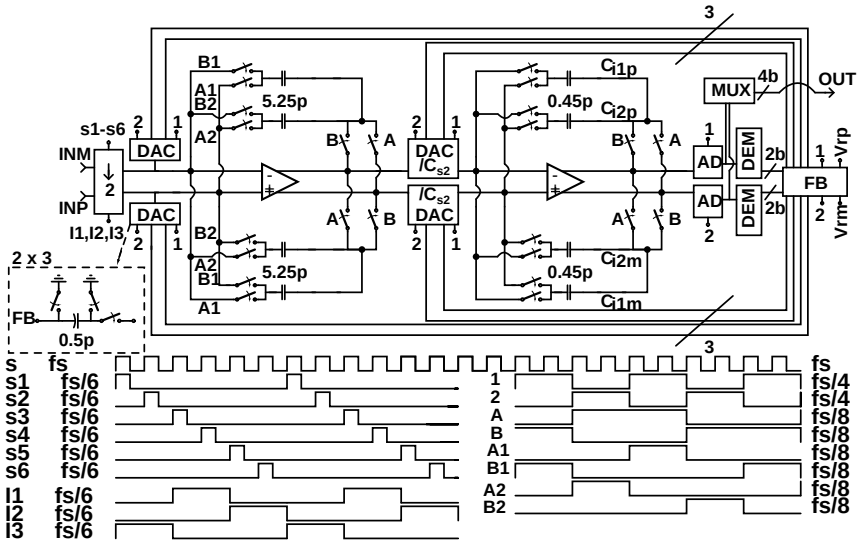


Figure 5.26 A simplified schematic of the implemented BP ΔΣM.

Section 4.5.3 and the amplifier was designed using the telescopic OTA topology depicted in Figure 5.27. This topology was selected to minimize the power dissipation of the opamps. The input pair were implemented using pMOS transistors, even though nMOS transistors would have an inherently larger transconductance. This way two analog ground levels are needed, a higher one for the opamp input (V_{cmi}) and a lower one for the output (V_{cmo}), which can also be used in the input sampling stage of the ΔΣ modulator. If a nMOS input pair is adopted, both ground levels in the opamp are over a mid-supply and a third ground level would be required for the input sampling because of the nMOS switches. On the other hand, the SR requirements set a lower limit for the opamp bias current, regardless of the input devices used, and speed requirements at the operating frequency of 20MHz are also easily met with pMOS transistors. The component values and ground levels used are listed in Table 5.6 and the simulated properties of the opamp are shown in Figure 5.27.

The total input sampling capacitance is 1.5pF (in the decimator) and the 1st-stage DACs include three 0.5pF capacitors. The reference voltage levels are selected as $\pm 0.7V$; hence, the maximum differential input is $2V_{PP}$. The kT/C noise of the second resonator is divided by the gain of the first resonator and therefore the DAC capacitances of the second resonator are selected as 0.1pF and, furthermore, shared with the 2nd-stage sampling capacitors so as to minimize the loading of the resonators (Figure 5.28). The internal signal swings at opamp outputs are much lower in a multi-bit loop than in a single-bit loop (see Section 2.4.2). Hence, the signal swings at the output

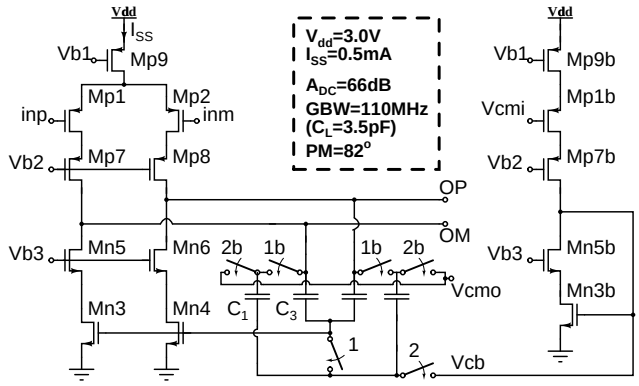


Figure 5.27 The telescopic OTA used.

Table 5.6 Component dimensions in the telescopic OTA (Figure 5.27).

Transistor	Dimensions	Transistor	Dimensions
M_{p1}	165/0.35	M_{p1b}	16.5/0.35
M_{n3}	110/0.7	M_{n3b}	11/0.7
M_{n5}	65/0.5	M_{n5b}	6.5/0.5
M_{p7}	125/0.35	M_{p7b}	12.5/0.35
M_{p9}	250/1.0	M_{p9b}	12.5/1.0
C_1	0.2pF	V_{cmi}	1.7V
C_3	0.4pF	V_{cmo}	1.0V

of the first resonator are scaled down only by a factor of 3.5, setting the integrating capacitances to 5.25pF. The down-scaling factor is about 2/3 of the values used earlier in single-bit circuits. Now, the gain of the second resonator has to be considered, too, and cannot be selected freely because the multi-bit ADC has a fixed gain. The gain of the second resonator was selected as 2/3 by using integration capacitances of 0.45pF. The nominal voltage references of the ADC are set to a third of the DAC references to realize the correct loop coefficients.

The clock signal generation of the decimation sampler was explained in the previous section. The clock signals for the BP $\Delta\Sigma$ modulator are generated using the same methods as in the earlier circuits but now the input clock signal for the cross-coupled clock generator is divided from the full-speed clock by four. Furthermore, the two separate clock generators are synchronized, using a control signal from the faster circuit to track the slower one (Figure 5.29). The switches connected to a lower ground level were implemented using nMOS transistors and the others using CMOS switches.

The 4b flash ADCs consist of similar blocks to those used earlier in a 3b flash (Figure 5.16). The ADCs are followed by dynamic element matching circuits which

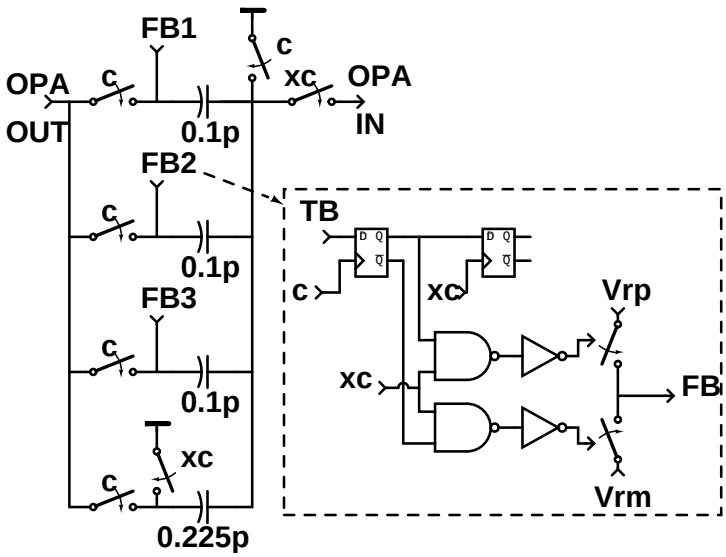


Figure 5.28 Combined sampling and DAC circuit of the second resonator (c=1 or 2, xc=2 or 1 and TB='a thermometer code bit').

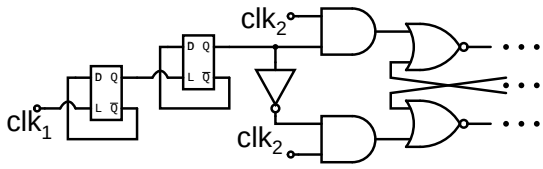


Figure 5.29 Synchronization principle between two clock generators (clk_1 and clk_2@80MHz from the other CLKG).

use a random selection dynamic element matching algorithm for the two MSBs before the DACs. The output is selected alternately from the two signal paths and the digital correction stage is realized in MATLAB.

5.3.3 Experimental Results

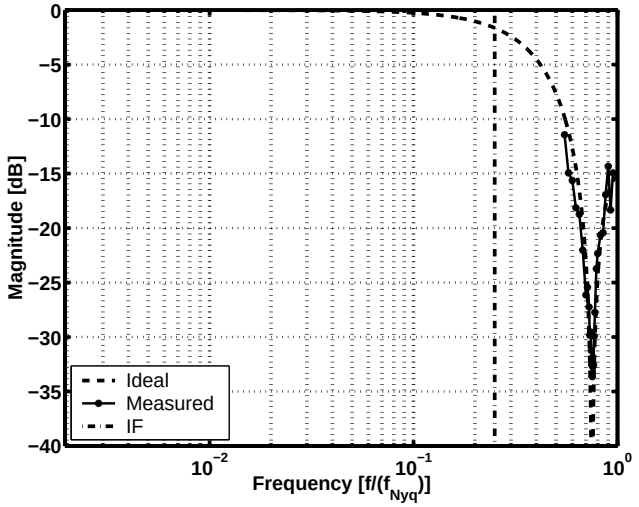
The implemented chip was packed in a 44-pin CQFP and in a 44-pin VFQFPN, which were directly mounted on separate 2-level PCBs. The results were mostly measured using the VFQFPN package and the measurement setup was similar to that used for the earlier measurements. A 90MHz input signal was low-pass filtered by a 100MHz LP filter and an 80MHz clock signal from a crystal oscillator was used as a reference signal for the RFG to reduce the phase noise of the input signal. A 32768 FFT was

performed for the 4b output data.

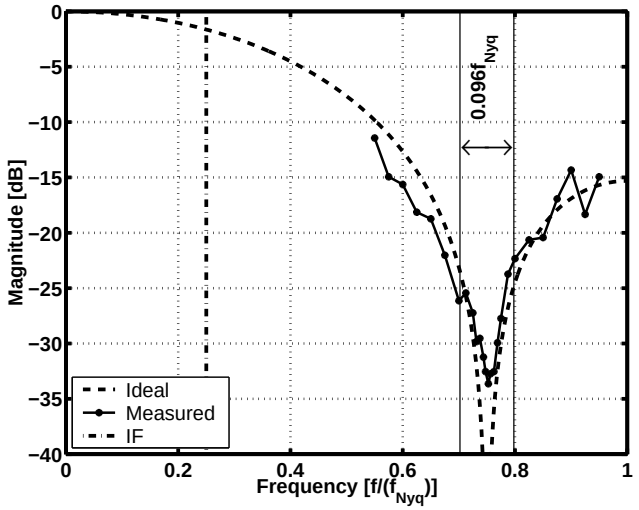
The decimator was measured using an input signal with a frequency offset of 35kHz from the IF_1 frequency of 90MHz and an interferer signal at the frequencies from 42-58MHz. The frequency response of the decimator is plotted in Figure 5.30 by comparing the signal and interferer level at the BP ΔΣM output. We can see that the measured frequency response is almost ideal and the attenuation achieved within the 3.84MHz bandwidth is over 22dB. Hence, the aliasing noise due to decimation by two does not tighten the passive IF filtering requirements. The possible interferer signals near the 30, 50, 110, and 130MHz frequencies, which alias over the GSM signal band, are attenuated over 32dB. Noise and interferers at frequencies around 110MHz are the main target when a 90MHz IF signal is adopted, because this frequency band is least attenuated by the IF filter.

The measured output spectrum of the 40MHz DS 2b/4b 4th-order BP ΔΣ modulator merged with the 80MHz BP decimation sampler is shown in Figures 5.31a-d. The third harmonic is 60dB below the signal level (Figure 5.31c), the image signal 52dB, and the clock feedthrough component 39dB below the signal level (Figure 5.31d). The noise floor is about 70dB below the signal level, which is roughly 20dB too high. The reason is probably the internal 4b flash ADC, which does not work correctly. There is quite a large DC component in the BP ΔΣ modulator loop, caused by the internal ADC, which wastes part of the loop dynamic range. Therefore, the ADC references have to be set in such a way that mainly only the LSBs of the 2b DAC are used and the loop operates poorly, like a single-bit structure. Because of this the internal signal swings at the outputs of the opamps increase and the opamp biasing point has to be tuned considerably from the nominal value. Hence, the characteristics of the opamps are altered, which degrades the performance of the resonators and again increases the noise floor. The measured SNDR curves are plotted in Figure 5.32 but the measurement results are 10-20dB worse than expected. The degradation is larger with high OSRs (˜20dB) than with lower OSRs (˜10dB). Because of the high noise floor, the operation of the RDA DEM cannot be measured, or its effect is not visible.

Still, the performance is listed in Table 5.7 and a microphotograph of the circuit is shown in Figure 5.33. The measured power dissipation is 22mW, of which 52% is consumed by the analog parts, 31% by the digital cells, and the remaining 17% by the clock buffers. The current of the ADC and opamps was roughly doubled from the nominal values used in the simulations and hence a target power dissipation of about 16mW was largely exceeded.



(a)



(b)

Figure 5.30 Measured frequency response of the BP decimation filter. Measured by comparing interference at frequencies of 42-58MHz to a signal at 90.035MHz, $f_s = 80MHz \Rightarrow 0.096\,f_{Nyq}$=3.84MHz (zeros at 30MHz, 50MHz etc. and IFs 10MHz, 70MHz, 90MHz etc.).

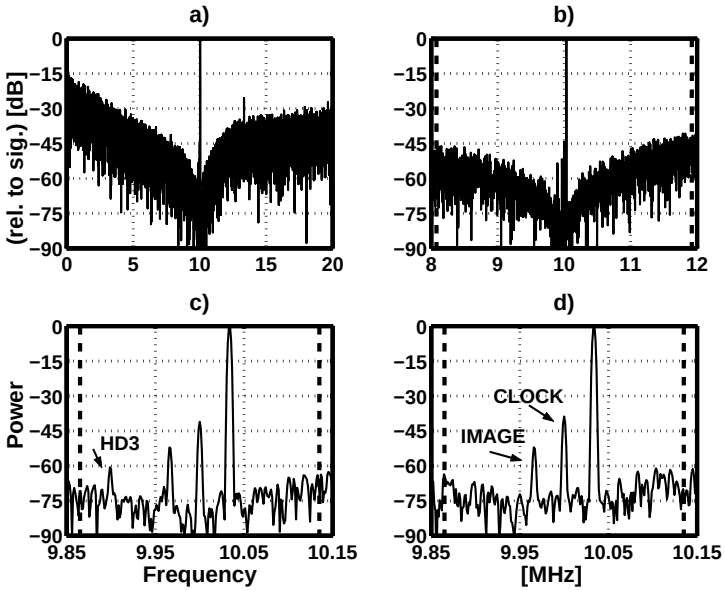


Figure 5.31 a,b) Measured output spectrum with 90.035MHz -2dBr, c) -5dBr and d) -7dBr input signal (dashed line b: WCDMA BW; c,d: GSM BW).

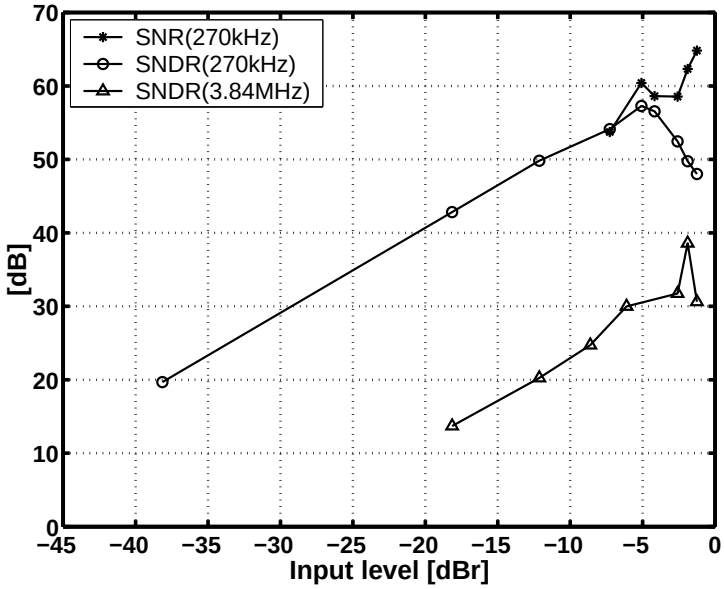


Figure 5.32 Measured SNR/SNDR curves over different bandwidths with a 90.035MHz input signal.

Table 5.7 Performance summary of the incomplete circuit.

Technology	0.35μm CMOS
Power Supply	3.0V
Power Consumption	22mW
Core Area	1.25sqmm
ADC / DAC	4b / 2b
OSR	74 / 5
Signal Frequency	90MHz
Sampling Frequency	80MHz
Operating frequency	20 / 40MHz
Bandwidth	270kHz / 3.84MHz
Peak SNDR	57dB / 38dB
Peak SNR	65dB / 38dB
Dynamic Range	60dB / 32dB
Image rejection	52dB
Clock feedthrough level	-46dBr

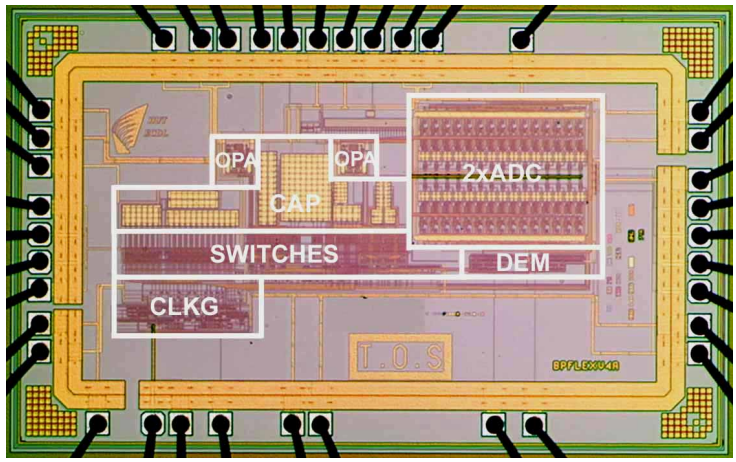


Figure 5.33 A chip microphotograph.

Table 5.8 Peak SNRs of the structures over different BWs (f_s=80MHz, a sinusoidal input signal offset 35kHz from IF).

Standard	**Bandwidth [MHz]**	**OSR [-]**	IF_1 **signal [MHz]**	**1b n=4**	**1b n=4**	**1b/4b n=4 (4-0)**	**1b n=8 (4-4)**	IF_1 **signal [MHz]**	**2b/4b n=4 (4-0)**
			Res. Ver.	I	II	II	II		III
			P. Dis.[mW]	56	24	38	37		
GSM	0.27	148	**SNR [dB]/**						[1]
			20	80	80	75	78	10	66
			60	80	80	71	78	70	63
			100	80	74	64	76	90	65
IS-95	1.25	32							
			20	63	63	68	76	10	47
			60	63	64	68	75	70	50
			100	63	59	62	75	90	46
DECT	1.762	23							
			20	56	58	62	70	10	48
			60	58	56	63	70	70	43
			100	56	56	60	70	90	42
WCDMA	3.84	10							
			20	39	40	55	41	10	35
			60	41	43	48	40	70	35
			100	42	38	48	42	90	38

[1] Decimation by two, $OSR' = OSR/2$ (incomplete performance).

5.4 Summary

The measurement results of the first circuit indicate a very high level of image rejection, even though the resonator employs two signal paths. Furthermore, the leakage component at $f_s/4$ is also low and independent of the signal, which means that it can be digitally corrected after the second down-conversion. The BP $\Delta\Sigma$ modulator provides a peak SNR of 80dB for 270kHz for an input signal sampled directly from 100MHz.

In the second circuit the power dissipation is reduced by 57%, compared to the first one, by using a single-opamp 4th-order BP $\Delta\Sigma$M structure and by careful circuit design. However, the clock jitter noise decreases the performance with high OSRs more than in the first circuit and a peak SNR of 80dB (GSM) is achieved for an input signal of 60MHz instead of 100MHz. It was found out that the clock jitter generated

in the internal clock circuit dominates the noise floor. The jitter may be reduced by adding more digital supply pins because the rather complicated clock generator, together with other digital gates on the chip, causes large peak currents.

Two cascade BP ΔΣ modulators were implemented to study the more effective quantization noise shaping with lower OSRs. One has 4b ADC combined with a single-opamp 4th-order BP ΔΣM. With the 4-0 architecture the highest benefit is achieved over a wide WCDMA bandwidth but with higher OSRs the resolution is low because the noise floor at the notch frequency rises compared to the pure 1b architecture. However, the overall performance with 38mW power dissipation is worse than expected. The main reason is probably the mismatch between the 1b ΔΣM loop filter and the digital filter. The other cascade architecture (4-4) consists of two single-opamp 4th-order BP ΔΣM stages. High dynamic ranges and SNDRs were achieved over the IS-95 (82dB/75dB) and DECT (72dB/69dB) bandwidths with 60MHz IF. The analog imperfections decrease the performance of the cascade BP ΔΣM and for WCDMA the OSR is so low that no improvement compared to the 4th-order is achieved by the higher-order loop filter. For GSM the cascade is over-designed, because the resolution with high OSRs is limited by the clock jitter.

A multi-mode mobile phone operating in the GSM, IS-95, cdma2000, and WCDMA systems would make possible a large covering area in both 2G and 3G networks. Operation in the DECT standard would increase usability at home, where the low-cost landline network is usable. If the implemented BP ΔΣMs are used in this kind of multi-mode digital IF receiver, the most power-efficient choice is to use the 1b 8th-order (4-4) BP ΔΣ modulator for the DECT and IS-95 modes. In the GSM and WCDMA modes the 2nd stage can be set to power-down, reducing the power dissipation by 35%. The low resolution in the WCDMA mode can be compensated with a passive IF filter.

The last implemented circuit indicates the potential of the BP decimation sampler to reduce the operating frequency of the BP ΔΣ modulator without affecting the system specifications. The 2b/4b BP ΔΣ modulator does not work as expected and hence the measured performance was much worse, and power dissipation larger, than simulated.

The SNRs achieved by different structures in all the standards mentioned earlier are collected in Table 5.8, even if the architectures have not been designed for using in each mode. However, the table shows how the OSR and frequency of the input signal affect the performance.

References

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[4] M. Waltari, L. Sumanen, T. Korhonen, K. Halonen, “A Self-Calibrated Pipeline ADC with 200MHz IF-Sampling Frontend,” Digest of International Solid State Circuits Conference, pp. 314-315, 2002. 124

[5] T. Leslie, B. Singh, “An improved Sigma-Delta Modulator Architecture,” IEEE International Symposium on Circuits and Systems, pp. 372-375, 1990. 125

[6] T. Salo, S. Lindfors, K. Halonen, “An 80MHz 8th-order Bandpass ΔΣ-Modulator with a 75dB SNDR for IS-95,” Custom Integrated Circuits Conference, pp. 179-182, May 2002. 128

[7] T. Salo, S. Lindfors, K. Halonen, “BP Decimation Filter for IF-Sampling Merged with BP ΔΣ-Modulator,” accepted to the IEEE International Symposium on Circuits and Systems (ISCAS’03), Bangkok, Thailand, 4 pages, May 2003. 132

Chapter 6

Benchmark

In this chapter, published ΔΣ modulators targeted at IF digitization are compared. A direct comparison of implemented BP ΔΣ modulators may not lead to an objective and faithful result but, nevertheless, it gives a rough estimate of circuit competence. There are several ways to compare ADCs and one is to calculate different figures of merit (FOMs) [1], which try simultaneously to observe a number of performance parameters (Section 2.1.4). A FOM is given by

$$FOM_1 = \frac{4kT \cdot DR \cdot BW}{P}, \tag{6.1}$$

where DR is the dynamic range (power as absolute value), BW the signal bandwidth [Hz], and P the power dissipation [W]. If the DR is replaced by the $SNDR$ (as absolute value) the linearity performance is also considered and we have

$$FOM_2 = \frac{4kT \cdot SNDR \cdot BW}{P}. \tag{6.2}$$

Equations (6.1) and (6.2) do not take into account technology, power supply, core area, image level, sampling frequency, or signal frequency, which can be important properties in some applications. For example, in a digital IF receiver the input signal (IF) frequency is of significant importance, as is the sampling frequency.

The first monolithic discrete-time BP ΔΣ modulator was published in May 1992 [2] [3] and the second BP ΔΣ modulator, a monolithic continuous-time architecture, a little later, in June 1992 [4] [5]. Since the year 1992 there have been several publications of BP ΔΣ modulators and the following sections aim to perform a comprehensive comparison of the circuits. First, an inspection is carried out for DT BP ΔΣ modulators which have been published in well-known journals or at conferences. After that,

Table 6.1 A comparison of 2nd-order DT BP ΔΣ modulators.

Reference	[6]	[7]	[8]	[9]	[10]	[11]
Year	2002	2001	1997	1996	1996	1995
Technology [μm CMOS]	0.18 / 0.35	0.35	0.5	1.2 Bi	0.8 Bi	0.8 Bi
Power Supply [V]	1.8 / 3.3	1.0	1.0	5	5	5
ADC / DAC [bits]	5 / 5	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
Resonator	BPF	BPF	LDI	DD	BPF (DD)	FE&LDI
Structure	1-stage	2-path	1-stage	1-stage	1-stage	1-stage
Power Consumption [mW]	75	12	0.24	30	350	60
Core Area [sqmm]	1.0	1.3	1.5	0.84	0.51	-
OSR	2058 / 93	107	45	107	125	107
Signal Frequency [MHz]	10.7	10.7	0.4	10.7	62.5	10.7
Sampling Frequency [MHz]	37.05	42.8	1.8	42.8	250	42.8
Bandwidth [MHz]	0.009 / 0.2	0.2	0.02	0.2	1.0	0.2
SFDR [dB]	-	42	-	-	-	-
Peak SNDR [dB]	80 / 67	42	-	-	-	-
Peak SNR [dB]	-	-	42	46	˜42	57
Dynamic Range [dB]	95 / 80	˜57	45	-	˜43	˜60
Image rejection [dB]	-	42	-	-	-	-
FOM_1 10^{-6}	6.1 / 4.3	0.135	0.04	-	0.0009	0.054
FOM_2 10^{-6}	0.2 / 0.2	0.004	< 0.02	<0.004	< 0.0007	<0.027

CT BP ΔΣ modulators are listed in order to obtain references for comparison. LP ΔΣ modulators can also be used for direct IF digitization, and circuits of this kind are dealt with next in order to achieve a fair comparison between different solutions. Finally, the different approaches are compared. It is worth mentioning that the power dissipation figures and FOMs listed do not include the power consumption of the decimation filter which is needed.

6.1 Discrete-Time BP ΔΣMs

There are several published DT BP ΔΣMs and in the following study they are classified into 2nd- (Table 6.1), 4th- (Tables 6.2 and 6.3), and higher-order (Table 6.4) structures. Most 2nd-order BP ΔΣMs are designed for an FM radio with an input signal frequency (IF) of 10.7MHz and they are, in that sense, comparable (Table 6.1). However, only two circuits [6] [7] are implemented with a 0.35μm technology. The circuit [7] is a low-voltage implementation and the circuit [6] is a solus multi-bit structure. A bipolar implementation [10] is designed to convert a 1MHz signal band around a 62.5MHz IF with a sampling frequency of 250MHz, but the approach led to very high power dissipation. Only Circuit [6] gives appropriate FOMs; even the power dissipation is

quite high as a result of the high capacitive load of the 5b ADC.

Most DT BP ΔΣMs have a 4th-order loop filter (Tables 6.2 and 6.3). There are implementations for very different signal frequencies (455kHz-100MHz) with sampling frequencies between 2-80MHz[1]. Only in one circuit [20] is a MASH topology selected. The multi-bit quantizer used reduces the leakage noise of the first cascade stage, leading to moderate FOMs. The circuits listed are designed for narrow bandwidths (mainly 30kHz or ˜200kHz), except Circuit [12], which achieves an SNDR of 47dB over the 1.25MHz bandwidth. The performance is low because of the poor SC resonators. The DT BP ΔΣMs presented in this book [19] [21] have considerably higher FOMs (270kHz bandwidth) than the other published circuits. Furthermore, high signal frequencies of 60 and 100MHz are used. The results over the 3.84MHz bandwidth are also listed, but then the FOMs achieved are low. A 1b ΔΣM with an OSR of only 10 does not lead to an effective result. It is hard to increase the sampling frequency and therefore a pure multi-bit structure may be a better choice. However, wide-bandwidth A/D conversion with high performance consumes a lot of power, regardless of the technique adopted. It seems that Equations (6.1) and (6.2) emphasize the DR or SNDR achieved but that the signal bandwidth is underrated.

Using a high-order loop filter the OSR can be decreased (Table 6.4). If only quantization noise is considered, this makes possible a lower sampling frequency [28] [30] for narrow-band applications (GSM) or a larger signal bandwidth [24] [27] [29] for wide-band systems (IS-95, DECT, WCDMA). Both the single-loop and MASH architectures are adopted, but no direct conclusion as to their superiority can be drawn. The implemented 1b 8th-order BP ΔΣM [24] has the highest FOMs with an OSR of 32. Actually, Circuits [25], [27], and [29] can be classified as LP-type ΔΣ modulators rather than to BP ΔΣ-modulators because they consist of front-end mixers and LP ΔΣ-modulators. In these structures the simplicity of signal demodulation at the $f_s/4$ frequency is utilized by performing a multiplication by (1,-1) in the analog domain, thus making possible the use of LP ΔΣ modulators for separate I and Q branches.

The performance plots of the published DT BP ΔΣ modulators are depicted in Figure 6.1. In each subplot the circuits with a higher performance are in the upper part of the figure and the faster circuits are on the right-hand side. Hence, the circuits in the right upper corner have the highest capacity. We can see that the circuits presented in this book are state-of-the-art BP ΔΣ modulators. The two 'o' marks in the right lower corner show the capability of the circuits to convert a 3.84MHz WCDMA signal bandwidth. Because the circuits have been optimized to the narrow-bandwidth GSM mode, the comparison result is moderate in this wide-band mode. From Figure 6.1

[1] Effective $f_s = 160MHz$ in [12] and 109.9MHz in [23] using DS structure.

Table 6.2 1/2 a comparison of 4th-order DT BP ΔΣ modulators, 1993-1998.

Reference	[12]	[13]	[14]	[15]	[16]	[17]	[3]
Year	1997 / 98	1997	1997	1996	1995	1993	1993
Technology [μm CMOS]	0.5	0.8	0.6	1.2 Bi	2.0	1.0	3.0
Power Supply [V]	3.0	5.0	3.3	5.0	3.3	5.0	10.0 ($\pm$5)
ADC / DAC [bits]	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
Resonator	DD	(integrator)	2xHPF	DD	(integrator)	DD	LDI
Structure	DS MFB single-loop	quadrature single-loop	2-path MFB single-loop	MFB single-loop	2xLP MFB single-loop	MFB single-loop	FF+MFB single-loop
Power Consumption [mW]	65	130	72	50	0.8	-	480
Core Area [sqmm]	1.1	4.3	2.7	1.44	1.0	-	24.5
OSR	400	166 / 25	200	107	133	120	115
Signal Frequency [MHz]	40	3.75	20	10.7	2.0	1.8	0.455
Sampling Frequency [MHz]	160	10	80	42.8	8.0	7.2	1.852
Bandwidth [MHz]	1.25	0.03 / 0.2	0.2	0.2	0.03	0.03	0.008
SFDR [dB]	39	-	42	-	56	-	-
Peak SNDR [dB]	47	69 / 62	70	-	-	73	˜54
Peak SNR [dB]	-	-	72	54	56	-	63
Dynamic Range [dB]	-	77 / 67	75	-	69	89	-
Image rejection [dB]	39	˜>45	42	-	56	-	-
FOM_1 [10^{-6}]	-	0.19 / 0.12	1.4	-	4.8	-	-
FOM_2 [10^{-6}]	0.02	0.03 / 0.04	0.4	< 0.02	<0.2	-	0.00007

Table 6.3 2/2 a comparison of 4th-order DT BP ΔΣ modulators, 1999- (*)in this book).

Reference	[18]	[19]*	[20]	[21]*	[22]	[23]
Year	2002	2002	2001/02	2001 / 02	2000	1999
Technology [μm CMOS]	0.25	0.35	0.25	0.35	0.35	0.35
Power Supply [V]	0.8	3.0	2.5	3.0	3.3	3.0
ADC / DAC [bits]	1 / 1	1, 4 / 1	3 / 3	1 / 1	1 / 1	1 / 1
Resonator	2xHPF	DD (Ver. II)	LDI	DD (Ver. I)	DD	2xHPF
Structure	2-path MFB single-loop	MFB single-loop	2-2 MASH	MFB single-loop	DS MFB single-loop	2-path MFB single-loop
Power Consumption [mW]	2.5	24 / 38	77	56	5.5	18
Core Area [sqmm]	2.1	0.79	5.6	0.58	-	-
OSR	83	148 / 10	20	148 / 10	167 / 25	275
Signal Frequency [MHz]	1.25	60	0.566	100	2.5	82.4
Sampling Frequency [MHz]	5	80	10	80	10	109.9
Bandwidth [MHz]	0.03	0.27 / 3.84	0.25	0.27 / 3.84	0.03 / 0.2	0.2
SFDR [dB]	-	61	-	62	43	-
Peak SNDR [dB]	61	78 / 48	-	72 / 42	-	54
Peak SNR [dB]	-	80 / 48	77	80 / 42	62 / 52	-
Dynamic Range [dB]	68	86 / 50	~79	84 / 46	68 / 54	-
Image rejection [dB]	-	70 / 61	-	62	43	>40
FOM_1 [10^{-6}]	1.2	72.5 / 0.2	4.2	19.61 / 0.04	0.56 / 0.15	-
FOM_2 [10^{-6}]	0.2	11.5 / 0.1	< 2.6	1.24 / 0.02	<0.14 / <0.09	0.05

Table 6.4 A comparison of 6th- and 8th-order DT BP ΔΣ modulators (*)in this book).

Reference	[24]*)	[25]	[26]	[27]	[28]	[29]	[30]
Year	2002	2001	2000 / 01	2000	1999	1999	1996
Technology [μm CMOS]	0.35	0.25	0.35	0.25	0.8 Bi	0.25	0.8
Power Supply [V]	3.0	2.5	3.3	2.5	5.0	2.5	3.0
Order	8	6 (2 x 3)	6	8	8	6 (2x3)	6
ADC / DAC [bits]	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	4 / 1-4	1 / 1
Resonator	DD (Ver.II)	(integrator)	LDI	(integrator)	FE	(integrator)	DD
Structure	MFB (4+4) MASH	FF single-lo.[1)]	FF+MFB single-lo.	2-path MFB MASH[2)]	FF+MFB single-lo.	2-path MFB single-lo.[1)]	MFB (4+2) MASH
Power Consumption [mW]	37	11.5 / 13.5	76	110	157	90	7
Core Area [sqmm]	1.0	0.36	1.0	4.0	2.9	0.9	-
OSR	32 / 23	260 / 18	2378 / 107	16	36	32	32
Signal Frequency [MHz]	60	78 / 138	10.7	16	10.7	20	3.25(81.25)
Sampling Frequency [MHz]	80	104 / 184	42.8	64	14.3	80	13
Bandwidth [MHz]	1.25 / 1.762	0.2 / 5.0	0.009 / 0.2	2.0	0.2	1.25	0.2
SFDR [dB]	45	40 / 41	-	40	66	53	-
Peak SNDR [dB]	75 / 69	71 / 51	75 / 61	70	-	72	63
Peak SNR [dB]	75 / 70	74 / 52	75 / 61	71	59	73	63
Dynamic Range [dB]	82 / 72	84 / 53	88 / 74	75	67	80	72
Image rejection [dB]	45	40 / 41	-	40	-	53	-
FOM_1 [10^{-6}]	87 / 12	70.7 / 1.2	1.21 / 1.07	9.3	0.10	22.5	7.3
FOM_2 [10^{-6}]	17 / 6	3.5 / 0.8	0.06 / 0.05	2.9	<0.02	3.6	0.9

[1)] Actually, a passive $f_s/4$ mixer and two LP ΔΣ modulators
[2)] Consists of passive mixers and 2nd-order LP ΔΣ modulators

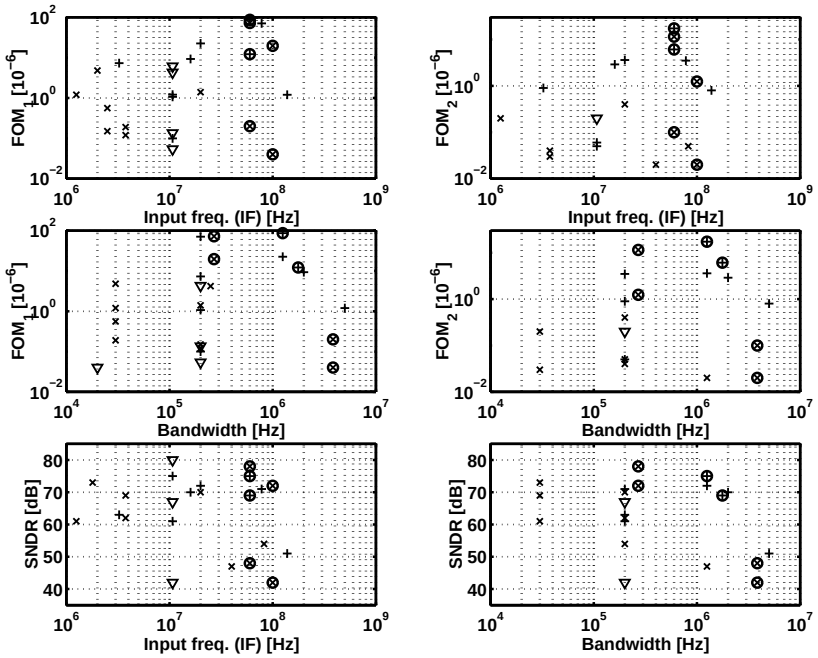

Figure 6.1 Data plots of the DT BP ΔΣ modulators ('∇'=Table 6.1, 'x'=Table 6.2 or 6.3, '+'=Table 6.4, 'o'=circuit of this book).

we also observe that there are both 4th-order and higher-order high-performance DT BP ΔΣ modulators. It is worth mentioning the fact that almost all the circuits are pure single-bit architectures and an entirely multi-bit topology has only been adopted in a few circuits [6] [20].

6.2 Continuous-Time BP ΔΣMs

During the last five years CT BP ΔΣ modulators have been assiduously researched. Published 2nd-order CT BP ΔΣMs are listed in Table 6.5 and they differ in many senses. One circuit [37] is implemented with HBT technology and operates with a 4GHz sampling frequency; another [31] is implemented with 0.18μm CMOS technology and uses a sampling frequency of 20MHz. The power dissipation of these circuits differs hugely, or by 1.398W. Actually, just these two circuits have moderate FOMs and the results are of the same order as the FOMs calculated for 2nd-order DT BP ΔΣMs. Most circuits employ an RC or g_mC technique and a monolithic inductor is adopted in only one circuit [35].

CT BP ΔΣ modulators with a 4th- or 6th-order loop filter are listed in Table 6.6.

Table 6.5 A comparison of 2nd-order CT BP ΔΣ modulators.

Reference	[31]	[32]	[33]	[34]	[35]	[36]	[37]
Year	2002	2002	2001	2000	1998	1997	1997
Technology [μm CMOS]	0.18	0.65 Bi	1.5	0.5	0.5 Bi	0.8 Bi	HBT 80G
Power Supply [V]	1.8	2.7	1.2	2.5	5.0	5.0	-
ADC / DAC [bits]	4 / 4	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
Structure	RC MFB	RC FF+MFB	RC BPF	g_mC MFB	LC BPF	g_mC BPF	g_mC BPF
Power Consumption [mW]	1.75	22	2.1	39	135	-	1400
Core Area [sqmm]	0.36	6.0	2.9	0.36	0.63	-	0.56
OSR	10	50	100	700	9500	500	5464 / 32
Signal Frequency [MHz]	2.0	1.0	1.0	70	950	50	55.5
Sampling Frequency [MHz]	20	100	4.0	280	3800	200	4000
Bandwidth [MHz]	1.0	1.0	0.02	0.2	0.2	0.2	0.366 / 62.6
SFDR [dB]	-	40	-	-	-	-	-
Peak SNDR [dB]	51	56	45	42	˜49	-	92 / 44
Peak SNR [dB]	51	-	-	-	57	46	92 / 44
Dynamic Range [dB]	53	˜60	40	˜40	˜60	˜45	˜80 / ˜48
Image rejection [dB]	-	40	-	-	-	-	-
FOM_1 10^{-6}	1.8	0.7	0.002	0.0008	0.024	-	0.42 / 0.05
FOM_2 10^{-6}	1.2	0.3	0.005	0.0013	0.002	-	6.7 / 0.02

Circuit [41] has a high dynamic range over a very narrow (9kHz) bandwidth and the result has been achieved without external components. The best result has been obtained by combining the advantages of the LC loop, RC technique, and SC technique [38]. The LC loop does not consume any power and a very accurate resonator is implemented using an external inductor and a trimmed capacitor array. The performance of the RC resonator is high enough to implement the second resonator with a low current consumption. However, a programmable capacitor array is required to tune the RC resonator. The last resonator stage utilizes a high Q-value and an accurate SC resonator notch frequency. The calculated FOM_1 is higher than that achieved with DT BP ΔΣ modulators. However, a direct comparison is not fair because of the external inductor used.

6.3 LP ΔΣMs for IF Digitization

High-performance LP ΔΣMs are inherently easier to design and implement than BP ΔΣMs. This results from the difficulty of designing a monolithic resonator with a high Q-value and accurate resonance frequency, which is the main consideration in this book. From the system aspect of radio receivers, direct IF digitization is an attractive

Table 6.6 A comparison of 4th- and 6th-order CT BP ΔΣ modulators.

Reference	[38]	[39]	[40]	[41]	[5]
Year	2002	2000	1999	1999	1993
Technology [μm CMOS]	0.35 Bi	SiGe Bi	0.35	0.5	1.2 Bi[1)]
Power Supply [V]	3.1	3.0	2.7 / 3.3	3.3 / 5.0	9.0
ADC / DAC [bits]	3 / 3	1 / 1	1 / 1	1 / 1	1 / 1
Order	6	4	4	6	4
Structure	LC+RC+SC external L	g_mC BPF	LC+SC(LP) external L	RC FF	LC external LC
Power Consumption [mW]	50	64	330	60	1350
Core Area [sqmm]	5.0	0.52	3.2	0.36	35+10[1)]
OSR	48	2000 / 203	1000	2222 / 100	65
Signal Frequency [MHz]	4.0	200	100	10.7	6.5
Sampling Frequency [MHz]	32	800	400	40	26
Bandwidth [MHz]	0.333	0.2 / 1.97	0.2	0.009 / 0.2	0.2
SFDR [dB]	-	-	50	-	-
Peak SNDR [dB]	-	-	45	76 / 64	-
Peak SNR [dB]	77	68 / 58	54	-	55
Dynamic Range [dB]	90	˜66 / ˜56	49	81 / 67	-
Image rejection [dB]	-	-	50	-	-
FOM_1 10^{-6}	107.7	0.20 / 0.20	0.0008	0.3 / 0.3	-
FOM_2 10^{-6}	< 5.4	<0.3 / <0.3	0.0003	0.1 / 0.1	<0.0008

[1)] 1.2μm BiCMOS analog/digital array

Table 6.7 A comparison of LP ΔΣ modulators for IF digitization.

Reference	[42]	[43]	[44]	[45]	[46]
Year	2001	2000	2000	1999	1997
Technology [μm CMOS]	0.35 Bi	0.35	0.25	0.8 Bi	1.2
Power Supply [V]	2.7	2.5	2.5	5.0	3.3
ADC / DAC [bits]	1 / 1	1 / 1	1 / 1	1 / 1	1 / 1
Order	2	4	2 x 5	2	2
Type	DT SC	CT RC+g_mC	CT RC+g_mC	CT passive	CT passive
Structure	sampler +2xLP MFB	mixer +2xLP FF	mixer +2xLP FF	2x (mixer+LP) LPF	2x (mixer+LP) LPF
Power Consumption [mW]	2 x 22	2 x 1.8	8.0	2 x 18	2 x 0.25
Core Area [sqmm]	2 x 0.42	0.2	0.55	1.5	2 x 0.4
OSR	250	65	2341 / 105	500	250
Signal (IF) Frequency [MHz]	50	13	10.7	400	10
Sampling Frequency [MHz]	50	13	21.07	20	10
Bandwidth [MHz]	2 x 0.1	2 x 0.1	0.009 / 0.2	2 x 0.02	2 x 0.02
SFDR [dB]	-	-	-	-	-
Peak SNDR [dB]	-	-	-	66	67
Peak SNR [dB]	81	82	94 / 79	-	-
Dynamic Range [dB]	88	82	97 / 82	72	78
Image rejection [dB]	-	-	49	-	-
FOM_1 10^{-6}	46.4	142	91 / 64	0.28	81.6
FOM_2 10^{-6}	-	-	-	0.07	6.5

choice and hence, a good deal of research has also been conducted to determine the suitability of LP ΔΣMs for an IF-sampling receiver (Table 6.7). Table 6.7 lists the LP ΔΣMs which convert an IF signal directly to the I and Q-paths at the baseband. Earlier, in Table 6.4, three equivalents for BP ΔΣMs which consist of LP ΔΣMs were listed [25] [27] [29]. Measurements of both the I and Q-branches and the image rejection level achieved have been presented only in [44] though all the circuits listed in Table 6.7 aim at the digitization of a complex IF signal. One circuit [42] has been implemented with the SC technique and the others are continuous-time implementations. The signal frequencies (IFs) used vary from 10MHz up to as much as 400MHz in [45], but the circuits with a lower IF have considerably higher FOMs. If the circuits are compared using only the calculated FOMs the continuous-time implementations seem to be an optimum choice. However, they were measured using lower input signal frequencies than the 50MHz used in the discrete-time implementation in [42]. Hence, the clock jitter and RF front-end requirements can differ greatly between different approaches.

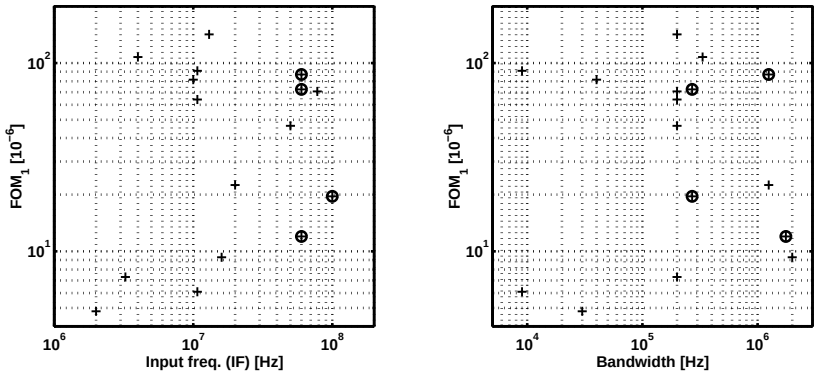

Figure 6.2 Data plots of the highest performance ΔΣMs for IF digitization ('o'=circuit of this book).

6.4 Summary

In this chapter, three different approaches to direct IF digitization were listed in tables using different performance parameters. The first method employed to perform the ΔΣ modulation of complex signals was the utilization of BP ΔΣ modulators using resonators. The method is adopted in this book using discrete-time SC resonators, even if continuous-time circuits have also been studied in many publications. To avoid difficulties in designing a high-quality resonator, two LP ΔΣMs with a simple mixer stage can be used to replace a BP ΔΣM if a digital intermediate frequency of $f_s/4$ or $3f_s/4$ has been adopted [25] [27] [29]. The second way to use LP ΔΣMs is to convert I and Q signals directly to DC and perform the AD conversion at the baseband. Depending on the architecture selected, the first IF may be fixed to the sampling frequency of the LP ΔΣMs [42] or can be freely selected [43].

Figure 6.2 shows the highest FOM_1 values calculated in Tables 6.1-6.7. Some LP ΔΣM implementations and a CT BP ΔΣM [38] exploiting an external inductor have slightly higher FOM_1 values than the discrete-time SC BP ΔΣMs studied in this book. However, when the input signal frequency is considered or the converted bandwidth is emphasized, the highest-capacity IF digitizers are some of the BP ΔΣMs presented in this book (Figure 6.2).

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Chapter 7

Conclusions

In this thesis, bandpass ΔΣ modulators and their suitability for IF digitization have been studied. Utilization of the digital IF receiver architecture is a method to move the analog-digital boundary to higher frequencies. This is a desirable property, because it makes easier the implementation of the required multi-mode functions. Furthermore, the development of IC technologies is easier and faster to exploit in digital circuits than in their analog counterparts. However, the transition from analog to digital functions also has to be feasible in the sense of power dissipation and not solely in terms of increased flexibility. Therefore, at first it may be reasonable to divide some functions between the analog and digital sides instead of adopting a fully digital approach. For example, in this work the conversion of narrow-band signals (GSM) with a high resolution is pursued, but the channel selection of wide-band systems (WCDMA) is mainly performed with a passive IF filter.

The SC resonators published earlier have some limitations and a new double-delay SC resonator has been designed to solve the main problems. The operation of all three of the designed evolution versions has been ascertained by the implementation of a BP ΔΣ modulator. The measured performance of the implemented BP ΔΣ modulators compares well even to their published LP equivalents. Multi-mode functionality has also been added to the A/D conversion by using a cascade BP ΔΣ modulator in modes in which a high resolution is required over a wide bandwidth (IS-95). The LP decimation principle has been expanded to a BP decimation sampler to reduce the power dissipation of a BP ΔΣ modulator without tightening IF filtering or clock jitter requirements. The feasibility of the method has been tested by measurements.

The measurements verify the possibility of performing a high-resolution A/D conversion directly from a fairly high intermediate frequency with a reasonable power

dissipation. However, the total current consumption of the channel selection, including the digital part, has not been verified with measurements. Another challenging task is to generate the required low-jitter clock signal by means of an on-chip clock generator. In fact, the clock jitter seems to set a fundamental limit to the input signal frequency because of the high oversampling rate that is needed. The achieved resolution (˜13b) over the GSM bandwidth may not be adequate for a final product, or at least the specifications of the automatic gain control and IF filtering will be very stringent. Therefore, in the GSM mode the resolution should be further improved by about 6dB. In the WCDMA mode the resolution is adequate for signal detection but the extra resolution would relieve the requirements of the passive channel filter.

In the near future the digital IF receiver can be an alternative to the direct conversion receiver in the implementation of multi-mode mobile phone receivers. It is not reasonable to keep any architecture as a sole alternative but other possibilities have to be researched when the technology evolves. Regardless of the radio architecture selected, the common target is to increase the digital signal processing as it is a cost-effective way.

Appendix A

Ideal In-Band Noise Power

The ideal noise transfer function (NTF) of the 2N-order $f_s/4$ BP $\Delta\Sigma$ modulator is

$$NTF(z) = \left(1+z^{-2}\right)^N. \tag{A.1}$$

The noise power spectral density (NPSD) at the modulator output is

$$\begin{cases} NPSD(f) = N_q\left[NTF(z) * NTF(z^{-1})\right] \\ z = exp\left(\frac{j2\pi}{f_s} f\right) \end{cases} \tag{A.2}$$

$$\Rightarrow NPSD(f) = 2^N \cdot N_q \left[1+cos\left(\frac{4\pi}{f_s} f\right)\right]^N. \tag{A.3}$$

To calculate the in-band noise power (n_0^2) the NPSD has to be integrated over the passband

$$n_0^2 = \int_{f_1}^{f_2} NPSD(f)\, df, \tag{A.4}$$

where $f_{BW} = f_2 - f_1$ is the band of interest. By substituting Equation (A.3) into Equation (A.4) we have

$$\begin{aligned} n_0^2 &= 2^N \cdot N_q \int_{f_1}^{f_2} \left[1+cos\left(\tfrac{4\pi}{f_s} f\right)\right]^N df \\ &= 2^{2N} \cdot N_q \int_{f_1}^{f_2} sin^{2N}\left(\tfrac{\pi}{2} - \tfrac{2\pi}{f_s} f\right) df \end{aligned}, \tag{A.5}$$

which is approximately

$$n_0^2 \approx 2^{2N} \cdot N_q \int_{f_1}^{f_2} \left(\frac{\pi}{2} - \frac{2\pi}{f_s} f\right)^{2N} df. \tag{A.6}$$

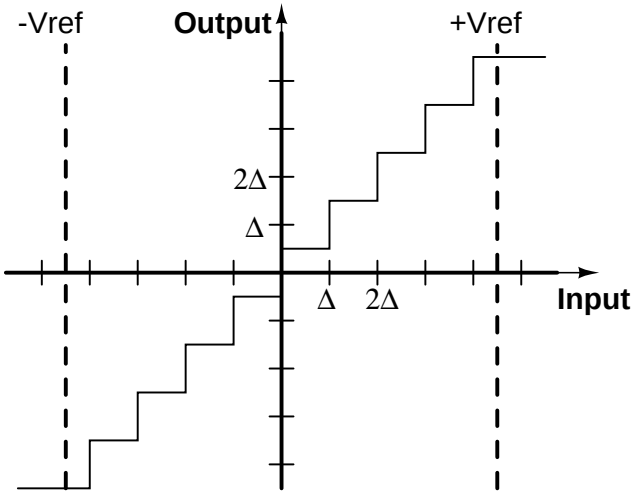

Figure A.1 The quantization step.

Assuming that the band of interest is around $\pi/2$ we obtain

$$n_0^2 \approx \frac{\pi^{2N}}{2N+1}\frac{e_{rms}^2}{OSR^{(2N+1)}}, \tag{A.7}$$

where the OSR is the oversampling rate ($f_s/2f_{BW}$).
If the internal ADC of the ΔΣM is not overloaded the quantization error is

$$e_n \in \left[-\frac{\Delta}{2}, \frac{\Delta}{2}\right], \tag{A.8}$$

where Δ is the quantization step (Figure A.1). According to Figure A.1 the maximum input signal amplitude of the quantizer (A_{Qmax}) is

$$A_{Qmax} = \frac{1}{2}(R-1)\Delta, \tag{A.9}$$

where R is the number of quantization levels. If the ADC has B bits we have

$$R = 2^B. \tag{A.10}$$

Using Equation (A.7) we may write the theoretical maximum DR for a sinusoidal

input signal as

$$DR \approx 10log_{10}\left(\frac{\left(\frac{A_{Qmax}}{\sqrt{2}}\right)^2}{\frac{\Delta^2}{12}}\frac{(2N+1)OSR^{(2N+1)}}{\pi^{2N}}\right) . \qquad (A.11)$$
$$= 10log_{10}\left(\frac{3}{2}(2^B-1)^2\frac{(2N+1)OSR^{(2N+1)}}{\pi^{2N}}\right)$$

Equation (A.11) also gives theoretical SQNR if a 1-bit quantizer is utilized or B=1 because the largest sine wave that the $\Delta\Sigma$ modulator will accommodate without saturating has peak values of $\Delta/2$ [1]. By adding more bits to the quantizer the quantization noise is reduced by 6.02dB per added bit and we may write

$$SQNR_{max} \approx 10log_{10}\left(\frac{3}{2}\frac{(2N+1)OSR^{(2N+1)}}{\pi^{2N}}\right) + 6.02\cdot(B-1). \qquad (A.12)$$

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Appendix B

Nonideal In-Band Noise Power

If we assume a basic single-loop BP ΔΣ modulator structure (Figure 2.7) and eliminate the possible poles of the noise transfer function, the NTF of the 2N-order BP ΔΣ modulator is

$$NTF(z) = \left(1 - p_1 z^{-1} + p_2 z^{-2}\right)^N, \tag{B.1}$$

where p_1 (ideally zero) and p_2 (ideally one) for $\pi/2$-resonator describe the effects of the nonidealities.

The noise power spectral density (NPSD) at the BP ΔΣ modulator output is

$$NPSD(f) = N_q \left[(1 + p_1^2 + p_2^2) - 2p_1(1 + p_2)cos\left(\frac{2\pi f}{f_s}\right) + 2p_2 cos\left(\frac{4\pi f}{f_s}\right)\right]^N. \tag{B.2}$$

It is reasonable to calculate the in-band noise power for a 4th-order(N=2) modulator for simplicity. Assuming that the band of interest is around $\pi/2$, and using Equation (A.4), we get

$$n_0^2 = N_q f_s \left[\frac{k_1}{OSR} - \frac{k_2}{\pi} sin\left(\frac{\pi}{OSR}\right) + \frac{k_3}{\pi} sin\left(\frac{2\pi}{OSR}\right)\right], \tag{B.3}$$

where

$$\begin{cases} k_1 = 0.5 + 2p_1^2 + 2p_2^2 + 2p_1^2 p_2 + 2p_1^2 p_2^2 + 0.5p_1^4 + 0.5p_2^4 \\ k_2 = p_1^2 + 4p_1^2 p_2 + p_1^2 p_2^2 + 2p_2 + 2p_2^3 \\ k_3 = 0.5p_2^2 \end{cases}. \tag{B.4}$$

The result can be approximated in a polynomial form as

$$n_0^2 \approx N_q f_s \left[\frac{h_1}{OSR} + \frac{h_2 \pi^2}{OSR^3} + \frac{h_3 \pi^4}{OSR^5}\right], \tag{B.5}$$

where

$$\begin{cases} h_1 = k_1 - k_2 + 2k_3 \\ h_2 = \frac{1}{6}(k_2 - 8k_3) \\ h_3 = \frac{1}{120}(32k_3 - k_2) \end{cases} . \tag{B.6}$$

In a cascaded ΔΣ modulator the transfer function of the leakage noise power (H_{le}) depends on the match between the digital (H_d) and analog (H_a) transfer functions and hence we obtain

$$\begin{aligned} H_{le}(z) &= H_a(z) - H_d(z) \\ &= \left(1 - p_1 z^{-1} + p_2 z^{-2}\right)^N - \left(1 + z^{-2}\right)^N \end{aligned} . \tag{B.7}$$

If the first stage is a 4th-order BP ΔΣ modulator (N=2) we have

$$H_{le}(z) = -2p_1 z^{-1} + (2p_2 + p_1^2 - 2)z^{-2} - 2p_1 p_2 z^{-3} + (p_2^2 - 1)z^{-4}. \tag{B.8}$$

The leakage power at the signal band is

$$n_{0le}^2 = e_{rms1}^2 \left(\frac{a}{OSR} - \frac{2b}{\pi} sin\left(\frac{\pi}{OSR}\right)\right), \tag{B.9}$$

where e_{rms1}^2 is the quantization noise power of the first stage and

$$\begin{cases} a = 4p_1^2(1 + p_2^2) + (p_2^2 - 1)^2 + (2p_2 + p_1^2 - 2)^2 \\ b = 2 - p_1^2 + (4p_1^2 - 2)p_2 + (p_1^2 - 2)p_2^2 + 2p_2^3 \end{cases} . \tag{B.10}$$

In a polynomial form we can approximate

$$n_{0le}^2 \approx e_{rms1}^2 \left(\frac{c}{OSR} + \frac{\pi^2}{3} \frac{b}{OSR^3} \right), \tag{B.11}$$

where

$$c = -3 + 2p_1^2(3 + p_2^2) - 2p_2(4p_1^2 - 2) + 2p_2^2 - 4p_2^3 + p_2^4 + (2p_2 + p_1^2 - 2)^2. \tag{B.12}$$

Appendix C

Amplifier Equivalent Load

A typical loading situation of amplifiers in switched-capacitor ΔΣ modulators is shown in Figure C.1. To the input are connected a sampling capacitor (C_s), a feedback loop DAC-capacitor (C_{dac}), and, further, the amplifier input parasitic (C_{pi}) increases the total capacitive load (C_{in}) at the input. The total capacitive load between output node and ground (C_{out}) consists of the bottom plate parasitics (C_{bb}) of all the capacitors connected to the output node, the output parasitics and common-mode feedback load of the amplifier (C_{po}), and the load of the next stage (C_{load}). The next stage is another integrator/resonator or an ADC. The integration capacitor (C_i) closes the loop.

When a folded-cascode or a telescopic-cascode opamp is used the unity-gain bandwidth is given by

$$\omega_u = \frac{g_m}{C_L}, \tag{C.1}$$

where g_m is the transconductance of the opamp and C_L the load seen at the opamp output. The -3dB frequency of the closed-loop amplifier depends on the unity-gain bandwidth and on the feedback factor (β) given by

$$\beta = \frac{C_i}{C_{in}+C_i}. \tag{C.2}$$

From Figure C.1b the load of the closed loop amplifier is

$$C_L = C_{out} + \frac{C_{in}C_i}{C_{in}+C_i}. \tag{C.3}$$

Hence, we obtain

$$\omega_{-3dB} = \beta\omega_u = \beta\frac{g_m}{C_L} = \frac{g_m}{C_{eq}}, \tag{C.4}$$

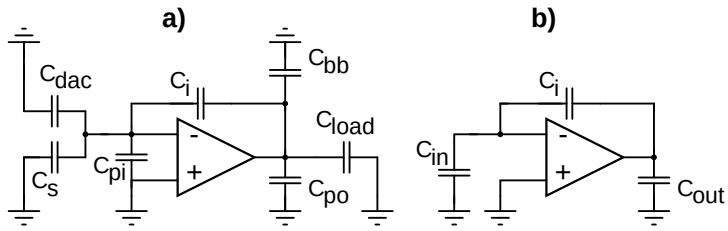

Figure C.1 a) Typical amplifier loading in ΔΣ modulators and b) equivalent circuit.

where C_{eq} is the equivalent capacitive load of the opamp in the feedback configuration, or

$$C_{eq} = C_{in} + C_{out} + \frac{C_{in}C_{out}}{C_i}. \tag{C.5}$$

During linear settling the settling time constant of the amplifier is given by

$$\tau = \frac{1}{\omega_{-3dB}} = \frac{C_{eq}}{g_m}. \tag{C.6}$$