Helsinki University of Technology Institute of Intelligent Power Electronics Publications
Espoo 2004 Publication 8

LOW-POWER PFC AND FORWARD CONVERTERS – METHODS TO IMPROVE PERFORMANCE

Thesis for the degree of Doctor of Science in Technology

Vesa Tuomainen

Dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the Department of Electrical and Communications Engineering for public examination and debate in Auditorium S4 at Helsinki University of Technology (Espoo, Finland) on the 4th of June, 2004, at 12 noon.

Helsinki University of Technology
Department of Electrical and Communications Engineering
Power Electronics Laboratory

Teknillinen Korkeakoulu
Sähkö- ja tietoliikennetekniikan osasto
Tehoelektroniikan laboratorio

Distribution:
Helsinki University of Technology
Power Electronics Laboratory
P.O. Box 3000
FIN-02015 HUT
Fax: +358-9-451 2432

ISBN 951-22-7098-6
ISSN 1456-0445

Otamedia Oy
Espoo 2004

Abstract

The number of power electronic appliances is growing. Power electronic converters can be used to convert the ac line voltage to a dc voltage, and further through dc-dc conversion stages to desired dc voltages for different loads. This Thesis deals with three single-stage power factor correction converters and a forward type dc-dc converter.

Single-stage converters can be considered as low cost solutions for power factor correction. This is because only one active switching stage is used in the converters. Small signal and steady state analysis are performed for the dither converter. A resonant type snubber is analyzed for the BIFRED and BIBRED converters and a new type of clamp circuit is developed for the BIFRED converter.

The dc-dc conversion part of the Thesis deals with a forward converter with active clamp circuit and self-driven synchronous rectifiers. Resonant transition of the converter is analyzed in detail. Emphasis of the research is on improving the efficiency of the converter. Findings show that the minimization of the turn-on losses in the converter is not necessarily advantageous. The analysis is verified with a 3.4 V and 30 A prototype converter.

Preface

It has been a great pleasure for me to do this Thesis. In this Preface I want to thank all of those people who have helped and supported me in my work.

First of all, I am grateful to Professor Jorma Kyyrä, who supervised the research, for his guidance, invaluable advice and suggestions for this Thesis and for the research behind it. I also want to thank the former heads of the laboratory, Professors Jorma Luomi and Seppo Ovaska.

I want to thank all the people who work and have worked, during the time I have worked for the laboratory, at the Power Electronics laboratory for creating a pleasant and enthusiastic atmosphere. Special thanks are due to secretary of the laboratory Anja Meuronen and to laboratory technician Ilkka Hanhivaara for their assistance in practical matters. I also want to thank the former secretaries Ulla Ahlgren, Tuula Mylläri and Leena Väisänen.

I also want to thank my present and former colleagues for their contribution to my research. M.Sc. Juha Wallius, D.Sc. Vlad Grigore, D.Sc. Veli-Matti Leppänen, M.Sc. Marko Hinkkanen, M.Sc. Petri Mäki-Ontto and M.Sc. Konstantin Kostov

The research work was financially supported by the Graduate School of Electrical Engineering. Some of the research was done in the framework of two projects: the PFC project and the EFF project, which were financially supported by TEKES (the Technology Development Centre of Finland), ABB Industry Oy and Efore Oyj. I want to thank the Graduate School for giving this opportunity to prepare and write this Thesis and I also want to express my thanks to all of the board members of the two projects for setting goals and providing valuable ideas.

I express my gratitude to Tekniikan edistämissäätiö (TES), Finnish Cultural Foundation, Ulla Tuomisen säätiö and Teknillisen korkeakoulun tukisäätiö for their financial support for this Thesis.

Suuri kiitos kuuluu myös omaisilleni, isovanhemmilleni, sedilleni, tädeilleni ja rakkaille serkuilleni. Erityinen kiitos kuuluu vanhemmilleni, Tapani ja Liisa Tuomaiselle, jotka ovat aina tukeneet työtäni ja kannustaneet minua eteenpäin, sekä henkisesti että taloudellisesti. Ajoittain on saattanut vaikuttaa jopa siltä, että he ovat olleet, jos mahdollista, vieläkin innokkaampia työni edistymisen suhteen kuin minä itse. Lisäksi olen suuressa kiitollisuudenvelassa vanhemmalle veljelleni, DI Petri Tuomaiselle, joka on aina ollut minulle esimerkkinä ja innoituksen lähteenä. Kiitos kaikille.

”Taide on yksi luonnon monista ilmaisukeinoista,
niinkuin leivosen laulu, niinkuin myrskyävä meri, niinkuin tuulen humina puissa.
Tästä seuraa, ettei taiteen tarkoitus voi olla jäljitellä luontoa, vaan tulkita sitä”

V.A. koskenniemi,Matkasauva,
WSOY Porvoo 1926, s. 47.

Otaniemi, June 2004
Vesa Tuomainen

Contents

List of Publications

This thesis consists of an overview and the following publications:

P[1] Tuomainen, V. and Kyyrä, J. (2002). Steady state analysis of modified dither converter. *Proceedings of Nordic Workshop on Power and Industrial Electronics, NORPIE 2002*, Stockholm, Sweden, 12-14 August 2002, on CD-ROM.

P[2] Tuomainen, V. and Kyyrä, J. (2003). Small signal analysis of dither converter with a tapped transformer. *Proceedings of 10th European Conference on Power Electronics and Applications, EPE 2003*, Toulouse, France, 2-4 September 2003, on CD-ROM.

P[3] Tuomainen, V. and Kyyrä, J. (2002). Analysis of a lossless snubber for BIFRED and BIBRED. *Proceedings of 10th International Power Electronics and Motion Control Conference, EPE-PEMC 2002*, Cavtat & Dubrovnik, Croatia, 9-11 September 2002, on CD-ROM.

P[4] Tuomainen, V. (2003). A Passive clamp circuit for BIFRED converter. *Proceedings of 18th Annual IEEE Applied Power Electronics Conference and Exposition, APEC'03*, Miami Beach, Florida, 9-13 February 2003, Vol. 2, pp. 658-663.

P[5] Tuomainen, V. and Kyyrä, J. (2002). Improved switching condition for a forward with active clamp. *Proceedings of 10th International Power Electronics and Motion Control Conference, EPE-PEMC 2002*, Cavtat & Dubrovnik, Croatia, 9-11 September 2002, on CD-ROM.

P[6] Tuomainen, V. and Kyyrä, J. (2002). Effect of the magnetization inductance on forward converter with active clamp. *Proceedings of Nordic Workshop on Power and Industrial Electronics, NORPIE 2002*, Stockholm, Sweden, 12-14 August 2002, on CD-ROM.

P[7] Tuomainen, V. and Kyyrä, J. (2003). Effect of resonant transition on efficiency of forward converter with active clamp and self-driven sr's. *Proceedings of 34th Annual IEEE Power Electronic Specialists Conference, PESC'03*, Acapulco, Mexico, 15-19 June 2003, Vol. 3, pp. 1333-1338. Provisionally accepted for publication in *IEEE Transactions on Power Electronics*.

P[8] Tuomainen, V. and Kyyrä, J. (2003). Design considerations of resonant transition forward converter with active clamp. *Proceedings of 10th European Conference on Power Electronics and Applications, EPE 2003*, Toulouse, France, 2-4 September 2003, on CD-ROM.

The research reported in publications P[1] - P[8] was performed by the Author alone, who also wrote the publications. However, all work was carried out under the supervision of Professor Jorma Kyyrä, who read the publications and gave the author constructive ideas and valuable suggestions.

List of abbreviations

A	Ampere
A	Area
AC	Alternating current
BIBREB	Boost Integrated with Buck Rectifier/Energy storage /Dc-dc converter
BIFRED	Boost Integrated with Flyback Rectifier/Energy storage/Dc-dc converter
C	Capacitor
CCM	Continuous conduction mode
D	Diode
DC	Direct current
DCM	Discontinuous conduction mode
ESR	Equivalent series resistance
FAC	Forward with active clamp
Hz	Hertz
IC	Integrated circuit
kHz	Kilohertz
L	Inductor
MOSFET	Metal oxide semiconductor field effect transistor
RMS	Root mean square
PFC	Power factor correction
PCB	Printed circuit board
SMPS	Switched mode power supply
V	Volt
ZVS	Zero voltage switching

List of symbols

C	Capacitance
DPF	Displacement power factor
$\hat{d}_1$	Duty ratio variation
d_1	Duty ratio
D_1	Steady state duty ratio
$D_{1,\max}$	Maximum duty cycle
D_2	Relative portion of switching cycle during which the current of an inductor falls from peak value to zero
D_3	Relative portion of switching cycle during which the current of a DCM inductor is zero
f	Frequency
f_o	Resonance frequency
f_{line}	Frequency of the line voltage
f_s	Switching frequency
i_C	Capacitor current
$\langle i_{C,+} \rangle_{T\text{line}}$	Average current brought to capacitor C during a line cycle
$\langle i_{C,-} \rangle_{T\text{line}}$	Average current taken from capacitor C during a line cycle
$\langle i_{C,+} \rangle_{T\text{s}}$	Average current brought to capacitor C during a switching cycle
$\langle i_{C,-} \rangle_{T\text{s}}$	Average current taken from capacitor C during a switching cycle
i_D	Diode current
I_D	Average of diode current
i_{in}	Line current / input current
$i_{in,1}$	Line frequency component of the line current
$\langle i_{in} \rangle_{T\text{s}}$	Average line current during a switching cycle
$I_{in,peak}$	Peak value of the line current
$I_{in,rms,1}$	Rms value of the line frequency component of line current

$I_{\text{in,rms}}$	Rms value of the line current
$I_{\text{in,rms, }n}$	Rms value of n:th harmonic of the line current
i_{L}	Inductor current
I_{L}	Peak value of inductor current*
$I_{\text{L,max}}$	Maximum peak value of inductor current
I_{M}, I_{LM},	Peak value of the magnetizing current of a transformer
L_{M}, L_{m}	Magnetizing inductance of a transformer
L_{lk}	Leakage inductance
n	n:th multiple of the line frequency
N_1	Number of turns in the primary winding of a transformer
N_2	Number of turns in the secondary winding of a transformer
N_3	Number of turns in a tertiary winding of a transformer
N_4	Number of turns in a fourth winding of a transformer
$N_{1\text{A}}$	Number of turns in the upper part of the primary winding of a tapped transformer
$N_{1\text{B}}$	Number of turns in the lower part of the primary winding of a tapped transformer
N_1/N_2	Turns ratio of a transformer
P	Power
PF	Power factor
R_{load}, R_{l}	Load resistance
S	Apparent power
t	Time
t_{off}	Switch off time of a switching cycle
t_{on}	Switch on time of a switching cycle
THD	Total harmonic distortion
T_{line}	Length of a line cycle, inverse of the line frequency
T_{s}	Length of a switching cycle, inverse of the switching frequency
v_{DS}	Drain-source voltage of a MOSFET
v_{in}	Sinusoidal line voltage, $V_{\text{in}} \sin(\omega_{\text{line}} t)$

$v_{in,1}$	line frequency component of the line voltage
$\|v_{in}\|$	Rectified line voltage
$\langle\|v_{in}\|\rangle_{Ts}$	Average of the rectified line voltage during a switching cycle
V_{in}	Peak value of the line voltage*
$V_{in,rms,1}$	RMS value of the line frequency component of the line voltage
$V_{in,rms}$	RMS value of the line voltage
v_C	Voltage of a capacitor
V_C	Dc-voltage of a capacitor or control voltage
V_{C1b}	Dc voltage of capacitor C_{1b} (BIBRED converter)
V_{out}, V_o	Output voltage
ϕ_l	Phase difference between the line frequency voltage and current
ω_{line}	Angular frequency of the line voltage, $2\pi f_{line}$
Δt , Δt_1	Time delay required for turn at V_{in} level in the FAC converter
Δt_2	Time delay required for ZVS in the FAC converter

* Markings differ in publication P[2].

1 Introduction

The number of switched mode power supplies (SMPSs) and other power electronic appliances is growing. SMPSs are needed to convert electrical energy from one form to another. Since electrical sources can be either dc or ac, there are four basic types of converters; namely, conversion can be from ac to ac, dc to ac, ac to dc, and dc to dc. We will consider in this Thesis the two latter directions of conversion of electrical energy. For this reason, the Thesis is roughly divided into two parts. The first part deals with power factor correction converters, i.e. ac to dc conversion, and the second part deals with dc to dc conversion. It should be noted, also, that only relatively low power equipment fed from a dc or a single-phase ac source are considered in the Thesis.

The Thesis is composed of an introductory part and eight publications: P[1], P[2], P[3], P[4], P[5], P[6], P[7] and P[8], which have been presented in international conferences. The introductory part gives background information on the power factor correction and dc-dc conversion with forward converter.

1.1 Ac-dc conversion

Ac to dc rectifiers usually interface with the mains. These devices convert the sinusoidal line voltage to a dc voltage. It is a well-known fact that the input current of a SMPS tends to have a non-sinusoidal, distorted waveform. The distorted line current of a power converter is composed of the line frequency component and higher frequency harmonic components of the current. It should be noted that only the line frequency component of the current is carrying power when voltage is sinusoidal.

As use of energy is growing, the requirements for the quality of the supplied electrical energy are becoming stricter. This means that power electronic converters are used, or have to be used, to convert the input voltage to a precisely regulated dc voltage for the load.

Since the number of electronic appliances that are fed by power converters is soaring, an increasing amount of non-sinusoidal current is drawn from the distribution network. Consequently, due to the increasing amount of harmonic currents drawn, the distribution network becomes more and more polluted. As a direct consequence, available power from the grid becomes less. This is because unnecessary current components, which contribute to the rms value of the line current, are drawn from the grid. On the other hand, the harmonic currents distort the line voltage waveform and may cause malfunction in sensitive electrical equipment connected to the grid, Redl et al. 1995b, Redl 1996 and Redl et al. 1997.

Standard IEC 61000-3-2 (IEC 1995, IEC 2000 and IEC 2001) and its European version EN 61000-3-2, set limits for the allowed harmonic content of the line current of a power supply. Because of the standards and because of the problems related to the distorted line current, power supply manufacturers most probably have to equip their products with power factor correction (PFC) circuits. The main task for a PFC circuit is to shape the input current to resemble the waveform of the sinusoidal line voltage, i.e. to reduce the harmonic content of the line current of a power converter.

An additional PFC circuit in front of a power supply, however, adds to the cost and size of the device. This cost depends naturally on the chosen topology and the complexity of the circuit. Tolerance for any additional cost, however, in low power supply manufacturing is relatively low, owing to the fact that low power SMPSs tend to be mass production devices and sold in an extremely competitive market, Redl et al. 1995b. For this reason, there may well be a niche for low-cost power factor correction converters in which for example the component count is minimized.

As mentioned earlier, the standard and the harmful effects of the line current harmonics, Redl et al. 1995b, Redl 1996 and Redl et al. 1997, bring about a growing need for PFC converters. Single-stage converters combine the two desired objectives, line current shaping and output voltage regulation, into a single power processing stage. This means that power is processed only by one active switching stage, albeit that two separate goals are to be met. Therefore, at least one switch and the control circuitry for it are saved with this arrangement compared to two-stage PFC converters in which two separate converters are cascaded, Zhang et al. 1999. Single-stage

converters offer thus a reduction in the component count and they can be considered as a low-cost alternative for PFC.

In this Thesis three single-stage power factor correction circuits are investigated: the dither converter with a tapped transformer, the BIFRED converter and the BIBRED converter. It should be mentioned, however, that power factor correction properties of these three converters are not investigated in detail in this Thesis. This is because it is assumed, based on earlier research, that these converters can be designed to achieve a line current that satisfies the requirements set by the standard. Instead, the research reported here is concentrated on giving more insight into the operation and design of the converters or on improving the performance of the converters.

For the dither converter we have performed a steady state and small signal analyses. For the BIFRED and BIBRED converters a resonant type non-dissipative snubber is analyzed in detail. Additionally, we have developed and analyzed a passive clamp circuit for the BIFRED converter.

These three power factor correction converters are presented in Chapter 3 and in publications P[1], P[2], P[3] and P[4].

1.2 Dc-dc conversion

Switched mode supplies are widely used in dc-dc conversion. Input voltage for these converters is, as the name indicates, a dc voltage source. The input dc voltage source for a dc-dc converter can be, for example, rectified line voltage, output voltage of a PFC circuit, battery or fuel cell voltage.

A relatively high switching frequency that is used in these power converters enables the use of small reactive components, which reduces the overall size of the power supply. Also, a high switching frequency and small reactive components improve the converter's dynamic behavior, i.e. it is able to cope rapidly to changes in the load and input voltage.

One additional advantage of switched mode power supplies is a relatively high efficiency. Ideally, the energy conversion process would be without losses. However, in practice the components that are used to implement a converter are non-ideal and these non-idealities cause losses in the energy conversion process. Therefore, the efficiency of the conversion process is less than 100 percent. However, although the

perfect efficiency seems to be unattainable, it is well worth striving to get as close as possible to that goal, i.e. to minimize losses.

Efficiency of a power supply is an important design factor. The small but inevitable amount of electric losses transforms to thermal energy, i.e. to heat, in the power supply. Heating due to these losses has to be taken into account in the design process and adequate cooling should be provided for the device. Cooling or heat removal from the power supply is needed in order to ensure that the temperature of the device, and its individual components, do not exceed their maximum allowable operating temperatures. Also, additional cooling may be needed in order to ensure that the components actually do operate somewhat below their maximum limits since operating in a relatively high temperature affects adversely to the expected life-time of a component, for example Stevens et al. 2002.

A small size for a power supply is desirable. As mentioned earlier, a small size is attainable by using a relatively high switching frequency. However, because of the conversion losses there should be a way to conduct the heat out of the device. This means that, for example, a heat sink should be attached to the heat-generating component or components of the converter in order to prevent overheating. This, naturally, increases the physical size of the power supply.

However, even a seemingly small improvement in the efficiency of the conversion process can lead to a somewhat noticeable reduction in the need for cooling. For example, if the efficiency of a power supply is increased from 90 % to 91 %, this means that in other words that the losses are cut by approximately 10 %.

A high efficiency in low voltage dc-dc conversion is a challenge. For example, state-of-the-art electronic devices require relatively low operating voltages, for example 3.3 V, 2.5 V, 1.8 V, 1.5 V, and even sub-1V output voltages can be expected in the future, Lidow et al. 2003. However, the load current for these low voltage outputs should be of several tens of amperes. The high load current can easily cause considerable voltage drops in the rectifying stage and in the power carrying leads of the printed circuit board (PCB). A considerable voltage drop means here that the voltage drop, which together with the current defines the loss of energy, is considerable in relation to the load voltage. This means that, if the load current flows

through a noteworthy voltage-drop somewhere else than in the actual load, the efficiency cannot be very good.

Rectification losses of a power converter can be reduced with synchronous rectifiers, Chryssis 1989. This means that rectifier diodes are replaced with MOSFETs. These MOSFET synchronous rectifiers need, however, synchronized control signals and some energy in order to be driven appropriately. A cost-effective arrangement is to use self-driven synchronous rectifiers in which the control signals for the rectifiers are taken from the windings of the converter's transformer or the output inductor.

The single switch forward dc-dc converter is discussed in Chapter 4. Four passive and one active reset method for the transformer of the forward converter are presented and the suitability of the reset circuits for self-driven synchronous rectification are assessed. Further background information on forward converter with active clamp reset circuit and with self-driven synchronous rectifiers is given in the chapter. The research results on the active clamp forward converter are reported in publications P[5], P[6], P[7] and P[8].

The research reported in P[5], P[6], P[7] and P[8] is concentrated on giving more insight in to the operation of the active clamp converter and on techniques to improve the efficiency of the converter topology. The research results in the publications have been verified with a 3.4 V and 30 A prototype converter.

2 Background of power factor correction

2.1 Standard IEC 61000-3-2

The introduction of the standard IEC 61000-3-2, IEC 1995, IEC 2000 and IEC 2001, set limits for the harmonic content of the line current of a power converter and prompted a need for power factor correction circuits. The IEC (International Electrotechnical Committee) standard has also been adopted by the European Committee for Electrotechnical Standardization (CENELEC) as standard EN 61000-3-2.

The standard divides electrical equipment into four classes: A, B, C and D. The four classes include electrical equipment as follows, IEC 2001:

Class A: Balanced three-phase equipment, household appliances (excluding equipment identified as class D), tools (excluding portable tools), dimmers for incandescent lamps and audio equipment.

Class B: portable tools and arc welding equipment which is not professional equipment.

Class C: lighting equipment.

Class D: personal computers and personal computer monitors, and television receivers (active input power equal or less than 600 W).

Additionally, class D limits are reserved, according to IEC 2001, to equipment that can be shown to have a pronounced effect on the public electricity supply system.

Limits for class A and class D equipment are shown in Table 2.1 and 2.2, respectively. Class A limits are in absolute values whereas the class D limits are given in power related terms. Therefore, for a low power converter, class D limits seem to be stricter. Also, class D applies to equipment with input power $P_{in} \leq 600$ W that can be shown to have a pronounced effect on the public supply system.

Table 2.1. Harmonic limits for class A devices, IEC 2000.

Harmonic order ***n***	**Maximum permissible harmonic current** A
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \le n \le 39$	$0.15\frac{15}{n}$
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \le n \le 40$	$0.23\frac{8}{n}$

Table 2.2. Limits for class D equipment, IEC 2000.

Harmonic order ***n***	**Maximum permissible harmonic current per watt** mA/W	**Maximum permissible harmonic current** A
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \le n \le 39$ (odd harmonics)	$\frac{3.85}{n}$	See Table 2.1

2.2 Line harmonics in switched mode power supplies

Switched mode power supplies are notorious for having a distorted input current, which is rich in harmonic currents. A high harmonic content of the input current of a power converter reduces the available power, which can be drawn from the utility grid. The harmonic components of the current also pollute the utility grid, Redl et al. 1995b, which can cause malfunction in sensitive electrical equipment connected to the same grid.

A typical non-power factor corrected front-end power converter is depicted in Fig. 2.1.

The input side of the converter in Fig. 2.1 presents a combination of a large energy storage capacitor and a diode bridge. The diode bridge is composed of the four rectifier diodes, D_{R1}, D_{R2}, D_{R3} and D_{R4}, and it is the power supplies' interface to the mains.

Capacitor voltage v_C of capacitor C_1 is the input voltage for the high frequency dc-dc conversion stage of the converter. This stage consists of the transformer, switch and the whole secondary side of the circuit. The bulk capacitor, C_1, should be able store enough energy to cover a momentary blackout of the power grid, Mohan et al. 1995 page 347, and it should also be able to balance the fluctuation of input power at twice the line frequency. Therefore, the bulk capacitor, C_1, usually has a relatively high capacitance.

The combination of a large capacitor and the diode bridge is the cause for the distortion in the line current. This is because the diodes in the bridge are able to conduct and deliver energy from the mains to the circuit only when the rectified sinusoidal line voltage, $|v_{in}|$, has a greater value than capacitor voltage v_C. Since C_1

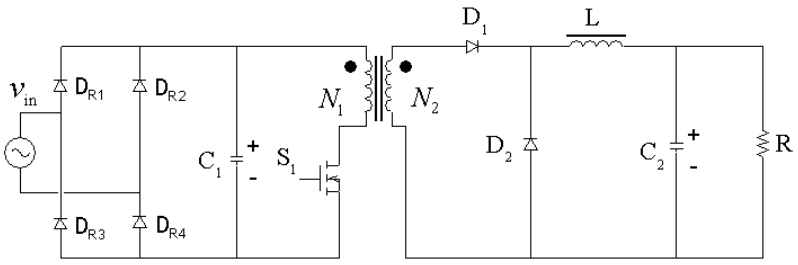

Figure 2.1. A forward type SMPS used as a front-end converter.

has a relatively high capacitance, the voltage of it does not drop considerably during two consecutive peaks of the line voltage, i.e. during a half line cycle. The time interval during which the rectified sinusoidal line voltage has a higher value than the capacitor voltage is, therefore, rather short.

Simulated waveforms of line current i_{in}, capacitor voltage v_C and rectified line voltage $|v_{in}|$ in the case of a non-power factor corrected converter is shown in Fig. 2.2. Simulation parameters were: $V_{in,rms}$ = 230V, C_1 = 330 µF and the load was modeled as a 235 W constant power load.

The simulation result clearly shows that the current has a non-sinusoidal, distorted waveform. Rms values of the line frequency component and the six first odd harmonics of the line current, depicted in Fig. 2.2, are shown along with class D limits of standard IEC 61000-3-2 in the bar chart of Fig. 2.3. It is obvious that the device does not meet the limits set by the standard.

The harmonic components of the line current are at frequencies that are odd multiples of the line frequency. The harmonics are denoted as $I_{in,rms,n}$ where the letter n marks the frequency of the harmonic, which is the n:th multiple of the line frequency.

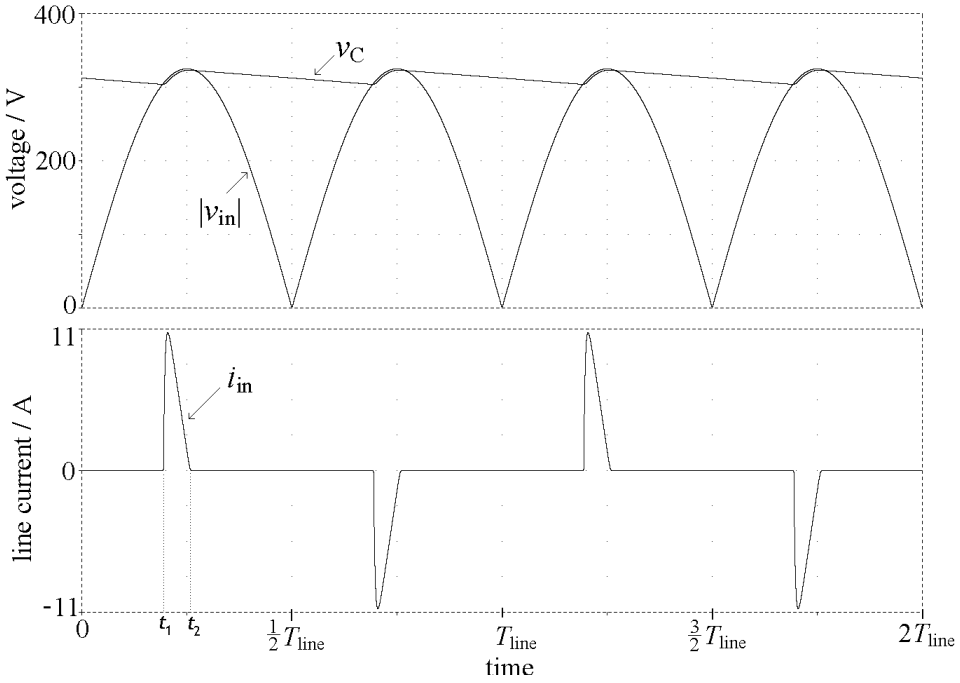

Figure 2.2. Rectified sinusoidal line voltage and the bulk capacitor voltage in the upper part and resulting line current in the lower part of the picture.

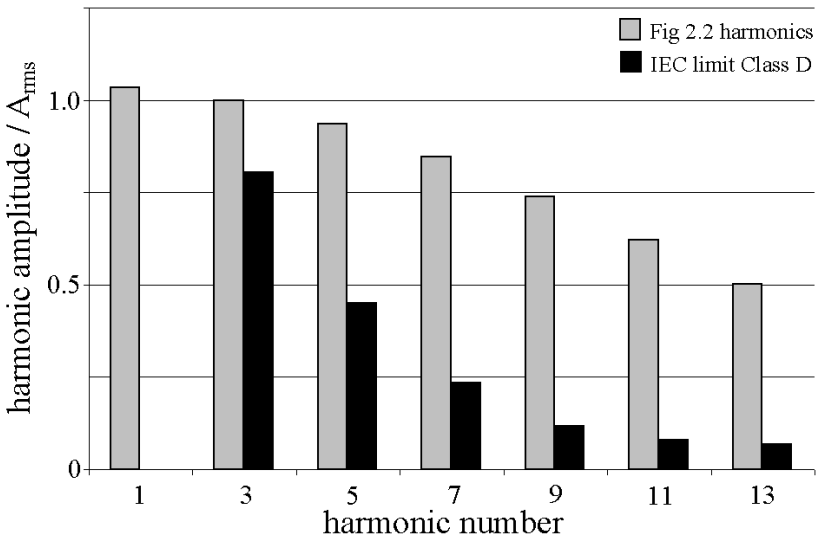

Figure 2.3. Line frequency component and the six first odd harmonics of the line current depicted in Fig. 2.2. Class D limits of standard IEC 61000-3-2 are also shown.

2.3 Basic definitions in power factor correction

The distorted line current, depicted in Fig. 2.2, has a relatively rich content of harmonics. The current is also said to have a high crest factor, Mohan et al. 1995, a quantity that describes the ratio of the peak value of the current to the total rms value of the current.

$$\text{Crest factor} = \frac{I_{\text{in,peak}}}{I_{\text{in,rms}}} \qquad (2.1)$$

The rich content of harmonics leads to a poor power factor (*PF*). Quantity *PF* is used to measure the ratio of power *P* to apparent power *S* drawn from the utility grid. *PF* is defined as follows, Mohan et al. 1995.

$$PF = \frac{P}{S} = \frac{V_{\text{in,rms,1}} I_{\text{in,rms,1}}}{V_{\text{in,rms}} I_{\text{in,rms}}} \cos\phi_1 \approx \frac{I_{\text{in,rms,1}}}{I_{\text{in,rms}}} \cos\phi_1 \qquad (2.2)$$

In Eq. (2.2) $V_{\text{in,rms}}$ and $V_{\text{in,rms,1}}$ are the rms values of the line voltage and line frequency component of the line voltage, respectively, and $I_{\text{in,rms}}$ and $I_{\text{in,rms,1}}$ are defined correspondingly. Parameter ϕ_1 depicts the difference in phase between the fundamental components of the line voltage and line current, that is between $v_{\text{in,1}}$ and $i_{\text{in,1}}$. It is assumed in Eq. (2.2) that the line voltage is not distorted.

The cosine of the phase difference ϕ_1 is called displacement power factor *DPF,* Mohan et al. 1995.

$$DPF = \cos\phi_1 \qquad (2.3)$$

In power supply applications, the displacement ϕ_1 between the line frequency components is usually close to zero. Quantity *PF* can hence be approximated with good accuracy in power supply applications by the ratio of the two currents in Eq.(2.2). Therefore, a good *PF* is achieved if the harmonic content is reduced in relation to the line frequency component of the line current.

Total harmonic distortion (*THD*) measures the ratio of the total rms value of the harmonic currents to the rms value of the line frequency component, Mohan et al. 1995.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_{\text{in,rms},n}^2}}{I_{\text{in,rms},1}} \qquad n = 3,5,7... \qquad (2.4)$$

If the line voltage is not distorted, *PF* and *THD* share the following relationship, Mohan et al. 1995.

$$PF = \frac{1}{\sqrt{(1+THD^2)}} DPF \qquad (2.5)$$

3 Single-stage power factor correction circuits

3.1 General

The family of single-stage converters is an interesting alternative to low-cost power factor correction. A variety of suitable topologies of single-stage converters can be found from literature, for example: Cha et al. 1998, Garcia et al. 1999, Garcia et al. 2000, Jin et al. 2001, Lee et al. 1996, Lee et al. 1997, Madigan et al. 1992, Oba et al. 1998, Redl et al. 1994, Brkovic et al. 1992 and Takahashi et al. 1991.

Properties of and design considerations for a number of single-stage converters have been reported in literature, for example: Jovanović 1994, Newton 2000, Simonetti 1992 and Redl 1995a.

The distinctive property of a single-stage converter is that it has only one active switching element. The active element is used, on one side, to regulate the isolated output voltage as in a normal power supply. The other task for the active element is to shape the line current to resemble as closely as possible the sinusoidal line voltage waveform. There are, hence, two tasks for the one switching element. This means that the other goal has to be reached more or less inherently.

Single-stage converters, in most cases, utilize the fact that the envelope of a discontinuous conduction mode (DCM) inductor current automatically follows the feeding voltage waveform, Liu et al. 1989, Lazar et al. 1995 and Wang et al. 1996. There are also reports of discontinuous capacitor voltage mode PFC circuits, Grigore et al. 1999a, Grigore et al. 1999b and Grigore 2001.

Line current shaping in single-stage converters can, therefore, be dealt with by allowing the input side reactive element to operate in the DCM. The one degree of freedom, duty ratio of the active switch in constant frequency applications, is used to regulate the output voltage. We will assume in the following analyses of the three single-stage converters that they operate, in steady state, with constant duty ratio D_1.

We do not go into detail of the power factor correction properties of the single-stage converters presented in this Thesis. Instead, we assume that a fairly good line current, that satisfies the requirements of the standard, is reachable with these three single-stage converters.

As an example of the PFC properties of a single-stage converter, the line current of a constant duty ratio BIFRED converter, with input power $P_{in} \approx 235$ W, is shown in Fig. 3.1 a). It can be seen from the figure that the current resembles closely the desired sinusoidal waveform. The fundamental component and the first six harmonics of the current, shown in Fig. 3.1 a), are shown along with class D limits of standard IEC 61000-3-2 in Fig. 3.2, Tuomainen 1999. It is easy to see that the converter fulfills the requirements set by the standard. Fig. 3.1 b) shows the current of the BIFRED's DCM boost inductor.

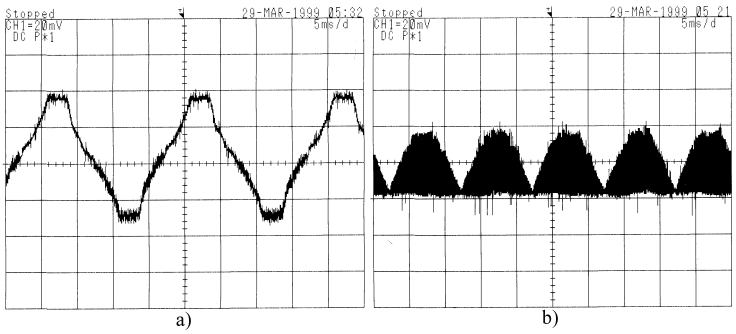

Figure 3.1. Line current in a) and boost inductor current in b) of constant duty ratio BIFRED converter, Tuomainen 1999. Scale in a) 1 A/div and in b) 2 A/div.

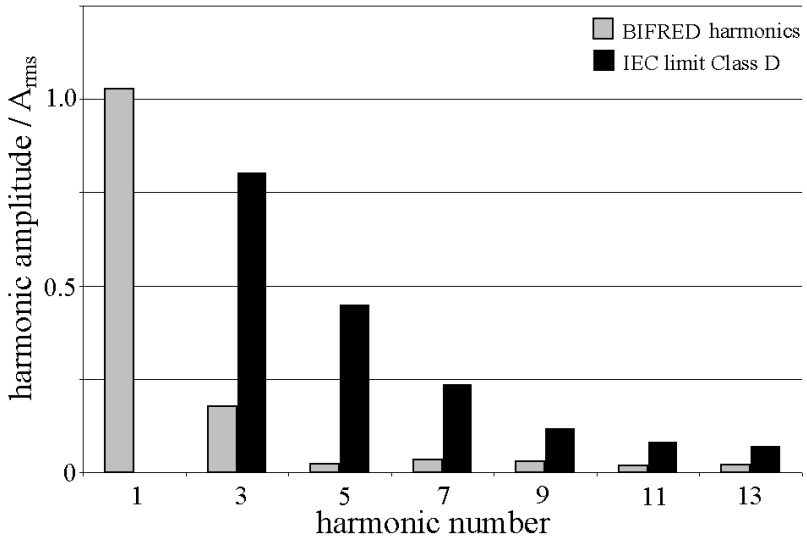

Figure 3.2. Line frequency component and six first harmonics of the line current in Fig. 3.1. a), Tuomainen 1999.

3.2 Dither converter

3.2.1 General

The dither converter, Oba et al. 1998, is an interesting candidate for a single-stage power factor correction converter. A schematic of the converter is shown in Fig. 3.3. The converter is a buck-boost type single-stage converter in which the power factor correction is dealt with by allowing inductor L_1 to operate in the DCM.

The converter can be designed so that the forward part of the converter operates in the continuous conduction mode (CCM). This is due to the fact that capacitor C_1 is not charged directly from the mains and, therefore, the steady state voltage of the capacitor can be considerably lower than the peak of the line voltage.

Usually, in single-stage converters in which the isolation part of the converter operates in the CCM the bulk capacitor voltage has a strong dependence on the load.

That means that the voltage may reach a relatively high level at light loads, which means that the energy storage capacitor has to sustain the voltage stress. Naturally, a high initial voltage on the capacitor aggravates the situation.

The capacitor voltage in the dither converter is, also, dependent on the load but since the voltage can have low steady state values at high loads, there is room for it to rise as a consequence of load reductions. This situation is difficult to achieve, for example, in the BIFRED and BIBRED single-stage converters, in which the minimum primary side energy storage capacitor voltage has to be greater than the peak line voltage. This will be discussed later in Section 3.3.

As mentioned above, the dither converter can be designed to operate in the DCM – CCM operation mode. This allows for smaller current ripple as well as smaller high

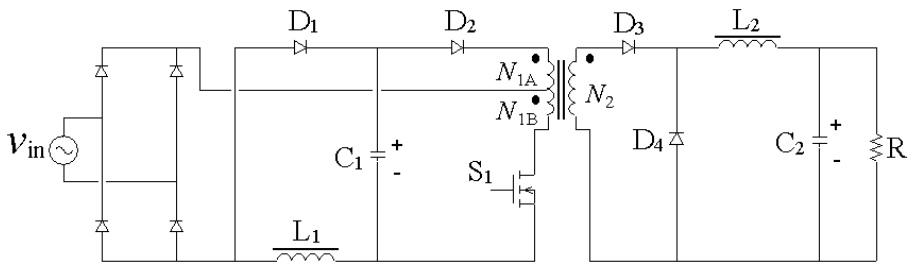

Figure 3.3. Dither converter with a tapped transformer, Oba et al. 1998.

frequency flux swinging in the output inductor. This eventually reduces conduction losses in the transformer and in the secondary side and core losses in the inductor. Also, a current with lower ripple reduces the need for filtering capacity.

The research reported in this Thesis, concerning the dither converter with a tapped transformer, is concentrated on finding a steady state representation and a small signal model for the converter. In the following two sections the principles and derivation of the steady state and small signal models of the dither converter, are presented respectively.

3.2.2 Steady state analysis

The tapping in the transformer of the converter disables the diode bridge at low instantaneous line voltage values. This introduces zero crossing distortion to the line current. The diode bridge is able to conduct, and power flow to the circuit is enabled, when the instantaneous line voltage is above the following limit:

$$|v_{\text{in}}| > \frac{N_{1B}}{N_1} V_{C1} = \frac{N_{1B}}{N_{1A} + N_{1B}} V_{C1} \qquad (3.1)$$

Line voltage, during a half line cycle, is illustrated in Fig. 3.4. Angles α and (π - α), which denote the points at which the line voltage crosses the level that enables/disables diode bridge are also drawn in the figure. The sine of angle α can be defined as follows:

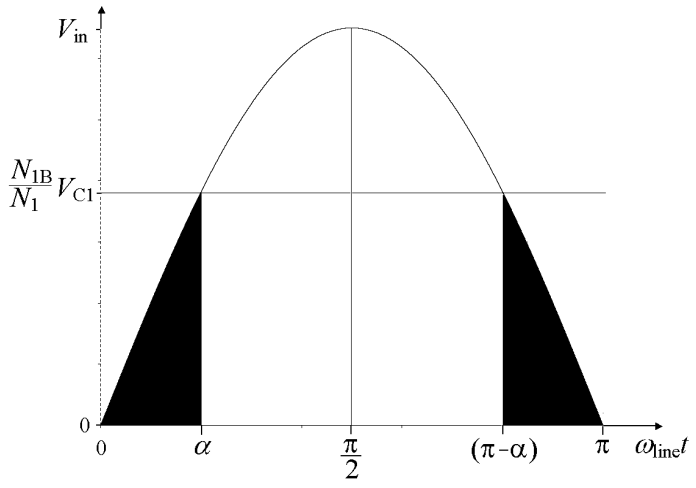

Figure 3.4. Line voltage during a half line cycle. Black areas indicate the portions of a half line cycle during which the diode bridge is not able to conduct.

$$\sin(\alpha) = \frac{N_{1B}}{N_1}\frac{V_{C1}}{V_{in}} = \frac{N_{1B}}{N_2}\frac{V_{out}}{V_{in}}\frac{1}{D_1} \qquad (3.2)$$

D_1 in Eq.(3.2) denotes the duty ratio of the switch.

Some principles of the steady state operation of the dither converter were reported in Oba et al. 1998, Tuomainen 1999 and Tuomainen et al. 1999. There was, however, no accurate and complete analysis available on this topic in the literature. Therefore, the steady state operation of this converter was investigated and the results of the analysis are reported in publication P[1].

The steady state analysis was made for an ideal converter, therefore the following assumptions were made: the switch, diodes and reactive components were treated as ideal components. Additionally, it was assumed that the capacitances of the two energy storage capacitors of the circuit, C_1 and C_2, were large enough so that the voltage over them was considered a ripple free dc voltage and that the output inductor current i_{L2} was constant. It should be noted that despite these assumptions the simulations that were made with non-ideal semi-conductor component models and capacitor and inductor models with finite capacitances and inductance returned results that were very close to the computed results based on the analysis.

The idea behind the analysis was to average the operation of the converter over a switching cycle, i.e. to define the current that was taken from and brought to capacitor C_1 during switching cycle T_s. The average current that is taken from the capacitor can be expressed as follows:

$$\left\langle i_{C1,-} \right\rangle_{T_s} = \left(\frac{N_2}{N_1}\right) I_0 D_1 \qquad 0 \le \omega_{line} t \le \alpha \qquad (3.3)$$

$$\left\langle i_{C1,-} \right\rangle_{T_s} = \left(\frac{N_2}{N_1}\right) I_0 D_1 - \frac{1}{2}\left(\frac{N_{1B}}{N_1}\right) I_{L1} D_1 \qquad \alpha < \omega_{line} t \le \frac{\pi}{2} \qquad (3.4)$$

Similarly, the current that is brought to the capacitor during a switching cycle can formulated as follows:

$$\left\langle i_{C1,+} \right\rangle_{T_s} = 0 \qquad 0 \le \omega_{line} t \le \alpha \qquad (3.5)$$

$$\left\langle i_{C1,+} \right\rangle_{T_s} = \frac{1}{2} I_{L1} D_2 \qquad \alpha < \omega_{line} t \le \frac{\pi}{2} \qquad (3.6)$$

Both of the two currents have to be expressed in two parts. The reason for this is the disabled diode bridge at low instantaneous line voltage values.

It can be noted from Eqs. (3.3 – 3.6) that the average currents that charge and discharge the capacitor are not equal from switching cycle to switching cycle. Therefore, the steady state operating point had to be defined by averaging the operation of the converter over a line cycle.

Calculated behavior of the bulk capacitor voltage of the dither converter is shown in Fig. 3.5. The capacitor voltage was determined as a function of load in eight different winding arrangements, which are listed in Table 3.1. Additionally, fifteen simulated points have been added to the figure. As can be seen from Fig. 3.5 the calculated and simulated results are in good agreement.

Details and results of the steady state analysis are presented in publication P[1].

Table 3.1. Turns ratios of the transformer used in the simulations.

Model	a	b	c	d	e	f	g	h
N_2 / N_1	1.25	1.25	1.25	1.25	1.25	1.25	1.25	1.25
N_{1B} / N_1	0	0.25	0.35	0.42	0.50	0.57	0.63	0.69
N_2 / N_{1B}	-	5.00	3.57	3.00	2.50	2.19	2.00	1.80

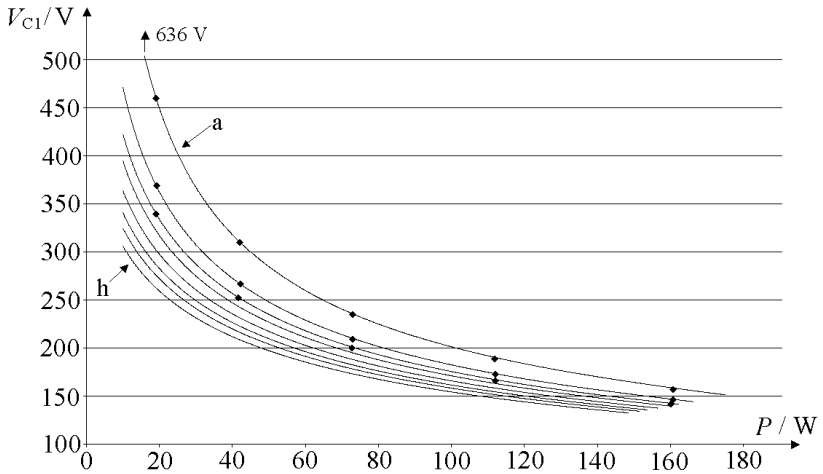

Figure 3.5. Calculated behavior of the bulk capacitor voltage in eight cases. Fifteen simulated points have been added.

3.2.3 Small signal analysis

Once the steady state operation of the converter had been investigated, the next step was to find a small signal description for the converter. The need for the dynamic model of the converter stemmed from the fact that there were no reports of the dynamic behavior of the converter available in literature.

The small signal analysis was made for an ideal converter model. The only parasitic element that was included in the analysis was the equivalent series resistance (ESR) of the output capacitor.

It should be noted, that the small signal model was analyzed only for the case when the line voltage is as in Eq. (3.1), i.e. the diode bridge is able to conduct. This decision was made since firstly, the converter operates most of the time in this operation mode and secondly, the small signal model of the converter at low instantaneous values of the line voltage resembles a normal forward converter fed by a large dc capacitor, which does not, however, receive any charge to compensate for the energy delivered to the load.

The chosen method for the small signal analysis was state space averaging, Cúk et al. 1977a. Due to the discontinuity of the input side inductor we had to use state space averaging for converters in discontinuous mode, Cúk et al. 1977b. State space averaging and derivation of a small signal model for single-stage converters with multiple discontinuous conduction modes are reported in Schenk et al. 1997 and Schenk et al. 1998.

We identified four reactive components in the circuit, magnetizing inductance of the transformer was omitted, and voltages of the two capacitors and currents of the two inductors were chosen as state variables.

$$\mathbf{x} = \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix}, \quad \dot{\mathbf{x}} = \frac{d}{dt}\mathbf{x} \tag{3.7}$$

The matrices that describe the three states, depicted in Fig. 3.6, of the converter during a switching cycle can be written as follows:

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 & -\frac{N_B}{L_1} & 0 \\ 0 & 0 & \frac{N}{L_2} & -\frac{r_p}{L_2} \\ \frac{N_B}{C_1} & -\frac{N}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{(R+R_s)C_2} \end{bmatrix} \quad (3.8)$$

$$\mathbf{A}_2 = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & -\frac{r_p}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{(R+R_s)C_2} \end{bmatrix} \quad (3.9)$$

$$\mathbf{A}_3 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{r_p}{L_2} \\ 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{(R+R_s)C_2} \end{bmatrix} \quad (3.10)$$

$$\mathbf{B}_1 = \begin{bmatrix} (L_1)^{-1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \mathbf{B}_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}, \mathbf{B}_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (3.11)$$

The following markings were used in Eqs. (3.8 – 3.11) in order to simplify the representation:

$$\frac{N_{1B}}{N_1} = N_B, \quad \frac{N_2}{N_1} = N, \quad r_p = \frac{R}{R+R_s} \quad (3.12)$$

The relative lengths of the three different states during a switching cycle can be denoted as d_1, d_2, and d_3 and they are defined as follows:

$$
\begin{aligned}
d_1 &= D_1 + \hat{d}_1 \\
d_2 &= D_2 + \hat{d}_2 \\
d_3 &= D_3 + \hat{d}_3 \\
d_1 + d_2 + d_3 &= 1
\end{aligned}
\qquad (3.13)
$$

The small signal state space representation for the converter can be written as follows, Cúk et al. 1977b:

$$
\dot{\hat{\mathbf{x}}} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{v}_{\text{in}} + \hat{d}_1\left[\left(\mathbf{A}_1 - \mathbf{A}_3\right)\mathbf{X} + \left(\mathbf{B}_1 - \mathbf{B}_3\right)V_{\text{in}}\right] + \hat{d}_2\left[\left(\mathbf{A}_2 - \mathbf{A}_3\right)\mathbf{X} + \left(\mathbf{B}_2 - \mathbf{B}_3\right)V_{\text{in}}\right] \qquad (3.14)
$$

in which matrices **A** and **B** are defined as:

$$
\begin{aligned}
\mathbf{A} &= d_1\mathbf{A}_1 + d_2\mathbf{A}_2 + d_3\mathbf{A}_3 \\
\mathbf{B} &= d_1\mathbf{B}_1 + d_2\mathbf{B}_2 + d_3\mathbf{B}_3
\end{aligned}
\qquad (3.15)
$$

The analysis resulted in control-to-output open-loop transfer function for the converter, which has the following form:

$$
\frac{\hat{v}_2}{\hat{d}_1} = \frac{\left(Fs + G\right)}{\left(As^3 + Bs^2 + Cs + D\right)} \qquad (3.16)
$$

Coefficients for Eq. (3.16) are as follows:

$$
\begin{aligned}
A &= \frac{L_2C_2C_1}{ND_1} \\
B &= \frac{L_2C_2}{ND_1}\left[\frac{1}{\left(R + R_{\text{s}}\right)}\frac{C_1}{C_2} + \frac{I_1}{V_1}\left(N_{\text{B}}D_1 + D_2\right) + \frac{I_1}{\left(V_{\text{in}} - N_{\text{B}}V_1\right)}N_{\text{B}}\left(N_{\text{B}}D_1 + D_2\right)\right] \\
C &= \frac{1}{ND_1}\left[C_1r_{\text{p}} + \frac{I_1}{V_1}\frac{L_2}{\left(R + R_{\text{s}}\right)}\left(N_{\text{B}}D_1 + D_2\right) + \frac{I_1}{\left(V_{\text{in}} - N_{\text{B}}V_1\right)}\frac{L_2}{\left(R + R_{\text{s}}\right)}N_{\text{B}}\left(N_{\text{B}}D_1 + D_2\right) + C_2\left(ND_1\right)^2\right] \\
D &= \frac{1}{ND_1}\left[\frac{I_1}{V_1}\left(N_{\text{B}}D_1 + D_2\right)r_{\text{p}} + \frac{I_1}{\left(V_{\text{in}} - N_{\text{B}}V_1\right)}r_{\text{p}}N_{\text{B}}\left(N_{\text{B}}D_1 + D_2\right) + \frac{1}{\left(R + R_{\text{s}}\right)}\left(ND_1\right)^2\right] \\
F &= C_1V_1\frac{1}{D_1} \\
G &= \left(\frac{V_{\text{in}}}{V_1} + 2\frac{D_2}{D_1} + N_{\text{B}}\left(1 + D_1\right) + \frac{V_1}{\left(V_{\text{in}} - N_{\text{B}}V_1\right)}\frac{N_{\text{B}}\left(N_{\text{B}}D_1 + D_2\right)}{D_1}\right)I_1 - NI_2
\end{aligned}
\qquad (3.17)
$$

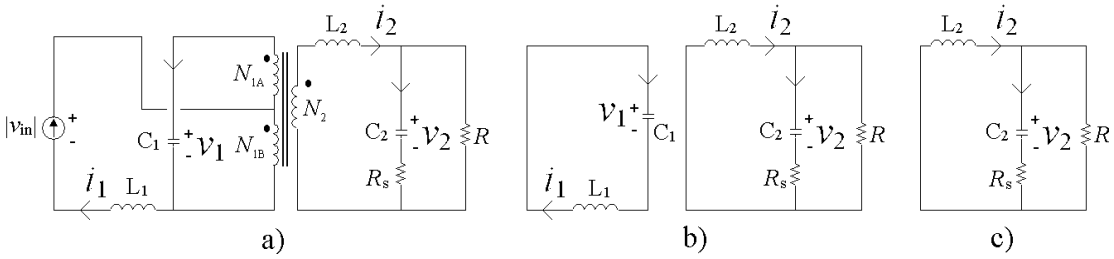

Figure 3.6. Equivalent circuits of the dither converter during a switching cycle. Line voltage v_{in} is sufficiently high. a) switch on, b) switch off and c) switch off and $i_1 = 0$.

Derivation of the small signal model for the dither converter is given in publication P[2].

Simulation setup for determining the small signal transfer function

The small signal analysis was verified with simulations in a PSpice simulation environment. A converter model was built using near ideal components, i.e. the diodes and the switch had a voltage drop when conducting but not, for example, parasitic capacitances. Additionally, small resistances had to be added in series with the reactive components in order to run the simulations properly.

Due to the time-varying line voltage and due to the limited simulation time, a noise component at the target frequency was observed at the simulated output even without any disturbance in the control voltage. Therefore, for each simulated point shown in publication P[2] six separate simulations were carried out: one without control disturbance and five with a control disturbance with five different initial angles of $\phi_C = 0^o$, 45^o, 90^o, 135^o and 180^o.

Simulation setup for the case without a control disturbance is depicted in Fig. 3.7 a). In this case, a constant control voltage V_C was used to generate constant duty ratio D_1. Simulation setup for the case with a control disturbance is depicted in Fig. 3.7 b), in which a low-amplitude control disturbance was added on the top of the control voltage.

Generation of the duty ratio from the control voltage with the help of a sawtooth waveform is shown in Fig. 3.8.

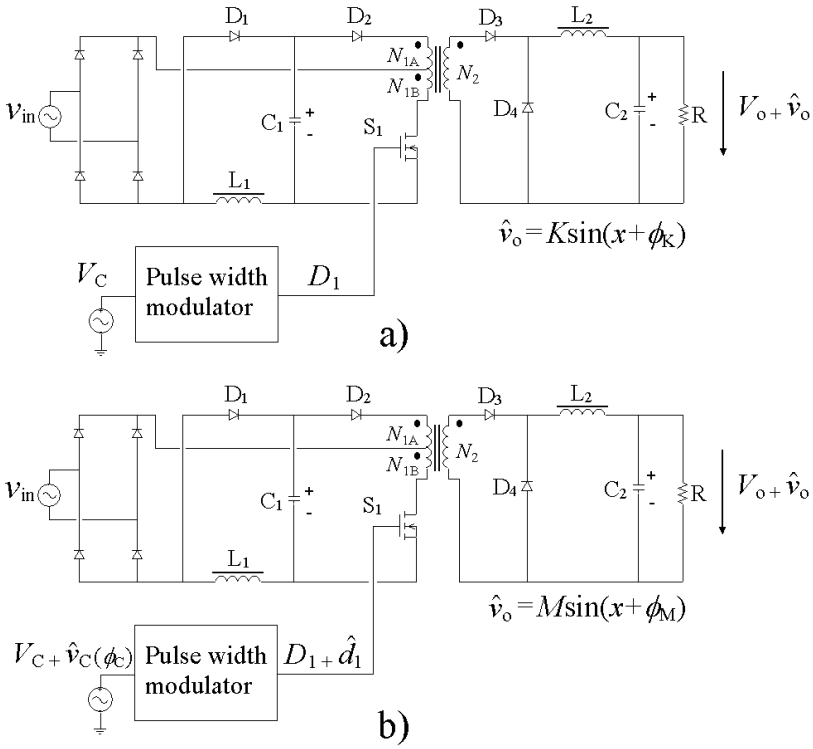

Figure 3.7. a) Simulation setup without a control disturbance and b) setup with a control disturbance.

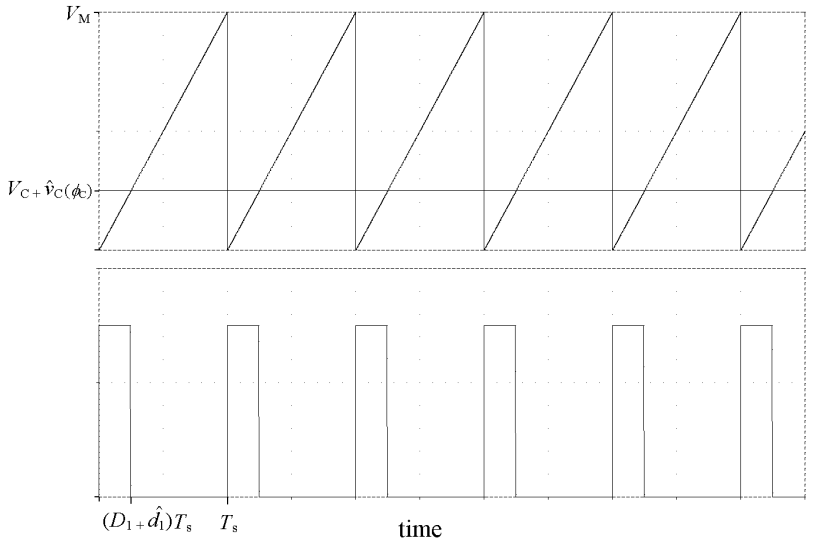

Figure 3.8. Sawtooth waveform, control voltage and the resulting duty ratio.

The control disturbance and the disturbance in the duty ratio share the following relation, Erickson et al. 2001 pp. 255.

$$D_1 + \hat{d}_1 = \frac{V_C + \hat{v}_C}{V_M} \qquad (3.18)$$

Amplitude of the sawtooth waveform, V_M, was in the simulated case V_M = 1V, which means that the control disturbance and the disturbance in the duty ratio shared the same magnitude.

When the control disturbance was present, the observed, simulated output at the disturbance frequency was a sum of the noise observed without the disturbance and the component that was due to the disturbance for the control signal. The propagation of the control-to-output disturbance could then be extracted from the simulation data by finding a suitable angle and amplitude, ϕ_L and L, for the control-to-output disturbance component.

$$M\sin(x+\phi_M) = K\sin(x+\phi_K) + L\sin(x+\phi_L) \qquad (3.19)$$

In Eq. (3.19) K and M are the amplitudes of the noise at the output without and with the control disturbance. Angles ϕ_K and ϕ_M are the corresponding phases for the two components observed at the output. The amplitude and angle for the disturbance at the output was obtained graphically, i.e. by matching two sinusoidal waveforms.

An example of the extraction of the control-to-output disturbance at frequency 1721 Hz is presented in Table 3.2. The first column of Table 3.2 gives the initial settings for the simulation, the second, third and fourth column gives the data obtained from the simulations. The fifth and sixth columns give the wanted data that was extracted by trial and error from the simulation data.

It should be noted that the control-to-output phase difference, which is given in the seventh column, is obtained by subtracting the extracted phase ϕ_L (sixth column) from the phase of the simulated control disturbance (second column). The reason for this is that the fourier analysis of PSpice program, despite the initial settings (given in the first column), returned, in this simulation example, the initial phase for the control disturbance –66,61^o degrees shifted (second column).

By using this method to determine the propagation of a small disturbance in the control signal to the output voltage we were able to verify the analysis. As can be seen from Fig. 3.9, the obtained simulation results correspond to the computed and expected behavior of the converter with good accuracy.

The computed gains and phases of the transfer function in Fig. 3.9 have been determined for six different instantaneous values of the line voltage, which are listed in Table 3.3.

Table 3.2. Simulation results for determining control-to-output gain and phase of the dither converter at frequency 1721 Hz.

$\hat{v}_C$ / mV	$\phi_{C,sim.}$	M / mV	ϕ_M	$L = \hat{v}_2$ / mV	ϕ_L	ϕ_{v2} *
0.5 ($\phi_C = 0^o$)	-66,61^o	80,2	105,8	118	-235	-168,39
0.5($\phi_C = 45^o$)	-21,61 ^{o}	56,74	165,5	106,8	-199	-177,39
0.5 ($\phi_C = 90^o$)	23,39 ^{o}	98,13	-113,6	110	-140	-163,39
0.5 ($\phi_C = 135^o$)	68,39 ^{o}	121,1	-69,89	93,5	-92	-160,39
0.5 ($\phi_C = 180^o$)	113,4 ^{o}	170,5	-34,11	121,5	-38,5	-151,9 ^{o}
Average of L and ϕ_{v2} were used			**Avg.**	**110 mV ⇒ 46,8db**	-	**-164,3 ^{o}**

*$\phi_{v2} = \phi_L - \phi_{C,sim}$

K = 50,23 mV, ϕ_K = -23,11^o

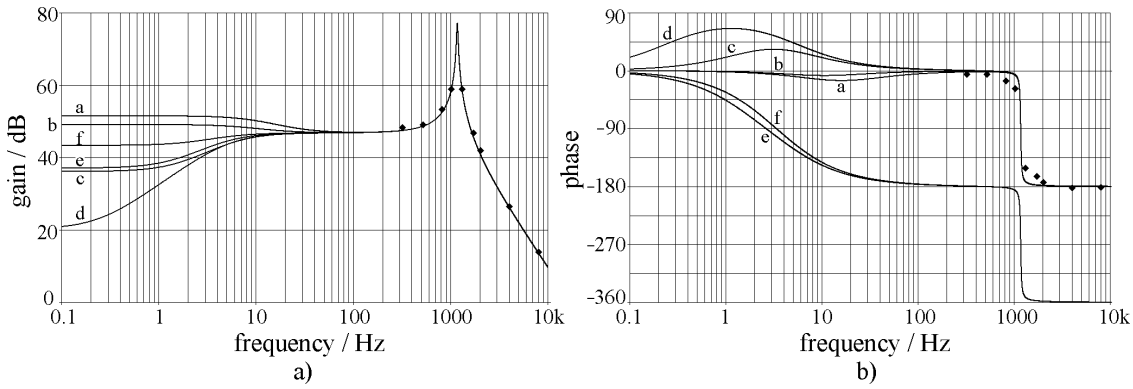

Figure 3.9. Computed gain and phase of the control-to-output transfer function, D_1 = 0.25. Nine simulated points have been added to the figure.

Table 3.3. Instantaneous line voltage values used in the calculations.

Symbol	**a**	**b**	**c**	**d**	**e**	**f**
V_{in} / V	325	265	165	145	115	85

3.3 BIFRED and BIBRED converters

3.3.1 General

The BIFRED (Boost Integrated with Flyback Recitifier/Energy storage/Dc-dc converter) and BIBRED (Boost Integrated with Buck Rectifier/Energy storage /Dc-dc converter) are two single-stage converters, first presented by Madigan et al. 1992 and 1999. Both converters are capable of producing an input current with a low harmonic content and, also, a regulated and isolated output voltage. Line current shaping, i.e. power factor correction, and the output voltage regulation are attained in these two converters by using only one switch.

As mentioned in Section 3.2, the dither converter can be designed to operate in the DCM – CCM and that it is difficult to achieve the same situation with the BIFRED and BIBRED. For example, for European line voltage, the peak of the line voltage is $V_{\text{in}} \approx 325$ V, above which the bulk capacitor voltage of the BIFRED and BIBRED should be. Electrolytic capacitors for power electronic equipment, however, tend to have a limit for maximum voltage at around 450 - 500 V, Sarjeant et al. 2001 and Stevens et al. 2002. This voltage limit for the electrolytic capacitors is easily exceeded with European line voltage and with DCM – CCM BIFRED and BIBRED converters.

It is, therefore, reasonable to design the BIFRED and BIBRED converters to operate in the DCM – DCM mode, which means that the input inductor and the output inductive element both operate in the DCM mode. For this reason, we have assumed in our analyses that these two converters operate in the DCM – DCM operation mode.

It should be noted here, that the BIFRED converter bears a strong resemblance with the isolated version of the SEPIC converter. Also, the BIBRED converter resembles the isolated version of the Cúk converter.

Design considerations for the BIFRED converter were reported, for example, in Willers et al. 1994 and Willers et al. 1999. Small signal analysis of the SEPIC (BIFRED) converter was reported in Schenk et al. 1997.

Variable frequency control was researched for the BIBRED converter in Jovanović et al. 1994. Small signal dynamics of the isolated version of the Cúk converter (BIBRED) were reported in Vorperian 1996. Small signal considerations for

Cúk and SEPIC converters as power factor correction circuits were reported in Simonetti et al. 1992.

3.3.2 Research background

The BIFRED and BIBRED converters actually include two converters, which are integrated so that both of them utilize the same switch. The BIFRED converter is an integration of a discontinuous conduction mode (DCM) boost converter and a flyback converter. In the BIBRED, the corresponding parts are a DCM boost converter and a forward converter. Schematics of the BIFRED and BIBRED converters are shown in Fig. 3.10 a) and b), respectively.

The tight integration of the two sub-converters in these two single-stage converters causes some problems. One of them arises from the leakage inductance of the transformer, which has, in both converters, a pronounced effect on the voltage stress on the switch. Namely, the current in the leakage inductance has to be changed at turn-off instant of the switch from a positive peak value, i.e. the peak current of the transformer, to a negative peak value in a short period of time. The negative peak value means here the peak value of the DCM boost inductor current which is to be directed to flow through the primary winding of the transformer after the switch has been opened.

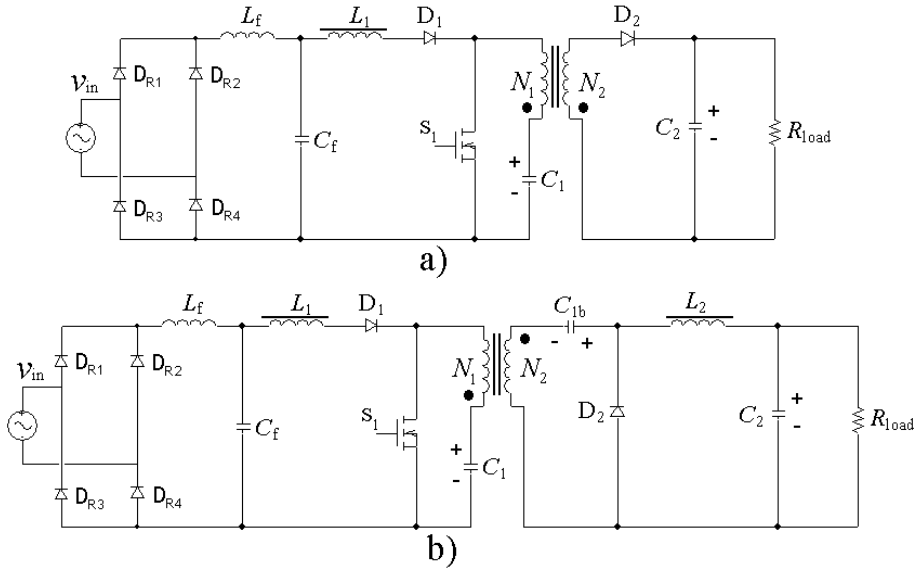

Figure 3.10. a) Schematic of the BIFRED converter and b) schematic of the BIBRED converter.

However, the boost inductor current cannot be immediately rerouted to flow through the winding due to the presence of the leakage inductance. Therefore, it is necessary to apply a voltage across the leakage inductance in order to achieve the desired change in the magnitude and flowing direction of the current. For that purpose a snubber circuit has to be employed, on one side, to provide the needed voltage and, on the other side, to provide an alternative path for the two inductive currents for the duration of the process of changing the direction of the current.

3.3.3 Resonant type snubber

A resonant type non-dissipative snubber was presented and analyzed for flyback converter in Shaughnessy 1980, Domb et al. 1982, Ninomiya et al. 1985 and Ninomiya et al. 1988, and for the forward converter in Tanaka et al. 1988. The references contain detailed analyses of the snubber for flyback and forward converters.

The same snubber circuit was proposed for BIFRED in Willers et al. 1999 and for BIBRED in Jovanović et al. 1994. The proposed snubber is, without doubt, a suitable circuit for the BIFRED and BIBRED topologies.

Previous studies, however, do not provide a detailed analysis of the circuit in these two single-stage converters, despite the fact that these two converters, due to the tight integration, pose a tougher challenge for the snubber than, for example, a flyback converter. Moreover, there are some differences in the operation of the snubber circuit in the BIFRED and BIBRED applications at turn-off instant of the switching device, which are due to the presence of the boost inductor and, therefore, two inductive currents.

The voltage produced by the snubber circuit is directly linked to the voltage stress on the switching device, and, consequently, the switch has to be selected so that it is able to withstand the expected voltage stress. However, a switch that can sustain high voltages tends to be more expensive or, at least, it tends to have a higher on-resistance than a switch with a lower voltage rating. Therefore, a switch with a lower voltage rating saves in the costs or improves the efficiency of the converter, or both. It was, therefore, important to analyze the operation of the non-dissipative snubber in the two single-stage converters and to find out the expected maximum voltage stress as a function of the circuit parameters.

The BIFRED and BIBRED converters with resonant type non-dissipative snubber circuits are presented in Figs. 3.11 a) and b), respectively.

Turn-off transition in BIFRED converter

The snubber circuit protects the switch from voltage spikes and provides a path for the two inductive currents right after the switch has been turned off. During a period that we call here turn-off transition, a voltage is developed in the snubber capacitor, which allows for the current in the leakage inductance to change appropriately. The turn-off transition initiates from the turn-off of the switch and ends when the current in the leakage inductance has changed its direction and magnitude appropriately.

The turn-off transition is divided into two phases that we call here the first and the second phase. The first phase begins when the main switch is turned off and it ends when the snubber capacitor has been charged to a voltage level that allows for the secondary side diode, D_2, to become forward biased. The equivalent circuit of the BIFRED converter during the first phase is shown in Fig. 3.12 a).

The second phase of the turn-off transition begins, naturally, at the end of the first phase and it ends when snubber diode D_{sn1} becomes reverse biased. Equivalent circuit of the BIFRED converter during the second phase is shown in Fig. 3.12 b).

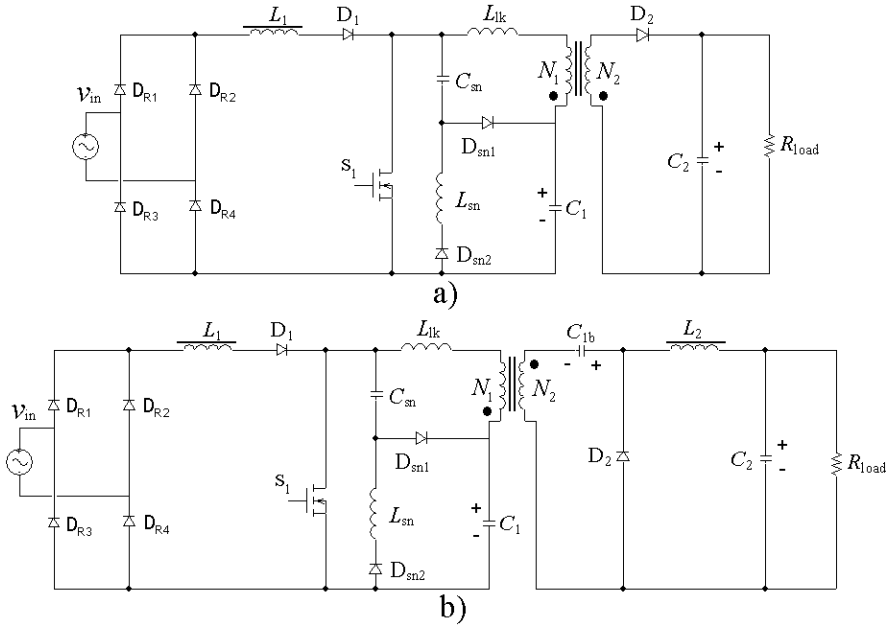

Figure 3.11. a) BIFRED and b) BIBRED with non-dissipative snubber circuit.

Simulated waveforms of the voltage and current of the snubber capacitor and current of the leakage inductance during the first phase ($0 \le t \le t_1$) and second phase ($t_1 \le t \le t_2$) of the turn-off transition are depicted in Figs. 3.13 a) and b).

It can be seen from the figure that the bulk of the needed change in the current of the leakage inductance, $i_{L,lk}$, takes place during the second phase. On the other hand, the snubber capacitor is being charged with a nearly constant current during the whole of the first phase.

A simulated example of the voltage stress over the switch of the BIFRED converter is shown in Fig. 3.14. The figure shows the voltage stress in four different cases. Line voltage v_{in} in Fig 3.14 a) is approximately zero and in b) in the vicinity of the peak line voltage.

It can be seen from Fig. 3.14 that a rapid turn-off transition requires small capacitance C_{sn}. A small capacitance, however, causes a relatively high voltage stress over the switch. On the other hand, a lower voltage stress is attainable with a larger C_{sn}. This, however, lengthens the duration of the turn-off transition, which can become relatively long, especially at low line voltages.

A detailed analysis of the non-dissipative snubber for the BIFRED and BIBRED converters can be found from publication P[3].

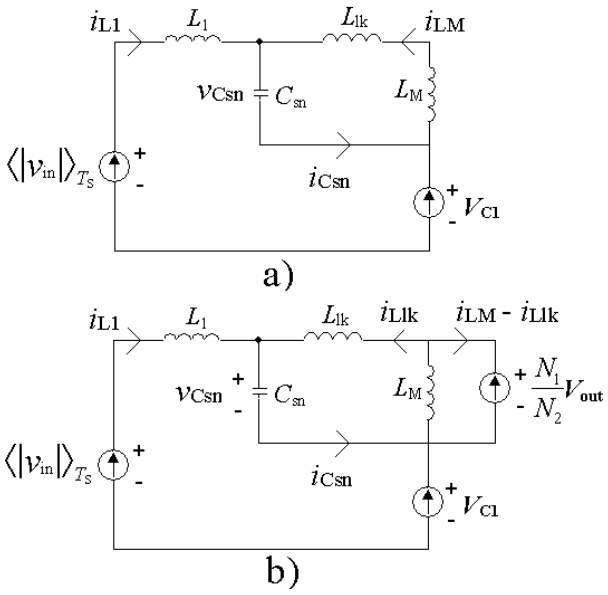

Figure 3.12. a) Equivalent circuit of BIFRED: a) during the first phase, and b) during the second phase of the turn-off transition.

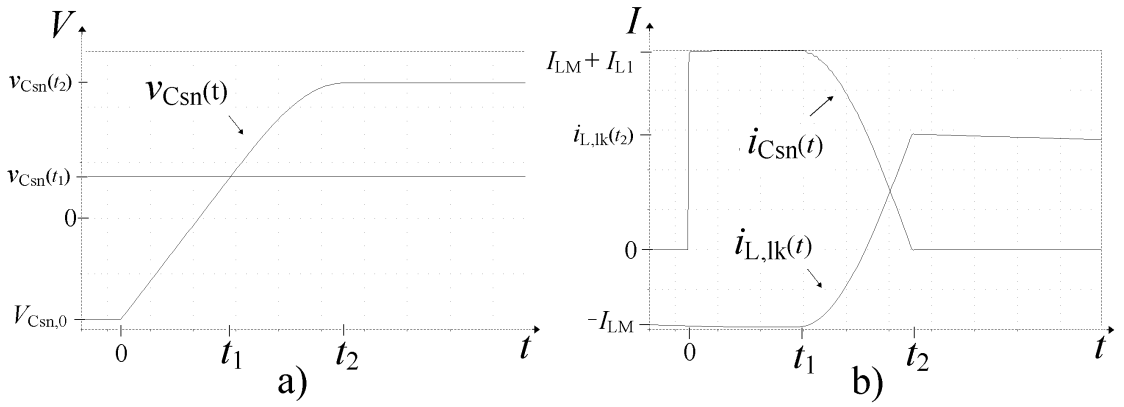

Figure 3.13. a) Simulated voltage of the snubber capacitor and b) simulated current of the snubber capacitor and the leakage inductance during the turn-off transition.

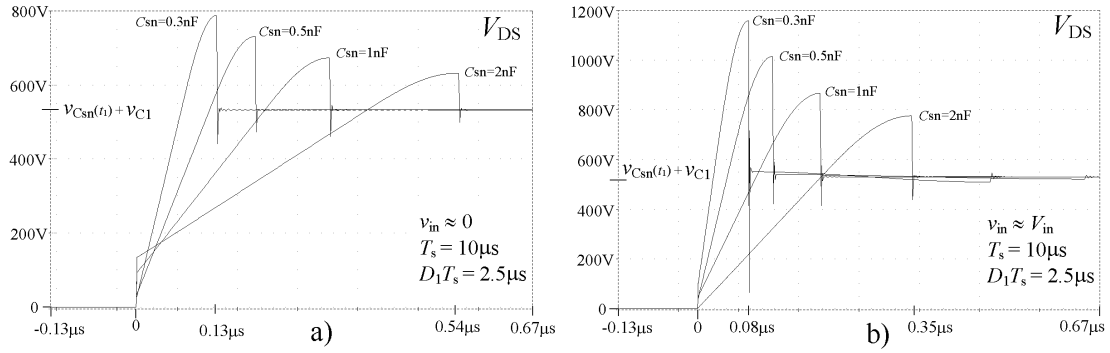

Figure 3.14. Simulated voltage over the switch of BIFRED at turn-off: a) $v_{in} \approx 0$ V and b) $v_{in} \approx 325$ V . Snubber capacitances: C_{sn} = 0.3 nF, 0.5 nF, 1 nF, and 2 nF.

3.3.4 Passive clamp circuit for BIFRED

As mentioned above, the BIFRED converter poses a tougher challenge for the snubber circuit than, for example, a flyback converter. This is due to the fact the direction of the current in the leakage inductance of the transformer has to be changed rather than to merely suppress it to zero after the switch has been turned off. For this reason, the voltage stress on the switching device may become unnecessarily high.

With the resonant type non-dissipative snubber, a switch with a relatively high voltage rating has to be used and this degrades the efficiency of the converter as explained above.

It might be, therefore, advantageous to clamp the voltage over the switch at turn-off to a known dc voltage rather than to charge the resonant snubber, from a negative initial voltage, to a high and somewhat unknown positive voltage at every turn-off.

We developed and presented in publication P[4] a passive clamp circuit for the BIFRED converter. It should be mentioned, however, that the circuit could be used for the BIBRED converter as well.

The BIFRED converter with the passive clamp circuit is presented in Fig. 3.15. The schematic of the passive clamp circuit is similar to that of the resonant snubber circuit.

The idea in the passive clamp solution is that the circuit is designed so that clamp capacitor C_{sn} retains a steady dc voltage. Therefore, the voltage over the switch becomes clamped at every turn-off to a voltage level defined by the sum of the voltages of capacitors C_{sn} and C_1.

Voltage of the clamp capacitor can be determined from charge balance. The current brought to the capacitor comprises the current that flows through the capacitor during the time the current changes direction in the leakage inductance right after the switch has been turned off. The current, and therefore, the charge that is taken from the capacitor during a switching cycle is determined by inductance L_{sn}. Since the voltage over the clamp capacitor is a dc voltage, the current rises linearly in the clamp circuit inductor during the time the switch is conducting. Therefore, the size of the inductance determines the average current taken from the capacitor and the dc voltage in the capacitor. This is the opposite of the resonant type snubber in which the size of the snubber capacitance determines the voltage stress on the switch and the inductor is merely chosen to provide a high enough resonance frequency for the resonant circuit, publication P[3].

Simulated waveforms of current of the passive clamp capacitor and voltage across the passive clamp inductor during two successive switching cycles are depicted

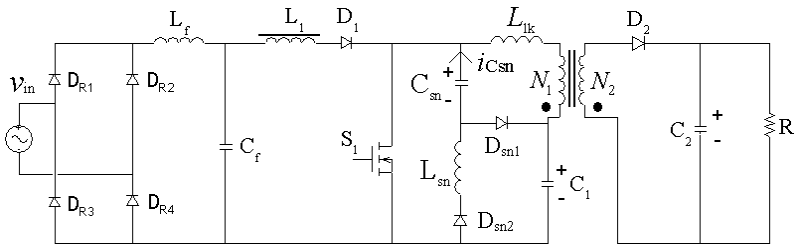

Figure 3.15. BIFRED converter with a non-dissipative protective circuit for the switch. Leakage inductance of the transformer is shown as L_{lk}.

in Fig. 3.16. The positive direction of clamp capacitor current i_{Csn} is shown in Fig. 3.15.

Switching cycle T_s in Fig. 3.16 is divided into four intervals, A, B, C and D, and from which the passive clamp circuit is active during the three first intervals. Equivalent circuits of the converter for the four intervals are shown in Fig. 3.17.

In the derivation of the operation of the passive clamp circuit we assumed that voltage V_{C1} of capacitor C_1, output voltage V_o and clamp capacitor voltage V_{sn} are constants. We also assumed that the converter operates in the DCM – DCM operation mode with a constant duty ratio.

Voltage stress over the switch of the BIFRED converter at turn-off is shown in five different cases in Fig. 3.18. Three of the cases shown are simulated with resonant type snubber and the two other cases are attained with the passive clamp circuit.

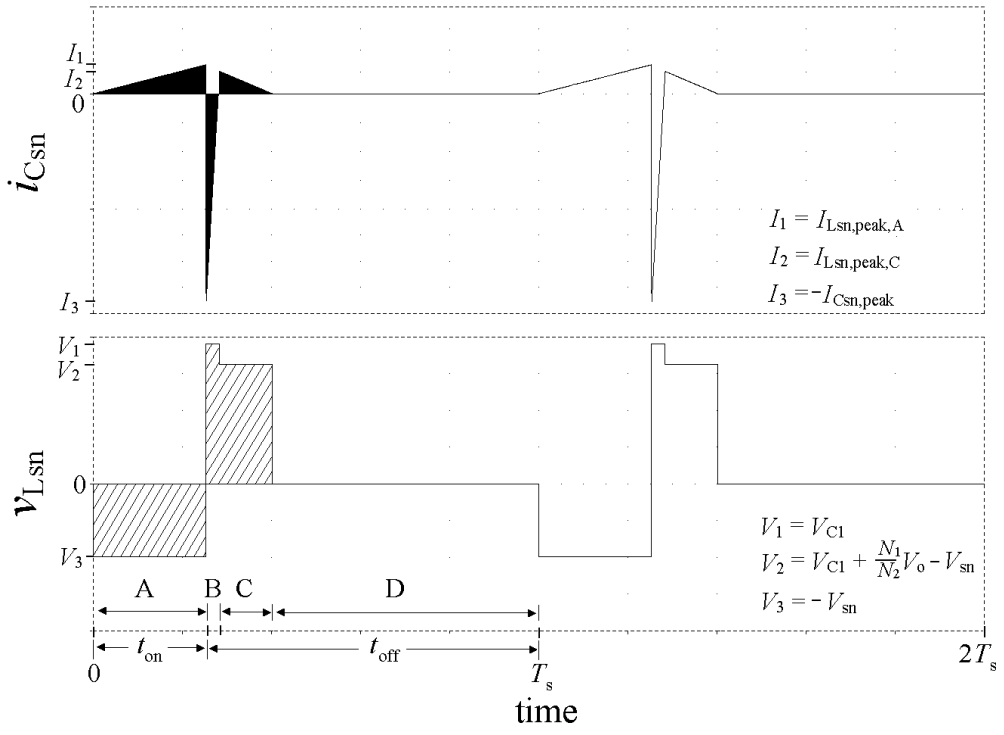

Figure 3.16. Current and voltage of the passive clamp circuit.

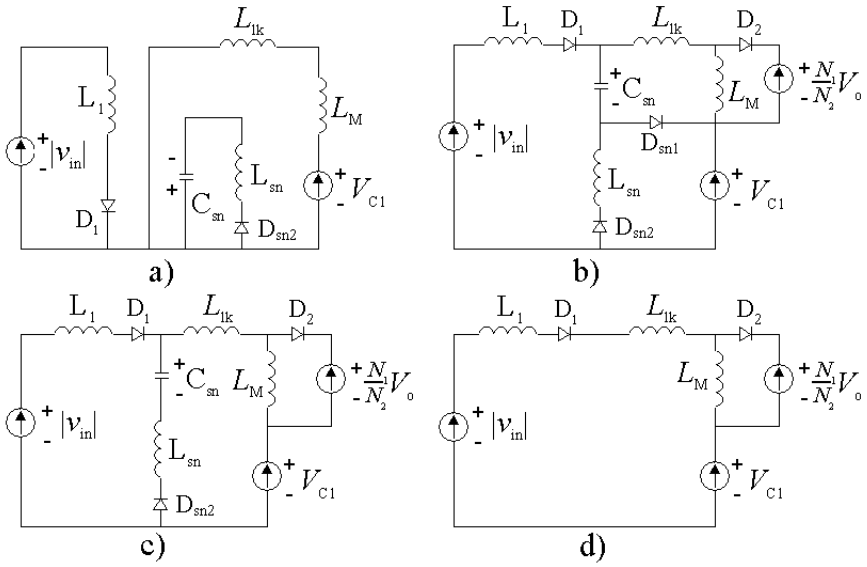

Figure 3.17. Equivalent circuits of the BIFRED with the passive clamp. Intervals A, B, C and D are depicted in a), b), c) and d), respectively.

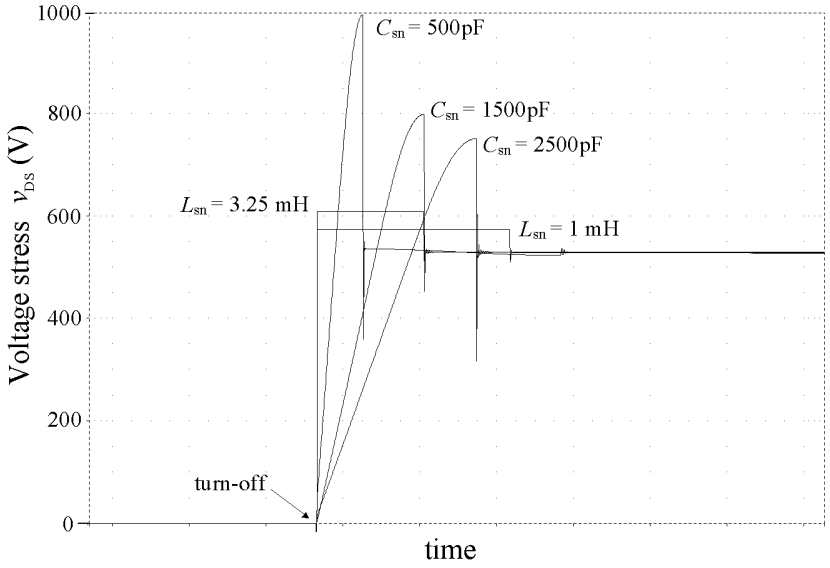

Figure 3.18. Simulated voltage stress over the switch at turn-off. Passive clamp: L_{sn} = 1 mH and 3.25 mH and C_{sn} = 2.2 μF. Resonant snubber: C_{sn} = 500, 1500 and 2500 pF and L_{sn} = 50 μH.

It can be seen from the simulation result that in the case of the passive clamp circuit the voltage over the switch becomes clamped to a dc voltage immediately after the switch has been turned off. Additionally, the voltage remains constant throughout the turn-off transition.

The advantage of the passive clamp circuit becomes obvious if the simulation results of the passive clamp circuit are compared with the corresponding results from the resonant type snubber circuit. Clearly, the passive clamp circuit can be designed

so that the voltage stress over the switch is lower than in the case of the resonant type snubber and/or so that the turn-off transition is shorter than in the resonant type snubber. Additionally, it can be shown that the voltage stress is not dependent on the load in the case of the passive clamp circuit. On the contrary, the voltage stress is dependent on the load in the case of the resonant snubber.

A prototype of the BIFRED converter was built to verify the analysis. Details of the prototype are given in publication P[4].

Measured waveforms of the voltage over the switch of the BIFRED prototype with the passive clamp circuit are shown in Fig. 3.19. In each figure the lower part shows the voltage during the off time of the switch, t_{off}, and the upper part shows a detail from the lower part of the respective figure. It is easy to see that the circuit clamps the voltage over the switch, after turn-off, to a certain voltage level.

The measurement results correspond well with the simulated and expected behavior of the circuit. The obtained voltage levels for the clamp capacitor voltage, V_{sn}, in the measurements were 10 - 14 % lower than the calculated and expected values. This is mainly due to the losses in the circuit and due to the fact that the parasitic drain-source capacitance of the switch has to be charged before voltage over the switch becomes clamped to the desired level. This additional charging of the parasitic capacitance and the losses in the circuit slightly reduce the peak current that flows to the clamp capacitor, and hence, reduce the charging current of the capacitor. Therefore, the obtained dc voltage in the clamp capacitor in practice is a little bit lower than the theoretical and expected value. It can be said, therefore, that the analysis gives the means to determine the upper limit for the dc voltage in the clamp capacitor.

The small oscillation in the voltage after the turn-off transition, visible in Fig. 3.19, is caused by the parasitic drain-source capacitance of the switch and the leakage inductance of the flyback transformer.

Measured voltage over the switch with the resonant type snubber is presented in Fig. 3.20. The peak voltage is clearly higher than what it was in the case of the passive clamp. Also, it can be seen from Fig. 3.20 b) that if a relatively large resonant snubber capacitance is used, the time required for charging the capacitance to a

certain voltage, which allows for the change to take place in the leakage inductance current, becomes longer.

It is also evident that the oscillation, caused by the parasitic capacitance and the leakage inductance, is much stronger, because of a high voltage level, than what it was in the case of the passive clamp.

It should be noted, also, that the peak voltage over the switch does depend on the load in this case since the voltage generated by the resonant snubber capacitor depends on the magnitude of the currents of the boost inductor and the flyback inductance, publication P[3]. Additionally, load and line transients do also affect the

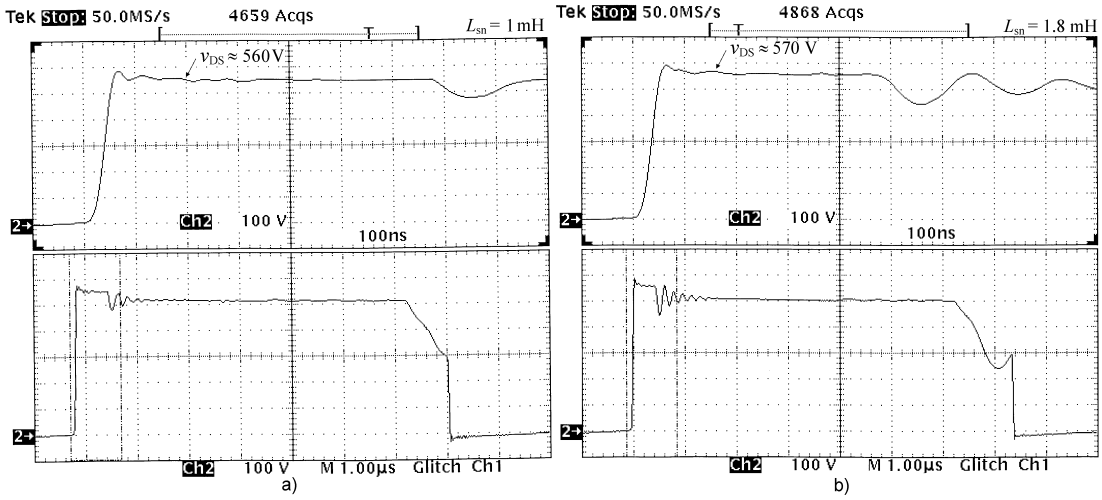

Figure 3.19. Voltage over the switch in the BIFRED prototype with the passive clamp circuit. In a) L_{sn} = 1 mH, b) 1.8 mH. Scale 100 V/div.

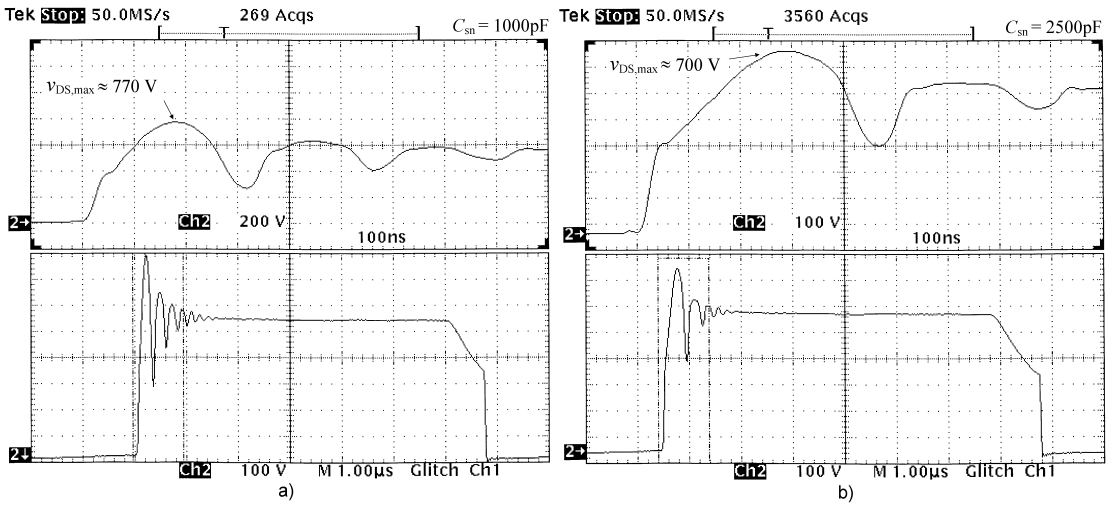

Figure 3.20. Voltage over the switch in the BIFRED prototype over the switch with a resonant type snubber. In a) 1000pF, scale 100V/div in the lower and 200 V/div in the upper figure, and in b) 2500 pF, scale 100 V/div.

voltage stress, and consequently, the voltage rating of the switch has to be designed accordingly. As mentioned earlier, the passive clamp voltage does not depend on the load.

Publication P[4] contains a detailed analysis of the passive clamp circuit in the BIFRED converter.

4 Forward type dc-dc converter

Forward type switched mode power supply topology is a derivation from buck topology, which is perhaps the most basic switcher circuit. Forward topology is widely used in low and medium power level converters mainly due to its simple structure and non-pulsating output current. A schematic of the forward converter is presented in Fig. 4.1.

Forward topology exhibits a few advantages. It is a simple construction with relatively low component count and it is able to provide an isolated output voltage. Also, the transformer allows for, besides the isolation, the input voltage to be considerably higher than the output voltage. The last named feature is especially interesting when the converter is designed to generate a low output voltage, Alou et al. 2000.

4.1 Passive reset methods for forward transformer

The transformer of the forward topology has a certain magnetizing inductance, and consequently, there has to be a way to demagnetize it after every on period, during which the inductance is magnetized, of the active switch.

In the following paragraphs, we will briefly analyze four passive reset circuits for a single switch forward converter.

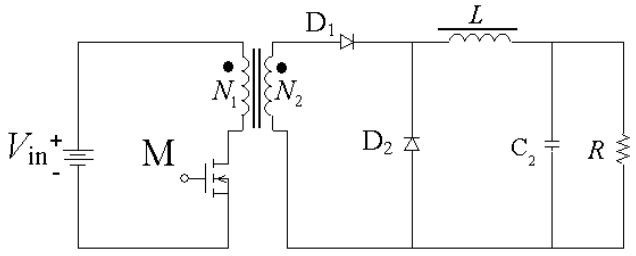

Figure 4.1. Schematic of the forward converter.

4.1.1 Third winding scheme

A traditional way to demagnetize the inductance in a single-switch forward converter is to add a third winding in the transformer, Erickson et al. 2001 pp. 154. A diode is also needed in series with the winding as shown in Fig. 4.2.

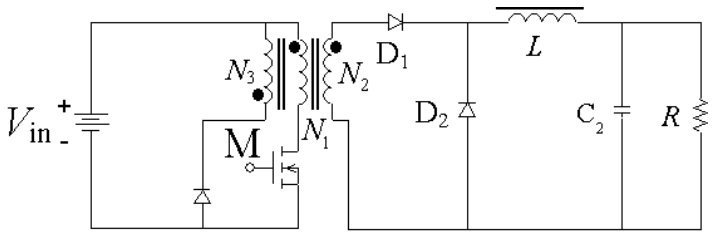

Figure 4.2. Forward with third winding reset.

Simulated waveforms of primary winding current i_{N1}, demagnetizing winding current i_{N3}, and output inductor current i_{L1}', referred to the primary side, are shown in the upper part of Fig. 4.3. The lower part of the figure shows the voltage over the primary winding, v_{N1}.

It should be noted that the magnetizing current builds up during the on period of the switch. For example, in Fig 4.3 the magnetizing current would be the difference between i_{N1} and $i_{L'}$ during the on period of the switch.

During the off period of the switch, the demagnetizing winding, N_3, offers a path for the inductive current to flow. The only direction the current can flow is back to the input, and therefore, the magnetizing energy is recycled to the input voltage source.

The magnetizing current flows towards the input as long as a volt-second balance across the inductance has been reached, i.e. the two hatched boxes, above and below zero, in the lower part of Fig 4.3 should have the same area.

Voltage over the primary winding during the off period of the switch can be determined from the following:

$$v_{N1} = \frac{N_1}{N_3} V_{in} \quad t_{on} < t \le T_s \qquad (4.1)$$

It should be noted that in this demagnetizing scheme only the magnetizing energy is recycled and the energy stored in the leakage inductance of the transformer is not. Moreover, the switch in this configuration most probably needs an additional

protection circuit, i.e. a snubber, against a voltage spike caused by the leakage inductance at the turn-off moment, Leu et al. 1992.

With the third winding reset scheme the transformer of the forward converter is magnetized only into one direction and it therefore operates in the first quadrant of the B-H curve. Also, the reset scheme limits the duty ratio of the switch typically to half, i.e. $D_1 \leq 0.5$.

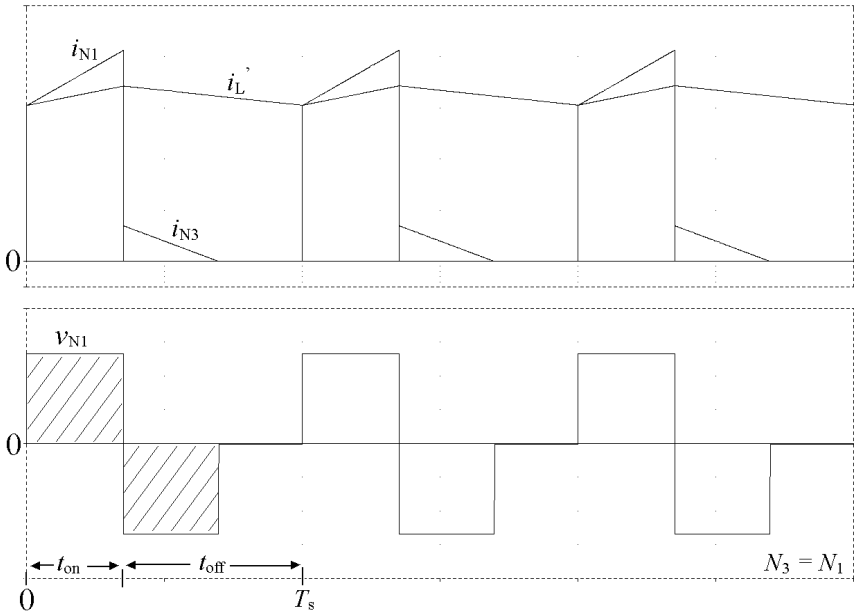

Figure 4.3. Third winding scheme.

4.1.2 RCD-clamp

Another passive way to demagnetize the inductance is to employ an RCD clamp circuit. The demagnetizing circuit is composed of a diode and a parallel connection of a resistor and capacitor, which in turn are parallel with the transformer, Leu et al. 1992 and Bridge 2000. The RCD clamp demagnetizing scheme in forward topology is depicted in Fig 4.4.

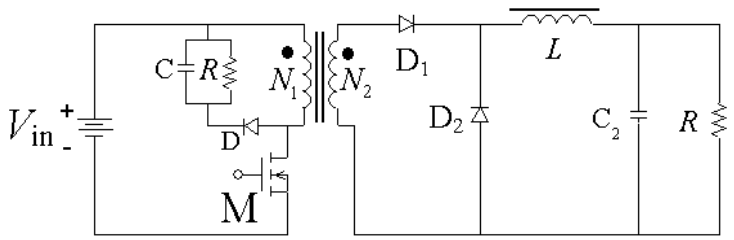

Figure 4.4. Forward with RCD clamp reset circuit.

Simulated waveforms of the primary winding current, reflected output inductor current and the voltage over the primary winding are shown in Fig. 4.5. It can be seen from the simulated result that the primary winding carries the magnetizing current during the on and off periods of the switch.

After the switch has been turned off, the diode in the clamp circuit starts to conduct. This means that the clamp capacitor becomes connected across the primary winding and it demagnetizes the transformer. As in the previous reset scheme, the magnetizing current cannot, in principle, become negative. However, as reported in Leu et al. 1992 and Bridge 2000, a resonance between the magnetizing inductance and parasitic capacitances of the circuit at the end of the off period may force the magnetizing current slightly on the negative side. This resonance also recycles some of the magnetizing and leakage energy.

The RCD clamp reset circuit is able to protect the switch from voltage spikes due to the leakage inductance of the transformer. This means that there is not necessarily a need for an additional snubber for the switch.

It should be noted, however, that the RCD clamp circuit does not recycle the charge stored in the clamp capacitor. Instead, charge balance in the capacitor is maintained with the dissipative clamp resistor. This arrangement naturally causes losses and inevitably decreases the efficiency of the converter.

The voltage of the clamp capacitor in the RCD clamp can be determined by the means reported in literature. Bridge and Leu found out that the clamp voltage is independent of the input voltage, Bridge 2000 and Leu et al. 1992. Additionally, Bridge reported that the clamp voltage is also independent of the load current, Bridge 2000.

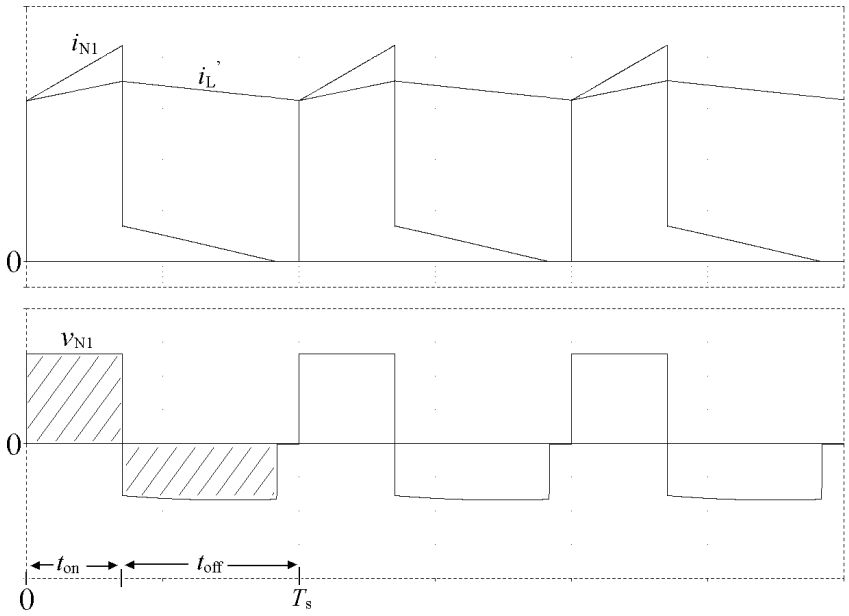

Figure 4.5. Waveforms of the RCD clamp demagnetizing scheme.

4.1.3 Non-dissipative snubber

A lossless or non-dissipative snubber circuit, Domb et al. 1982 and Tanaka et al. 1988, is shown in Fig. 4.6. The snubber consists of two diodes, a capacitor and an inductor.

This reset method is able to recycle energy that is stored in the magnetizing and leakage inductance of the transformer. Since it is able to deal with the leakage energy, and as the name of the reset circuit indicates, there is no need for an additional snubber circuit for the switch.

A non-dissipative snubber can be designed so that it is able not only to demagnetize the transformer but also able to magnetize it in the negative direction, Tanaka et al. 1988. This can be seen from the simulated waveforms shown in Fig. 4.7, where the magnetizing current is clearly negative at the end of the off period. As a result, the core of the forward transformer is better utilized since it operates in the first and third quadrants of the B-H curve.

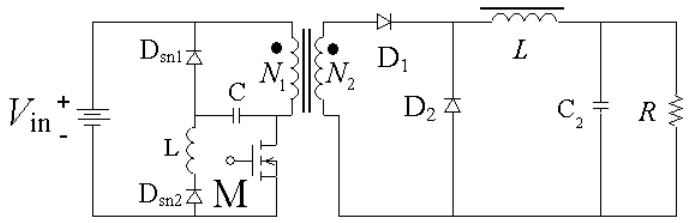

Figure 4.6. Forward with non-dissipative snubber circuit.

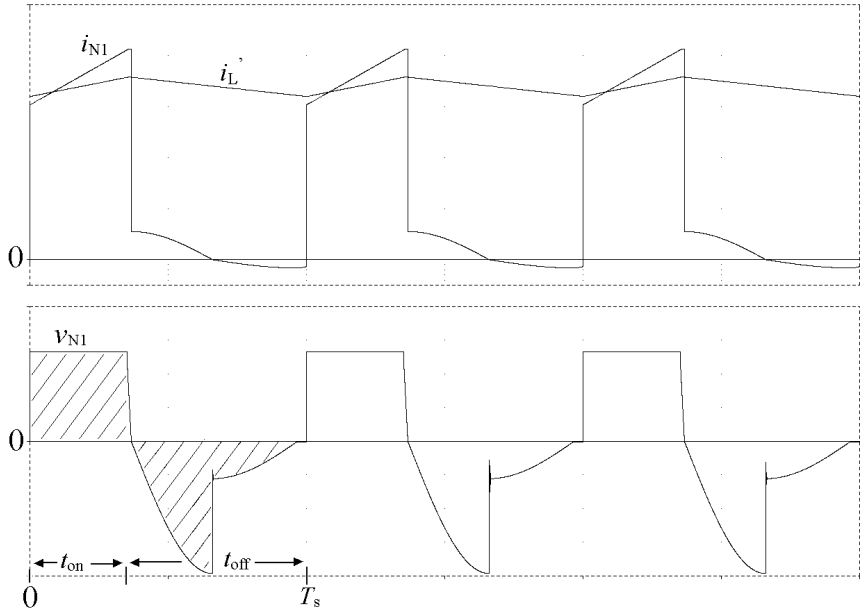

Figure 4.7. Simulated waveforms of the forward converter with non-dissipative snubber.

4.1.4 Resonant reset

The resonant reset demagnetization scheme is shown in Fig 4.8, Murakami et al. 1988. This reset scheme utilizes the parasitic capacitance that is seen across the main switch. One of the advantages of the reset scheme is that it does not necessarily need any additional components.

Capacitance C_p and magnetizing inductance L_M are drawn as discrete components in the figure in order to illustrate the principle of the reset scheme.

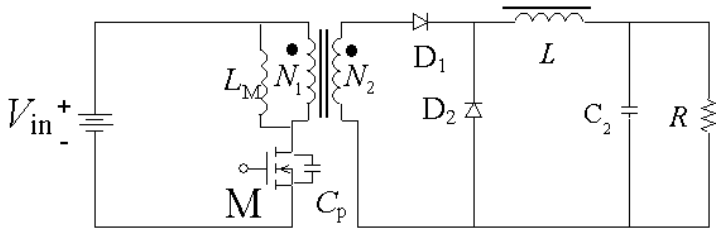

Figure 4.8. Forward with resonant reset. Magnetizing inductance L_M and parasitic capacitance C_p are drawn in the figure.

Right after the switch has been turned off the magnetizing current starts to flow through the parasitic capacitance of the switch. Because of the current, voltage starts to build up in the capacitance.

After the voltage has risen to the level of the input voltage, the difference between the input voltage and the capacitor voltage demagnetizes the inductance and eventually magnetizes it towards the negative direction. This means that the initial and

the remaining voltage of the capacitor is V_{in} and that the magnetizing current changes its flowing direction but not the magnitude during the resonance. This, of course, requires that there is enough time for the resonant circuit, i.e. L_M and C_p, to complete a half of their mutual resonance cycle during the off period of the switch. The length of a half of the resonance cycle between the two components can be determined from the following:

$$t = \pi\sqrt{\left(C_p L_M\right)} \qquad (4.2)$$

It should be noted that the duration of the resonance does not depend on the magnitude of the magnetizing current. This is indicated in Eq. (4.2) and in the simulated waveforms of the resonant reset shown in Fig. 4.9.

In conclusion, the resonant reset recycles the magnetizing energy as well as the leakage energy. Additionally, the transformer is magnetized, if the off time is long enough, symmetrically around zero.

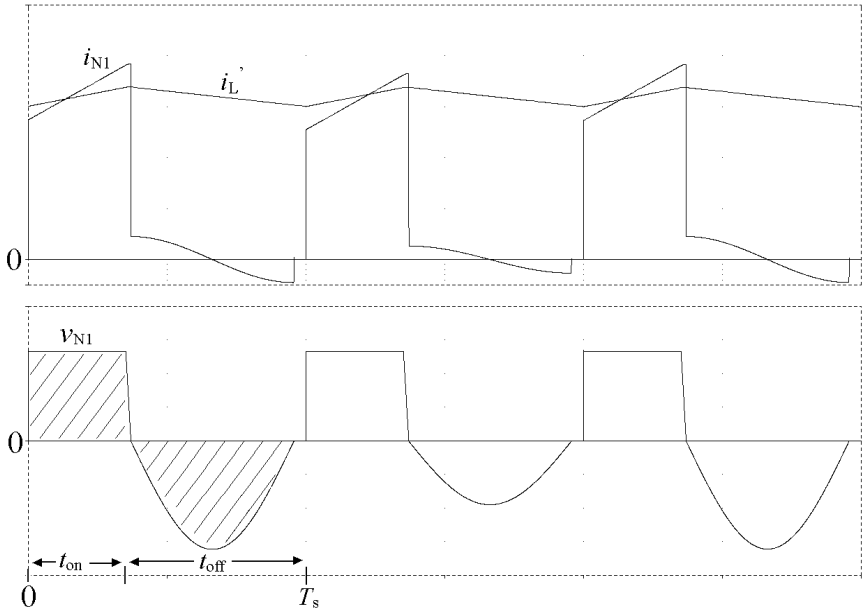

Figure 4.9. Simulated waveforms of forward converter with resonant reset.

4.2 Forward with active clamp

An active reset circuit for demagnetization of the transformer is depicted in Fig. 4.10. This reset circuit comprises of a switch and a capacitor and it is called an active clamp.

The active clamp reset circuit can be implemented in the primary side in two ways: either with a P-channel MOSFET (for example Cobos et al. 1993) or with an N-channel MOSFET (for example Ji et al. 1994), as shown in Figs. 4.10 a) and b), respectively. We will consider, however, in this Thesis the circuit that is shown in Fig. 4.10 a).

The active clamp circuit clamps the voltage over the transformer, after the switch has been turned off, to the level that equals the clamp capacitor voltage. It should be noted that the voltage in the capacitor is a dc voltage with only a relatively small ripple at the switching frequency imposed on it, i.e. the resonance frequency of L_M and C_R is much lower than the switching frequency.

The capacitor voltage is across the switch, in principle, during the whole off period of the switch. This means that there is a voltage over the primary winding of the transformer all the time. Consequently, the magnetizing current is continuous and it is, in principle, symmetric around zero, Jitaru 1991. This can be seen from the simulated waveforms of the forward with active clamp in Fig. 4.11. Additionally, the duty ratio can be above 50%, Carsten 1990.

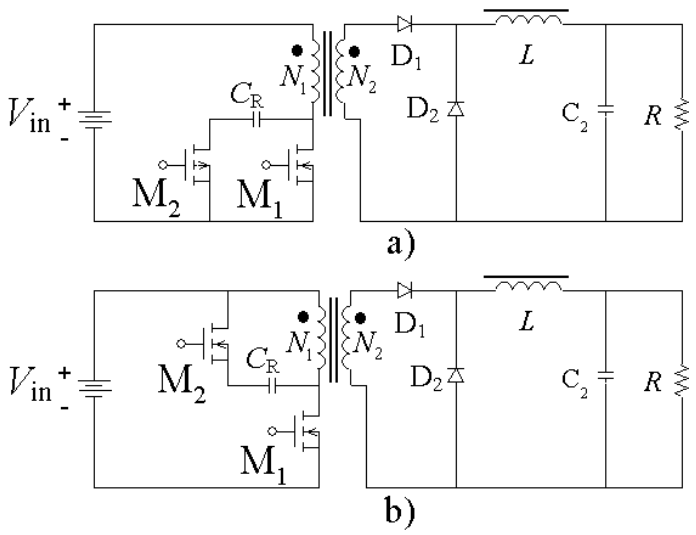

Figure 4.10. Forward with active clamp. Active clamp implemented with a P-channel MOSFET in a) and with an N-channel MOSFET in b).

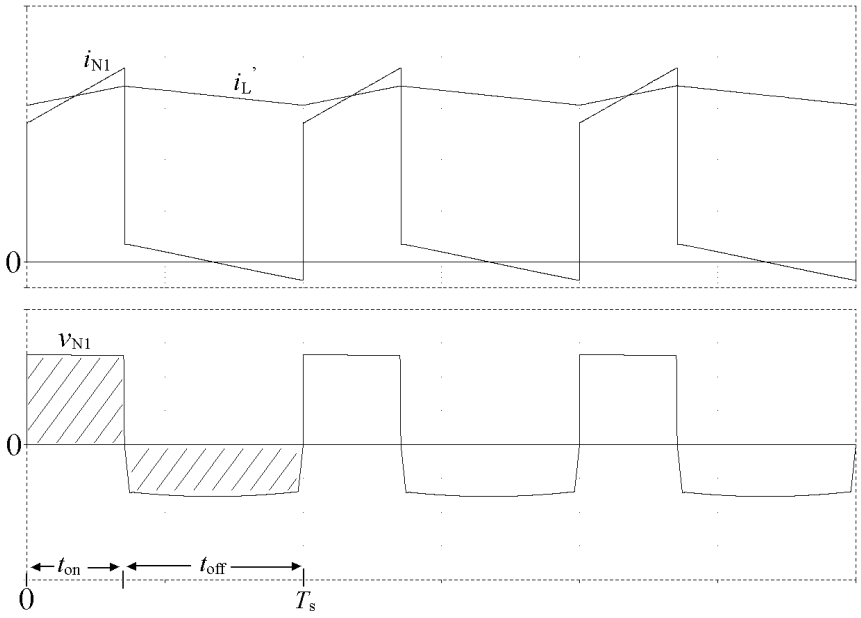

Figure 4.11. Simulated waveforms of the forward with active clamp.

The clamp capacitor voltage can be obtained from the following, Jitaru 1991:

$$V_C = \frac{V_{in}}{1 - D_1} \qquad (4.3)$$

The active clamp circuit recycles the magnetizing and leakage energy. It also acts as a snubber circuit protecting the switch from voltage spikes due to the switching action.

Downsides of the active clamp are, compared to the passive methods, that it requires an active switch and control circuitry.

4.3 Reset circuits and self-driven synchronous rectification

4.3.1 Introduction

Reset method for the transformer in the forward converter is an important design aspect. For forward converters with self-driven synchronous rectifiers it is especially important. This is because the voltage that is generated over the windings of the transformer is used to drive the synchronous rectifiers at the secondary side, Chryssis 1989.

A forward converter with self-driven synchronous rectifiers is depicted in Fig. 4.12. It should be noted that it is possible to also take the control signals from additional secondary windings or from the output inductor, Chryssis 1989.

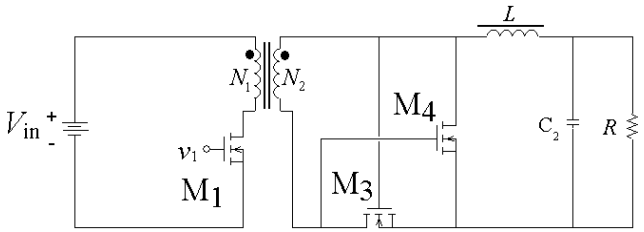

Figure 4.12. Forward converter with self-driven synchronous rectifiers.

If the voltage over the windings of the transformer is zero during a part of the off period of the main switch, it will disable the control from synchronous rectifier M_4. This 'dead time' in the voltage increases losses, since without a control signal the body diode of the MOSFET takes over to carry the load current.

An example of an ideal-like voltage waveform over the primary winding of the forward transformer for driving self-driven synchronous rectifiers is shown in Fig. 4.13. The two key points in the voltage waveform is that firstly, there are no dead times and secondly, the voltage stays above the threshold voltage V_{GS} of a MOSFET.

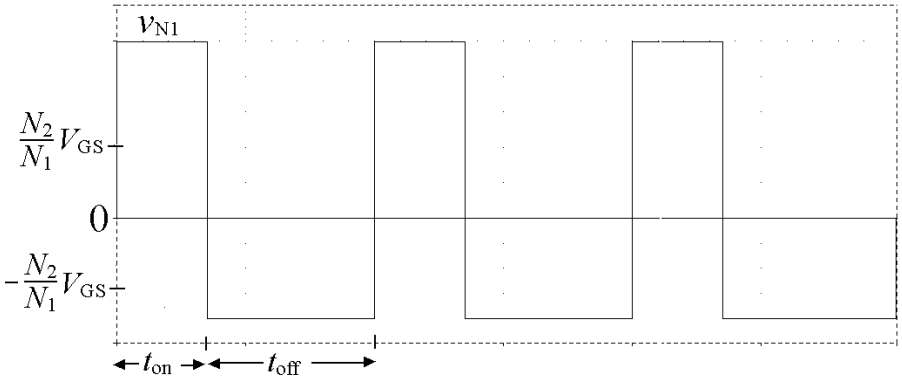

Figure 4.13. An example of a suitable voltage waveform to drive self-driven synchronous rectifiers.

4.3.2 Summary of the reset schemes

The four passive methods to demagnetize the transformer are simple, reliable and easy to implement. However, they have some shortcomings from the point of view of self-driven synchronous rectification.

In the third winding scheme the magnetizing current cannot become negative. It is desirable to bring the current down to zero before the beginning of a new switching cycle. This should be done in order to prevent the magnetizing current from accumulating and eventually causing the transformer to saturate. This means that there is a dead time in the voltage over the windings of the transformer at the end of

every off period, i.e. the voltage over the windings is zero during the time that the current is zero. Also, voltage stress over the switch is in this case relatively high, Leu et al. 1992.

It is also desirable to completely reset the transformer in the case of the RCD clamp scheme, Leu et al. 1992. To ensure a complete reset, the circuit should be designed so that it is able to reset completely with the lowest input voltage and maximum output current, Leu et al. 1992. This means, however, that with higher output voltages there inevitably exists a dead time in the winding voltage. This is because the clamp capacitor voltage is independent of the input voltage. Advantage of the RCD clamp circuit is a relatively low voltage stress over the switch. However, the dissipative nature of the RCD clamp is a drawback for the reset scheme. A study of the RCD-clamp reset scheme in forward converter with self-driven synchronous rectifiers was reported in Cobos et al. 1993.

The non-dissipative snubber circuit and the resonant reset circuit both rely on resonance between the magnetizing inductance and the capacitive element. Therefore, the voltage has a curved waveform and at least at the beginning of the off period the winding voltage lingers below the threshold voltage for some time. This means that the secondary side MOSFET does not receive a appropriate control signal immediately at the beginning of the off period. This time can shortened by, for example, reducing the capacitance of the capacitive element. This in turn, however, increases the voltage stress over the switch and decreases the duration of the resonance period, which may easily lead to a considerable dead time at the end of the off period.

However, the resonant reset method has been used for self-driven synchronous rectification and studies of its use have been reported in literature. For example, Blanc 1991, Cobos 1994 and Alou 1997 have shown that this scheme can be used with some success for self-driven synchronous rectification. However, Alou 1997 concluded that it is very difficult to optimize the overall performance of the converter with large input voltage variations.

The forward with active clamp, on the other hand, provides a voltage waveform over the windings of the transformer that is closest to the desired one. Moreover, the voltage of the active clamp capacitor is able to adapt to changes in the duty ratio so

that the voltage over the windings is without dead times. This means that the control voltage for the synchronous rectifiers is without dead times despite input voltage and/or load changes. Also, voltage stress over the switch in the case of FAC converter is relatively low. For these reasons, we selected the active clamp circuit for further research.

4.4 Low voltage conversion with forward with active clamp

4.4.1 Introduction

Operating voltages in many electronic appliances are getting lower, Lidow 2003. This means that power supplies, which provide the operating voltages, have to be designed to produce lower output voltages and higher output currents. Higher output current is needed if we assume that there are no considerable reductions in the power demand.

A combination of a high output current and a low output voltage sets a tough challenge for the power supply designer. This is because a small overall size, low-cost and high efficiency have to be maintained or even improved.

In low voltage power supplies the secondary side rectification loss is the major contributor to poor efficiency, de la Cruz et al. 1993. Synchronous rectifiers can be used in the secondary rectification, instead of rectifier diodes, to improve the efficiency, Chryssis 1989, de la Cruz et al. 1993, Blanc 1991, Ji et al. 1994, Chen et al. 1995 and Xuefei et al. 1999.

The forward with active clamp (FAC) is a well-known converter. The schematic of the converter was first developed and presented, according to Carsten 1990, in 1977 by Carsten. However, the active clamp reset circuit was patented in 1984 by Vinciarelli, Vinciarelli 1984. A modification, which allows for zero voltage switching (ZVS) for the main switch, to the active clamp circuit in forward topology was presented and patented by Jitaru, Jitaru 1991 and Jitaru 1992.

The FAC converter has been widely reported in literature. Li et al. 1999 considered the dc bias that is present in the magnetizing current due to the leakage inductance of the transformer and the parasitic capacitances of the converter. Large signal transient analysis of the FAC converter with output-voltage feedback control was reported by Li et al. 1998 and 2002. Design consideration for large signal transient behavior of the converter with current mode control was reported in Li et al.

2000 and 2003. These reports point out that there might exist problems with excessive voltage over the switch, diode reverse recovery problems of the body diode of the clamp switch or transformer core saturation due to large signal transients if the converter is not properly designed.

A remedy for the excessive switch voltage, during transients, of the FAC converter was reported by Jitaru 2003. This method however, introduces a dead time in the primary winding voltage and therefore degrades the performance of the converter from the point of view of self-driven synchronous rectification.

A self-driven driving method for the N-channel construction of the FAC converter was reported by Lim et al. 2002. In this scheme, the active clamp switch is driven from an auxiliary winding rather than from a control IC.

Small signal analysis of the FAC converter with peak current mode control was reported in Fontán et al. 1998.

Reports about the FAC converter with self-driven synchronous rectifiers were given, for example, in Cobos et al. 1993, Ji et al. 1994, Chen et al. 1995 and Xie 1999. A study of the ZVS FAC converter with self-driven synchronous rectifiers was reported in Acik et al. 2003.

4.4.2 Research background

The FAC is a convenient topology for a low output voltage converter because the active clamp circuit enables an easy use of self-driven synchronous rectification. This is because the converter's reset circuit provides a voltage over the windings of the forward transformer that is without dead times. The FAC converter with SRs that are driven from auxiliary secondary windings is depicted in Fig. 4.14.

One additional advantage of the FAC converter is that the turn-on loss of the main switch can be reduced or even virtually removed. This is due to the fact that

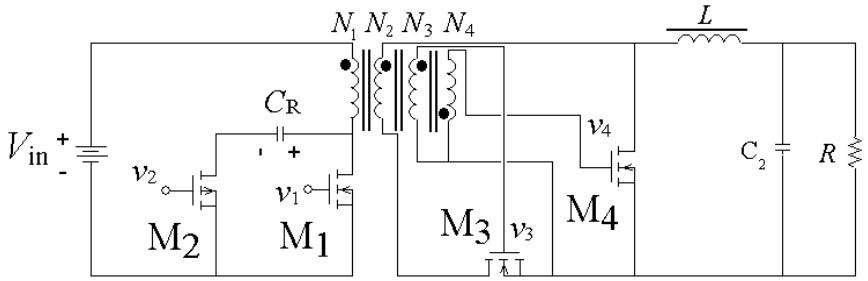

Figure 4.14. Forward with active clamp (FAC) and self-driven synchronous rectifiers that are driven from auxiliary windings N_3 and N_4.

switch M_2 has to be turned off before switch M_1 can be turned on. This should be done in order to avoid short-circuiting the clamp capacitor. When, at the end of off period, neither of the switches is conducting, the magnetizing current flows toward the input through the parasitic drain-source capacitance of the main switch. This, of course, reduces the voltage over the switch right before it should be turned on.

In an FAC converter without self-driven synchronous rectification, minimization of turn-on losses (Jitaru 1991) for the main switch is without doubt an advantageous solution, at least to some extent. However, if self-driven synchronous rectifiers are used, instead of diodes, the situation is more complicated. Namely, if the voltage over the switch before turn-on is lowered below a certain level, the control signal for synchronous rectifier M_4 is lost and the body diode of it is turned on. This, naturally, increases rectification loss, which is not necessarily insignificant with a high load current.

Turn-on at input voltage level

In the FAC converter depicted in Fig. 4.14, the lowest possible voltage level for turn-on of M_1, in theory, is the input voltage level, which corresponds with a zero voltage over the primary winding. Therefore, the voltage over the switch that does not remove control from the synchronous rectifier is:

$$V_{\mathrm{DS}} = V_{\mathrm{in}} + \frac{N_1}{N_4} V_{\mathrm{GS}} = V_{\mathrm{in}} + V_{\mathrm{GS}}^{'} \qquad (4.4)$$

This voltage is, or at least it should be, lower than the clamp capacitor voltage, Eq. (4.3), which in turn is the maximum voltage over the switch. In high output current applications it might be advantageous to lower the voltage over the switch to the level given in Eq. (4.4) and not to the input voltage level. This turn-on strategy

would increase the turn-on loss for M_1 a little bit, but on the other hand it would keep rectifier M_4 turned on to the end of the off period of M_1.

During the time between the turn-off and turn-on of switches M_2 and M_1, respectively, the magnetizing current flows through the parasitic drain-source capacitance of M_1, toward the input voltage removing charge from the capacitance prior to turning M_1 on. Reduction in the voltage level, during the resonant transition (Jitaru 1991), is therefore determined by the length of the delay between the switches and the magnitude of the magnetizing current during the transition. This means that a low voltage over switch M_1, prior to turning on, is obtained by increasing the delay or by increasing the magnetizing current or both.

The current of switch M_1 in three different cases is shown in Fig. 4.15 a). The current is the sum of the reflected load current I_o' and the magnetizing current i_m. A low magnetizing inductance yields a high magnetizing current and gives the possibility to lower the voltage over the switch to the input voltage level rapidly. This is depicted in Fig. 4.15 b), where the shortest delay between the two switches, $\Delta t = (T_s - t_c)$, is achievable in the case where the magnetizing current has the highest amplitude. On the contrary, the longest delay, $\Delta t = (T_s - t_a)$, is required in the case in which the current has the lowest amplitude. Parameter Δt (Δt_1 in publication P[5]) can be defined as follows:

$$\Delta t = \frac{1}{\omega_o} \arctan\left[\frac{2}{\omega_o T_s (1 - D_1)}\right], \quad \omega_0 = \frac{1}{\sqrt{L_M C}} \qquad (4.5)$$

Derivation of Eq. (4.5) can be found from publication P [5]. It should be noted that the time delay can also be determined by means reported in Ji et al. 1994.

However, if a shorter time delay is applied, the switch will be turned on at a higher voltage level. This is depicted in Fig. 4.15 c), where delay $\Delta t = (T_s - t_a)$ results in turn on at level $v_{DS} = V_{in}$ and shorter delays $(T_s - t_{a'})$ and $(T_s - t_{a''})$ result in a turn on at the higher voltage levels, denoted as v_3 and v_2, respectively. Here, v_{DS} means the drain-source voltage of M_1.

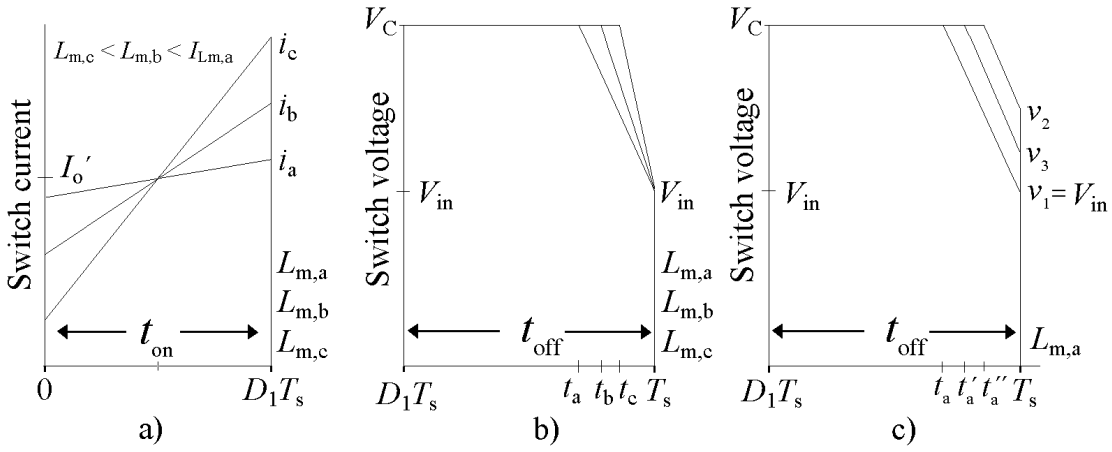

Figure 4.15. a) Current of switch M_1, b) and c) voltage over M_1.

For example, if we define level v_2 to correspond with level V_{DS} in Eq. (4.4), then some of the inevitable turn-on loss is reduced, i.e. the voltage is lowered from V_C to V_{DS}, and, at the same time, rectifier M_4 is kept on until a new switching cycle begins. A measurement example of the drain-source voltage of the FAC converter in two cases is shown in Fig. 4.16. In Fig. 4.16 a), the time delay is set to 240 ns and the voltage over the switch is lowered to V_{in} = 48 V level. In Fig. 4.16 b), a time delay of 140 ns is used and the voltage drops only to level V_{DS} = 66 V before turn-on of the main switch.

Selection of a suitable turn-on voltage level for the main switch is therefore a trade-off between switching losses in the primary side and rectification losses in the secondary side.

An additional parameter is, naturally, the magnetizing current that defines the needed time to achieve the desired voltage level. A low magnetizing current reduces conduction losses in the primary side but it might not be enough to reach the desired voltage over the switch, unless an unreasonable long time delay is used. On the other hand, a shorter time delay can be used if the magnetizing current is increased, which in turn increases conduction losses. Increase in the magnetizing current in this case can be achieved by reducing the value of the magnetizing inductance, Chen et al. 1995 and Jitaru 1991.

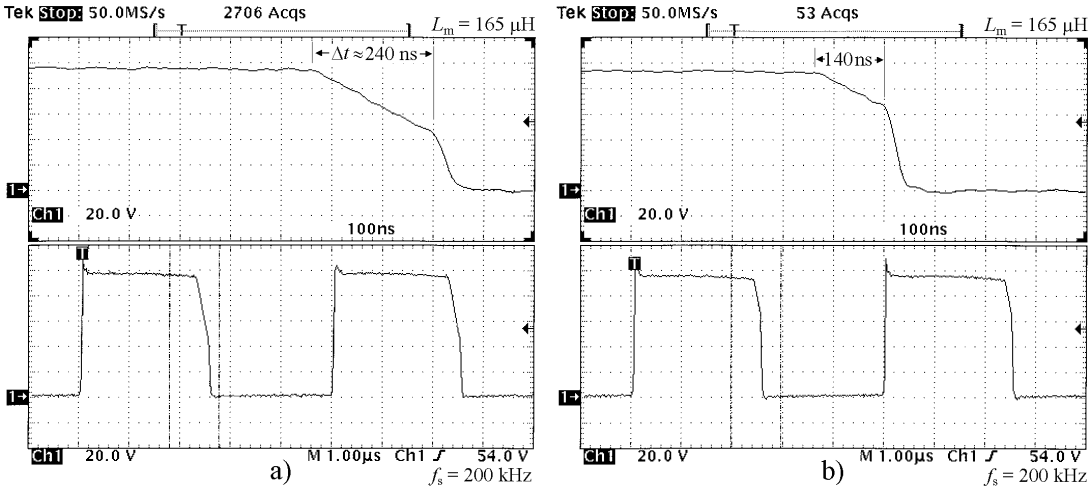

Figure 4.16. Measured voltage over switch M_1 with two different time delays, a) $v_{DS} = V_{in}$ = 48 V and b) $v_{DS} = V_{DS}$ = 66 V. f_s = 200 kHz, L_m = 165µH and I_o = 25 A.

For this type of FAC converter, in which SRs are driven either from auxiliary windings or straight from the secondary winding, it has been suggested in literature that the turn-on loss for the main switch should be minimized. For example, Lim et al. 2002, Zhang et al. 1996, Chen et al. 1995 and Ji et al. 1994 suggested that the voltage over the main switch should be lowered to the input voltage level before turning on the switch. It should be noted, however, that in Cobos et al. 1993, there was a brief mention that it might be better to turn on the main switch before the voltage over it lowers to V_{in}.

In publication P[7], the effect of the voltage level over the switch on the efficiency of the FAC converter with self-driven synchronous rectifiers is investigated. It was found that at high loads it would be more advantageous to turn-on the switch at the level given in Eq. (4.4) in order to maximize the efficiency of the converter. This can be seen from Fig. 4.17 where the efficiency of the FAC prototype is depicted in the two cases. In the measured cases, voltage levels v_{DS} = 48 and 66 V were used. The first one, 48 V, corresponds with the input voltage and the second, 66 V, with the level given in Eq. (4.4).

It can be seen from Fig. 4.17 that turn-on at high voltage returns a clearly lower efficiency than the lower voltage level turn-on. At high loads however, turn-on at the higher level returns a better efficiency.

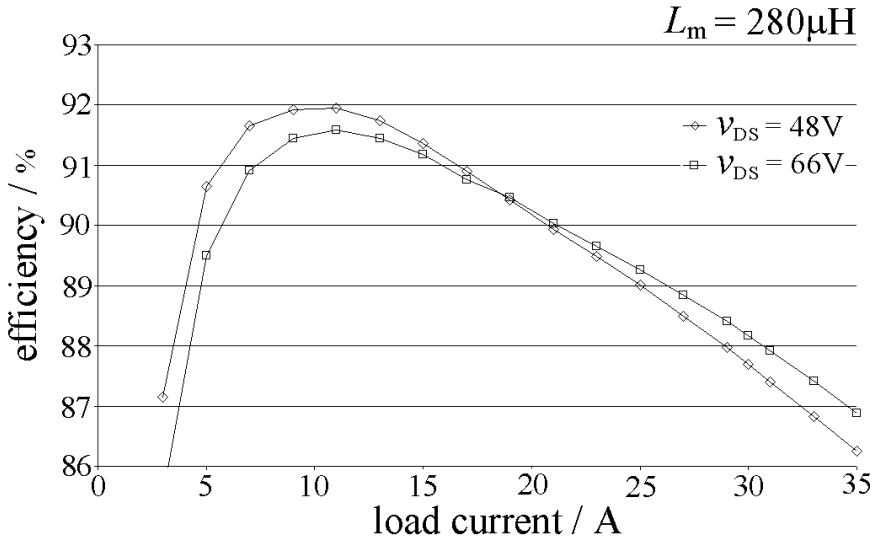

Figure 4.17. Efficiency of the FAC prototype as a function of the load current.

Zero voltage switching

As mentioned earlier, it is also possible to turn-on the main switch of the FAC converter from zero level (Jitaru 1991). This would virtually remove the turn on loss for the main switch. In order to achieve ZVS, i.e. turn-on at zero level, an additional component is needed, as shown in Fig. 4.18. This additional component can be a switch or a saturable reactor, Jitaru 1992. The purpose of the component is to prevent the body diode of M_3 turning on prematurely. Without the additional component, the diode would shunt the secondary of the transformer after the voltage over M_1 has descended to V_{in} level preventing any further reduction in the switch voltage.

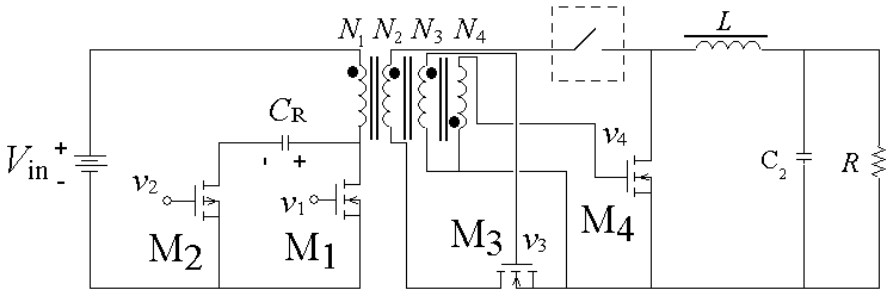

Figure 4.18. FAC with self-driven SRs and an additional component for enabling ZVS.

The required time delay between switches M_1 and M_2 for ZVS can be obtained from the following:

$$\Delta t_2 = \frac{1}{\omega_0}\sin^{-1}\left[\frac{A + B\sqrt{A^2 + B^2 - 1}}{A^2 + B^2}\right], \quad A = \frac{\omega_0 D_1 T_s}{2}, B = \frac{D_1}{1 - D_1} \qquad (4.6)$$

A detailed derivation of Eq. (4.6) can be found from publication P[5].

The ZVS strategy reduces turn-on losses for the main switch to virtually zero. This is without doubt advantageous, at least at high switching frequencies. It should be noted that in high output current applications the efficiency of the converter is, however, also strongly dependent on the on-resistance of the additional element.

In publication P[7] a comparison between expected losses with and without the ZVS strategy in the FAC converter with self-driven synchronous rectifiers is reported.

5 Description of the laboratory setup

5.1 Laboratory equipment

In the case of the BIFRED prototype measurements were committed with a resistive load. With the FAC prototype measurements an electronic load, Agilent 6051A, was used.

Measurements were carried out with Tektronix TDS 714L oscilloscope and with Tektronix P5200 and P5205 high voltage differential probes. Numerical values for the input and output voltages and currents were obtained with NORMA D6000 wide band power analyzer system.

Input voltage for the BIFRED converter was taken from the mains. Input voltage for the FAC converter and supply voltages (V_{CC}) for the PWM ICs of the two prototypes were taken from two TT*i* EX354T laboratory power supplies. A photograph of the measurement setup is shown in Fig 5.1.

5.2 BIFRED prototype

Schematic of the prototype is shown in Fig. A.1 in Appendix A. In this prototype converter a constant duty ratio was used and there were no feedback from the output voltage. The duty ratio was adjusted manually with trimmer R7 (see Fig. A.1 in Appendix A). The measurements for the BIFRED equipped with either resonant type snubber or passive clamp were committed with the same converter. Only the capacitor and the inductor in the snubber circuit were changed to form the desired construction.

5.3 FAC prototype

Measurements with the FAC prototype converter were done with closed feedback loop. Peak current mode control with slope compensation was used and the used PWM IC was UC2842. As can be seen from Fig. A.2 in Appendix A, the supply voltage for the secondary side electronics were obtained from the auxiliary secondary windings. The delay between the turn-off of M_2 and turn on off M_1 was adjusted with

trimmer R24. (see Fig. A.2 in Appendix A). A photograph of the FAC prototype is shown in Fig. 5.2.

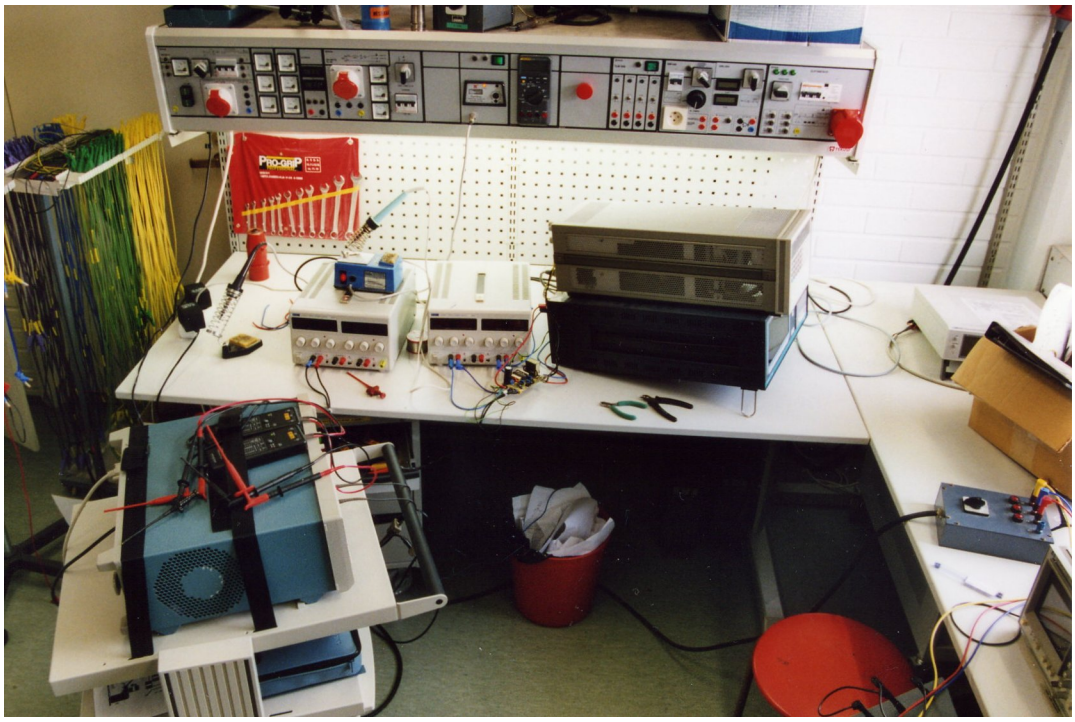

Figure 5.1. Photograph of the laboratory setup. FAC prototype converter in the middle on the table.

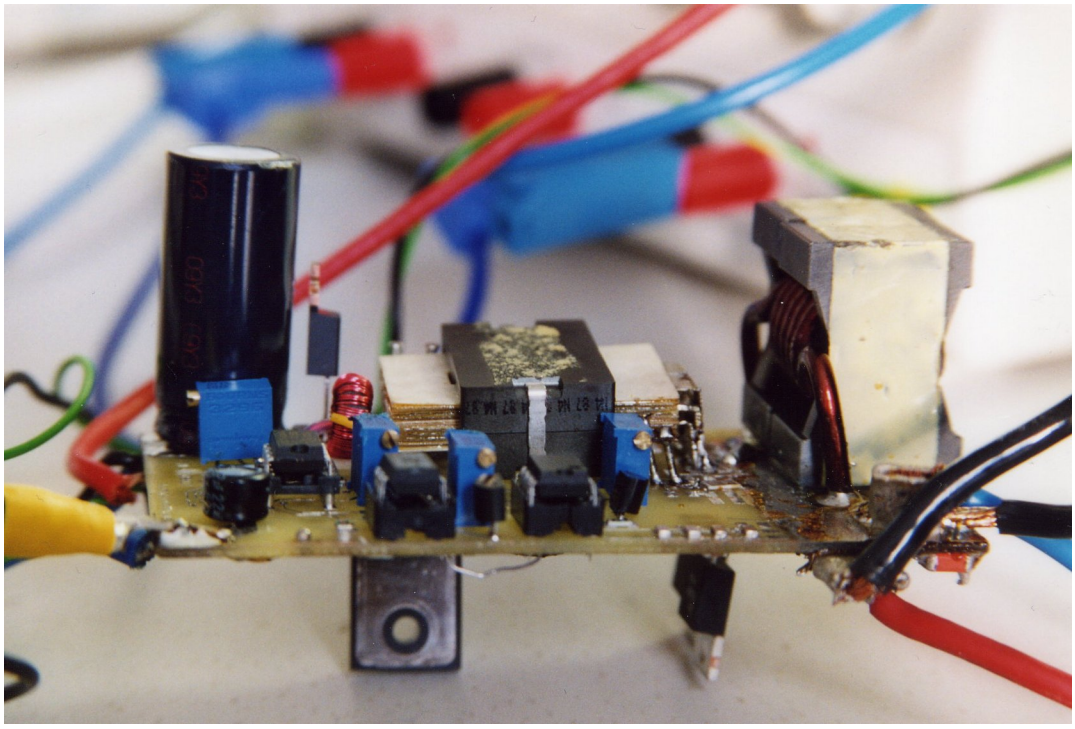

Figure 5.2. Close-up photograph of the FAC prototype converter.

6 Summaries of the publications

Publication P[1]

Publication P[1] presents a detailed steady state analysis of the dither converter with a tapped transformer. It should be noted that the analysis is valid for a dither converter even without a tapping in the transformer.

The analysis gives accurate means to define the steady state operation point of the converter. Also, it gives useful information for a designer to determine the needed inductance for inductor L_1 for a certain rated power as well as means to determine maximum duty ratio and the minimum and maximum voltage stresses on the bulk capacitor.

Publication P[2]

Publication P[2] presents a detailed small signal analysis of the dither converter with a tapped transformer. Propagation of a control-to-output disturbance can be obtained with the small signal model presented in the paper.

The dynamic behavior of the converter and the applicability of the model were verified with a set of simulations in a PSpice simulation environment.

Publication P[3]

Publication P[3] considers a resonant type non-dissipative snubber for the BIFRED and BIBRED converters. A detailed analysis of the snubber circuit is performed for the two converters. The study presented in the publication gives means to determine the expected voltage stress over the switch of the two converters.

Publication P[4]

A passive clamp circuit for the BIFRED converter is presented in this publication. The passive clamp circuit clamps the voltage over the switch to a relatively low and

predictable value at turn-off. This allows for the use of a switching device of a lower voltage rating, and therefore, a device with lower on-resistance and conduction losses.

A detailed analysis of the clamp circuit is given in the publication. An equation to determine the clamp voltage as a function of the circuit parameters is given. The validity of the clamp circuit and the analysis was verified with simulations and measurements.

Publication P[5]

The operation principle of the forward converter with active clamp is discussed in publication P[5]. The publication contains a detailed study of the behavior of the FAC converter during the resonant transition. Analytical equations to determine the voltage over the switch, voltage over the primary winding, current in the drain-source capacitance of the switch and current in the parasitic capacitances across the primary winding are derived for the resonant transition period.

Requirements for low-voltage on switching for the primary switch of the converter are determined. Equations to determine suitable time delays between the switches for turn-on at the input voltage level and for ZVS are deduced and presented. It is also noted that the most suitable parameter to alter the required delay is the magnetizing inductance of the converter. Validity of the equations for determining the time delays is verified with simulations.

Publication P[6]

Publication P[6] contains a study of the effect of the magnetizing inductance on the performance of the forward with active clamp and self-driven synchronous rectifiers. It is noted that the magnetizing inductance can be used to alter the required time delay if a low-voltage turn on is desired for the main switch.

Voltage ripple on the clamp capacitor voltage is also determined. The ripple is dependent on the magnetizing inductance, and moreover, the ripple is visible in the control voltage for one of the two self-driven synchronous rectifiers.

The publication includes measurement results from a 3.4 V 30 A FAC converter with self-driven synchronous rectifiers. Measurements show the effect of the magnetizing inductance on the drain-source voltage during the resonant transition and

on the control voltage for the self-driven synchronous rectifiers. Also, the effect of a too lengthy time delay between the primary side switches is shown in the measured figures.

Publication P[7]

This paper presents a study of the applicability and advantage of the use of the resonant transition in forward with active clamp and self-driven synchronous rectifiers. The emphasis is on the comparison of the achieved efficiency with different voltage levels over the primary switch prior to turning on. A comparison between expected losses with different turn-on voltage levels for the main switch is performed. Calculations and measurements show that, at low loads, a reduced voltage level improves the efficiency but, on the other hand, at high loads the advantage is not so significant or it may be totally lost, mainly due to the increased losses of the self-driven synchronous rectifiers. The publication includes discussion on the effect of the magnetizing inductance on the efficiency of the converter and the optimal voltage level at which the primary switch should be turned on.

Publication P[8]

In publication P[8], an analysis of the impact of the turn-on voltage level on the efficiency of the FAC converter with self-driven synchronous rectifiers is given. The study reported in the publication is similar to that of publication P[7]. However, ZVS, i.e. zero voltage switching was included in this analysis and the loss comparison was performed for the ZVS and the normal construction of the FAC converter. It was found out that at relatively high switching frequencies ZVS strategy could return the best efficiency. However, it was noted that the efficiency of the ZVS FAC converter depends strongly on the on-resistance of the additional component, which is needed in ZVS.

7 Contribution of this Thesis

The work presented in this Thesis had two main directions: single-stage PFC circuits and low output voltage dc-dc conversion. The motivation behind the research was to find ways to improve the performance of the presented converter topologies. Main contributions of this Thesis are summarized as follows:

- One of the main results in the field of single-stage PFC converters was the steady state and small signal analyses that were performed for the dither converter.
- The other main result in the same area was the development of the passive clamp circuit for the BIFRED converter. It was shown that the passive clamp reduces voltage stress over the switch.
- Equations for determining the delay for turn-on at the input voltage level and for ZVS were determined for the FAC converter. The analysis was verified with a set of simulations.
- A method of loss comparison was developed to assess the effect of different voltage levels over the main switch at turn-on on the efficiency of the FAC converter. Additionally, the loss contributors were determined.
- It was shown that the minimization of the turn-on losses for the main switch of the FAC converter with synchronous rectifiers is not necessarily advantageous from the point of view of overall efficiency of the converter. Careful measurements were performed to verify the analysis.

This Thesis contributes new ideas and methods to improve the performance of the researched switched mode converters.

8 Conclusions

Three single-stage power factor correction converters and a forward type dc-dc converter were considered in this Thesis. The power factor correction converters are used to shape the line current to resemble the line voltage waveform. On the other hand, dc-dc converters are used to provide regulated load voltages.

Stricter requirements and harmful effects of distorted line current have prompted a need for power factor correction converters. An additional power processing stage in a power supply increases the cost of the product. Low power supplies are, however, mass production devices, and are therefore sensitive to any additional increase in the manufacturing cost. Single-stage power factor correction converters offer an interesting alternative to the two-stage PFC solution. This is due to the fact that in a single-stage converter only one active switching stage is used, and therefore, the component count is lower than in a two-stage power supply topology.

Steady state and small signal analyses were performed for the dither converter. The converter is an interesting single-stage converter since it does not suffer from high initial bulk capacitor voltage. The analyses were verified with simulations and good agreement between the analyses and simulations were obtained. For further research, the steady state and small signal analyses could be verified with measurements from a dither prototype.

The BIFRED and BIBRED converters are two well-known single-stage converters. The two converters resemble isolated versions of SEPIC and Cúk converters, respectively. In these two converters the leakage inductance of the transformer causes, with a traditional kind of resonant snubber, a relatively high voltage stress on the switch at turn-off. The turn-off transition for these two converters with a resonant type of snubber was analyzed. It was concluded that with a short resonant transition the voltage stress is high. In order to relieve the problem the duration of the transition period has to be made longer. Moreover, voltage stress over

the switch is determined by the boost inductor and transformer current at every turn-off. Therefore, the voltage stress is dependent on load and line transients.

A passive clamp circuit was developed for the BIFRED converter. A detailed description of the operation principles of the circuit was given. The idea of the passive clamp circuit is to clamp the switch voltage to a known dc voltage at every turn-off. With this clamp circuit, the voltage stress on the switch can be reduced or the duration of the resonant transition can be made shorter with a moderate voltage stress. A lower voltage stress allows for the use of a switch with a lower voltage rating. This may reflect in savings in the manufacturing cost or reduced conduction losses. Only the DCM – DCM operation mode of the BIFRED with passive clamp circuit was analyzed. For further research, analysis of the DCM – CCM behavior of the converter would be interesting. Also, a comparison of achieved efficiencies between a BIFRED converter with passive clamp and with resonant snubber could be of interest.

A forward converter with active clamp was analyzed in the dc-dc part of this Thesis. The active clamp circuit is used to demagnetize the transformer after every on period of the main switch. The active clamp circuit also acts as a snubber circuit for the main switch and is able to recycle the magnetizing and leakage energy. This converter is particularly interesting for low voltage conversion. This is because the active clamp circuit provides a voltage waveform over the windings of the transformer that is virtually without dead times, i.e. the voltage is not zero during the off period of the main switch. The FAC converter can therefore be used with self-driven synchronous rectification, which is more or less mandatory in low voltage and high current conversion, without causing excessive body diode conduction on the secondary side.

The time intervals that are required for turn-on of the main switch at input voltage and at zero voltage level were determined. The analysis was verified with simulations. Also, the effect of the turn-on voltage level over the main switch on the efficiency of the converter with self-driven synchronous rectifiers was investigated. It was found that it is not necessarily advantageous to try to minimize the turn-on loss for the main switch, a feature that is attainable with the FAC converter relatively easy. The reason for this is that the control signal will be lost for the synchronous rectifier for a small period of time at the end of the off period and that causes additional

rectification losses. The analysis was verified with a FAC prototype converter. A topic for further research could investigate the comparison of achieved efficiencies with different turn-on voltage levels over the main switch so that zero voltage switching is also included.

References

Acik, A. and Cadirci, I. (2003). Active clamped ZVS forward converter with soft-switched synchronous rectifier for high efficiency, low output voltage applications. *IEE Proceedings - Electric Power Applications*, Vol. 150 Issue: 2, March 2003, pp. 165-174.

Alou, P., Cobos, J.A., Garcia, C., Prieto, R. and Uceda, J. (1997). Design guidelines for a resonant reset forward converter with self-driven synchronous rectification. *Proceedings of 23rd International Conference on Industrial Electronics, Control and Instrumentation, IECON'97,* New Orleans, Louisiana, 9-14 November 1997, Vol. 2, pp. 593-598.

Blanc, J. (1991). Practical application of MOSFET synchronous rectifiers. *Proceedings of 13th International Telecommunications Energy Conference, INTELEC'91,* Kyoto, Japan, 5-8 November 1991, pp. 495-501.

Bridge, C.D. (2000). Clamp voltage analysis for RCD forward converters. *Proceedings of 15th Annual IEEE Applied Power Electronics Conference and Exposition, APEC'00,* New Orleans, Louisiana, 6-10 February 2000, Vol. 2, pp. 959-965.

Brkovic, M. and Cúk, S. (1992). Input current shaper using Cúk converter. *Proceedings of 14th International Telecommunications Energy Conference, INTELEC'92,* Washington, D.C., 4-8 October 1992, pp. 532-539.

Carsten, B. (1990). Design techniques for transformer active reset circuits at high frequencies and power levels. *Proceedings of High Frequency Power Conversion Conference, HFPC'90,* Santa Clara, California, May 1990, pp. 235-246.

Cha, Y.K., Ryu, M.H., Choi, Y.T., Choi, B.C. and Kim, H.G. (1998). Single stage AC/DC converter with low conduction loss and high power factor. *Proceedings of 29th Annual IEEE Power Electronics Specialists Conference, PESC'98,* Fukuoka, Japan, 17-22 May 1998, Vol. 2, pp. 1362-1367.

Chen, W., Dai, N., Hua, G., Sable, D. and Lee, F.C. (1995). Design of a High-Efficiency, Low-Profile Forward Converter with 3.3V Output. *Converters and Distributed Power Systems,* V*irginia Power Electronics Center* (*VPEC)*, 1995, Vol. VIII, pp. 11-18.

Chryssis, G. (1989). *High-Frequency Switching Power Supplies: Theory and Design* (2nd edition). McGraw-Hill, 1989, 287 p.

Cobos, J.A., Garcia, O., Sebastian, J. and Uceda, J. (1993). Active clamp PWM forward converter with self driven synchronous rectification. *Proceedings of 15th International Telecommunications Energy Conference, INTELEC'93,* Paris, France, 27-30 September 1993,Vol. 2, pp. 200-206.

Cobos, J.A., Garcia, O., Sebastian, J. and Uceda, J. (1993). RCD clamp PWM forward converter with self driven synchronous rectification. *Proceedings of International Conference on Industrial Electronics, Control and Instrumentation, IECON'93,* Lahaina, Hawaii, 15-18 November 1993, Vol. 2, pp. 1336-1341.

Cobos, J.A., Garcia, O., Sebastion, J. and Uceda, J. (1994). Resonant reset forward topologies for low output voltage on board converters. *Proceedings of 9th Annual Applied Power Electronics Conference and Exposition, APEC'94,* Orlando, Florida, 13-17 February 1994, Vol. 2, pp. 703-708.

Cúk, S. and Middlebrook, R. D. (1977a). A general unified approach to modeling switching-converters power stages. *International Journal of Electronics*, June 1977, Vol. 42, No. 6, pp. 521-550.

Cúk, S. and Middlebrook, R. D. (1977b). A general unified approach to modeling switching dc-to-dc converters in discontinuous conduction mode. *Proceedings of IEEE Power Electronics Specialists Conference, PESC'77,* Palo Alto, California, 14-16 June 1977, pp. 36-57.

de la Cruz, E., Vazquez, M. and Rodriguez, J.J. (1993). Analysis of suitable PWM topologies to meet very high efficiency requirements for on-board DC/DC converters in future telecom systems. *Proceedings of 15th International Telecommunications Energy Conference, INTELEC'93,* Paris, France, 27-30 September 1993, Vol. 2, pp. 207-214.

Domb, M., Redl, R. and Sokal, N.O. (1982). Nondissipative turn-off snubber alleviates switching power dissipation, second-breakdown stress and V_{CE} overshoot: analysis, design procedure and experimental verification. *Proceedings of 13th Annual IEEE Power Electronics Specialists Conference, PESC'82,* Cambridge, Massachusetts, 14-17 June 1982, pp. 445-454.

Erickson, R. W. and Maksimovic, D. (2001). *Fundamentals of Power Electronics* (2nd edition). Kluwer Academic Publishers, 2001, 883 p.

Fontán, A., Ollero, S., de la Cruz, E. and Sebastian, J. (1998). Peak current mode control applied to the forward converter with active clamp. *Proceedings of 29th Annual IEEE Power Electronics Specialists Conference, PESC'98,* Fukuoka, Japan, 17-22 May 1998, Vol. 1, pp. 45-51.

Garcia, O., Cobos, J.A., Alou, V, Prieto, V. and Uceda, J. (1999). A simple single-switch single-stage AC/DC power converter with fast output voltage regulation. *Proceedings of 30th Annual IEEE Power Electronics Specialists Conference, PESC'99,* Charleston, South Carolina, 27 June – 1 July 1999, Vol. 1, pp. 111-116.

Garcia, O., Cobos, J.A., Alou, V, Prieto, V. and Uceda, J. (2000). Simple AC/DC converters to meet IEC 1000-3-2. *Proceedings of 15th Annual IEEE Applied Power Electronics Conference and Exposition, APEC'00,* New Orleans, Louisiana, 6-10 February 2000, Vol. 1, pp. 487-493.

Grigore, V. and Kyyrä, J. (1999a). Analysis of a high power factor rectifier based on discontinuous capacitor voltage mode operation. *Proceedings of 30th Annual IEEE Power Electronics Specialists Conference, PESC'99,* Charleston, South Carolina, 27 June – 1 July 1999, Vol. 1, pp. 93-98.

Grigore, V. and Kyyrä, J. (1999b). High power factor rectifier based on buck converter operating in discontinuous capacitor voltage mode. *Proceedings of 14th Annual IEEE Applied Power Electronics Conference, APEC'99,* Dallas, Texas, 14-18 March 1999, Vol. 1, pp. 612-618.

Grigore, V. (2001). *Topological issues in single-phase power factor correction*. Doctoral Dissertation, Helsinki University of Technology, Helsinki, Finland, 2001, 114 p.

IEC 1000-3-2 (1995-3) (1995). Ed. 1: Electromagnetic compatibility (EMC) –Part 3-2: Limits - Limits for harmonics current emission (equipment input current ≤16 A per phase), IEC 1995.

IEC 61000-3-2-aml (2001-8) (2000). Ed. 2: Electromagnetic compatibility (EMC) – Part 3-2: Limits - Limits for harmonics current emission (equipment input current ≤16 A per phase), IEC 2000.

IEC 61000-3-2-aml (2001-8) (2001). Amendment 1: Electromagnetic compatibility (EMC) –Part 3-2: Limits - Limits for harmonics current emission (equipment input current ≤16 A per phase), IEC 2001.

Ji, H.K. and Kim, H.J. (1994). Active clamp forward converter with MOSFET synchronous rectification. *Proceedings of 25th Annual IEEE Power Electronics Specialists Conference, PESC'94,* Taipei, Taiwan, 20-25 June 1994, Vol. 2, pp. 895-901.

Jin, C.-F. and Ninomiya, T. (2001). A novel soft-switched single-stage AC-DC converter with low line-current harmonics and low output-voltage ripple. *Proceedings of 32nd Annual Power Electronics Specialists Conference, PESC'01,* Vancouver, Canada, 17-22 June 2001, Vol. 2, pp. 660-665.

Jitaru, I.D. (1991). Constant frequency, forward converter with resonant transition. *Proceedings of High Frequency Power Conversion Conference, HFPC'91,* Toronto, Ontario, Canada, 9-14 June 1991, pp. 282-292.

Jitaru, I.D. (1992). Fixed frequency single ended forward converter switching at zero voltage. U.S. Patent No. 5,126,931. 30th June 1992.

Jitaru, I.D. (2003). Self-driven constant voltage reset circuit. *Proceedings of 18th Annual IEEE Applied Power Electronics Conference and Exposition, APEC'03*, Miami Beach, Florida, 9-13 February 2003, Vol. 2, pp. 893-897.

Jovanović M.M., Tsang, D.M.C. and Lee, F.C. (1994). Reduction of voltage stress in integrated high-quality rectifiers-regulators by variable-frequency control. *Proceedings of 9th Annual IEEE Applied Power Electronics Conference and Exposition, APEC'94,* Orlando, Florida, 13-17 February 1994, pp. 569-575.

Lazar, J. and Cúk, S. (1995). Open loop control of a unity power factor, discontinuous conduction mode boost rectifier. *Proceedings of 17th International Telecommunications Energy Conference, INTELEC'95,* The Hague, The Netherlands, 29 October – 1 November 1995, pp. 671-677.

Lee, J.-Y., Moon, G.-W., Jung, Y.-S. and Youn, M.-J. (1996). A new single-stage AC/DC converter with high efficiency and high power factor. *Proceedings of 18th International Telecommunications Energy Conference, INTELEC'96,* Boston, Massachusetts, 6-10 October 1996, pp. 263-270.

Lee, Y.S., Siu, K.W. and Lin, B.T. (1997). Novel single-stage isolated power-factor-corrected power supplies with regenerative clamping. *Proceedings of 12th Annual Applied Power Electronics Conference and Exposition*, *APEC'97,* Atlanta, Georgia, 23-27 February 1997, Vol. 1, pp. 259-265.

Leu, C.S., Hua, G., Lee, F.C. and Zhou, C. (1992). Analysis and design of R-C-D clamp forward converter. *Proceedings of High Frequency Power Conversion Conference, HFPC'92,* San Diego, California, May 1992, pp. 198-208.

Li, Q., Lee, F.C. and Jovanovic, M.M. (1998). Large-signal transient analysis of forward converter with active-clamp reset. *Proceedings of 29th Annual IEEE Power Electronics Specialists Conference, PESC'98,* Fukuoka, Japan, 17-22 May 1998, Vol. 1, pp. 633 -639.

Li, Q., Lee, F.C and Jovanovic, M. M. (1999). Design considerations of transformer DC bias of forward converter with active-clamp reset. *Proceedings of 14th Annual IEEE Applied Power Electronics Conference and Exposition, APEC'99,* Dallas, Texas, 14-18 March 1999, pp. 553-559.

Li, Q. and Lee, F.C. (2000). Design consideration of the active-clamp forward converter with current mode control during large-signal transient. *Proceedings of 15th Annual IEEE Applied Power Electronics Conference and Exposition, APEC'00,* New Orleans, Louisiana, 6-10 February 2000, Vol. 2, pp. 966-972.

Li, Q., Lee, F.C. and Jovanovic, M.M. (2002). Large-signal transient analysis of forward converter with active-clamp reset. *IEEE Transactions on Power Electronics*, Vol. 17 Issue: 1, Jan. 2002, pp. 15-24.

Li, Q. and Lee, F.C. (2003). Design consideration of the active-clamp forward converter with current mode control during large-signal transient. *IEEE Transactions on Power Electronics*, Vol. 18 Issue: 4, July 2003, pp. 958-965.

Lidow, A. and Sheridan, G. (2003). Defining the future for microprocessor power delivery. *Proceedings of 18th Annual IEEE Applied Power Electronics Conference and Exposition, APEC'03,* Miami Beach, Florida, 9-13 February 2003, Vol. 1, pp. 3-9.

Liu, K.-H. and Lin, Y.-L. (1989). Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters. *Proceedings of 20th Annual IEEE Power Electronics Specialists Conference, PESC'89*, Milwaukee, WI, 26-29 June 1989, Vol. 2, pp. 825-829.

Madigan, M.T., Erickson, R.W. and Ismail, E.H. (1992). Integrated high-quality rectifier-regulators. *Proceedings of 23rd Annual IEEE Power Electronics Specialists Conference, PESC'92*, Toledo, Spain, 29 June – 3 July 1992, Vol. 2, pp. 1043-1051.

Madigan, M.T., Erickson, R.W. and Ismail, E.H. (1999). Integrated high-quality rectifier-regulators. *IEEE Transactions on Industrial Electronics*, Vol. 46 Issue: 4, August 1999, pp. 749-758.

Mohan, N., Undeland, T.M. and Robbins, W.P. *Power Electronics Converters Applications and Design* (2nd edition). John Wiley & Sons, Inc. 1995.

Murakami, N. and Yamasaki, M. (1988). Analysis of a resonant reset condition for a single-ended forward converter. *Proceedings of 19th Annual IEEE Power Electronics Specialists Conference, PESC'88,* Kyoto, Japan, 11-14 April 1988, Vol. 2, pp. 1018-1023.

Newton, A., Green, T.C. and Andrew, D. (2000). AC/DC power factor correction using interleaved boost and Cúk converters. *Proceedings of 8th International Conference on Power Electronics and Variable Speed Drives (IEE Conference Publication No. 475),* London, U.K., 18-19 September 2000, pp. 293-298.

Ninomiya, T., Tanaka, T. and Harada, K. (1985). Optimum design of nondissipative snubbers by the evaluation of transistor's switching loss, surge voltage and, surge

current. *Proceedings of 16th Annual IEEE Power Electronics Specialists Conference, PESC'85,* Toulouse, France, 24-28 June 1985, pp. 283-290.

Ninomiya, T., Tanaka, T. and Harada, K. (1988). Analysis and optimization of a nondissipative LC turn-off snubber. *IEEE Transactions on Power Electronics*, Vol. 3 Issue: 2 , April 1988, pp. 147-156.

Oba, T., Murabayashi, H., Murasige, S. and Takahashi, I. (1998). Single-switch buck-boost type dither PFC converter. *Proceedings of 29th Annual IEEE Power Electronics Specialists Conference, PESC'98,* Fukuoka, Japan, 17-22 May 1998, pp. 1822-1827.

Redl, R., Balogh, L. and Sokal, N.O. (1994). A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage. *Proceedings of 25th Annual IEEE Power Electronics Specialists Conference, PESC'94*, Taipei, Taiwan, 20-25 June 1994, Vol. 2, pp. 1137-1144.

Redl, R. and Balogh, L. (1995a). Design considerations for single-stage isolated power-factor-corrected power supplies with fast regulation of the output voltage. *Proceedings of 10th Annual Applied Power Electronics Conference and Exposition, APEC'95,* Dallas, Texas, 5-9 March 1995, Vol. 1, pp. 454-458.

Redl, R., and Kislovski, A.S. (1995b). Telecom power supplies and power quality. *Proceedings of 17th International Telecommunications Energy* Conference*, INTELEC'95,* The Hague, The Netherlands, 29 October – 1 November 1995, pp. 13-21.

Redl, R. (1996). Power electronics and electromagnetic compatibility. *Proceedings of 27th Annual IEEE Power Electronics Specialists Conference, PESC'96,* Baveno, Italy, 23-27 June 1996, Vol. 1, pp. 15-21.

Redl, R., Tenti, P. and Daan van Wyk, J. (1997). Power electronics' polluting effects. *IEEE Spectrum*, Vol. 34 Issue: 5, May 1997, pp. 32-39.

Sarjeant, W.J. Clelland, I.W. and Price, R.A. (2001). Capacitive components for power electronics. *Proceedings of the IEEE*, Vol. 89 Issue: 6, June 2001, pp. 846-855.

Shaughnessy, W. (1980). Modelling and design of non-dissipative LC snubber networks. *Proceedings of 7th National Solid-State Power Conversion Conference, POWERCON 7*, San Diego, California, 24-27 March 1980, pp. G4.1-G4.9.

Simonetti, D.S.L., Sebastian, J., dos Reis, F.S. and Uceda, J. (1992). Design criteria for SEPIC and Cúk converters as power factor pre-regulators in discontinuous conduction mode. *Proceedings of the 1992 International Conference on Industrial Electronics, Control, Instrumentation and Automation*. *'Power Electronics and Motion Control',* San Diego, California, 9-13 November 1992, Vol. 1, pp. 283-288.

Stevens, J.L., Shaffer, J.S., Vandenham, J.T. (2002). The service life of large aluminum electrolytic capacitors: effects of construction and application. *IEEE Transactions on Industry Applications*, Vol. 38 Issue: 5, Sept.-Oct. 2002, pp. 1441-1446.

Tanaka, T., Ninomiya, T. and Harada, K. (1988). Design of a nondissipative turn-off snubber in a forward converter. *Proceedings of 19th Annual IEEE Power Electronics Specialists Conference, PESC'88,* Kyoto, Japan, 11-14 April 1988, Vol. 2, pp. 789-796.

Schenk, K. and Cúk, S. (1997). Small signal analysis and design of a single active switch converter providing power factor correction and full regulation. *Proceedings of 19th International Telecommunications Energy Conference, INTELEC'97*, Melbourne, Australia, 19-23 October 1997, pp. 124-131.

Schenk, K. and Cúk, S. (1998). Small signal analysis of converters with multiple discontinuous conduction modes. *Proceedings of 29th Annual IEEE Power Electronics Specialists Conference*, *PESC'98*, Fukuoka, Japan, 17-22 May 1998, Vol. 1, pp. 623-629.

Takahashi, I. and Igarashi, R.Y. (1991). A switching power supply of 99% power factor by the dither rectifier. *Proceedings of 13th International Telecommunications Energy Conference, INTELEC'91,* Kyoto, Japan, 5-8 November 1991, pp. 714-719.

Tuomainen, V. (1999). *Analysis of three single-stage converters for power factor correction.* Master of Science Thesis, Helsinki University of Technology, Helsinki, Finland, 1999, 67 p.

Tuomainen, V., Grigore, V., Wallius, J. and Kyyrä, J. (1999). Comparison of three single-stage solutions for low cost PFC. *Proceedings of 8th European Conference on Power Electronics and Applications, EPE 1999*, Lausanne, Switzerland, 7-9 September 1999.

Tuomainen, V. (2002). *Single-phase single-stage rectifiers – analysis and reduction of low-frequency output voltage ripple*. Licentiate of Science Thesis, Helsinki University of Technology, Helsinki, Finland, 2002, 56 p.

Vinciarelli, P. (1984). Optimal resetting of the transformer's core in single ended forward converters. U.S. Patent No. 4,441,146. 3rd April 1984.

Vorperian, V. (1996). The effect of the magnetizing inductance on the small-signal dynamics of the isolated Cúk converter. *IEEE Transactions on Aerospace and Electronic Systems*, Vol. 32 Issue: 3, July 1996, pp. 967-983.

Wang, J., Dunford, W.G. and Mauch, K., (1996). Input inductor current for unity power factor operation. *Proceedings of 27th Annual IEEE Power Electronics Specialists Conference, PESC'96*, Baveno, Italy, 23-27 June 1996, Vol. 2, pp. 1177-1183.

Willers, M.J., Egan, M.G., Murphy, J.M.D. and Daly, S. (1994). A BIFRED converter with a wide load range. *Proceedings of 20th International Conference on Industrial Electronics, Control and Instrumentation, IECON'94,* Bologna, Italy, 5-9 September 1994, Vol. 1, pp. 226-231.

Willers, M.J., Egan, M.G., Daly, S. and Murphy, J.M.D. (1999). Analysis and design of a practical discontinuous-conduction-mode BIFRED converter. *IEEE Transactions on Industrial Electronics*, Vol. 46 Issue: 4, Aug. 1999, pp. 724-733.

Zhang, J., Jovanovic, M.M. and Lee, F.C. (1999). Comparison between CCM single-stage and two-stage boost PFC converters. *Proceedings of 14th Annual Applied Power Electronics Conference and Exposition*, *APEC'99,* Dallas, Texas, 14-18 March 1999, Vol. 1, pp. 335-341.

Zhang, M.T. and Lee, F.C. (1996). Commutation analysis of self-driven synchronous rectifiers in an active-clamp forward converter. *Proceedings of 27th Annual IEEE Power Electronics Specialists Conference*, *PESC'96,* Baveno, Italy, 23-27 June 1996, Vol. 1, pp. 868-873.

Xie, X., Chung, H.Y. and Pong, M.H. (1999). Studies of self-driven synchronous rectification in low voltage power conversion. *Proceedings of the IEEE International*

Conference on Power Electronics and Drive Systems, PEDS'99, Hong Kong, 27-29 July 1999, Vol. 1, pp. 212-217.

Appendix A

Schematics of the BIFRED and FAC prototype converters

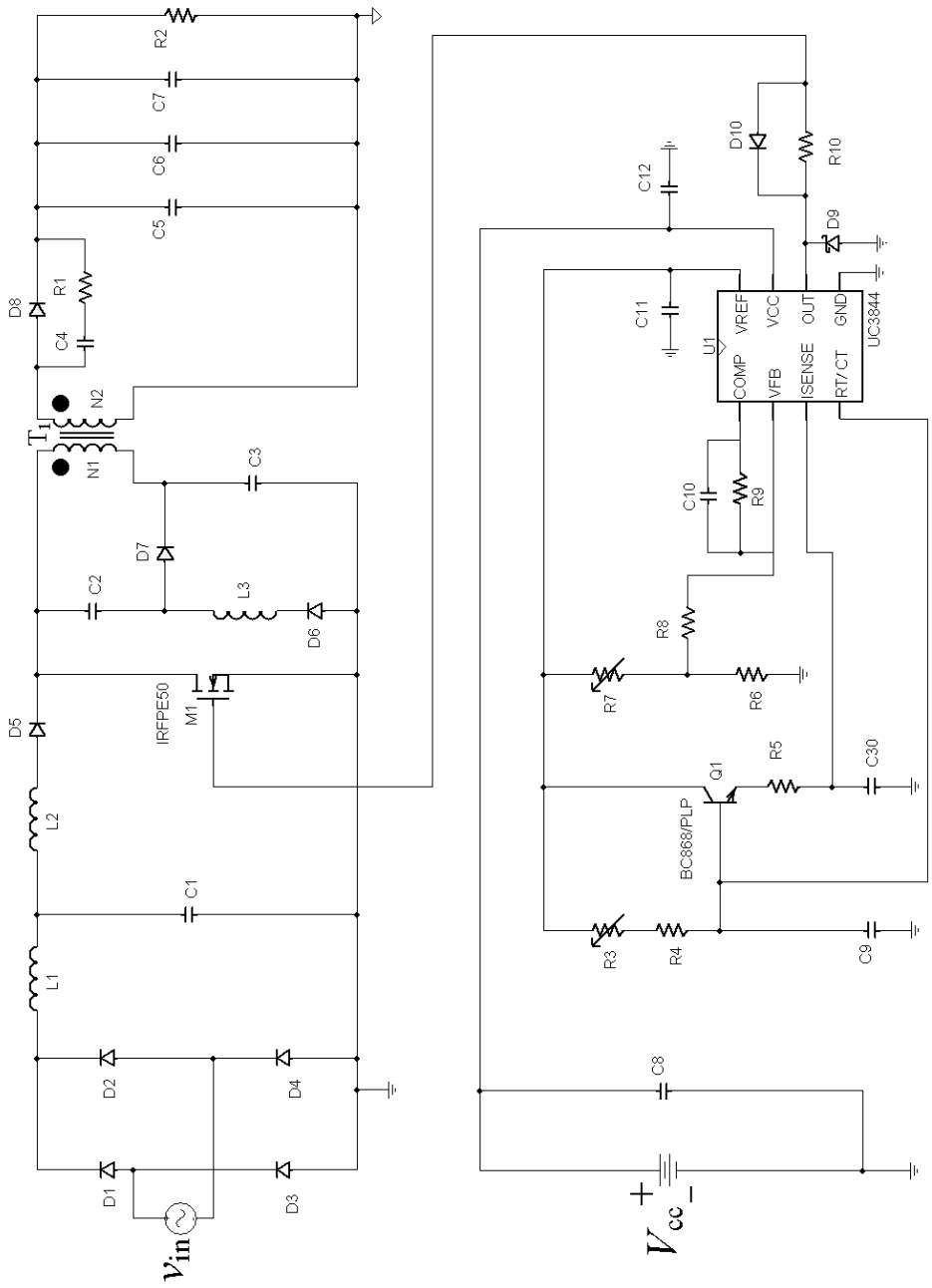

Figure A.1 Schematic of the BIFRED prototype converter.

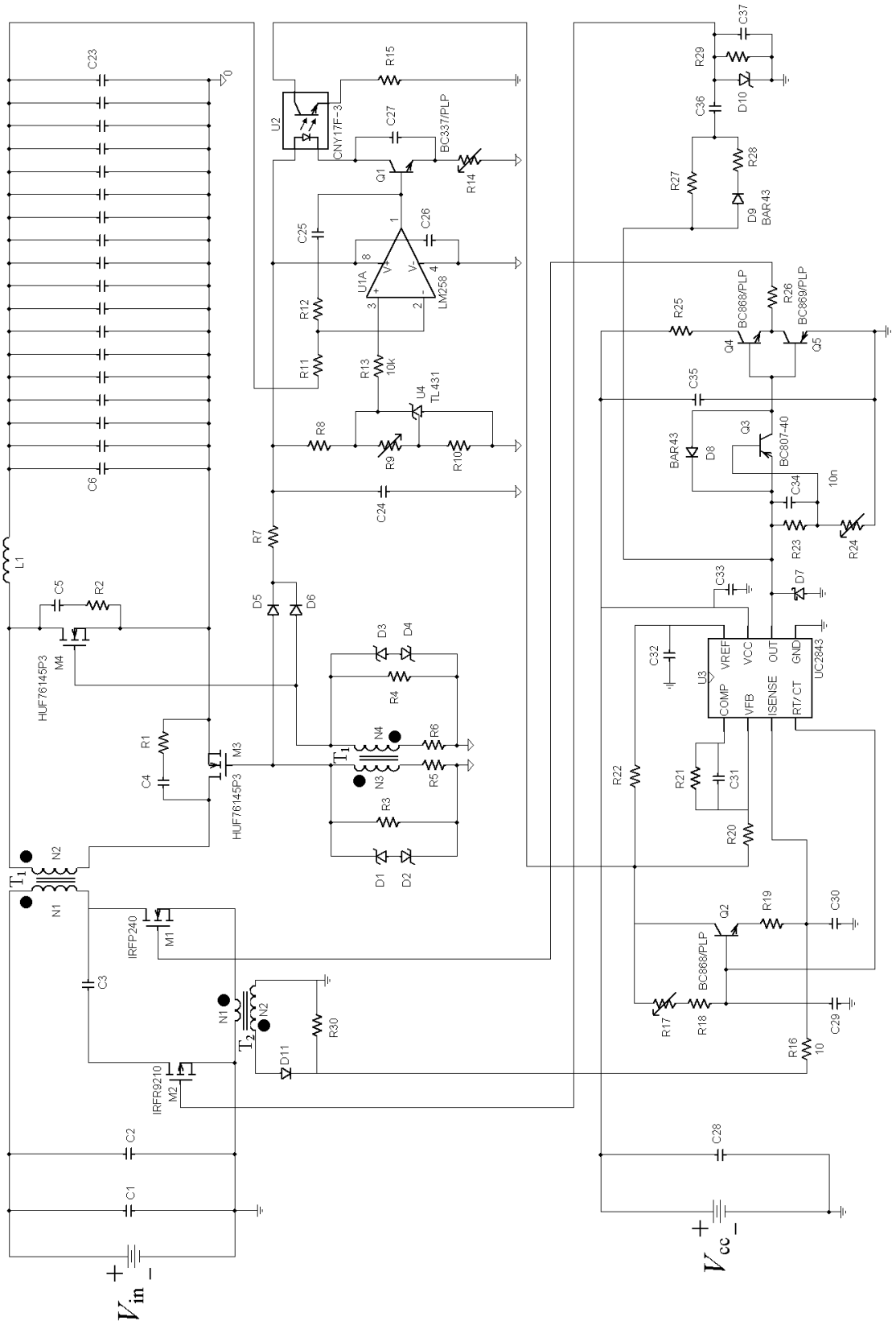

Figure A. 2 Schematic of the FAC prototype converter.