© 2002 Institute of Physics Publishing Ltd. Reprinted with permission from Journal of Micromechanics and Microengineering 12, number 2, pages 177-186.
http://www.iop.org/journals/jmm

INSTITUTE OF PHYSICS PUBLISHING JOURNAL OF MICROMECHANICS AND MICROENGINEERING

J. Micromech. Microeng. **12** (2002) 177–186 PII: S0960-1317(02)30930-6

Microelectromechanical capacitors for RF applications

H Nieminen, V Ermolov, K Nybergh, S Silanto and T Ryhänen

Nokia Research Center, PO Box 407, FIN-00045 NOKIA GROUP, Finland

E-mail: heikki.nieminen@nokia.com

Received 19 November 2001, in final form 25 January 2002
Published 18 February 2002
Online at stacks.iop.org/JMM/12/177

Abstract
This paper describes the design principles of electrostatically actuated microelectromechanical capacitors. Key properties, such as capacitance tuning range, quality factor (Q), different control methods, thermal stability, effect of radio frequency signal on capacitance and gas damping are examined. Experimental devices were designed and fabricated using the design principles. The two-gap capacitor has a measured nominal capacitance of 1.58 pF and achieves a tuning range of 2.25:1 with parasitics. When all parasitic capacitances to the substrate are extracted the measured nominal capacitance is 1.15 pF and the tuning range is 2.71:1. The device is made of electroplated gold and has a Q of 66 at 1 GHz, and 53 at 2 GHz. In addition, two- and three-state capacitors were designed, fabricated and characterized.

1. Introduction

Variable capacitors are key elements in many microwave and millimeter wave applications, such as electrically tunable filters, matching circuits and voltage controlled oscillators (VCOs) [1, 2]. The variable capacitors that are required in these applications can be implemented using a pn-junction [3]. The aforementioned applications require a high quality factor (Q), a wide tuning range and good linearity. A high Q is required for instance to minimize loss in the circuit. In addition filters require high Q devices, since the dynamic range of the filter is proportional to Q_F^2 [1], where Q_F is the quality factor of the whole filter. Furthermore, a wide tuning range allows applications in which the desired frequency band can be changed and the process and temperature variations compensated.

It has been proposed that one way to meet the aforementioned requirements is to use microelectromechanical (MEM) devices, for example MEM capacitors, as the main building blocks for radio frequency (RF) applications [4–8]. The main advantages of a MEM capacitor are a high Q when using metal as a structural material, a mechanical structure that isolates the control circuit from the signal circuit and mechanical inertia that prevents modulation of the capacitance value by the RF signal. State-of-the-art micromachined devices are mostly made of polysilicon, because polysilicon has superb mechanical properties and its technology is well known [9]. However, for RF devices such as the micromachined tunable capacitor, it is critical to minimize ohmic loss and to achieve a high Q. This has led to the use of metals. A Q of 62 at 1 GHz for a 2.11 pF capacitance value has been achieved with aluminum [10]. A polysilicon structure with an additional gold layer to increase conductivity has been reported to achieve a Q of 256 at 1 GHz for a 0.101 pF capacitance value [11]. A MEM capacitor also provides in theory a very high continuous tuning range. Using electrostatic actuation Dec and Suyama [12] have demonstrated a tuning range of 87% using a three-plate capacitor with a nominal capacitance of 4.0 pF and a Q of 15.4 at 1 GHz. In addition, Zuo *et al* [13] have demonstrated a tuning range of 69.8% using a two-gap metal capacitor that has separate signal and control electrodes.

The good linearity of a MEM capacitor is due to mechanical inertia. This isolates the voltage-controlled low frequency behavior of the capacitor from the effect of the RF signal. The RF signal does not modulate the capacitance because the mechanical inertia effectively damps any movement that is well above the first resonance frequency. However, the effective value of the RF signal voltage over the capacitor still affects the capacitance value of the MEM capacitor.

This paper presents several different MEM capacitors. The presented two-gap MEM capacitor has the largest tuning range reported to date. Section 2 describes and reviews the operational principles of a MEM capacitor. Key properties,

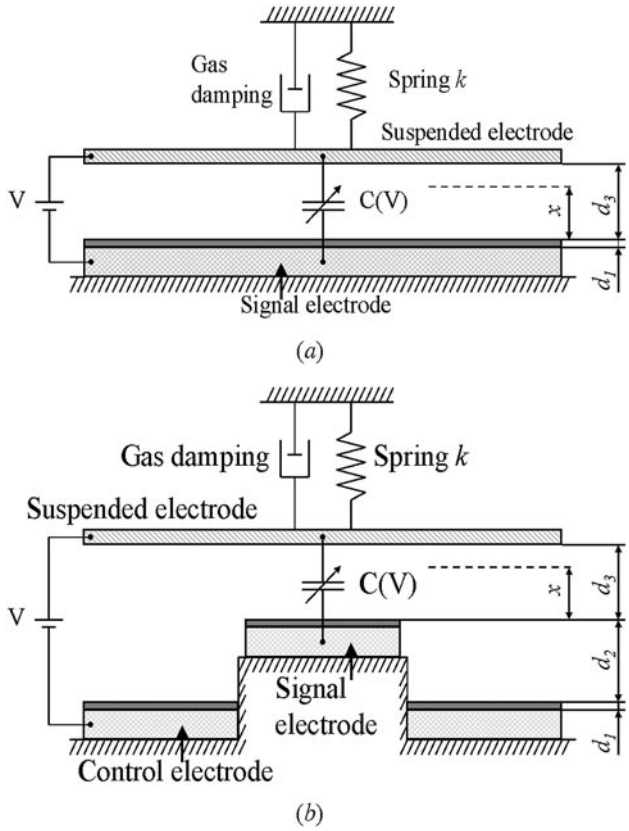

Figure 1. (*a*) Functional model of a one-gap MEM capacitor. (*b*) Functional model of a two-gap MEM capacitor.

such as the capacitance tuning range, different control methods, effect of the ac signal, thermal stability and the gas damping are discussed. Section 3 applies this information to the MEM capacitor design. The measurement results that are obtained from the fabricated components are presented in section 4. Finally, conclusions of the measurements are presented in section 5.

2. Operational principles

2.1. Parallel plate capacitor

A MEM tunable capacitor usually consists of two parallel plates: one plate is fixed and the other one is suspended using a mechanical spring with a spring constant k so that the control voltage V can vary the gap between the plates. The functional model of the one-gap MEM capacitor is shown in figure 1(*a*). d_1 is the thickness of the dielectric layer on top of the lower electrode, d_3 is the air gap between the electrodes under zero control voltage and x is the air gap when the control voltage is applied. The capacitance value can be controlled by the voltage difference or by controlling the charge on the capacitor plates. In the case of the voltage control, the voltage difference attracts the suspended electrode towards the fixed electrode until equilibrium between the spring force and the electrical force is reached. Mathematically this can be formulated as follows:

$$k(d_3 - x) = -\frac{\partial}{\partial x}\frac{1}{2}CU^2 = \frac{\varepsilon_0\varepsilon_r^2 AU^2}{2(d_1 + \varepsilon_r x)^2} \tag{1}$$

where A is the area of the capacitor plates, U is the control voltage, ϵ_r is the effective dielectric constant of the dielectric layer on top of metal 1 and ϵ_0 is the permittivity of the vacuum. Since the spring force is a linear function of the air gap and the electric force is inversely proportional to the second power of the air gap, there exists a stable equilibrium point only when

$$x \geqslant \frac{2}{3}d_3 - \frac{d_1}{3\varepsilon_r}. \tag{2}$$

After this point pull-in happens and the suspended electrode collapses on top of the fixed electrode. If the control voltage is decreased, the suspended electrode remains in its pull-in state until some voltage level, the release voltage, is reached. The pull-in limits the theoretical continuous tuning range of the voltage-controlled one-gap MEM capacitor to 50%. One way to get around the pull-in phenomenon is to use separate control and signal electrodes. In this case the air gap between the control electrode and the suspended electrode can be made larger than the gap between the signal electrode and the suspended electrode.

Figure 1(*b*) shows the functional model of the two-gap MEM capacitor structure. Dimension d_2 in the figure is the difference between the signal electrode air gap and the control electrode air gap. If for the gap d_3 between the signal electrode and suspended electrode the relation

$$d_3 \leqslant \frac{1}{2}d_2 + \frac{d_1}{2\varepsilon_r} \tag{3}$$

holds true, then pull-in due to the control voltage does not occur before the suspended electrode touches the signal electrode. In this case, the capacitance due to the dielectric layer defines the theoretical maximum tuning range.

Another way to increase the tuning range is to use charge control. In this case the equation between mechanical spring force and electrical force changes to

$$k(d_3 - x) = -\frac{\partial}{\partial x}\frac{1}{2}CU^2 = \frac{\partial}{\partial x}\frac{1}{2}\frac{q^2}{C} = \frac{q^2}{2\varepsilon_0 A} \tag{4}$$

where q is the charge pumped to the electrode. The force due to the charge is now independent of the gap and thus in the ideal case charge control allows full control of the capacitor air gap. However, in reality the parallel parasitic capacitance limits the maximum control range and leakage currents make the control of the amount of charge difficult. Several people have demonstrated different voltage and charge control methods. Table 1 compares the advantages and disadvantages of these methods.

A simple parallel plate capacitor as shown in figure 1(*a*) has a hysteretic capacitance as a function of voltage, due to pull-in. This hysteretic behavior can be used to operate a MEM capacitor in a multi-state mode as an alternative to a continuous operation mode. In the multi-state mode, the most important device parameters are the zero voltage and the pull-in capacitances, C_{off} and C_{on}, the pull-in voltage $U_{\text{pull-in}}$, and the release voltage U_{release}. Estimations for the capacitance values can be calculated using the parallel plate approximation. Estimation for the pull-in and the release voltage can be calculated assuming a linear spring force. This yields relationship between the ratio of the pull-in and the release voltage and the capacitance change ratio

$$\frac{U_{\text{release}}}{U_{\text{pull-in}}} = \frac{1}{\alpha}\left(\frac{3}{2}\right)^{\frac{3}{2}}\sqrt{\frac{2(\alpha - 1)}{\alpha}} \tag{5}$$

Table 1. Different MEM capacitor control methods.

Method	Advantages	Disadvantages
Charge control with IC control circuit [14]	Requires just slightly larger supply voltage than the pull-in voltage of the capacitor [15]	Resetting consumes power, can be sensitive to leakage currents
Charge control using a coil [16]	Very low ac control signal	Requires high Q coil
Two-gap capacitor structure [13]	Simple, separate control and signal electrodes	Large control voltage
Charge control using capacitive feedback [17]	Simple	Large control voltage, can be sensitive to leakage currents

where

$$\alpha = \frac{C_{\text{off}}}{C_{\text{on}}}. \tag{6}$$

2.2. Effective value of ac voltage over MEM capacitor

MEM capacitors typically resonate mechanically at frequencies below 100 kHz. This creates the key benefit of the micromachined tunable capacitors: the radio frequency signals do not modulate the capacitance value. However, the RMS value of the ac voltage influences the capacitance value. This can be seen from the equation for the electrostatic force between the capacitor plates:

$$\begin{aligned} F_{\text{RF}} &= \frac{\varepsilon_0 \varepsilon_r^2}{2\,(d_1 + \varepsilon_r x)^2} (\hat{U}_{\text{ac}} \sin \omega t)^2 \\ &= \frac{\varepsilon_0 \varepsilon_r^2}{2\,(d_1 + \varepsilon_r x)^2} \hat{U}_{\text{ac}}^2 \left(\frac{1}{2} - \frac{1}{2} \cos 2\omega t \right). \end{aligned} \tag{7}$$

This means that the RMS value of the ac voltage ($U_{\text{RF}} = \hat{U}_{\text{RF}}/\sqrt{2}$) limits the available tuning range, because it can cause pull-in. The critical point in the gap when the RF signal causes pull-in is the first zero of the equality pair

$$\begin{cases} F_{\text{total}} = F_{\text{control}}(x) + F_{\text{RF}}(x) - F_{\text{mech}}(x) = 0 \\ \nabla F_{\text{total}} = \nabla F_{\text{control}}(x) + \nabla F_{\text{RF}}(x) - \nabla F_{\text{mech}} = 0 \end{cases} \tag{8}$$

on the positive side of the origin. Inserting (1) and (7) into (8) yields

$$\begin{cases} \dfrac{\varepsilon_0 \varepsilon_r^2 A_2}{2(d_1 + \varepsilon_r (x + d_2))^2} U^2 + \dfrac{\varepsilon_0 \varepsilon_r^2 A_1}{4\,(d_1 + \varepsilon_r x)^2} \hat{U}_{\text{RF}}^2 \\ \quad - k(d_3 - x) = 0 \\ -\dfrac{\varepsilon_0 \varepsilon_r^3 A_2}{(d_1 + \varepsilon_r (x + d_2))^3} U^2 - \dfrac{\varepsilon_0 \varepsilon_r^3 A_1}{2\,(d_1 + \varepsilon_r x)^3} \hat{U}_{\text{RF}}^2 + k = 0. \end{cases} \tag{9}$$

Equation (9) can be solved numerically using the dimensions of the two-gap MEM capacitor. The two-gap MEM capacitor dimensions are $d_1 = 0.1\ \mu$m, $d_2 = 1\ \mu$m, $d_3 = 0.5\ \mu$m, $\varepsilon_r = 1.67$, $A_1 = 204\ \mu\text{m} \times 308\ \mu\text{m}$, $A_2 = 2 \times 96\ \mu\text{m} \times 308\ \mu\text{m}$. Figure 2 shows the result: the theoretical maximum tuning range as a function of the RMS value of the RF voltage that is normalized to the pull-in voltage of the signal electrode.

2.3. Capacitance behavior due to mechanical stress and temperature variation

There are two problems when metal is used as a structural material in micromechanical devices. First, there is a large temperature-dependent stress that is caused by the difference between the coefficient of thermal expansion (CTE) of the substrate and the metal. The second problem is warping of the thin suspended metal membrane, due to the variation of the intrinsic stress over the membrane. The second problem is considered to be a process development issue that cannot be solved by changing the design parameters. However, the temperature-dependent stress is a design issue. For a gold film on top of a silicon substrate, the temperature dependence of the stress is ~1 MPa °C^{-1}.

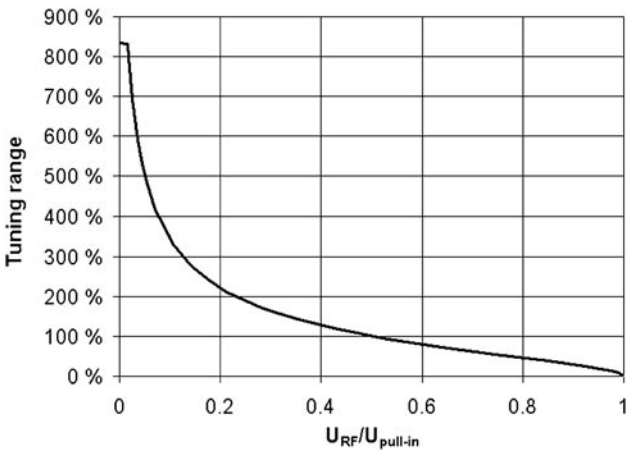

Figure 2. The maximum tuning range as a function of the RMS value of the RF signal normalized to the pull-in voltage of the signal electrode. The two-gap MEM capacitor dimensions are $d_1 = 0.1\ \mu$m, $d_2 = 1\ \mu$m, $d_3 = 0.5\ \mu$m, $\varepsilon_r = 1.67$, $A_1 = 204\ \mu\text{m} \times 308\ \mu\text{m}$, $A_2 = 2 \times 96\ \mu\text{m} \times 308\ \mu\text{m}$.

Figure 3 shows how this temperature-dependent stress affects the capacitance as a function of control voltage of the two-gap capacitor. Figure 3 is simulated using a finite difference model of a two-gap capacitor with the dimensions mentioned in the caption of figure 2 and depicted in figure 4. The initial condition in the simulation was that the intrinsic stress at room temperature was 65 MPa. Several methods have been suggested to eliminate the temperature-dependent stress. Corrugations of the diaphragm [18] and springs [10, 12] have been used.

2.4. Acceleration sensitivity

Inertial force always affects the freestanding micromechanical structures. In order to evaluate the effect of acceleration on

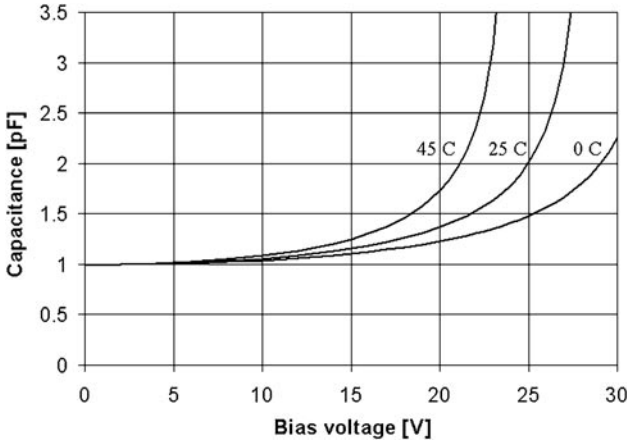

Figure 3. Simulated effect of temperature on the two-gap capacitor behavior. Shown are the capacitance as a function of the control voltage at temperatures 0, 25 and 45 °C. Dimensions as in figures 2 and 4.

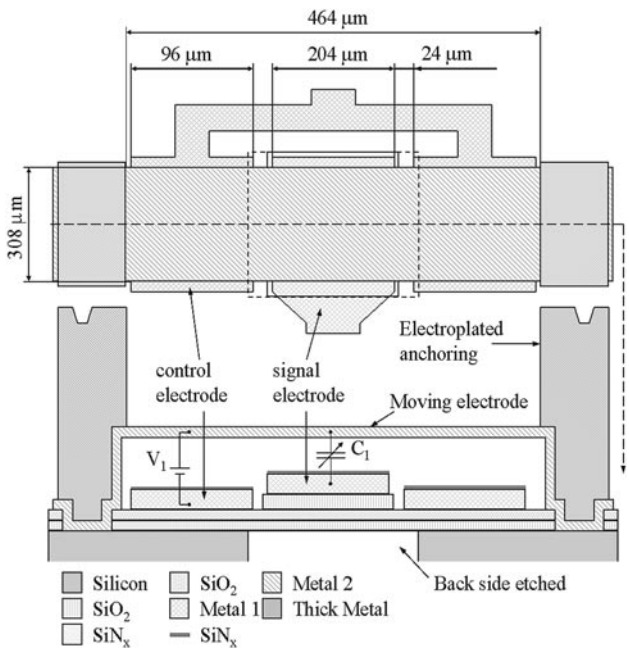

Figure 4. Top and cross-section view of the capacitor structure with separate control and signal electrodes and two different air gaps.

the bending of the micromechanical bridge, the acceleration-induced bending has to be compared with the electrostatic force used for bending the structure. One way is to calculate the capacitance change due to random acceleration a:

$$C_a = \left(\frac{\partial C}{\partial p}\right) \cdot \left(\frac{\partial p}{\partial a}\right) \cdot a \tag{10}$$

$$\frac{\partial p}{\partial a} = \rho \cdot t \tag{11}$$

where $\partial C/\partial p$ is the pressure-to-capacitance transfer function, $\partial p/\partial a$ is the acceleration-to-pressure transfer function, ρ is the density and t is the thickness of the suspended electrode. Table 2 shows a list of different acceleration sources and values that can be used for them. The third and the fourth columns show the calculated capacitance change due to acceleration.

Table 2. Different acceleration sources.

Source	Input value, a	$(C_a - C_0)/C_0$ (25 MPa)	$(C_a - C_0)/C_0$ (65 MPa)
Earth gravitational field	1 g	0.01%	0.005%
Strong shock	50 g	0.6%	0.3%

Table 3. Layer thicknesses.

Layer	Thickness (μm)
Silicon dioxide	1
Silicon nitride	0.5
Step silicon dioxide	1
Metal 1 (gold)	1
Dielectric layer (SiN_x)	0.1
Sacrificial layer (polymer)	0.5/1.5
Metal 2 (gold)	0.5
Thick electroplated gold	10

The capacitor used in simulations is a two-gap bridge capacitor that is in tensile stress and has dimensions shown in figure 4 and table 3.

2.5. Transient behavior of the MEM capacitor

The mechanical frequency response and the switching time characterize the transient behavior of MEM devices. The switching time can be roughly approximated by 1/4 period of the membrane vibration in the first resonance frequency mode. The resonant frequency is dependent mainly on the geometry and the stiffness of the structure. The more rigid the structure the higher the first mechanical resonant frequency mode and also shorter the switching time. However, the required control voltage also increases.

Experiments show that the ambient gas pressure also has a strong influence on the mechanical frequency response due to the gas damping effect [19, 20]. The effect of the gas damping on the device performance varies as a function of ambient pressure. Consequently, gas damping can be divided in three regions depending on the gas pressure: (1) viscous damping (>10 mbar), (2) molecular damping (0.1–10 mbar) and (3) negligible gas damping (<0.1 mbar) compared to the internal material losses.

The components presented here are designed for the viscous damping regime. The design parameters that affect the damping, in addition to the gas pressure, are the relative size and the arrangement of the perforation holes compared to the air gap size. At the time when the design was made the model for the transient analysis of the device did not include the effect of many small perforation holes [20]. However, development for a compact model for squeezed-film damping is under way by Veijola and Mattila [21, 22].

3. Design of the MEM capacitor

Several different MEM capacitors were designed and fabricated by surface micromachining. In order to reduce cost, the devices were fabricated on low resistivity silicon (∼1 Ω cm). Because the low resistivity substrate causes losses, it was selectively removed under the fixed electrodes

as shown in figure 4. The structural material of the devices was chosen to be gold due to its high conductivity and due to fabrication issues. Since there was no suitable MEMS fabrication process available, a new process was developed by Tronic's Microsystems, France. The fabrication process uses gold to form both the fixed electrodes (metal 1) as well as the suspended electrodes (metal 2). On top of the metal 1 layer a silicon nitride dielectric layer ($\varepsilon_r = 7.5$) was formed. This isolates the suspended electrode from the fixed electrodes in the case of pull-in. The air gap was realized using a polymer as a sacrificial material. In order to remove the sacrificial material from underneath the metal 2 film, perforation holes were made to the suspended electrodes. The perforation holes were $4 \times 4\ \mu m^2$ in size with 12 μm spacing. The two-gap structures were realized using an additional oxide layer under selected fixed electrodes and by planarizing the polymer before the deposition of metal 2. In addition, the process contains a third metal layer, a thick electroplated gold layer that is used as a structural material in the capacitors and to form high Q coils.

3.1. Continuously tunable capacitor design

Figure 4 shows a simplified top and cross-section view of the designed capacitor structure with separate control and signal electrodes and two different air gaps. Table 3 shows the thicknesses of the layers used in the device. The design goals for the capacitor were a nominal capacitance value of 1.0 pF and a tuning range of 100%, when there is a 4 V peak-to-peak sinusoidal RF voltage over the capacitor.

The design procedure of the device begins from the signal electrode capacitance value. The capacitance is dependent on the gap between the electrodes and the area of the electrodes. In order to minimize the total area used, the gap should be as small as possible. Due to the process limitations the smallest nominal air gap between the signal electrode and the suspended electrode is 0.5 μm. As a result, the desired signal electrode capacitance of 1.0 pF can be achieved with a signal electrode area of $204 \times 308\ \mu m^2$.

The gap between the signal and the suspended electrode determines the gap between the control and the suspended electrode. According to equation (3), the nominal air gap between the control and the suspended electrode must be at least 1.5 μm to prevent pull-in. To prevent shorting between the signal and the suspended electrode during operation there is a 100 nm thick dielectric layer on top of the signal electrode. This dielectric layer is patterned to form square shaped dimples that are $4 \times 4\ \mu m^2$ in size with 12 μm spacing. The purpose of the pattern is to reduce the probability of stiction of the suspended electrode during contact.

According to figure 2 the maximum tuning range of the designed capacitor is dependent on the RMS value of the RF voltage over the capacitor and the pull-in voltage of the capacitor. The design target requires the capacitor to have a tuning range of 100%, when the RMS voltage over the capacitor is 1.42 V (4 V peak-to-peak sinusoidal signal). Using the data in figure 2 the design target for the signal electrode pull-in voltage can be calculated to be 2.82 V.

The parameters that affect the signal electrode pull-in voltage but not the capacitance value, are the thickness, stress and the length of the suspended electrode. The thickness of the suspended electrode (0.5 μm) is a process parameter. Using it as a design parameter should be avoided. The stress in the suspended electrode is also a process parameter. At the time of the design work the target value for the intrinsic stress at room temperature was 65 MPa. That leaves the length of the suspended electrode as the only free design parameter. A two-dimensional finite difference (FD) model of the two-gap capacitor is used to simulate the effect that the length of the bridge has on the pull-in voltage. The simulations show that the signal electrode pull-in voltage of 2.86 V is achieved when the length of the suspended bridge is 464 μm.

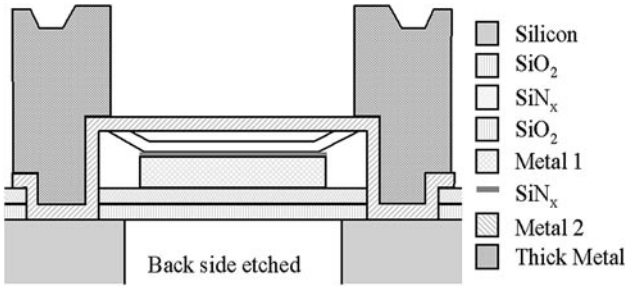

Figure 5. Cross-section view of a two-state capacitor structure.

The length of the bridge limits the size of the control electrodes. This in turn affects the required control voltage. The available size for the two control electrodes is $2 \times 96\ \mu m \times 308\ \mu m$. Because all the electrode sizes are known, the FD model can be used to estimate the required control voltage. Simulation that ignored the effect of the RF signal showed that the required control voltage to change the signal electrode capacitance 300% is 27 V. The major flaw in the design flow is that the temperature-dependent stress is not taken into account. This was done on purpose since research for a structure that eliminates the temperature-dependent stress but not the intrinsic stress is still going on.

3.2. Multi-state capacitor design

Figure 5 shows a cross-section view of a two-state capacitor. The design goals for the capacitor were $C_{on} = 15$ pF, $C_{off} = 1$ pF, and a pull-in voltage in the range of 3 to 5 V. The design procedure of the capacitor roughly follows the procedure used for the continuously tunable capacitor. The main difference is that now some of the process parameters have to be used as design parameters. The on/off capacitance ratio for instance, is only dependent on the air gap, the dielectric layer thickness, and the surface roughness. In order to get a required on/off capacitance ratio of 15 with an air gap of 0.5 μm the dielectric layer thickness has to be 100 nm. This calculation takes into account that in pull-in the average air gap remaining between the upper electrode and the dielectric layer due to the surface roughness is 20 nm. In contrast to the continuously tunable capacitor, the dielectric layer of the capacitor is now not patterned. With the mentioned layer thicknesses, the target capacitance values can be achieved with a signal electrode area of $240 \times 236\ \mu m^2$.

It was explained in section 2 that the capacitance ratio defines the ratio between the pull-in and the release voltage. According to (5) the ratio $U_{\text{pull-in}}/U_{\text{release}}$ is 6.0 when C_{on}/C_{off}

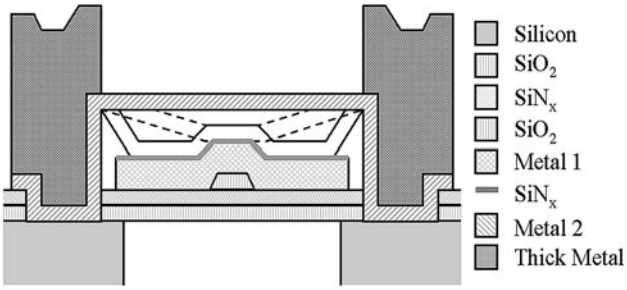

Figure 6. Cross-section view of a three-state capacitor structure.

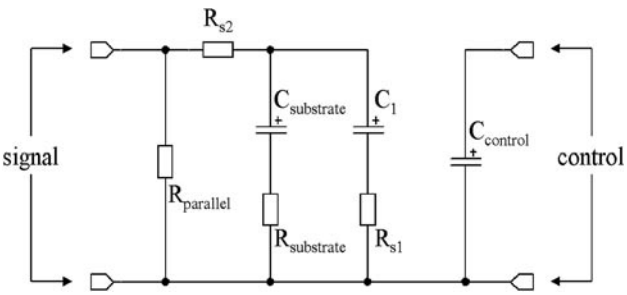

Figure 7. Electrical equivalent circuit of the two-gap capacitor. R_{s1}, R_{s2} and $R_{substrate}$ are the resistances for the moving electrode and the anchorings, the fixed electrode and the substrate, respectively. $R_{parallel}$ is the parasitic parallel resistance of the capacitor. C_1, $C_{control}$ and $C_{substate}$ are the signal electrode, the control electrode and the parasitic substrate capacitances, respectively.

is 15. The parameters that affect the pull-in voltage but not the capacitance value are the thickness, stress and the length of the suspended electrode. Following the continuously tunable capacitor design flow, the thickness of the suspended electrode is assumed to be 0.5 μm and the stress at room temperature is 65 MPa. A two-dimensional FD simulation shows that a pull-in voltage of 3.56 V can be achieved with a 332 μm long bridge.

Figure 6 shows a cross-section view of a three-state capacitor. The device operates in the same way as the two-state capacitor. The difference is that by adding a bump at the center of the fixed electrode, the suspended electrode is first pulled to the bump. When the control voltage is increased further, the rest of the structure is pulled down. As a result, the capacitor has three capacitance states.

3.3. Electrical parameters

Figure 7 shows the electrical equivalent circuit of the two-gap capacitor with separate control and signal electrodes. Simulations show that the Q of the device is strongly dependent on the parasitic capacitance to the ground. This is due to loss in the resistive substrate. In the proposed structure, the substrate is selectively removed under the signal electrode to reduce the parasitic capacitance. However, replacing the substrate with a non-conducting material like glass should increase the Q still considerably. In the results section, the equivalent circuit will be fitted to the measured data to extract electrical parameters for the capacitor.

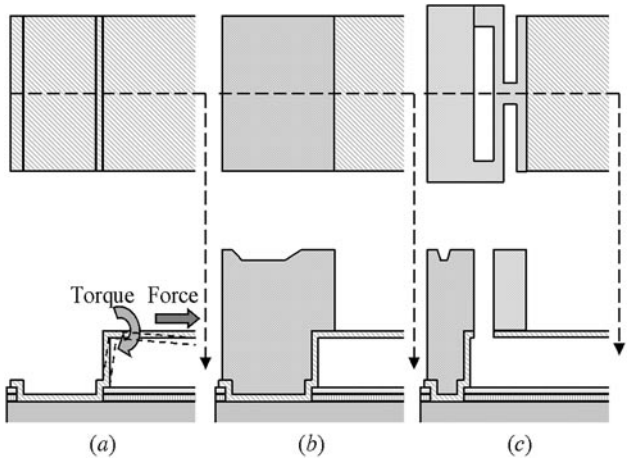

Figure 8. (*a*) Torque on suspended membrane due to stress induced force. (*b*) Proposed firm anchoring structure using thick electroplating. (*c*) Advanced anchoring structure that uses thick electroplating to form springs that have low series resistance.

3.4. Anchoring design

The challenge with the MEM capacitor is that the air gap has to be controlled accurately. The accuracy of the air gap is mainly dependent on the planarity of the suspended electrode and the stability of the anchoring. It was shown in section 2 that the suspended bridge has intrinsic stress and thermal stress. Finite element modeling shows that these stresses can create forces that act on the anchoring points. Figure 8(*a*) shows how these forces can cause a torque on the suspended electrode at the anchoring point. Even a small torque can cause severe warping of the suspended electrode.

Figure 8(*b*) shows the solution to the anchoring problem. Finite element modeling proved that when the thick electroplated metal is used to enforce anchoring, the torque on the suspended membrane can be minimized. Furthermore, the thick electroplated metal can be used to create high Q inductors on the same chip. Figure 8(*c*) shows a more advanced anchoring structure. The thick electroplating is used to form a spring that connects the anchoring point to the suspended bridge. The spring is meant to reduce the residual stress in the released bridge.

4. Measurement results and discussion

All measurements were carried out at room temperature using a Karl Suss PA 200-II probe station that has temperature control and a dry air flow-system. Low frequency capacitance as a function of voltage was measured using an HP 4284A LCR meter and an HP 6634B dc voltage source. S-parameters were measured using a Rohde & Schwarz ZVCE vector network analyzer. Open and short structures that are located besides every device on the wafer were used to remove pad parasitics from the S-parameter measurement results. The capacitance as a function of time was measured using a self-made one port vector network analyzer that operates at 836 MHz. It was noted that the vector network analyzer has rather poor capacitance measurement accuracy. However, this is not a problem since it is meant to evaluate capacitance transient behavior rather than the absolute value.

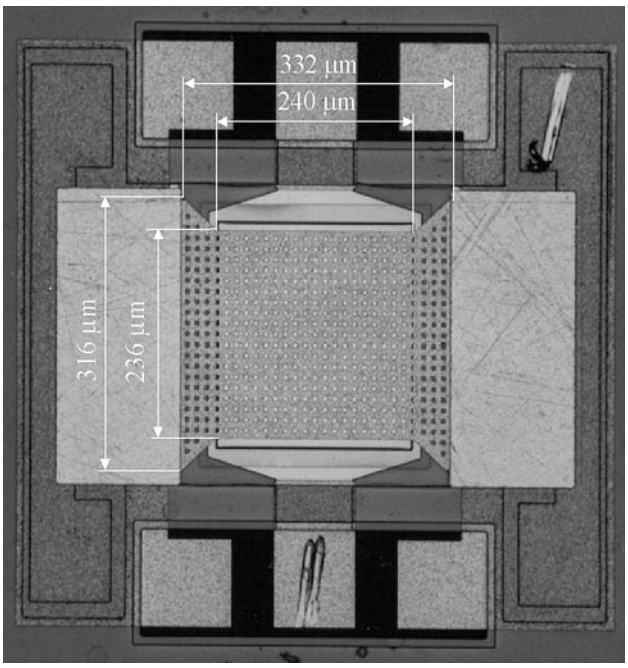

Figure 9. Photograph of a two-state MEM capacitor.

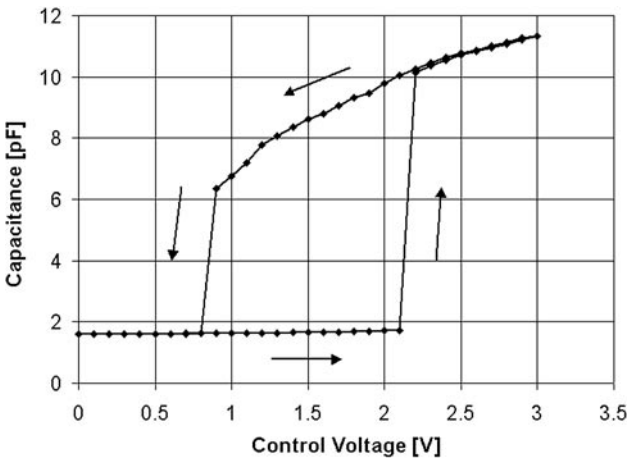

Figure 10. Measured capacitance as a function of voltage of the two-state capacitor.

4.1. Multi-state capacitors

Figure 9 shows a photograph of a two-state MEM capacitor. The dimensions of the device are shown in the figure and in table 3. The designed value for the air gap between the signal electrode and the suspended electrode was 0.5 μm. Figure 10 shows the measured capacitance as a function of voltage of the device. The capacitor has a measured off capacitance of 1.60 pF and the on capacitance after pull-in is 10.1 pF. The pull-in and the release voltages are 2.2 and 0.8 V, respectively. The capacitance increases still after the pull-in, reaching 15.5 pF with a control voltage of 20 V. However, stiction is a problem after the capacitance exceeds 14.4 pF at 11 V. The measured parasitic capacitance to the substrate is 0.62 pF. The high parasitic capacitance is due to the fact that the substrate was not removed under the signal electrode of the device used for the capacitance as a function of voltage characterization.

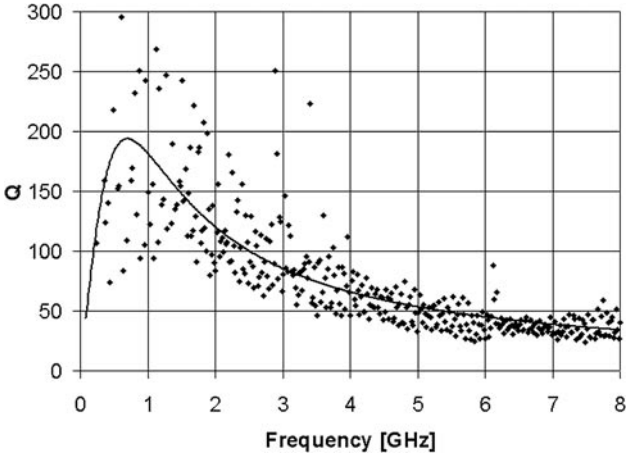

Figure 11. Dots are the measured Q of the device and the line is the simulated Q as a function of frequency.

When the parasitic capacitance to the substrate is removed, the ratio between the on and the off capacitance becomes 10.

Due to loss in the substrate, the measured Q of the device is 3.5 at 1 GHz when the substrate is not removed under the signal electrode. When the substrate is removed, the Q is 182 at 1 GHz and 119 at 2 GHz. Figure 11 shows the measured Q of the device as dots and the continuous line is the simulated Q as a function of frequency. The simulated Q is calculated by fitting the equivalent circuit to the measured S-parameter data. A drawback of the low resistivity substrate is that even if the substrate is removed underneath the signal electrode, the substrate loss still has a dominant impact on the Q. Another drawback is that the SiO_2–SiN_x membrane that holds the signal electrode, when the substrate is removed, is not very robust. The membrane is seen as a factor that decreases the process yield and the reliability of the device. Consequently, we expect future studies with glass as a substrate material to improve the Q and the reliability of the device considerably.

An estimation for the stress in the suspended electrode is calculated by fitting an FD model to the capacitance as a function of voltage using the stress as a parameter. According to the model the stress in the suspended membrane is 35 MPa. The capacitance as a function of voltage can be modeled relatively accurately before pull-in happens with the FD model. However, the major difference between the modeled and the real device is that the pull-in voltages are 2.7 and 2.2 V, respectively. The pull-in happens much earlier in the real device than predicted by the model. We believe that this is due to the limitations of the 2D model and the non-uniformity of the gap. In addition to the model mentioned here, there is also a circuit level model developed by Tinttunen *et al* [23], which can accurately simulate the behavior of the device during and after the pull-in.

Figure 12 shows the measured capacitance as a function of time of the two-state capacitor. The turn-on and turn-off times are about 250 and 450 μs, respectively. The slow switching speed is due to the requirement of low control voltage. The more rigid the structure the higher the first mechanical resonant frequency and thus the shorter the switching time. However, the more rigid the structure, the higher the control voltage must be.

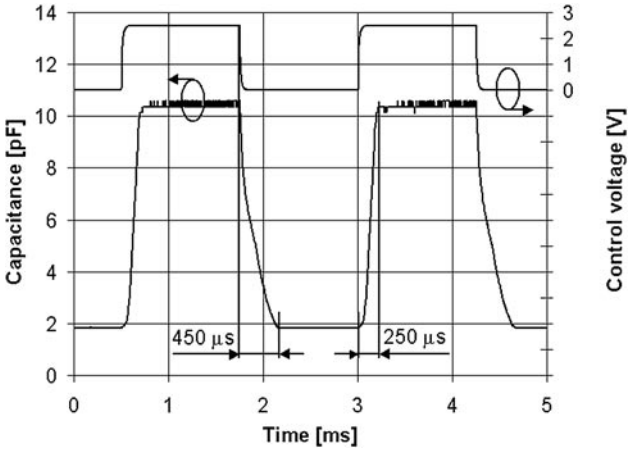

Figure 12. Measured capacitance as a function of time of the two-state MEM capacitor.

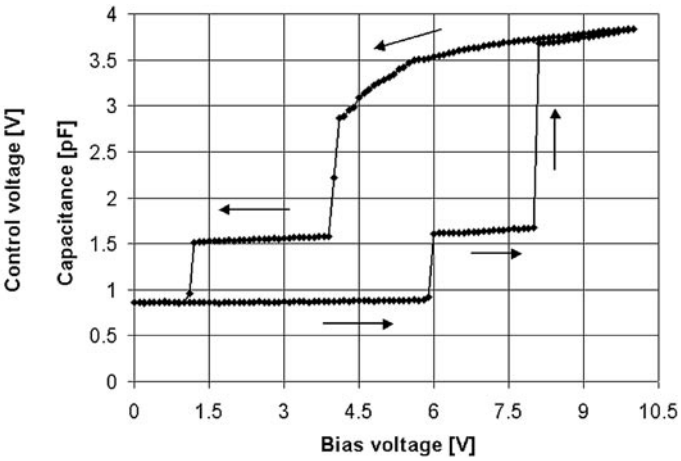

Figure 14. Measured capacitance as a function of voltage of the three-state MEM capacitor.

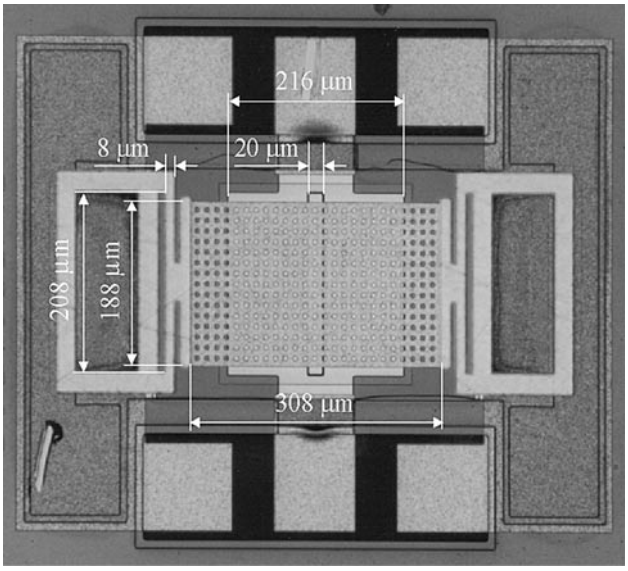

Figure 13. Three-state MEM capacitor with springs that connect the suspended membrane to the anchoring.

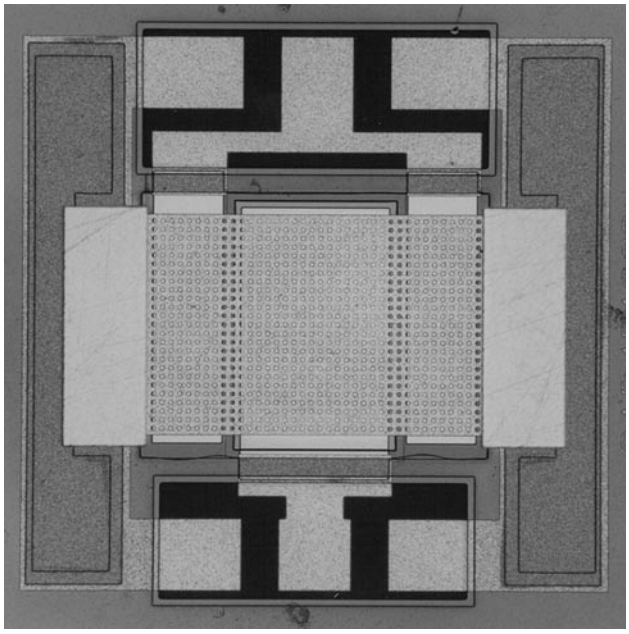

Figure 15. Photograph of a two-gap MEM tunable capacitor.

Figure 13 shows a photograph of a three-state MEM capacitor. The nominal air gap between the signal electrode and the suspended electrode is 1.5 μm. At the center of the signal electrode, there is a 20 μm wide and 1 μm high hill that causes the third capacitance state. The measured capacitance as a function of voltage of the device is shown in figure 14. The measured capacitance of the first, the second and the third state are 0.86, 1.61 and 3.68 pF, respectively. The pull-in and the release voltage of the second state are 6.0 and 1.1 V, respectively. The pull-in and the release voltage of the third state are 8.1 and 3.9 V, respectively. The substrate was not removed under the signal electrode of the device used for the capacitance-as-a-function-of-voltage characterization. As a result, the measured parasitic capacitance between the device and the substrate is 0.53 pF. The Q of the device is 2 at 1 GHz, when the substrate is not removed under the signal electrode. When the substrate is removed under the signal electrode, the Q is 94 at 2 GHz.

4.2. Continuously tunable capacitor

Figure 15 shows a photograph of the two-gap MEM capacitor with separate control and signal electrodes. The dimensions of the device are shown in figure 4 and table 3. Figure 16 shows the measured capacitance as a function of control voltage of the capacitor. The capacitor has a measured tuning range of 125%. When the control voltage is stepped from 0 to 17.7 V and then back to 0 V, the capacitance as a function of voltage changes from 1.58 pF up to 3.55 pF. The substrate was not removed under the devices used for the capacitance-as-a-function-of-voltage measurements. The measured parasitic capacitance from the device to the substrate is 0.43 pF. As a result, the measured capacitance tuning range of the device without the parasitic capacitance to the substrate is 171%. Future studies with reduced parasitic capacitance will improve the capacitance tuning range considerably. For comparison, a one-gap capacitor with separate signal and control electrodes

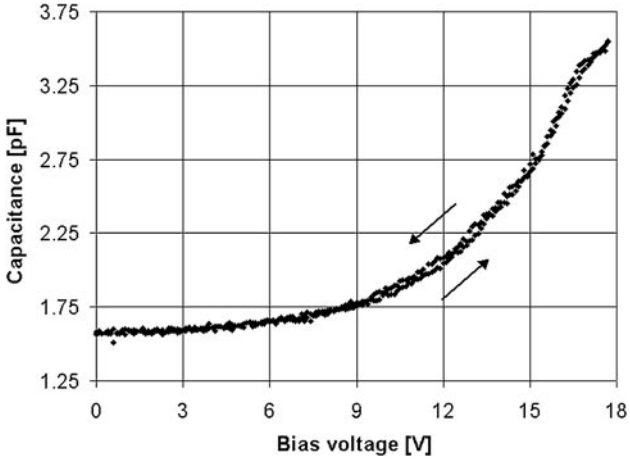

Figure 16. Measured capacitance as a function of voltage of a two-gap MEM capacitor, when the control voltage is stepped from 0 to 17.7 V and back to 0 V.

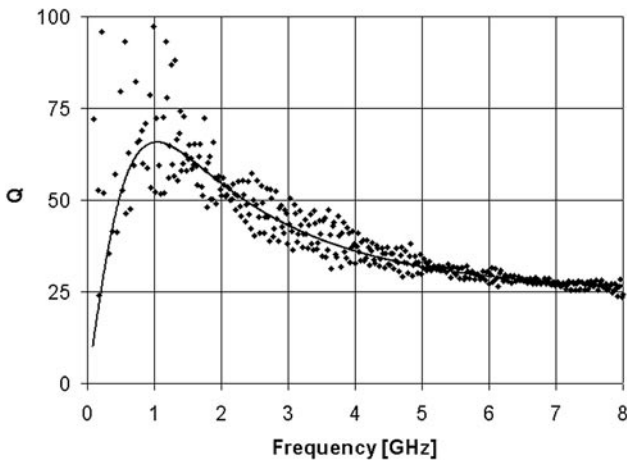

Figure 17. Dots are the measured Q of the two-gap MEM capacitor as a function of frequency. Continuous line is the Q of the equivalent circuit that is fitted to the measured S_{11}-data.

and an air gap of 1.5 μm was also measured. This MEM capacitor has a measured tuning range of 11% 1.37–1.52 pF, when all parasitics are included. The measured parasitic capacitance from the device to the substrate is 0.92 pF. When the parasitic capacitance is extracted from the measurement data, the capacitance tuning range becomes 32%.

There is a slight hysteresis visible in figure 16. It seems that the ac probe signal of the LCR meter causes the hysteresis. As was explained in section 2.2, the measuring ac signal is rectified due to a square law relation between the electrostatic force and the signal voltage. This causes an additional voltage component between the signal electrode and the suspended electrode. If some part of the suspended electrode touches the signal electrode, slight hysteresis results.

Figure 17 shows the measured Q of the two-gap MEM capacitor as dots. The continuous line shows the Q of the equivalent circuit that was fitted to measured S_{11}-data. The calculated equivalent circuit component values are listed in table 4. The capacitor has a measured high frequency capacitance of 1.34 pF, a Q of 66 (average) at 1 GHz and a Q of 53 at 2 GHz. The substrate is removed under the signal electrode.

Table 4. Calculated equivalent circuit component values.

Parameter	Single electrode capacitor
C_1	1.34 pF
R_{s1}	0.05 Ω
R_{s2}	0.003 Ω
R_{parallel}	15 kΩ
$C_{\text{substrate}}$	0.10 pF
$R_{\text{substrate}}$	180 Ω

Table 5. Summary of measurements.

Capacitor type	Two-state	Three-state	Two-gap
Fabricated devices	16	16	16
Functional devices	11	7	4
Designed capacitance	1.0 pF	0.24 pF	1.0 pF
Average measured capacitance	1.75 pF	0.90 pF	1.58 pF
Standard deviation	0.13 pF	0.05 pF	0.17 pF
Designed 2nd state capacitance/maximum capacitance	15.0 pF	1.54 pF	9.27 pF
Average measured capacitance	8.7 pF	1.6 pF	3.1 pF
Standard deviation	1.4 pF	0.1 pF	0.5 pF
Average measured control voltage	2.3 V	5.8 V	17.4 V
Standard deviation	1.1 V	0.7 V	1.9 V
Designed 3rd state capacitance	–	11 pF	–
Average measured capacitance	–	3.7 pF	–
Standard deviation	–	0.2 pF	–
Average measured control voltage	–	8.0 V	–
Standard deviation	–	0.5 V	–

The measurement results for the two-state and three-state capacitor, and the continuously tunable two-gap capacitor are summarized in table 5. Because the process is under development, the yield is not very high at the moment.

5. Conclusions

Several different metal MEM capacitors were fabricated using surface micromachining. The device types that were demonstrated were the two-state, the three-state and the continuously tunable capacitor. The best continuously tunable capacitor has a measured nominal capacitance of 1.58 pF and a tuning range of 125%. The required control voltage is 17.7 V.

Gold is used as the structural material for the capacitors. This allows in theory fabrication of very high Q devices. However, currently the low resistivity substrate dominates the Q. The Q of the devices is improved up to 119 at 2 GHz by removing the substrate under the signal electrode. Even in this case the substrate still has a significant effect on the Q. On the other hand, the SiO_2–SiN_x membrane that holds the signal electrode, when the substrate is removed, is not very robust. The membrane is seen as a factor that decreases the process yield and the reliability of the devices. Therefore, future

studies will concentrate on devices made on glass substrates. Nevertheless, high resistivity silicon could also be used.

The switching speed of the measured devices is slow for many telecommunication applications. A tradeoff must be made between low control voltage and device speed. Elimination of the temperature dependence of the MEM capacitors is an important issue. The development of temperature compensating structure is seen as a first priority for future studies. A second priority is the reliability of the devices and packaging studies.

Acknowledgments

The prototypes of the RF MEM capacitors were fabricated by Marjorie Trzmiel, Christian Pisella and Stéphane Renard of Tronic's Microsystems, Grenoble, France. The authors are also indebted to Panu Siukkonen and Mikael Ansersson of the Nokia Research Center for their help in RF measurements. We would also like to thank Jari Hyyryläinen of the Nokia Research Center for the self-made one port vector network analyzer that was used for the capacitance transient measurements.

References

[1] Pipilos S, Tsividis Y, Fenk J and Papananos Y 1996 *IEEE J. Solid State Circuits* **31** 1517–25
[2] Svelto F, Deantoni S and Castello R 2000 *IEEE J. Solid State Circuits* **35** 356–61
[3] Wong W, Hui P, Chen Z, Shen K, Lau J, Chan P and Ko P-K 2000 *IEEE J. Solid-State Circuits* **35** 773–9
[4] Brank J, Yao Z, Eberly M, Malczewski A, Varian K and Goldsmith C 2001 *Int. J. RF Microw. Comput. Aided Eng.* **11** 276–84
[5] Nguyen C, Katehi L and Rebeiz G 1998 *Proc. IEEE* **86** 1756–68
[6] Liu Y, Borgioli A, Nagra A and York R 2001 *Int. J. RF Microw. Comput. Aided Eng.* **11** 254–60
[7] Dec A and Suyama K 1999 *Microwave Symposium Digest, 1999 IEEE MTT-S International* pp 79–82
[8] Young D, Tham J and Boser B 1999 Solid state sensors and ctuators Transducers '99 pp 1386–89
[9] Howe R 1995 *The 13th Sensor Symposium* pp 1–8
[10] Young D and Boser B 1996 *Solid-State Sensors and Actuators Workshop* pp 86–9
[11] Feng Z, Zhang W, Su B, Harsh K, Gupta K, Bright V and Lee Y 1999 *Microwave Symposium Digest, 1999 IEEE MTT-S International* pp 1507–10
[12] Dec A and Suyama K 1998 *IEEE Trans. Microw. Theory Techniques* **46** 2587–96
[13] Zuo J, Liu C, Schutt-Aine J, Chen J and Kang S 2000 *IEDM Technical Digest. International 2000* pp 403–6
[14] Guardia R, Dehe A, Aigner R and Castañer L 2001 Solid state sensors and actuators *Transducers '01* vol 1 pp 760–3
[15] Castañer L and Senturia S 1999 *IEEE J. Microelectromech. Syst.* **8** 290–8
[16] Kyynäräinen J, Oja A and Seppä H 2001 *Analog Integr. Circuits Signal Process.* **29** 61–70
[17] Seeger J and Crary S 1997 Solid state sensors and actuators *Transducers '97* vol 2 pp 1133–36
[18] Zou Q, Wang Z, Lin R, Yi S, Gong H, Lim M, Li Z and Liu L 1997 *J. Micromech. Microeng.* **7** 310–5
[19] Starr J 1990 *Solid State Sensor and Actuator Workshop Technical Digest 1990*
[20] Veijola T, Kuisma H, Lahdenperä J and Ryhänen T 1995 *Sensors Actuators* A **48** 239–48
[21] Veijola T and Mattila T 2001 Solid state sensors and actuators *Transducers '01* vol 2 pp 1506–9
[22] Veijola T 2002 End effects of rare gas flow in short channels and in squeezed-film dampers at press
[23] Tinttunen T, Veijola T, Nieminen H, Ermolov V and Ryhänen T 2002 *Modeling and Simulation of Microsystems* Static equivalent circuit model for a captive MEMS RF switch at press