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Optimization of a Josephson voltage array based on frequency dependently damped superconductor–insulator–superconductor junctions

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We have developed a programmable Josephson voltage standard based on an array of superconductor–insulator–superconductor junctions. The junctions are damped by an external frequency-dependent shunt circuit, which allows operation at Shapiro steps with $n>1$. We derive optimization criteria for the design parameters for a fast and stable array with low power consumption. An array able to generate $1.0\,V_{RMS}$ ac voltage signal with sub-ppm accuracy is experimentally demonstrated. Theoretically it is also shown that a fast programmable 10 V array can be realized. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1582381]

I. INTRODUCTION

The programmable Josephson voltage standards have been a subject of extensive research recently. From the circuit technologies the intrinsically damped junctions, superconductor–normal conductor–superconductor (SNS)[1,2] or superconductor–insulator–normal conductor–insulator–superconductor (SINIS),[3,4] have been found appropriate for the purpose. We have studied the applicability of superconductor–insulator–superconductor (SIS) junctions. Although the low damping of SIS junctions introduces some difficulties and limitations, we show that they can be overcome and that the junction properties can even be utilized. For SNS and SINIS standards it has been found difficult to use constant voltage steps $V_n=nf/K_J$, with $n>1$ in long arrays due to large microwave attenuation. We show that this is not the case with SIS junctions and a proper circuit design. The basic idea is to damp the junction dynamics with an external frequency dependent shunt circuit in such a way that the pump signal is not attenuated, but the lower frequencies up to the plasma frequency are. In our case the pump signal f is blocked from the shunt resistor by an inductance thus preventing the attenuation.

We derive theoretically optimal design parameters for an externally shunted SIS (es-SIS) array producing a desired output voltage. The properties of interest are stability, power consumption and speed of an array, the last one of which determines the accuracy of ac voltage generation. We consider here especially the limitations in a binary type bias setup.[5–8] We also demonstrate experimentally that an es-SIS Josephson junction array (JJA) generates 1 V output using only 2310 junctions and the step $n=3$.

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II. THEORY

A. Voltage step quality

For stable operation and immunity to extrinsic noise it is preferable to have large step amplitudes (i.e., the range of low-frequency bias current Δi_n, with which a quantized voltage is reproduced). In this section we derive design criteria for a junction so that the step amplitudes would not be suppressed from the theoretical maximum. For SIS junctions, in which the impedance parallel to the tunnel element is essentially capacitive reactance at the pump frequency f, this can be written as[9]

$$\Delta i_n = 2\left| J_n\left(\frac{i_1}{\beta_c\Omega^2}\right)\right|, \tag{1}$$

where i_1 is the pump amplitude in units of critical current, $\beta_c=2\pi I_c R^2 C/\Phi_0$ is the Stewart–McCumber parameter, and $\Omega=(\Phi_0/I_cR)f$ is the dimensionless angular pump frequency, and J_n is the Bessel function of the first kind. A requirement for Eq. (1) to hold is that the pump frequency needs to exceed the plasma frequency of the junction, which is conventionally given as[9]

$$\Omega\sqrt{\beta_c}\gtrsim 3. \tag{2}$$

To find the effect of the external shunt circuit, simulations using the resistively shunted junction model were executed assuming that the circuit is a linear LR circuit parallel to the tunnel element and its capacitance C. The system of differential equations describing the circuit is

$$\begin{aligned}\beta_c\frac{d^2\Phi}{d\tau^2}+i_s+\sin\Phi &= i_0+i_1\sin\Omega\tau,\\ \beta_L\frac{di_s}{d\tau} &= \frac{d\Phi}{d\tau}-i_s,\end{aligned} \tag{3}$$

where Φ is the superconducting phase difference across the junction, $\tau=(2\pi I_cR/\Phi_0)t$ the dimensionless time, β_L

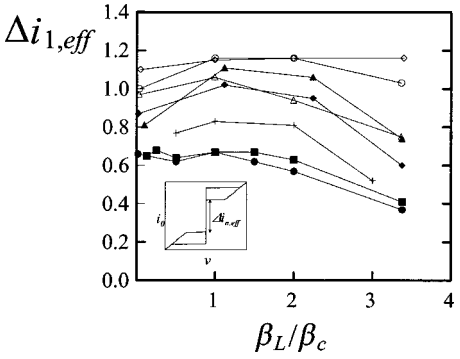

FIG. 1. The effective step height as function of β_L/β_c for different β_c and Ω. The definition is given in the inset. Parameters for: (open diamond) $\Omega=1.5$, $\beta_c=2.0$, (open circle) $\Omega=1.5$, $\beta_c=3.0$, (solid triangle) $\Omega=1.5$, $\beta_c=4.0$, (cross) $\Omega=1.5$, $\beta_c=6.0$; (solid square) $\Omega=1.5$, $\beta_c=8.0$, (open triangle) $\Omega=2.5$, $\beta_c=3.0$, (solid diamond) $\Omega=2.5$, $\beta_c=4.0$, and (solid circle) $\Omega=2.5$, $\beta_c=8.0$. Effective step amplitude is not more than about 25% smaller than the maximum amplitude if $\beta_c \lesssim 4$ and $\beta_L \lesssim 2\beta_c$.

$=2\pi LI_c/\Phi_0$ the dimensionless inductance, i_0 the low frequency bias current, i_1 the amplitude of the microwave pump, and i_s the current flowing through the shunt resistor. All currents are scaled to the critical current I_c. The flux quantum is $\Phi_0=h/2e$.

A series of simulations was executed varying β_c, β_L, and Ω. The pump amplitude was selected so that the step amplitude was maximized according to Eq. (1). It was found that, if Eq. (2) is roughly valid, the step amplitudes follow Eq. (1) as long as β_L is not too large. With large β_L the amplitudes were found to be suppressed. However, the reduced step amplitude was not found to be the upper limit of β_L, but rather the increased hysteresis within the step due to reduced damping. By hysteresis we mean here that for a given bias current i_0 there coexist two solutions. One reproduces the quantized voltage, and another one has ohmic current–voltage ($I-V$) characteristics. This is not acceptable, since it limits the ability to select a desired quantized output voltage by tuning i_0. We can require that the effective step amplitude (i.e., the range of constant voltage step, where the voltage is a single-valued function of i_0) is at least about 75% of the total step amplitude. The data from simulated $I-V$ curves for the first constant voltage step indicates that sufficient criteria are (see Fig. 1)

$$\beta_c \lesssim 4, \tag{4}$$

$$\beta_L \lesssim 2\beta_c. \tag{5}$$

These were found to be sufficient criteria for higher steps as well.

In addition, second kind of hysteresis appears if the steps become overlapping. This is prevented if (see, e.g., Ref. 1)

$$\Omega \gtrsim 1. \tag{6}$$

Inequalities Eqs. (2) and (4)–(6) now give the regime, where the simple Bessel function dependence of Eq. (1) can be used in case of an LR shunted junction.

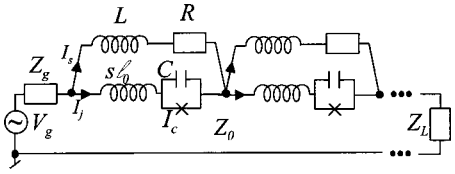

FIG. 2. The circuit equivalent of a JJA branch.

B. Microwave attenuation

Minimizing microwave attenuation in the array is essential, since all junctions need to be biased with sufficiently similar pump amplitude. Here we try to derive a simple analytic expression for the attenuation in circuit of Fig. 2. We assume that at pump frequency the current is mainly coupled capacitively through the junction, i.e., $1/2\pi fC \gg 2\pi fL_J$, where $L_J=\Phi_0/2\pi I_c$ is the Josephson inductance. We also assume that the transmission line inductance for the length of one junction is larger than the capacitive reactance, i.e., $s\ell_0 \gg 1/2\pi fC$, where s is the length occupied by one junction and ℓ_0 is the transmission line inductance per unit length. We further assume that the inductive reactance of the shunt circuit is larger than the shunt resistance, i.e., $2\pi fL \gg R$. The loss due to shunt resistors in a junction is $P_{\text{loss}}=(1/2)RI_s^2$, where I_s is the current flowing through the shunt resistor. The propagating power $P_{\text{prop}}=(1/2)Z_0I_j^2$, where I_j is the current flowing through the junction and Z_0 is the transmission line impedance. The ratio of current through the shunt I_s and the current through the junction I_j is approximately the inverse ratio of inductances, i.e., $I_s/I_j \approx s\ell_0/L$. Summing up, one can write the attenuation per junction in the form

$$\alpha=\frac{1}{2}\frac{P_{\text{loss}}}{P_{\text{prop}}}=\alpha_c\left(\frac{s\ell_0}{L}\right)^2, \tag{7}$$

where $\alpha_c=\frac{1}{2}R/Z_0$ describes the attenuation of the line composed of the Josephson junctions with pure resistive damping. The factor $(s\ell_0/L)^2$ indicates the improvement in transmission line attenuation due to the frequency dependent damping of the Josephson junction.

With the design parameters of our arrays $R=0.31\,\Omega$, $Z_0=2.6\,\Omega$, $L=4\,p$H, $l_0=14$ nH/m, $s=33\,\mu$m, Eq. (7) yields $\alpha=0.80\times10^{-4}$ Np per junction (0.007 dB per junction) in excellent agreement with the result obtained with the numerical model, where parasitic elements due to practical realization were also included and the approximations used here were not imposed.[10] It is noteworthy that $\alpha_c \approx 0.06$ Np per junction (0.5 dB per junction), i.e., inductance decreases the attenuation markedly.

C. ac calibration accuracy

A proposed setup for ac generation with a programmable JJA is introduced in Ref. 11, where the errors originating from different parts of the setup are considered. The accuracy limit set by the JJA itself is due to finite speed of switching between different constant voltage steps. To find an estimate for this, we assume that the switching transients are slow compared to Josephson and plasma oscillations. Therefore we assume that the state of the JJA moves from

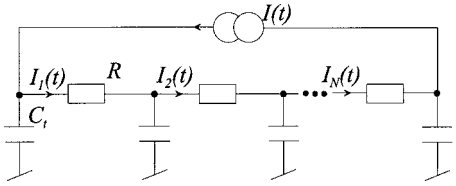

FIG. 3. The distributed RC_t circuit used in analyzing the device speed. $I(t)=0$ for $t<0$ and $I(t)=I_0$ for $t\geq 0$.

one step to another via the resistive branch of the $I-V$ curve. During the transient, the Josephson junctions and the transmission line look like a distributed RC_t circuit as shown in Fig. 3. The transmission line capacitance per junction is C_t. The bias current of ith junction obeys the following equation:

$$\frac{dI_i}{dt}=\frac{1}{RC_t}(I_{i+1}-2I_i+I_{i-1}). \tag{8}$$

If the difference of currents of subsequent junctions is assumed small, the above equation can be rewritten as[12]

$$\frac{\partial I(x,t)}{\partial t}=\frac{\Delta x^2}{RC_t}\frac{\partial^2 I(x,t)}{\partial x^2}, \tag{9}$$

where Δx is the distance between two junctions. This is a heat equation. If the transition is, say, from the zeroth step to another step, the initial and boundary conditions are $I(x,0)=0$ for $0<x<L$ and $I(0,t)=I(0,L)=I_0$, where L is the length of the array and I_0 is the bias current. The solution is

$$I(x,t)=I_0\left(1-\frac{1}{L}\sum_{n=0}^{\infty}\frac{4}{\pi(2n+1)}\sin\frac{(2n+1)\pi x}{L}\times\exp\left[-(2n+1)^2\frac{t}{\tau_{RC}}\right]\right), \tag{10}$$

where $\tau_{RC}=(RC_t/\pi^2)(L/\Delta x)^2$. The sum term describes the transient, and the slowest decaying term is $n=0$. Therefore the time constant is

$$\tau_{RC}=\frac{RC_t}{\pi^2}N^2, \tag{11}$$

where $N=L/\Delta x$ is the number of junctions.

To find out, how large an error in ac voltage generation this corresponds to, we assume binary,[5,6] or equivalent, bias setup, where the voltage consists of superposition of voltage pulses of the form shown in Fig. 4. For simplicity, we assume that the transients are exponentially shaped having a time constant τ_{RC} and that the rise time is the same for all transients. By Fourier transforming the generated signal and defining that the correct voltage is the first frequency component, we arrive to the relative error

$$\frac{\Delta V_1}{V_1}=2\pi^2(f_s\tau_{RC})^2, \tag{12}$$

where f_s is the frequency of generated ac signal. This is independent of the bit count or the exact shape of the generated signal. An issue is, of course, filtering out higher harmonics, but a method for doing this with high accuracy is

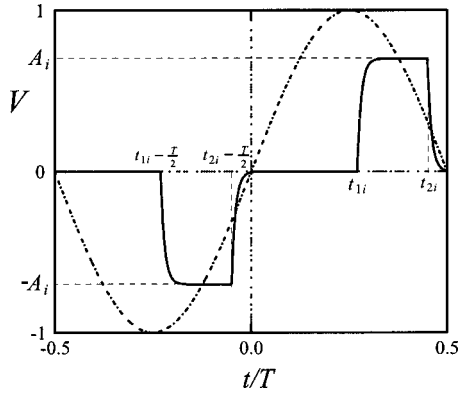

FIG. 4. The digitized sine wave generated with a JJA is assumed to be a superposition of pairs of pulses consisting of exponential edges. The amplitudes $A_i=nf/K_J$ are obtained with fundamental accuracy. The effects of transients, timing and filtering have to be analyzed in order to predict the error of the resulting rms value of the ac voltage.

presented in Ref. 11. For example, if one needs to generate 1 kHz signal with an accuracy of 0.1 ppm the array needs to have $\tau_{RC}\lesssim 70$ ns.

D. Optimization of the array design

Here we describe a process, where the results of the three previous sections are utilized to find optimal parameters for a circuit design. The objective is to provide design values for a given output voltage so that the step amplitudes and the ac accuracy of the device are maximized using as low microwave power as possible. The criteria to be satisfied are those of Eqs. (2) and (4)–(6). We assume that the junctions are in a microstripline geometry (width w and height h), whose impedance can be written as

$$Z_0=\sqrt{\frac{\mu_0}{\epsilon_0\epsilon_r}}\frac{h}{w}, \tag{13}$$

i.e., the effect of fringe fields and the kinetic inductance is neglected. We further assume that the surface of the transmission line is completely consumed by the Josephson junctions, i.e., that the space needed for junction boundaries etc. is negligible. We also assume that there are N junctions of width w and length s divided into M branches, each of which has an own pump microwave input.

The output voltage is

$$U_{\text{out}}=nN\Phi_0 f, \tag{14}$$

where n is the step number.

The pump current needed to maximize the amplitude of a given voltage step is

$$I_n=2\pi k_n\Phi_0 f^2 C\approx 2\pi(1+n)\Phi_0 f^2 C, \tag{15}$$

where $k_n\approx 1+n$ is the argument, which maximizes the nth Bessel function. This follows from Eq. (1). The power propagating at the microstriplines is $P_{\text{in}}=\frac{1}{2}Z_0 I_n^2 M$,

$$P_{\text{in}}=M\rho(1+n)^2 hws^2, \tag{16}$$

where $\rho=2\sqrt{\mu_0/\epsilon_0\epsilon_r}\pi^2\Phi_0^2 f^4 c_s^2$, and $c_s=C/ws$ is the capacitance per unit area.

The critical current density j_c is maximized so that the constraint set by Eq. (2) is satisfied. This leads to $\Omega\sqrt{\beta_c}=3$ [or equivalently $\sqrt{j_c/c_s}=(f/3)\sqrt{2\pi\Phi_0}$]. For a given fabrication process this is done by selecting a proper tunnel barrier thickness. The critical current is given as $I_c=j_c ws$. The amplitude of the nth step I_{cn} is approximately $(4/\pi\sqrt[3]{n})I_c$, i.e.,

$$I_{cn}=4\frac{j_c ws}{\pi\sqrt[3]{n}}, \tag{17}$$

which follows from Eq. (1) and properties of Bessel functions.

To minimize the attenuation per junction [Eq. (7)], the inductance should be maximized under the constraint set by Eq. (5), which can also be expressed as $L=2R^2C$ in the limiting case. Using also the definition of Ω, Eq. (13), and $\ell_0\approx\mu_0(h/w)$, the attenuation can be given as

$$\alpha=\sqrt{\mu_0^3\epsilon_0\epsilon_r}\left(\frac{\Omega j_c}{2\Phi_0 f}\right)^3\frac{1}{c_s^2 h s^3}.$$

The attenuation depends on $\Omega=3/\sqrt{\beta_c}$ [see Eq. (2)], and thus β_c should be maximized. According to Eq. (4) $\beta_c=4$ and thus $\Omega=1.5$. The total attenuation of all junctions in a branch [see Eq. (7)] can now be written as

$$\alpha_{\mathrm{tot}}=\frac{N}{M}(\kappa h s^3+\alpha_d s), \tag{18}$$

where $\kappa=(3j_c/4\Phi_0 f)^3\sqrt{\mu_0^3\epsilon_0\epsilon_r}/c_s^2$ and the second term is added to account for the dielectric attenuation, which is α_d per unit length.

If the current at the entrance of a branch is I_n as given by Eq. (15), it will be $I_n\exp[-\alpha_{\mathrm{tot}}]$ at the end of the branch. Using the properties of Bessel functions and Eq. (1), it can be found that a tolerable variation in pump current along a branch is about $2\pi\Phi_0 f^2 C$, i.e., we must require that $I_n-I_n\exp[-\alpha_{\mathrm{tot}}]<2\pi\Phi_0 f^2 C$. Using Eq. (15) we can now write

$$\alpha_{\mathrm{tot}}\lesssim\ln\left(1+\frac{1}{n}\right). \tag{19}$$

The requirement for the attenuation becomes stricter as n increases. From Eqs. (18) and (19) it follows that

$$\frac{N}{M}(\kappa h s^3+\alpha_d s)\lesssim\ln\left(1+\frac{1}{n}\right). \tag{20}$$

If we assume that $n\geqslant 3$ then an approximation $\ln(1+1/n)\approx 1/n$ can be used.

The array speed can be given, since τ_{RC} in Eq. (11) is (using $C_t=\epsilon_0\epsilon_r ws/h$, $R=\Phi_0 f/j_c ws\Omega$ and $\Omega=1.5$)

$$\tau_{RC}=\gamma N^2\frac{1}{h}, \tag{21}$$

where $\gamma=(2/3\pi^2)\Phi_0 f\epsilon_0\epsilon_r/j_c$.

The Eqs. (14), (16), (17), and (21) yield the quantities of interest U_{out}, P_{in}, I_{cn}, and τ_{RC} as functions of the design parameters, i.e., dimensions w, s, and h, step number n, the number of junctions N, and the number of branches M. These have to be selected so that Eq. (20) is satisfied. The other parameters j_c, ρ, κ, and γ are constant for a given fabrication process and a pump frequency. One should also remember that dimensions w and s should be selected so that the self-induced magnetic fields do not suppress the critical current, i.e., w, $s\lesssim 2\lambda_J$, where λ_J is the Josephson penetration depth (see, e.g., Ref. 12).

To quantify the above results, for our process, values $j_c\approx 3\times 10^5\ \mathrm{A/m^2}$ and $c_s\approx 0.05\ \mathrm{F/m^2}$ and $\epsilon_r\approx 6$ apply. For $f=70\ \mathrm{GHz}$, this leads to $\rho\approx 7.8\times 10^{14}\ \mathrm{W/m^4}$, $\kappa\approx 1.5\times 10^{16}\ \mathrm{l/m^4}$, and $\gamma\approx 1.7\times 10^{-21}\ \mathrm{sm}$. The measured value of dielectric attenuation is $\alpha_d\approx 5.8\ \mathrm{Np/m}$ (see Sec. III). From $\lambda_J\approx 50\ \mu\mathrm{m}$ it follows that $w=100\ \mu\mathrm{m}$ can be used.

If we choose $U_{\mathrm{out}}=1\ \mathrm{V}$ and $n=3$, it follows that $N=2300$ [Eq. (14)]. If we require that $I_{cn}=700\ \mu\mathrm{A}$, it follows that $s=27\ \mu\mathrm{m}$ [Eq. (17)]. Choosing $M=2$ it follows from Eq. (20) that $h\lesssim 350\ \mathrm{nm}$. To minimize the ac error $h=350\ \mathrm{nm}$ is selected, from which it follows that $\tau_{RC}=26\ \mathrm{ns}$ [Eq. (21)]. The power propagating in the transmission lines is $P_{\mathrm{in}}\approx 0.6\ \mathrm{mW}$ [Eq. (16)], which should be easily available from a Gunn diode.

If we instead choose $U_{\mathrm{out}}=10\ \mathrm{V}$, $n=3$, $I_{cn}=300\ \mu\mathrm{A}$, $M=8$, similar reasoning leads to $N=23\,000$, $s=11\ \mu\mathrm{m}$, and $h=2.0\ \mu\mathrm{m}$. The input power is $P_{\mathrm{in}}=2.4\ \mathrm{mW}$ and $\tau_{RC}=450\ \mathrm{ns}$. Comparing the two examples demonstrates the decreasing speed and step amplitude as a function of increasing output voltage. At one volt level it is relatively easy to design an array able to generate 1 kHz ac voltage with a sub-ppm accuracy, whereas for a 10 V array this is significantly more difficult.

To further study interdependencies of speed, output voltage, step amplitudes, and power consumption, we assume now for simplicity that $\alpha_d=0$, i.e., that the attenuation is only due to shunt resistors. Then, based on Eq. (20), we can set

$$M=\left(\frac{U_{\mathrm{out}}}{\Phi_0 f}\right)\kappa h s^3,$$

where also Eq. (14) was used. Using Eqs. (14), (16), (17), and (21) one can now derive the relation

$$\tau_{RC}=\frac{\sqrt{6}(n+1)}{512\sqrt{\pi}n^{7/6}}(c_r\Phi_0 j_c\lambda_J)^{-2}\frac{(U_{\mathrm{out}}I_{cn})^{5/2}}{f\sqrt{P_{\mathrm{in}}}}, \tag{22}$$

where it has also been set at $w=2\lambda_J$ and defined as $c_r=(\epsilon_r\epsilon_0\mu_0)^{-1/2}$. We conclude that the speed of the optimized array is fundamentally dependent on the required output voltage U_{out}, the step amplitude I_{cn}, and the required microwave power P_{in} according to Eq. (22). In order to double the output voltage without affecting the speed, the microwave power has to be more than 30 times higher, which is difficult in practice. One way around the problem might be to use a higher pump frequency. Since τ_{RC} is proportional to $j_c^{-4}f^{-1}$, and according to Eq. (2) $j_c\propto f^2$, the time constant is proportional to $1/f^5$.

III. DESIGN, FABRICATION, AND EXPERIMENTS

The fabrication process is based on the VTT superconducting quantum interference device process with some modifications.[13] The main processing steps are as follows:

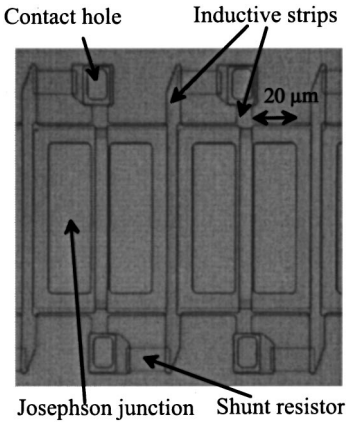

FIG. 5. Photographs of a piece of a transmission line.

(1) deposition and patterning of the first niobium layer to form the lower conductor in the microwave stripline. (2) Deposition of a 1 μm thick silicon oxide layer by the plasma enhanced chemical vapor deposition (PECVD) method. This insulator forms the stripline dielectric. (3) Deposition of the trilayer that forms the Josephson junctions. This multilayer structure has the following constitution: niobium–aluminum–aluminum oxide–niobium. The aluminum oxide forms the tunneling barrier which determines the critical current density of the Josephson junction. The area of the Josephson junction is delineated by anodizing the surrounding area. The layer formed by anodization is an insulator at low temperatures. This layer also forms the dielectrics of the capacitors. The lower niobium layer of the multilayer structure also forms the top conductor of the stripline. (4) Deposition and patterning of a 300 nm thick insulator layer (PECVD silicon oxide). (5) Deposition and patterning of the top niobium layer. This layer connects the upper electrode of the Josephson junction. (6) Deposition and patterning of the molybdenum layer. This forms the resistors. (7) Deposition and patterning of the passivation layer (PECVD silicon oxide).

The junction chains were a realization of the circuit in Fig. 2. A photograph of a piece of the chain is shown in Fig. 5. The inductance required for the microwave blockade is a narrow strip, which is in series with the shunt resistor.

Other circuit elements were designed in a conventional manner using standard microwave design methods. The 70 GHz pump is brought to the array chip via an *E*-type waveguide. The transition from the waveguide to the chip is provided by a finline taper, in which a design of PTB is used (see e.g., Ref. 14). After the transition there is a power distribution network, which divides the signal into branches. In the design there were 16 branches each having 154 or 218 junctions. The arrays can be binary biased with a four bit arrangement. Extra short circuits at low frequencies are inhibited by dc block capacitors. The series connection of branches at low frequencies is provided via low-pass filters.

Measured $I-V$ curves are shown in Fig. 6. The microwave power is selected so that the amplitude of the third constant voltage step is maximized. One can see, that the voltage steps appear flat within the given resolution. Larger resolution dc measurements have also shown that 1 V output voltage is reproducible within 1 nV with our arrays.[15] For

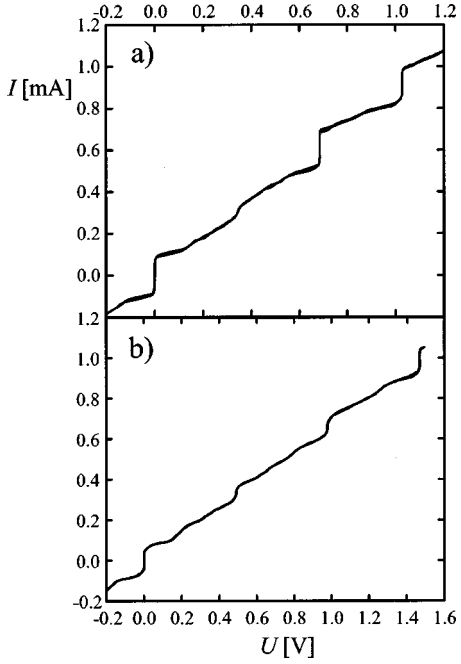

FIG. 6. Measured $I-V$ curves of: (a) 2310 and (b) 3270 junctions divided into 15 branches of equal length. The amplitude of the 70 GHz pump signal is chosen so that the amplitude of the third constant voltage step is approximately maximized. The components have critical currents of about 300 μA.

our current array design (3270 junctions) it follows from Eq. (12) that a signal of 1 kHz can be generated with an accuracy of about 0.1 ppm. However, it should be noticed that the our arrays are not yet optimal, so following the lines of Sec. II D, this could be improved.

The attenuation in a junction line was measured by measuring the amplitude of the superconducting step for the first and the last junctions in an array branch of 260 junctions (Fig. 7). A fit of the form $\Delta I_0 = 2I_c|J_0(B_i\sqrt{P_{\text{in}}})|$, where I_c is the critical current of the junction, P_{in} is the input power to the array, and B_i is a constant. By determining the constants B_i for the first and last junctions the attenuation can be calculated. The result was about 0.01 dB per junction in good agreement with the calculated result (0.007 dB, see Sec.

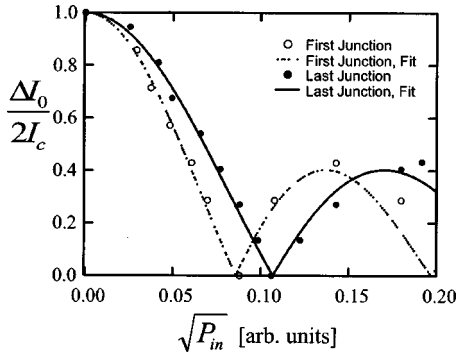

FIG. 7. The result of the attenuation measurement with an array branch having 260 junctions. Shown is the amplitude of the superconducting step as a function of the microwave amplitude at the input. The amplitude is measured for the first and last junctions of the array. Based on the fit of the zeroth Bessel function of the first kind, the attenuation is about 0.01 dB per junction.

II B). The attenuation was also experimentally found to be a significant factor in improving the voltage step quality. In Ref. 10 we studied an array design having much higher attenuation, and the resulting constant voltage steps were much more rounded, especially for the steps with index $n>1$.

In addition to the total attenuation of the transmission lines, the dielectric attenuation was measured with the method described in Ref. 16. In particular, different dielectric deposition processes were compared. The result was that the lowest attenuation (0.5 dB/cm) was obtained with the standard process (PECVD silicon oxide 50 nm at 120 °C+950 nm at 180 °C). This corresponds to the attenuation of about 0.002 dB per junction, so the main contribution comes from the shunt resistors in our current design.

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