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FAST JOSEPHSON ARRAYS FOR VOLTAGE AND IMPEDANCE METROLOGY

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Abstract

We introduce an optimized Josephson double array generating two independent voltages up to 1.5V using only one microwave input. Such an array, combined with the quantum Hall resistance, can provide the basic traceability for an electricity metrology laboratory from DC voltage to capacitance. We describe the array and present preliminary experimental results from DC measurements. Extending the output voltage up to 10V is discussed.

Introduction

Conventional undamped Josephson array voltage standards (JAVS) have nowadays a well established position as the primary source of DC voltage utilizing Josephson-relation $V=Nf/K_J$ where f is the bias frequency, $K_J \approx 2e/h$ is the Josephson constant and N is an integer. Realization of AC voltage using quantum voltage standards has been a subject of wide interest recently [1-4], since it would provide a more direct link from constants of nature to RMS voltage than the conventional methods. Development of fast programmable Josephson arrays has made it possible to tune the output voltage rapidly enough to generate AC waveforms. Furthermore, using two independent AC sources with adjustable amplitudes and phases it is possible to construct a bridge for comparisons of arbitrary impedances. This would, for example, make it possible to create link from quantum Hall resistance to the capacitance. In this Paper we present the design and preliminary experimental results from a new programmable JAVS suitable for the purpose. The array can be driven with a single microwave source, and it generates two independent, floating output voltages.

Array design and fabrication

The arrays are fabricated using externally shunted Superconductor-Insulator-Superconductor -junctions and the standard VTT niobium trilayer process. The devices are designed using frequency dependent damping of the junctions[1] and they are optimised to maximise stability and speed, while power consumption is simultaneously minimised[2]. In the optimum, these parameters are tied together approximately by

$$\frac{tP^{1/2}}{U\Delta I_n} \propto f^{-5}, \qquad (1)$$

where τ is the risetime of the signal, P the input power, U the output voltage, ΔI_n the step width and f the pump frequency .

In addition to optimal array design it is crucial to have a fabrication process, which reproduces junction and shunt parameter values to a high level of accuracy. We improved the temperature control during junction oxidization to reduce critical current spread across the wafer. It is found especially crucial to have a sufficiently low variation in shunt resisance values within a chip [1]. In our case the criterion for shunt resistances is about $DR = (R_{max} - R_{min})/2R < 6\%$. Here R_{max} and R_{min} are the values of the largest and smallest resistances on the chip and R is the average value. The scatter of film thickness was reduced by using the sputter in a mode, where the sample stage oscillates during the deposition. Furthermore, experiments with test structures measuring the effect of both film thickness and litography indicated that we are

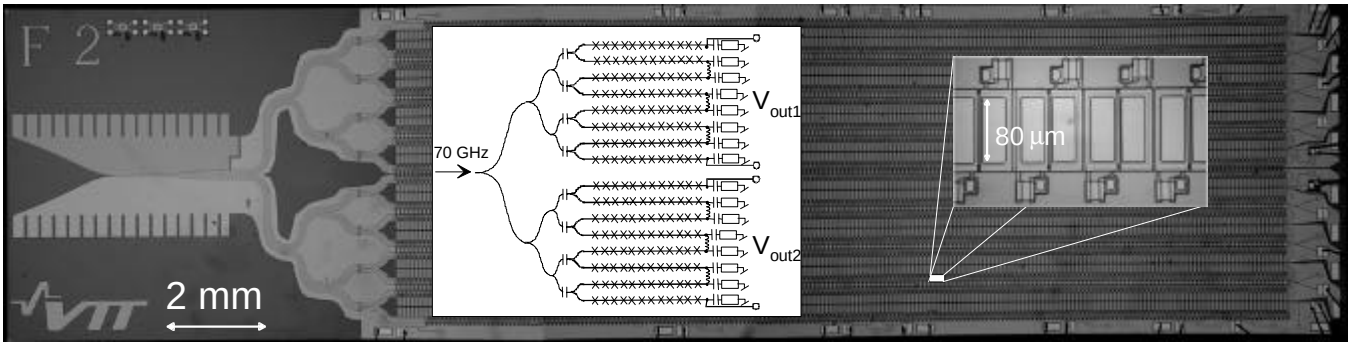

Fig. 1. A photograph of an array componet. The left inset shows a schematic of the two arrays as well as the microwave input and terminations. The right inset shows a magnification of a piece of junction chain with junctions (large rectangles) and shunts.

able to fabricate the required few thousand shunt resistors with *DR* as low as a few per cent.

The array is shown in Fig. 1. The fin-line taper provides transition from an E-band waveguide to the microstripline network, which delivers the power into two subarrays. Both subarrays have 3315 junctions in series divided into eight microwave branches. The maximum output voltages of the subarrays are about 0.5V, 1.0V and 1.5V for f » 70 GHz using the first, the second and the third voltage step (n = 1,2,3), respectively. The array bias is arranged in an 8 bit configuration. Furthermore a wiring of the voltage ratio 3124/2209 » $\sqrt{2}$ is provided for resistance-reactance calibrations. The critical current of the junctions is about 700 μA. The estimated time constant of the array is 100 ns, which enables generation of 1 kHz signal with a relative uncertainty of about 0.1 ppm. In our preliminary DC measurements we have obtained flat constant voltage steps up to n = 3 within measurement resolution of a few hundred nanovolts. An example IV plot at n = 2 is shown in Fig. 2. The calculated microwave power consumption of the array is 3.4 mW with n = 3 excluding the mismatch from the waveguide transition. From the experiment, the estimated total microwave power consumption was about 5 mW.

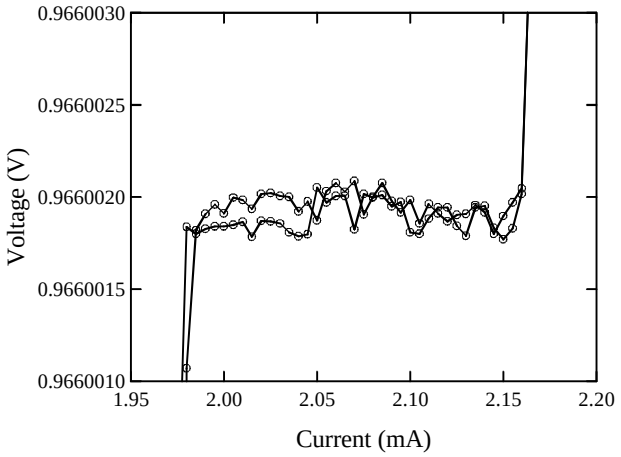

Fig 2 : Current-voltage plot of one half of the double-array chip at n = 2.

We are also currently developing 10V programmable JAVS components. First arrays have been fabricated and experimental results are expected soon.

AC and Impedance calibrations

A method to generate an accurate AC voltage with a fast Jospehson array is presented in [5]. The latest version of the electronics is described in [6]. In brief, the idea is to generate a square wave by switching between voltage steps $+n$ and $-n$ and to compare the first Fourier component to a reference source (e.g. a calibrator) using a lock-in amplifier as a null indicator.

Using the double array, a bridge circuit can be devised using a single microwave input. One possible bridge realisation is shown in Fig. 3. One array provides a stable current for the bridge. A tunable arm is used to provide a virtual ground. The second Josephson voltage is used to find the exact ratio of the two impedances. Fine-tuning the ratio can be done with frequency.

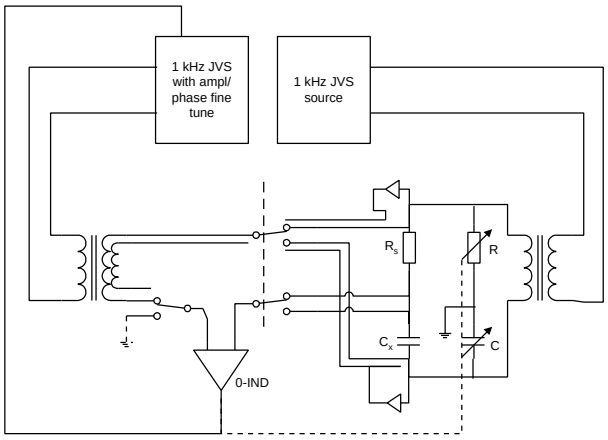

Fig 3 : Impedance bridge with two phase-locked AC Josephson voltage references.

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