Characterisation of European Millimetre-Wave Planar Diodes

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***Abstract* — This paper describes a process for characterisation of millimetre-wave planar diode chips. It comprises dc-characteristics, capacitance, and wide-band (7–220 GHz) scattering parameter measurements and parameter extractions from measurement results. As the first test items, we have characterised planar Schottky diode chips (varactor and mixer diodes) fabricated by Technical University of Darmstadt. We describe a coplanar waveguide test mount design applied for the measurements and show the measured and extracted results. The *S*-parameters at 7–220 GHz are obtained for several different bias voltages and currents.**

I. Introduction

High-performance implementation of millimetre- and submillimetre-wave solid-state circuits requires that electrical parameters of semiconductor components are known. For a proper circuit design, modeling of parasitic elements of semiconductor components is fundamental. We describe a method for characterisation of planar Schottky diode chips. The method is based on different measurements and computer-aided parameter extraction.

The different measurements are direct current (dc) characteristics, capacitance, and scattering (*S*) parameter measurements. The measurements are made on diode chips mounted on a coplanar waveguide (CPW) test structure. In addition, the capacitance is measured for discrete diode chips. Following the measurements, the electrical parameters of the diodes are extracted. Thus far, the parameters (series resistance R_s, ideality factor η, saturation current I_0, zero-bias junction capacitance C_{j0}, parasitic parallel capacitance C_p, built-in potential ϕ_{bi}) of a simple Schottky diode equivalent circuit (Fig. 1) are extracted. The characterisation process is briefly as follows:

1) capacitance measurement of discrete diode chips and extraction of C_{j0}, C_p, and ϕ_{bi};
2) capacitance measurement of diode chips on the CPW mount and extraction of C_{j0}, C_p, and ϕ_{bi};
3) dc-characteristics measurement of diode chips on the CPW mount and extraction of R_s, η, and I_0;
4) *S*-parameter measurement of diode chips on the CPW mount up to 220 GHz at different bias voltages and currents and extraction of C_{j0}.

In this paper, we describe the CPW test mount design, different measurements carried out, and the extraction of the parameters. Thus far, we have measured planar Schottky diode chips from Technical University of Darmstadt (TUD) [1], [2]. Finally, we draw conclusions of the characterisation procedure and qualitative observations of the characterised diode chips.

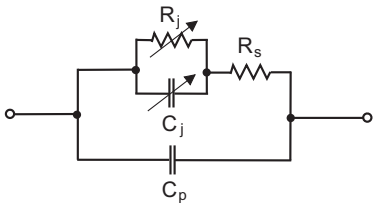
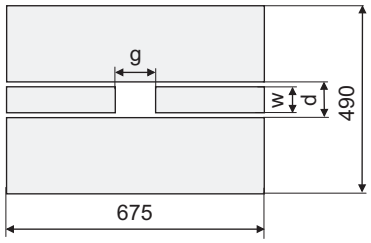
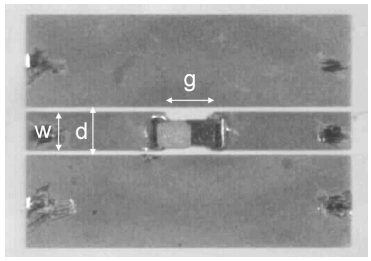


Fig. 1. Simple diode equivalent circuit. Parameters R_j and C_j are the junction resistance and capacitance.



(a)



(b)

Fig. 2. CPW test mount: (a) dimensions in micrometers and (b) a photograph of a flip-chip-soldered planar diode chip.

II. Coplanar Waveguide Test Mount

Fig. 2 (a) shows the CPW test mount applied in the measurements. The mount is a two-port structure with finite ground planes. Overall dimensions of the mount used in these measurements are ~700 μm × 500 μm. To enable the measurement of diode chips of different sizes (length and width) in a 50-Ω CPW, a number of mounts having a different center conductor width *w,* ground-to-ground spacing *d*, and gap length *g* were designed. The CPW mount consists of a 3-μm-thick gold metallization on a 500-μm-thick quartz.

Diode chips were flip-chip soldered over the gap in the center of the mount as shown in Fig. 2 (b). For the chips measured in this study, CPW mounts with w = 80 μm, d = 102 μm, and g = 100 μm were used. With these

dimensions, the width of the measured diode chips is close to w and, also, S-parameter measurements at G-band (140–220 GHz) with measurement probes having a pitch size of 75 µm are possible. Thru-reflect-line (TRL)-calibration elements required for S-parameter measurements also were made on the same quartz substrate. Quartz wafers with a diameter of 10 mm and comprising tens of test and calibration structures were fabricated. Sets of test and calibration units were separated by sawing. For the measurements, these sets were glued onto a separate low-permittivity (relative permittivity ε_r ~ 1) material in order to avoid parallel-plate modes.

III. Capacitance Measurement

We measure the capacitance of the diode chips at 1 MHz by using a precision LCR-meter (Agilent 4284A Precision LCR meter). The measurements are done on both discrete diode chips and chips mounted on the CPW test structure. The capacitance is measured over a wide dc-voltage range. Two "whisker" wires with a diameter of 12.5 µm work as measurement probes when a contact to the diode pads or to the ends of the centre conductor of the CPW is made. Two micromanipulators are used to precisely move and align the wires. The calibration is done by opening one of the probe contacts with a short upward movement and by measuring the capacitance of the caused open termination. This gives a reference capacitance for the measurements.

The operation of the measurement set-up was checked first by measuring a high-quality single-anode planar Schottky diode chip (SC1T5-S20 diode from Virginia Diodes Inc.). This chip suits well for the purpose since it has a very low total capacitance. The measured capacitance at 0 V [C(0 V)] is 8 fF which agrees well with a typical value of 7.5 fF given by the manufacturer.

The capacitances are measured over a wide dc-bias voltage range, typically from −8 V to +0.5 V for varactor diodes and from −3 V to +0.65 V for mixer diodes. Over most of the bias range, the measurement RF signal voltage is 100 mV_{rms}. The amplitude of the signal voltage affects the measured average capacitance of a diode chip. The error increases when the voltage is increased or when the bias voltage is increased. At higher bias voltages (voltages approaching the built-in potential ϕ_{bi}) the signal level is lowered to 40 mV. This reduces the error (estimated to be below 0.5% at a bias voltage of 0.5 V). However, also the variation of the measurement results increases. When measuring very small capacitances of ~10 fF as in this study, the variation should be as small as possible. At each voltage, the measurement (making and removing the probe contact) is repeated several times, typically 10, to decrease the effect of the variation. For 10 different measurements made at one bias voltage, the estimated maximum variation of averaged (averaging factor of 64) capacitance values is 3 fF for the 100 mV_{rms} signal level and 6 fF for the 40 mV_{rms} signal level. These variation estimations include the variation due to the LCR-meter and relative measurements. The absolute accuracy given by the manufacturer for the meter is ~20 % when the signal is 100 mV_{rms}, measurement frequency is 1 MHz, and the capacitance to be measured is about 20 fF.

A typical capacitance measurement result is shown in Fig. 3. Parameters: zero-bias junction capacitance C_{j0}, built-in potential ϕ_{bi}, and parasitic parallel capacitance C_p, are extracted from the measurement results. Extraction is made by fitting the non-linear capacitance equation [3], [4]

$$C(V_j) = \frac{C_{j0}}{\sqrt{1 - V_j/\phi_{bi}}} + C_p, \qquad (1)$$

where V_j is the bias voltage over the diode junction, to the measured data with a non-linear least square curve fitting method. In addition to these parameters, the measured capacitance at the zero bias is observed. The effect of the capacitance variation discussed above on the extracted values is reduced as the capacitance is measured over the wide bias range. Measured and extracted values for the diode chip mounted on the CPW are shown in Table I. Extraction shows C_{j0} of 10.7–24.2 fF for the varactor diodes and of 1.0–1.6 fF for the mixer diodes. By subtracting the parasitic capacitance of 12 fF of the CPW test mount (measured separately), the parasitic parallel capacitance is found to be $C_{p'}$ = 7.7–10.4 fF. For discrete diode chips, the parallel capacitance was measured to be 9.1–11.6 fF.

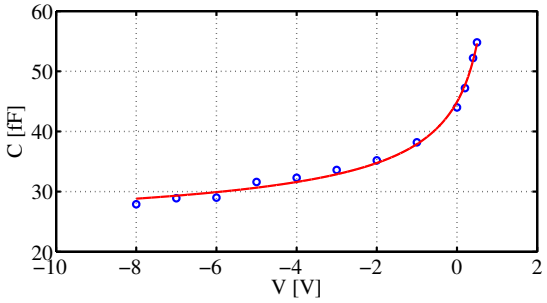


Fig. 3. Example of the capacitance measurement results at 1 MHz and fitted capacitance curve. TUD varactor diode chip: C_{j0} = 24.2 fF, ϕ_{bi} = 1.02 V, C_p = 20.7 fF (includes the parasitic capacitance of the CPW test mount of 12 fF).

IV. Direct Current Characteristics

The dc characteristics of the diode chips on the CPW mount are measured with an Agilent semiconductor analyser through bias tees connected to CPW measurement probes. Fig. 4 shows a general view of the test set-up. The resistance due to wires, bias tees, CPW measurement probes, and contacts between the measurement probes and CPW is measured with a similar set-up by using a bare CPW (Fig. 5). This resistance is reduced from the series resistances extracted from measurement results. Overall, the following parameters: series resistance R_s, saturation current I_0, ideality factor η, and breakdown voltage V_{br}, are extracted. Parameters η and R_s are determined from

$$\eta = \frac{q}{kT}\Delta V \log(e), \qquad (2)$$

TABLE I
CHARACTERISATION RESULTS FOR TUD DIODE CHIPS ON THE CPW TEST MOUNT

TUD varactor diodes	R_s[1] [Ω]	η[1]	I_0[1] [A]	C (0 V)[2] [fF]	C_{j0}[3] [fF]	C_p[3] [fF]	ϕ_{bi}[3] [V]	$C_{p'}$[4] [fF]	C_{j0}[5] [fF]
1	8.4	1.10	$1.95 \cdot 10^{-17}$	30.4	10.7	19.7	0.835	7.7	12.0
2	6.9	1.11	$73.2 \cdot 10^{-17}$	44.0	24.2	20.7	1.020	8.7	23.5
3	8.5	1.14	$8.0 \cdot 10^{-17}$	34.0	12.0	22.4	0.965	10.4	11.5
4	4.2	1.09	$2.1 \cdot 10^{-17}$	37.1	16.5	20.4	0.965	8.4	17.0
TUD mixer diodes									
1	14.4	1.22	$3.5 \cdot 10^{-17}$	23.8	1.0	22.4	0.735	10.4	1.5
2	7.7	1.18	$6.9 \cdot 10^{-17}$	23.4	1.3	20.8	0.690	8.8	2.0
3	7.8	1.20	$9.4 \cdot 10^{-17}$	22.6	1.4	20.6	0.690	8.6	1.5
4	7.8	1.19	$6.5 \cdot 10^{-17}$	23.0	1.6	21.4	0.690	9.4	1.0

[1] Parameter from the dc-characteristics extraction
[2] Measured capacitance of a diode chip on the CPW mount at 0 V
[3] Extracted parameter of a diode chip on the CPW mount
[4] Parasitic capacitance when the CPW test mount capacitance of 12 fF is subtracted
[5] Extracted from the *S*-parameter measurement results

$$R_s = \frac{V_2 - V_1 - \Delta V}{I_2 - I_1}, \tag{3}$$

where q is the electron charge, k is Boltzmann's constant, T is the absolute temperature, ΔV is the change in the junction voltage per decade of the current. Series resistance is determined at high current levels where the voltage drop across R_s is significant. Currents I_2 and I_1 are chosen so that $I_2/I_1 = 10$. V_2 and V_1 are the corresponding voltages applied to the diodes. Once η is known, I_0 can be calculated directly from the measured low-level currents using the common diode current equation. Varactor diodes were measured up to a 3 mA forward current and mixer diodes up to 1 mA. Table I shows the measured parameter values. Typical values for the varactor chips are: R_s = 4–9 Ω, $I_0 < 10^{-16}$ A and η ~1.1; and for the mixer diode chips: R_s = 7–15 Ω, $I_0 < 10^{-16}$ A and η ~1.2.

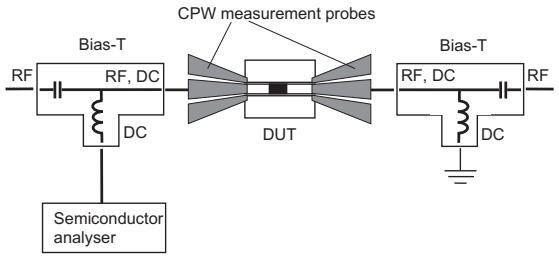


Fig. 4. General view of the dc characteristics test set-up.

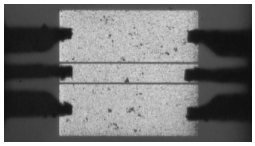


Fig. 5. Calibration measurement with a CPW and CPW measurement probes.

V. *S*-PARAMETER MEASUREMENT

S-parameters of the diode chips on the CPW test mount [Fig. 2(b)] are measured with a CPW on-wafer test station [based on the HP8510 vector network analyzer (VNA)] up to 220 GHz. The measurements are carried out in four different frequency ranges: 7–50 GHz, 50–75 GHz, 75–110 GHz, and 140–220 GHz. The test set-up is calibrated using the TRL-calibration method. Fig. 6 shows the CPW TRL-calibration structures. The structures B1–B3 and B7 work as the line element for the four different frequency ranges, respectively. The structure B4 is the thru element whereas B5 and B6 are the reflecting elements. Lengths of the B2, B3, and B7 lines were chosen to be λ/4 longer than the thru element B4 at the centre frequency of the 50–75 GHz, 75–110 GHz, and 140–220 frequency bands, respectively, for an optimal calibration. Length of B1 was set λ/4 longer than that of B4 at a frequency close to 30 GHz. Thus, it gives good calibration from 7 GHz to 50 GHz. Additional structures B8 and B9 shown in the figure can be used for verification of the calibration. By measuring the three standards at each frequency band, error terms are measured and the measurement system is calibrated automatically with the VNA calibration procedure. After the calibration procedure, the measurement reference planes are located 250 μm inward from the ends of the CPW mount of Fig. 2(a).

The *S*-parameters are measured at several current and voltage levels in each frequency range. The forward current levels used are: 0.1 mA, 0.2 mA, 0.3 mA, 0.5 mA, 1 mA, and 3 mA. Reverse bias voltages for the varactor chips are −5 V, −3 V, and −1 V, and for the mixer diode chips −2 V and −1 V. Fig. 7 shows an example of the *S*-parameter results of a varactor diode chip (not a TUD diode) from 7 GHz to 220 GHz and Fig. 8 shows reflection coefficient measurement results for a TUD mixer diode chip at different bias currents. *S*-parameter measurements of TUD diodes at 140–220 are scheduled to the end of this year due to Planck tests.

The low-frequency *S*-parameters measured at negative bias voltages and at the zero bias also are used to extract C_{j0}. In the extraction process, the pads of the diode chip and a short CPW between the measurement reference plane and the diode chip are modelled as short transmission lines. The diode mounted over the gap in the CPW [Fig. 2 (b)] is modelled with the extracted dc-characteristics parameters, parallel parasitic capacitance, and small parasitic capacitances to the ground at the edges of the gap. By studying the *S*-parameter changes over different bias points and fitting simulated (Agilent ADS simulator) results to the measured ones, the ratio between C_{j0} and C_p is found out and C_{j0} is extracted for the varactor and mixer diode chips. The results are shown in Table I. The results are congruent with the ones extracted from the direct capacitance measurements.

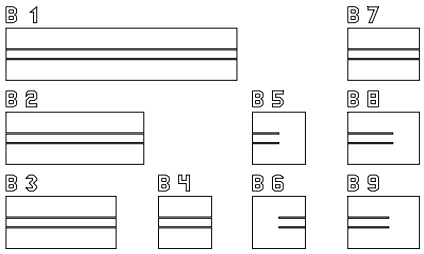


Fig. 6. CPW TRL-calibration elements.

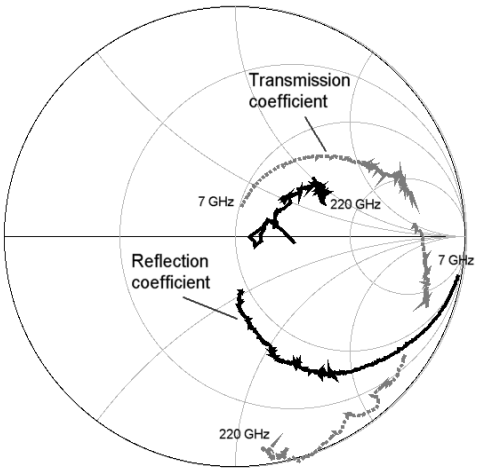


Fig. 7. *S*-parameter measurement results of a test item, a varactor diode chip, from 7 GHz to 220 GHz at 0 V. Due to different frequency ranges of the measurement set-up, results from 110 to 140 GHz are missing.

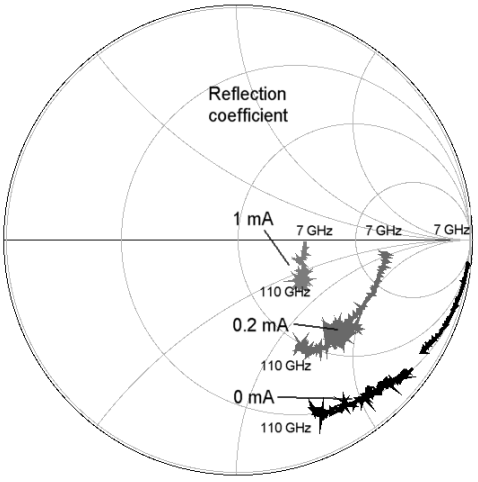


Fig. 8. Measured reflection coefficient of a mixer diode chip from 7 GHz to 110 GHz at 0 mA, 0.2 mA, and 1 mA.

VI. Conclusion

We have described a process for characterising millimetre-wave planar diode chips. It is based on dc-characteristics, capacitance, and wide-band *S*-parameter measurements whose results are used to extract diode parameters. A special coplanar waveguide mount is applied for *S*-measurements up to 220 GHz. In this paper, parameter extraction and *S*-parameter measurements up to 110 GHz are done on TUD planar Schottky diode chips. *S*-parameter results at 140–220 GHz have been measured for a test specimen.

Based on the characterization results, following conclusions can be drawn. Capacitance measurement results of the diode chips on the CPW mount show that the variation of C_{j0} is large, 10.7–24.2 fF for the varactor diodes and 1.0–1.6 fF for the mixer diodes. This indicates the non-uniformity of the Schottky junctions of the fabricated diodes. The extracted parasitic parallel capacitance of the chips is found to be $C_{p'}$ = 7.7–10.4 fF. This shows that the fabrication of the passive diode structure is more uniform. The measurement results of the discrete mixer diode chips support the above parasitic parallel capacitance result. For discrete diode chips, the parallel capacitance is 9.1–11.6 fF. The tested mixer diodes are very similar, having the extracted C_{j0} = 1.0–1.6 fF and the parasitic capacitance $C_{p'}$ = 8.6–10.4 fF. The analysis of the *S*-parameters yielded C_{j0} of 1–2 fF. Typical dc-characteristics values for the varactor chips are: R_s = 4–9 Ω, $I_0 < 10^{-16}$ A and η ~1.1; and for the mixer diode chips: R_s = 7–15 Ω, $I_0 < 10^{-16}$ A and η ~1.2. With the above capacitance values and dc characteristics these mixer diodes represent the state-of-the-art among European planar diodes.

This study shows that millimetre-wave diodes with very small capacitances can be reliably characterised by measurements. Thus far, we have extracted parameters of a simple Schottky diode model: R_s, η, I_0, C_{j0}, C_p, ϕ_{bi}. In future, wide-band *S*-parameter results can be used for extraction of a more specific model, e.g., to include a anode finger inductance. In addition to the extracted parameters, the process has produced valuable measurement results and information of the TUD planar diode chips. In this study, the diode chips are flip-chip soldered on the CPW mount. In future, the bump bonding and its effect on the vertical alignment accuracy will be studied.

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