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Reliability of CSP Interconnections Under Mechanical Shock Loading Conditions

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***Abstract*—Failure modes and mechanisms under mechanical shock loading were studied by employing the statistical and fractographic research methods, and the finite element (FE) analysis. The SnAgCu-bumped components were reflow-soldered with the SnAgCu solder paste on Ni(P)|Au-coated and organic solderability preservative-coated multilayer printed wiring boards with and without micro-via structure in the soldering pads. The component boards were designed, fabricated, assembled, and drop tested according to the JESD22-B111 standard for portable electronic products. The test data were analyzed by utilizing the Weibull statistics, and the characteristic lifetimes (η) and shape parameters (β) were calculated. Statistically significant differences in the reliability were found between the different coating materials and pad structures. The results on the failed assemblies showed good correlation between the failure modes and the FE calculations. Under high deformation rates the solder material undergoes strong strain-rate hardening, which increases the stresses in the interconnections as compared to those in the thermal cycling tests. Therefore, the failure mechanisms under high deformation rates differed essentially from those observed in thermal cycling tests.**

***Index Terms*—Chip scale package (CSP), drop test, finite element method (FEM), JESD22-B111, lead-free, printed wiring board (PWB) coating, reliability.**

I. Introduction

THE employment of new lead-free component metallizations, printed circuit board coatings, and lead-free solders increases the metallurgical complexity of the interconnections and the reliability of the different combinations of solder, component terminations, and printed wiring board (PWB) coatings is likely to be different from what it is with the conventional SnPb metallurgy. Furthermore, the increasing interconnection densities of portable electronic products make the assemblies mechanically more vulnerable. Even though the emphasis in reliability research has been on the thermomechanical performance, portable equipment are more likely to be damaged by the mechanical shocks produced by dropping than by thermomechanical stresses generated during their operation. Therefore, the reliability of lead-free electronic assemblies should be systematically studied under mechanical shock loading conditions with the same kind of miniaturized components as used in the latest portable electronic products.

Several studies carried out with commercial portable electronic products have showed that drop impact makes the component boards to bend and vibrate excessively [1]–[6]. Based on the results from product level impact tests, drop test methods for component boards were developed [7], [8]. The computational approach to study the drop impact of electronic assemblies has been widely adopted and numerous papers have been published in the literature [9]–[18]. The effect of different parameters such as drop height, bump height, and PWB thickness on the board-level reliability under drop conditions have been studied. Calculations predict that the interconnections most prone to failure are located at the component corners and the highest stresses are typically on the solder|under bump metallization (UBM) interface on the component side [9]. However, depending on the geometry of interconnections the highest stresses can locate also at the PWB side [14].

The near eutectic SnAgCu alloy has shown equal or better reliability as compared to the eutectic SnPb alloys under thermomechanical loading but no difference has been found under mechanical shock loading [19]–[21]. Furthermore, Kujala *et al.* found out that fracture of solder interconnections is the primary failure mode in drop tests under mechanical shock loading and the cracks are prone to propagate in the intermetallic compounds (IMCs) instead of the bulk solder [22], [23]. Thus, it is likely that the type and structure of IMCs formed between lead-free solders and component/PWB metallizations should affect the reliability performance under mechanical shock loading. The effect of PWB coating materials on the reliability has been studied extensively under thermomechanical loading [24]–[29], but their effect under fast deformation rates is still unclear.

In this paper, the effect of PWB protective coatings and pad structure (via-in-pad and no via-in-pad) on the reliability of chip scale package (CSP) interconnections will be investigated under the drop test conditions. The materials used in the reliability tests were chosen to represent those typically used in portable electronic products. The reliability will be evaluated by employing a large number of test structures assembled in a full-scale production line to enable comprehensive statistical analysis of assemblies manufactured as in volume production. The component boards are designed, assembled and tested according to the JESD22-B111 [7] drop test standard. Detailed microstructural investigations will be carried out to find relations between the different Weibull parameters and the failure modes, as well as to explain the differences in reliability. In addition to experimental tests, the behavior of the assemblies and the stresses generated in the solder interconnection during

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the drop tests will be analyzed by the finite element method (FEM).

II. Materials and Methods

The component was a lead-free CSP-sized SnAgCu-bumped 12 mm × 12 mm BGA having 500 μm bumps and 800 μm pitch. The heights of the bumps were 480 μm. The number of bumps per component was 144 and the weight of the component was ~0.3 g.

The high-density circuit boards were designed according to the JESD22-B111 drop test standard and were manufactured by Aspocomp Group. Two different protective coatings were used on the Cu soldering pads: Ni(P)|Au [Ni: 2 μm, ~9 wt-% P and Au: ~ 0.02 μm] and organic solderability preservative (OSP) [0.2–0.5 μm]. The PWB was a double-sided $1 + 6 + 1$ stack-up multilayer FR4 board. The layout of the board is shown in Fig. 1(a). The third component in the second row, C8, lies in the geometrical center of the board. The pad and conductor patterning on the board is the same on the two sides except that one side of the board has micro-vias in all of the soldering pads (400 μm in diameter, non-solder mask defined). Although the board is double-sided, components are mounted on one side only. The weight of a fully furnished assembly is 28.5 ± 0.3 g. Altogether 64 test boards were assembled: ten for the Weibull and six for analyzing the primary failure modes of each of the material combinations.

Before component assembly, all circuit boards were inspected for defects such as warpage. The component boards were assembled using Sn3.8Ag0.7Cu (wt-%) solder paste (Multicore). The solder paste was printed (DEK 265 Horizon) with a 100-μm thick electroformed Ni stencil and metal squeegees. The print speed, squeegee pressure, and stencil separation speed were optimized by utilizing the factorial design of experiment together with the analysis of variance. Statistical process control (SPC) was used during production to ensure the stability of the process. The mounting machine (Philips ACM Micro) was set to achieve the highest possible accuracy ($\mu + 5\sigma < 30$ μm, $C_{\rm pk} = 1.67$) and the reflow was carried out in the conventional forced convection oven (EPM/Heraeus EWOS 5.1 N_2) under air atmosphere. The temperature profile was set according to recommendations of the solder paste manufacturer. The peak temperature underneath the CSP component was measured (ECD Super M.O.L.E. Gold) to be 241±0.5°C, and the time above 217 °C was 50 ± 1 s depending on the component location. After assembly the component boards were inspected by X-ray and optical microscopy, and the resistance of the daisy-chain structures was measured and recorded.

After the post-reflow inspection the component boards were drop tested according to the JESD22-B111 standard. Two exceptions were made: a) multiple drops due to the bounce back after the initial impact were not eliminated because no means were available to do this. The first bounce back was about 30% (27 cm) of the initial drop height and b) 1.5-kΩ resistance through the daisy chain network was used as the failure criterion instead of 1 kΩ, in order to exclude the noise inherent in the measurements. The component boards were mounted on a base plate having four rods to support the board from its corners [Fig. 1(a)]. The component boards were attached with

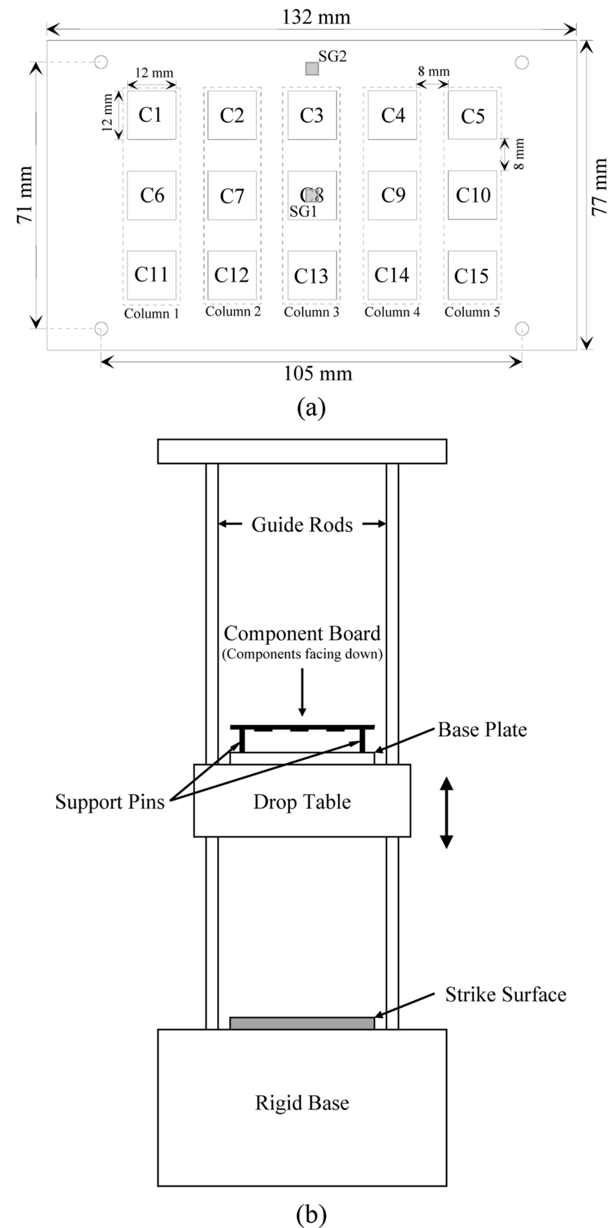

Fig. 1. Board level drop test method: a) layout and dimensions of the drop test board and b) drop test apparatus and mounting scheme.

screws and the components were facing downwards during the test. The base plate lies on a drop table, which moves up and down along the two guiding rods and strike a rigid base [Fig. 1(b)]. The drop height was set to satisfy the requirement of 1500-G peak deceleration and the type of strike surface on the rigid base was chosen to meet the 0.5 ms (half-sine pulse) pulse width requirement. Strains on the test board were measured (National Instruments PXI-6052E/SCI-1520/SCI-1314) with strain gauges (1 mm × 1 mm) attached on the PWB on several locations, two of which are shown in Fig. 1 (SG1 and SG2). The strain gauges were attached on the opposite side of the board relative to the components. Deceleration of the drop table was measured simultaneously. The event detector was connected to the test boards by soldering. A failure was recorded when the resistance through the daisy chain network

exceeded the threshold resistance for 200 ns three times in a sequence of five drops. All electrical connections were checked before interpreting the increase as a failure. The assemblies were dropped until all components had failed in order to obtain enough statistical data for the Weibull analysis. The primary failure mechanism was determined from additional assemblies that were dropped one, two, three, five, seven, and ten times and, if they had not failed by the tenth drop, dropping was continued until failure.

The failure modes were first investigated by conventional methods such as X-ray, acoustic, and optical microscopy. Failure mechanisms were studied from cross sections prepared by standard metallographic methods. Cross sections were analyzed by optical (Olympus BX60) and scanning electron microscopy (JEOL 6335F). The distributions of the elements in the interconnection interfaces were analyzed by energy dispersive X-ray spectroscopy (Oxford, INCA).

A factorial design was used for the drop tests, which is a series of experiments carried out according to principles of experimental design. Factorial design allows the main effects of each variable and their interactions to be investigated. In full factorial design, all possible combinations of the factor levels are used. Combined with statistical analysis, the statistical significance between the averages can be determined. Through replication of experiments, an estimate of the experimental error can be established, which is the basic measure for determining whether the observed differences in the data are statistically significant. Parametric methods for significance testing, such as the analysis of variance, rely on the assumption that the data is normally distributed. The test for normality can be carried out by the Shapiro–Wilk Test, for instance, which calculates a W statistic, which is given by

$$W = \frac{\left(\sum\limits_{i=1}^{n} a_i x_i\right)^2}{\sum_{i=1}^{n}(x_i - \overline{x})} \tag{1}$$

where x_i is the ordered sample value and a_i is constant generated from the mean, variance and covariance of the order statistics from a normal distribution [30]. The W statistic approaches one for normally distributed samples. When the drops-to-failure does not follow the normal distribution, nonparametric methods must be used to test the equality of two populations. The Wilcoxon Rank–Sum Test procedure is the most widely used test for such purposes [31].

The reliability of the solder interconnections was studied by employing the statistical Weibull reliability analysis. The three-parameter cumulative Weibull distribution function is given by

$$F(t) = 1 - \exp\left[-\left(\frac{t-\gamma}{\eta}\right)^{\beta}\right] \tag{2}$$

where $F(t)$ is the cumulative density function, η is the characteristic lifetime, β is the shape parameter, and γ is the failure-free lifetime. The η is a mean lifetime defined as the life at which 63.2% of a population has failed. The value of β has a distinct effect on the failure rate and therefore the failure mechanisms can be identified by its value. When β <1 the failure rate decreases towards the end of the projected lifetime and infant mortality type of failures are expected. When β =1 the failures are time-independent. When β >1 the failures become more frequent as the time elapses and failures of wear-out type are expected. Weibull distribution incorporating the γ-parameter can be utilized to better fit the function to the times-to-failure data. Typically γ is zero and the distribution function reduces to the common two-parameter form. It should be noted, however, that poor fit of the distribution may also be the result of several failure mechanisms acting simultaneously. For parameter estimation, (2) is written in the form $\log_{10}\ln\{[1 - F(t)]^{-1}\} = \beta\log_{10}(t-\gamma) - \beta\log_{10}(\eta)$, which is a straight line when $\log_{10}(t-\gamma)$ is taken as the abscissa. The slope is then equal to β and the intercept on the y-axis is $-\beta\log_{10}(\eta)$.

TABLE I
ELASTIC PROPERTIES

	E [GPa]	ν
Board	44	0.25
Copper	120	0.34
Solder	50.8	0.37
RCC	6.1	0.4
Epoxy (CSP)	8	0.4
Silicon (CSP)	107	0.4

The drop test results were analyzed with the help of the FEM. The analysis was carried out with the ABAQUS program using three different models. The first i.e. the assembly model consisted of the board (single layer S4R shell elements, 1 mm × 1 mm), the components (S4R shell elements, 36 per BGA), the solder interconnections (C3D8R continuum elements, 8 per interconnection), and the supporting rods (B31 beam elements, 10 per rod). This model was used to calculate the effect of the location on the loading of the components during the drop test. The material properties used are given in Table I. As the boundary condition the deceleration of the sledge measured in the tests was applied to the ends of the supporting rods. Because of high strain rates during the drop tests, all materials in the test assemblies were assumed to behave elastically [32]. Submodeling technique was utilized to calculate the stresses in an interconnection. The model of one component and 13 mm × 13 mm area of the board was made of continuum elements (C3D8R, ∼0.2 mm edge). The displacements around the interconnections were calculated employing this model using the results from the assembly model as the boundary conditions. The third i.e. the interconnection model consisted of the solder interconnection and small parts of the PWB (width 600 μm, height 150 μm) and the CSP ($600\ \mu\text{m} \times 100\ \mu\text{m}$). The interconnection model was made up of the C3D8R elements. This model was used to study the effect of the micro-via and the deformation rate on the stress distributions in solder interconnections. The hot deformation properties of the solder were included in the interconnection level $\dot{\varepsilon} = A\sinh^n(B\sigma)\exp(-Q/RT)$, where A =650, n =2, B = 120 1/GPa, Q = 62 400 J/mol, and R = 8.314 J/(mol K). The values for the parameters of the hot deformation equation were fitted to the measured values given by Reinikainen *et al.* [33]. The calculations to compare the differences in stress distributions in solder interconnections under thermomechanical and mechanical shock loading were carried out by changing only the deformation rate. The displacement was obtained from the drop

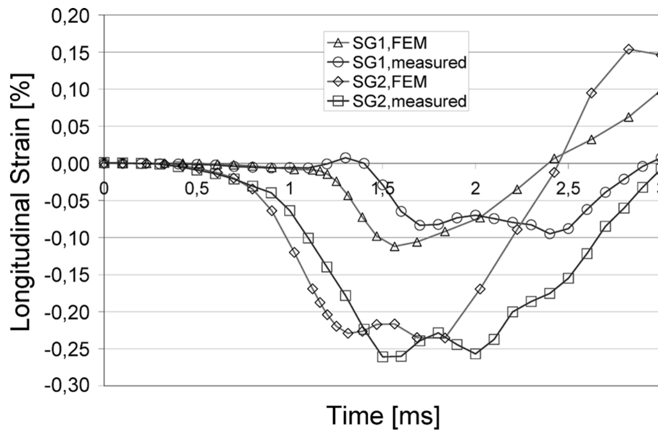

Fig. 2. Measured and calculated strains at locations SG1 and SG2.

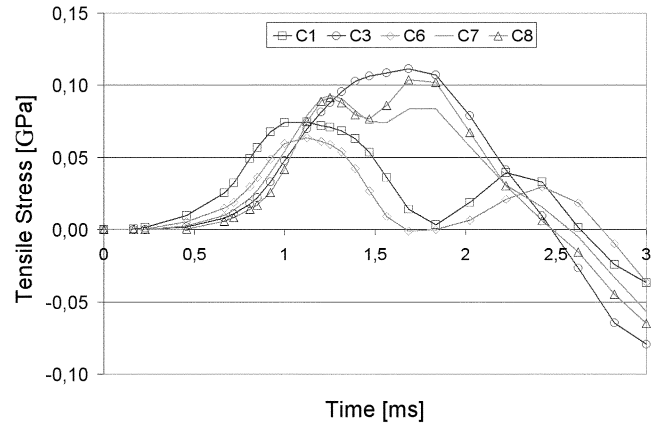

Fig. 3. Tensile stresses in the corner interconnections.

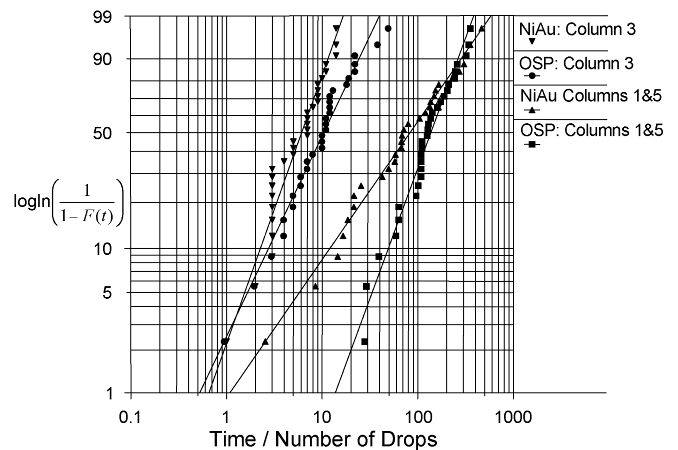

Fig. 4. Weibull plot of no via-in-pads assemblies.

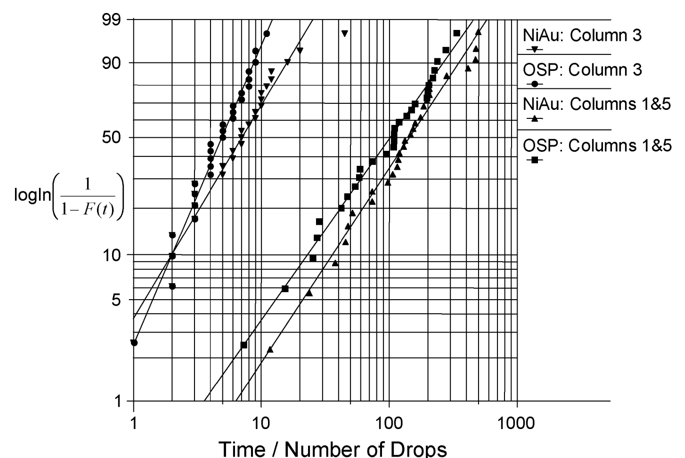

Fig. 5. Weibull plot of the via-in-pads assemblies.

test calculations. In the slow loading the deformation occurred in 1000 s, while in the fast loading it occurred in 1 ms.

III. Results and Discussion

The reliability test procedure was constructed as a full factorial design with ten replications. The type of PWB coating and the soldering pad structure were the main variables. There were marked differences in the number of drops to failure for the different component locations on the test boards. The stresses on the boards during impact are dissimilar in different locations of the board, and therefore the locations that yield similar results need to be determined.

The difference in the number of drops to failure between component locations was tested with the Wilcoxon Rank–Sum Test procedure because the Shapiro-Wilk Test for normality showed that the drops-to-failure data did not follow the normal distribution. Risk levels (α) equal to or less than 5% can typically be considered sufficient and therefore all tests in this work were carried out at less than that level. The results showed that two groups exist on the board, within which the average lifetimes of components were not significantly different. The differences in lifetimes between the two groups were highly significant, however. Components C3, C8, and C13 in the middle column [Column 3 in Fig. 1(a)] lasted just eight drops on average, while components C1, C6, and C11 (Column 1) and C5, C10, and C15 (Column 5) in the outside columns lasted, on average, more than 100 drops. The lifetimes in columns 2 and 4 overlapped with those in the middle and outside columns.

To validate the pooling of component locations into the middle and outside columns, the stresses in the interconnections were calculated by FEM. Strains on the test board were calculated and compared to those measured with strain gauges [SG1 and SG2 in Fig. 1(a)]. The calculated strain histories shown in Fig. 2 show good correlation with the measured ones. Fig. 3 presents the calculated stresses as a function of time in the corner interconnections of components C3, C6, C7, and C8 [see Fig. 1(a)]. The calculated stresses in the interconnections in the mid row (C3, C8) are close to each other and clearly larger than in the end row (C1, C6) while those of C7 are between the two groups. The stresses in components C1 and C2 depend largely on how the connection between the assembly and the supporting rod is modeled. In C2 the values are close to those in C3 or higher and in C1 close to those in C10 or much higher.

Figs. 4 and 5 present Weibull plots of via-in-pad and no via-in-pad Ni(P)|Au and Cu|OSP finished assemblies, respectively. The decision to use the two- or three-parameter form of the Weibull distribution was based on the goodness-of-fit test. The results from the parameter estimation are summarized in

TABLE II
ESTIMATED WEIBULL PARAMETERS

Location on Board	Soldering pads	Pad Structure	γ	η	β
Column 3	Ni(P)|Au	No Via-in-Pads	-	7	1,8
Column 3	Ni(P)|Au	Via-in-Pads	-	9	1,4
Column 3	Cu|OSP	No Via-in-Pads	-	13	1,4
Column 3	Cu|OSP	Via-in-Pads	-	6	2,1
Columns 1 & 5	Ni(P)|Au	No Via-in-Pads	30	121	1,0
Columns 1 & 5	Ni(P)|Au	Via-in-Pads	22	189	1,4
Columns 1 & 5	Cu|OSP	No Via-in-Pads	-	168	1,8
Columns 1 & 5	Cu|OSP	Via-in-Pads	27	136	1,3

Table II where η is the characteristic lifetime, β is the distribution shape parameter, and γ is the failure-free lifetime.

The significance of the differences between the η values cannot be statistically tested and instead must be evaluated indirectly. Therefore the effects of the coating materials and the pad structure were studied with the Wilcoxon Rank–Sum Test procedure, separately for the two groups (Column 3 and Columns 1 and 5). For the column 3, the results showed that the Cu|OSP with no via-in-pad structure is the most reliable, while the other structures are equally reliable but inferior to the Cu|OSP with no via-in-pad structure (at less than 5% risk level). Thus, the reliability of the assemblies on the Cu|OSP coated pads decreases significantly with incorporation of the micro-vias in the pad design, but the effect of the micro-via inclusion is insignificant for the Ni(P)|Au coated pads. The same analysis was carried out for the components in columns 1 and 5. No statistically significant differences were observed for the PWB coating or pad structure even though the difference between the highest and the smallest η was almost 70 drops. The lack of significance is explained by the considerably larger variation in the average drops-to-failure compared with column 3. Because neither the coating material nor the pad structure was a significant factor in columns 1 and 5, only the failure modes in column 3 will be discussed in the following.

β values correspond to the failure rates of the test specimens and therefore they are also expected to correlate with failure mechanisms. To establish a relation between the data collected during the testing and the failure mechanisms requires that the degrees of significance between the β parameters be tested. The 95% confidence interval was calculated for the difference in the β parameter values. All the differences were statistically significant except the difference between β of Ni(P)|Au via-in-pads and Cu|OSP no via-in-pads. Thus, the analysis suggests that at least three different failure mechanisms should be identified at the failure analysis stage.

A distinction should be made between the terms failure mode and failure mechanism. Failure mode is used in the following to describe the type of the failure. It may not be the principal factor leading to electrical failure of the component. Failure mechanism, on the other hand, describes how the failure occurs and what eventually makes the component fail electrically.

A. Difference Between Failure Modes in Thermal Cycling and Drop Tests

The β values of the drop-tested samples are considerably smaller than those typically encountered in thermal cycling tests and, accordingly, the failure mechanisms are expected to be different. At the failure analysis stage of the drop tested samples, four different failure modes were identified: 1) interconnection failure on the component side interface inside the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ IMC, 2) interconnection failure on the PWB side interface inside the $\mathrm{Cu}_6\mathrm{Sn}_5$ IMC (Cu|OSP assemblies), 3) interconnection failure on the PWB side below the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ (Ni(P)|Au assemblies), and 4) PWB failure in the resin-coated copper (RCC) build-up underneath the soldering pad. The failure modes of the drop tested samples are indeed very different from those observed for thermal cycling. The failure mode determined earlier in thermally cycled samples of the same material combinations was always an intergranular fracture in the bulk solder interconnection [24], [25].

What makes the crack propagate under drop test conditions inside the IMC rather than in the bulk solder as was typical for thermally cycled samples? At high homologous temperatures, i.e., temperatures above 0.5 T_{mp} in Kelvin [35], the strength of solder alloys becomes strain-rate dependent. The drop tests were carried out at room temperature, which is about 0.6 T_{mp}, and in the thermal cycling the temperature was varied between $-40\ ^\circ\mathrm{C}$ ($\sim$ 0.5 T_{mp}) and 125 °C ($\sim$ 0.8 T_{mp}). Thus in both tests the behavior of solder interconnections is strain-rate dependent [34]. In drop tests the deformation rate is very high and therefore the solder interconnections are much stronger than those in thermal cycling tests.

The effect of strain rate on the stresses inside the solder interconnections was analyzed with the help of FEM. The calculated average strain of the corner solder interconnection of C8 was in tension 0.1% and that in shear 0.3%. The maximum tensile stress increased from 64 MPa to 128 MPa when the strain rate changed from the low ($\sim 3 \times 10^{-4}\%/\mathrm{s}$) occurring in thermal cycling tests to the high ($\sim$300%/s) occurring in drop tests. Fig. 6(a) and (b) show how the von Mises stress distribution changes with the deformation rate. According to the calculations, the maximum stress in thermal cycling is half of that in drop test. Furthermore, under fast loading the stresses become more concentrated in the corners of the interconnection. If the amount of plastic deformation reduced to negligible level the stresses on the component side would be about 50% larger than on the board side.

Thus, because of the strain-rate hardening of the solder, the magnitudes of the stresses in the solder interconnections are very different under thermal cycling and drop test conditions. Owing to the much higher flow stress of the solder interconnections in the drop tests [33], [34], the IMC layers will experience significantly higher stresses than those that occur in thermal cycling, and therefore the IMC layers on either side of the solder

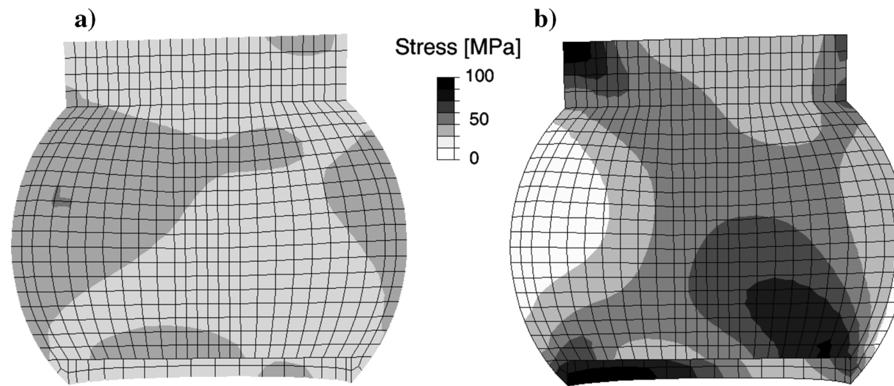

Fig. 6. Von Mises stress distributions in interconnections: a) deformation rate $3 \times 10^{-4}\%/\mathrm{s}$ and b) deformation rate 300%/s.

interconnections are more prone to failure. This explains why the cracks propagate inside the intermetallic layers instead of the bulk solder. In thermal cycling, where the strain rates are relatively low, the cyclic thermomechanical loading of the interconnections generates plastic deformation in the solder, which ultimately leads to propagation of fatigue fracture through the solder interconnections.

The failure mechanisms in drop testing are more complex than those in thermal cycling tests owing to the simultaneous presence of different failure modes. This is indirectly indicated by the smaller values of β, since small β is also an indication of large scatter in time-to-failure values. To study the relation between the β parameter and the failure mechanism, a detailed fracture analysis was carried out. Since many of the failures occur simultaneously, the emergence sequence needs to be determined as well as the primary failure mode causing the electrical failure of the component. The emergence sequence and the primary failure mode were investigated with the additional samples made for primary failure mode analysis. In the following, the primary failure modes are discussed in terms of the two PWB coatings and then in terms of sequence.

B. Cu|OSP Assemblies

The metallization on the component side of the interconnection was electrochemical Ni. On top of that, there had been a thin Au layer, but this has dissolved entirely into the bump material during the bumping stage reflow. The IMC formed on top of the Ni metallization was $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$. The micrograph taken with the optical microscope (Fig. 7) shows a typical component side failure in the no via-in-pad structure where the crack propagates through the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ IMC. The crack always nucleated in the corner of the interconnection, a safe distance away from the IMC in the solder, but it quickly jumped into the IMC layer, which being brittle provided a favorable path for the crack to propagate. The brittleness of the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ layer is emphasized in the relatively large number of small secondary cracks sometimes seen branching from the primary crack path. Cracks in the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ are sometimes visible even after reflow.

The intermetallic layer on the PWB side of the interconnection is pure $\mathrm{Cu}_6\mathrm{Sn}_5$ because the OSP evaporates during reflow and reveals the Cu pad underneath. On the PWB side the fracture propagates inside the $\mathrm{Cu}_6\mathrm{Sn}_5$ intermetallic layer, as shown in Fig. 8. Cracks on this side of the interconnection are not very common, however; they never propagated far, even though the assemblies were dropped dozens of times. Cracking on the component side was much more severe, and cracking on the PWB side cannot, therefore, be the primary mechanism for electrical failure of the interconnections soldered on the Cu|OSP-coated pads. What is notable, however, is that no secondary fractures such as those seen in the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ IMC were visible in the pure $\mathrm{Cu}_6\mathrm{Sn}_5$.

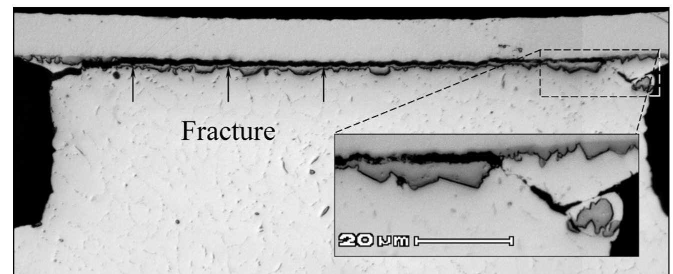

Fig. 7. Failure mode 1: fracture on the component side in the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$.

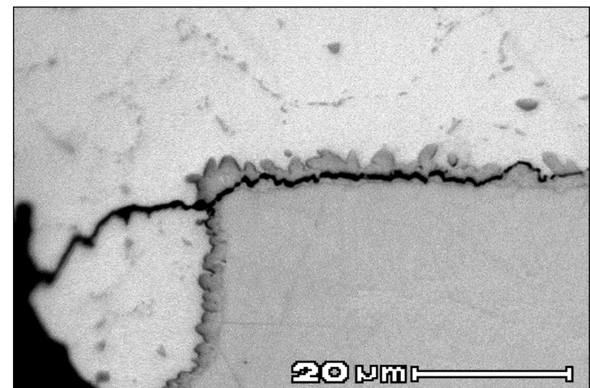

Fig. 8. Failure mode 2: fracture on the PWB side in the $\mathrm{Cu}_6\mathrm{Sn}_5$ (Cu|OSP assemblies).

The β calculated for the Cu|OSP with no via-in-pad combination was 1.4 and that for the Cu|OSP with via-in-pad combination 2.1. The difference between the β values, as well as between the η values for the two combinations, was significant. However, the primary failure mode was the same for the via-in-pad and the no via-in-pad structures. The only difference was the apparently smaller number of PWB side cracks.

Fig. 9. Failure mode 3: failure on the PWB side below the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ ("Black Pad" ⇔ Ni(P)|Au assemblies).

In order to find out the effect of the micro-via structure, the stress distribution of the interconnection was calculated by FEM. To make the results independent on the loading rate only elastic material properties were used. The maximum tensile stress on the component side of the interconnection was calculated for both the via-in-pad and the no via-in-pad structures. According to the calculation, the stress was one fifth higher in the case of the via-in-pad structure but the stress distributions were similar. Thus the micro-via makes the PWB side more rigid and thereby increases the stresses in upper parts of the interconnection. In both cases the stresses on the PWB side were smaller than on the component side.

C. Ni(P)|Au Assemblies

The Ni(P)|Au assemblies, unlike the Cu|OSP assemblies, exhibited severe cracking in the PWB side intermetallic layer. The fractures propagate very close to the nickel metallizations underneath the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ layer, as shown in Fig. 9. In the no via-in-pad assemblies, the fracture typically propagates completely through the interconnection upon a single or very few impacts. The fracture path was always very smooth and straight compared with the fractures discussed above. Energy dispersive spectroscopy (EDS) analysis close to the fracture interface indicated the presence of a phosphorus-rich layer in between the Ni(P) and $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$. The phosphorus in the Ni metallization originates from the chemical plating path where hydrophosphite is used to reduce Ni ions. The thin immersion Au layer has dissolved completely into the solder and the $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ is formed on the Ni(P) layer.

Owing to the presence of P, the structure of the IMC on PWB side is much more complex than the structure of IMC on the pure electrochemical Ni on the component side. The presence of P in the Ni layer creates complex reaction layers in between the Ni(P) and $(\mathrm{Cu,Ni})_6\mathrm{Sn}_5$ layers. The phase formed next to the Ni(P) metallization is a columnar two-phase layer composed of $\mathrm{Ni_3P}$ and Sn, where Sn has precipitated in between the $\mathrm{Ni_3P}$ columns. On top of this columnar layer, a thin amorphous ternary phosphide NiSnP layer containing numerous voids has been identified. The formation of this complex reaction structure has been discussed in detail elsewhere [34], [36]. The sponge-like layer would provide a favorable path for cracks to propagate.

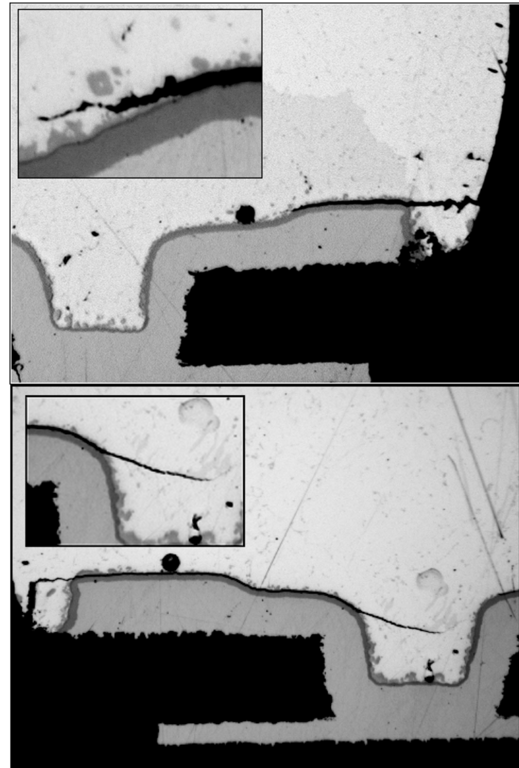

Fig. 10. Failure propagation path in the Ni(P)|Au via-in-pad structure.

As can be seen from Table II, the incorporation of the micro-via has a decreasing effect on the β parameter, and the average drops-to-failure of the interconnection is slightly increased. The reason for this behavior is the uneven pad surface due to the micro-via structure, despite the higher stress concentration on the component side, as discussed earlier. The crack propagation is hindered at the edges of the indentations, where the failure path often moves away from the brittle intermetallic layer into the ductile solder (see Fig. 10). This causes the interconnection in the via-in-pad assemblies to remain intact for a few drops more. Even though there was no statistically significant difference between the β value of the Ni(P)|Au with via-in-pad structure and the Cu|OSP with no via-in-pads, the failure mechanism is different.

D. Cracks in the RCC Build-Up Layer of the PWB

Cracks in the RCC build-up layer were identified in all assemblies (see Fig. 11). Cracks were typically observed only underneath the outermost periphery of interconnections in both the Ni(P)|Au and Cu|OSP assemblies. Even though severe cracks appeared underneath the soldering pad, the Cu wiring on the PWB connecting the two interconnections in the daisy-chain structure had not failed. This failure mode seldom leads to electrical failure of the interconnection and therefore, it is not directly seen in the drops-to-failure measurements, but once nucleated, the crack changes the stress distribution inside the interconnection and in this way affects the lifetime of the inter-

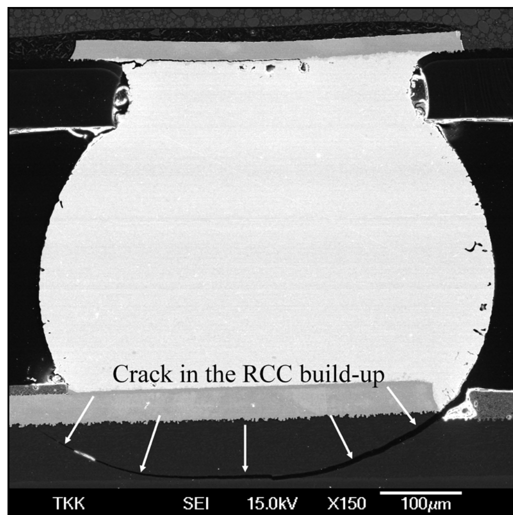

Fig. 11. Failure mode 4: failure in the RCC buildup.

connection. Furthermore, the crack inside the RCC is the first failure mode to appear in the assemblies. The cracks nucleate during the first three to five drops and gradually grow during subsequent impacts. This is the main reason for the larger deviation in the average lifetime under the drop test than with thermal cycling.

The crack nucleation and propagation sequence is slightly different in the no via-in-pad and micro via-in-pad assemblies. In the no via-in-pad assemblies, the crack nucleates on the outer side of the interconnection relative to the center of the component underneath the edge of the soldering pad and propagates toward the center of the component. Another crack may nucleate on the opposite side of the interconnection and meet the first crack, thus detaching the interconnection completely from the underlying resin layer while preserving the Cu wiring on the PWB. In the via-in-pad assemblies, in addition to the nucleation underneath the edge of the soldering pad, cracks are also nucleated at the corner where the micro-via joins the capture pad on the outermost Cu interface beneath the RCC. It should be emphasized that, because these tests were carried out to study the effect of different PWB coating materials on the reliability of a chosen component, the daisy chain was not linked through the micro-vias. Instead, the wirings on the PWB surface were utilized. The failure of the micro-via is shown indirectly in the drops-to-failure measurements and, therefore, the micro-via failures are not further discussed in this paper.

IV. Conclusion

The reliability of lead-free CSP components being reflow-soldered on four kinds of test boards was studied by the standard drop test. The test boards differed in the type of surface finish (Ni(P)|Au or Cu|OSP) and pad structure (via-in-pads or no vias). Both the pad coating materials and the pad structures had significant impacts on the reliability: the components soldered on Cu|OSP were more reliable than those soldered on Ni(P)|Au, and the no via-in-pad structure was more reliable than the via-in-pad structure.

The failure analysis revealed four different modes: 1) fracture in the component side the $(Cu, Ni)_6Sn_5$ layer, 2) fracture in the Cu_6Sn_5 layer on the PWB side (only in the Cu|OSP assemblies), 3) fracture below the $(Cu, Ni)_6Sn_5$ layer on the PWB side (only in the Ni(P)|Au assemblies), and 4) PWB failure in the RCC buildup underneath the soldering pads. Modes 2) and 4) did not cause the components to fail electrically.

The failure mechanism under mechanical shock loading is different from that under thermomechanical loading, where the localized recrystallization of solder enables the nucleation and propagation of cracks in the bulk solder. Under high deformation rates the strain-rate hardening of the solder material forces cracks to propagate in the IMC layers instead of the bulk solder.

According to the FE-calculations the stresses become more concentrated in the corner regions of the interconnections and their level on the component side is higher than on the board side. The micro-via-in-pad structure further increases the stresses in the component side interfacial region during the fast deformation, and therefore solder interconnections are prone to fail from the component side intermetallic layers much earlier than interconnections without via-in-pad structure.

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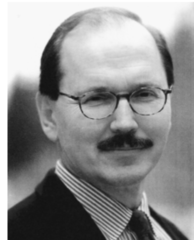

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