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Metallurgical Factors Behind the Reliability of High-Density Lead-Free Interconnections

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9.1. INTRODUCTION

Product reliability is an important factor especially in portable electronics, because these increasingly powerful and more complex electronic equipment experience different kinds of electrical, thermal, mechanical, and thermo-mechanical strains and stresses in their service environments. The importance of solder interconnection reliability is increased mainly due to two reasons: Firstly, higher interconnection densities, e.g., in small-scale Ball Grid Array, Chip Scale Packaged or Flip Chip components, are related to decreasing solder interconnection volumes (see Figure 9.1). Decreased size of solder interconnections has brought the components closer to the printed wiring boards (PWB) and therefore stresses experienced by these micro-interconnections are considerably increased. Furthermore, due to the small solder volumes there is a risk that too large fractions of solder interconnections will transform into brittle intermetallic compounds [1,2]. Secondly, the employment of lead-free solders, components under bump or lead metalizations, and PWB protective coatings add to the complexity of the interconnection metallurgies. The number of different material combinations increases markedly as the traditionally used SnPb-based solders and protective coatings are replaced with different lead-free alternatives. Solders are replaced with alloys such as Sn_{3.8}Ag_{0.7}Cu, Sn_{3.5}Ag_{3.0}Bi, Sn_{3.5}Ag, Sn_{0.7}Cu, Sn₅₈Bi, or Sn₁₀Zn [3–10]. PWB coatings are replaced with Organic Solderability Preservatives (OSP), matte Sn, electrochemical Ni(P) with a thin flash Au on top (Ni(P)|Au), Ni|Pd|Au, Ag or Bi, for instance [11,12]. The most common choices for the component metalization seems to be matte Sn, Ag|Pd, Ni|Au, Ag, Bi, or Ni(V)|Cu [12].

Because microstructures ultimately control reliability of soldered interconnections, reliability of each material combination is likely to be different. Therefore, it is of primary importance to investigate systematically metallurgical reactions in the effective joining region and resulting microstructures within the solder interconnections as well as to study their impacts on reliability with test samples assembled as in volume surface mount pro-

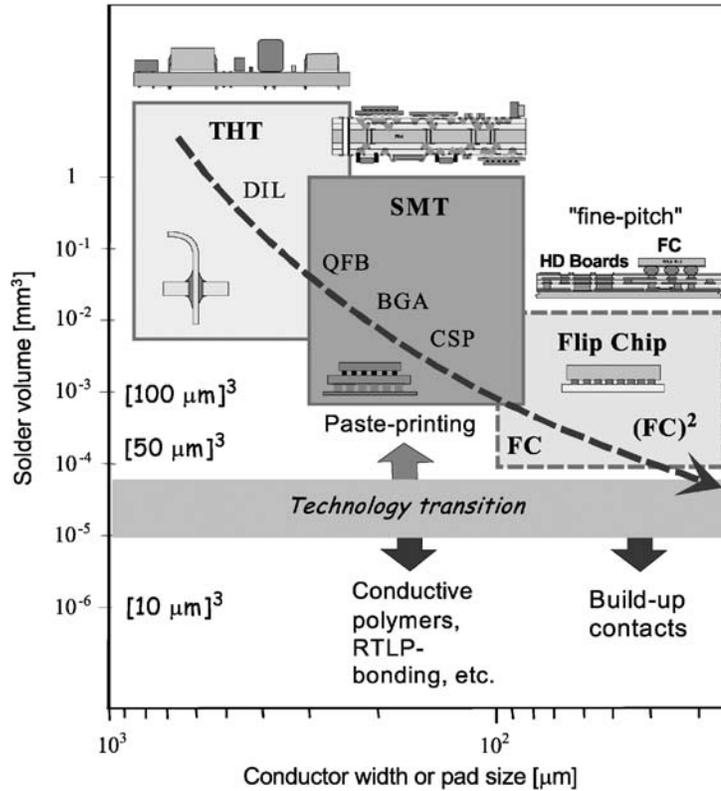


FIGURE 9.1. Impact of miniaturization on electronics production.

duction. The effective joining region can be defined as the region where concentrations of the components differ from those of the original contact materials [13,14]. Lead-free solder interconnections can contain more complex intermaterial layers such as phosphides, which weaken solder interconnections. Therefore it is anticipated that mechanical failures will be encountered more frequently in the future, especially if the fine-pitch components with metallurgically incompatible component metalizations or PWB coatings are introduced into electronic products. Moreover, the microstructures formed during soldering are not stable and will evolve during the operation of products. Hence, in order to ensure the best possible reliability of electronic assemblies against various loading conditions, much better understanding of interconnections microstructures and their evolution, including interfacial reaction products, is needed.

Portable electronic equipment experience during their use many different kinds of loading conditions, in which mechanical shocks and thermomechanical loadings are perhaps the most critical ones. As we shall see later on in this chapter, different loading conditions will evoke different failure mechanisms leading to dissimilar failure modes. Under thermomechanical loading nucleation and propagation of cracks is controlled by the microstructures formed during soldering and their recrystallization behavior during use [15–19]. Mechanical shock impacts, on the other hand, are known to produce entirely different kinds of failure modes [20,21]. Cracks in the newly soldered interconnections do not propagate through the bulk solder of the interconnections, but mainly in the brittle

1 intermetallic compound layers formed between solder and contact metalizations [20–23]. 1
2 However, portable products are seldom dropped soon after they are assembled; most likely 2
3 their components have been exposed to elevated temperatures or experienced thermome- 3
4chanical loadings, and therefore the microstructures of the solder interconnections have 4
5 also evolved. Dense continuous networks of grain boundaries may have already been pro- 5
6duced by recrystallization and so the above-mentioned two failure modes are mixed when 6
7 the products are dropped. 7

8 What has been stated above increases also the importance of reliability testing. This, 8
9 in turn, causes significant expenses to companies owing to the increased testing time as 9
10 well as adds to the costs following from longer time-to-market cycles. Therefore, the em- 10
11ployment of proper test procedures for different applications is becoming increasingly im- 11
12portant. To ensure the feasibility of the test results, a better understanding of the failure 12
13mechanisms occurring under different loading conditions and their correlation with the 13
14field environments must be obtained. Therefore, the employment of different simulation 14
15and statistical methods together with detailed microstructural studies are needed. 15

16 In this chapter we will concentrate on the evolution of microstructures during accel- 16
17erated reliability tests, since they eventually determine the failure mechanisms that con- 17
18trol reliability of electronic products. The focus is in identifying the factors driving the 18
19microstructural evolution in lead-free interconnections and the effects of different testing 19
20conditions, in particular those of mechanical shock loading and thermal cycling, because 20
21they are considered the most relevant tests for portable products. However, we will begin 21
22with a presentation describing the iterative approach adopted in the Laboratory of Elec- 22
23tronics Production Technology at the Helsinki University of Technology to emphasize that 23
24reliability of solder interconnections is not only a metallurgical issue but we have to incor- 24
25porate electrical, mechanical, thermal, and statistical aspects into our scope as well. 25

26 27 28 9.2. APPROACHES AND METHODS 28

29
30 The iterative approach for studying the reliability of soldered assemblies consists of 29
31 four major steps: (i) design and manufacturing of test assemblies, (ii) reliability testing and 30
32 simulation of the devices under test, (iii) statistical analysis of the reliability test results, 31
33 (iv) non-destructive inspection and detailed (destructive) microstructural characterization 32
34 of failed interconnections. The role of simulation and modeling tools in this process cannot 33
35 be overemphasized, since most of the major steps involve to some extent either electrical, 34
36 thermal, mechanical, statistical, or materials modeling. 35

36 37 38 9.2.1. *The Four Steps of The Iterative Approach* 38

39
40 The approach illustrated in Figure 9.2 establishes an iterative loop in which the de- 39
41 signs are constantly improved on the basis of simulation and experimental results. In this 40
42 subchapter some of the steps involved in the reliability studies are introduced. It should 41
43 be noted, however, that the extent of design and simulation tools needed depends on the 42
44 type of test chosen. For example, in the thermomechanical and mechanical shock tests 43
45 discussed later in this chapter electrical simulation has a minor role, whereas thermal, me- 44
46chanical, and microstructural simulations play a more central part. Electrical and thermal 45
47 simulations, on the other hand, are vital tools in studies on power cycling. Because differ- 46
48ent kinds of simulation tools are used in different stages of the iteration loop, modeling and 47
49 simulation are discussed collectively in Section 9.2.2. 48
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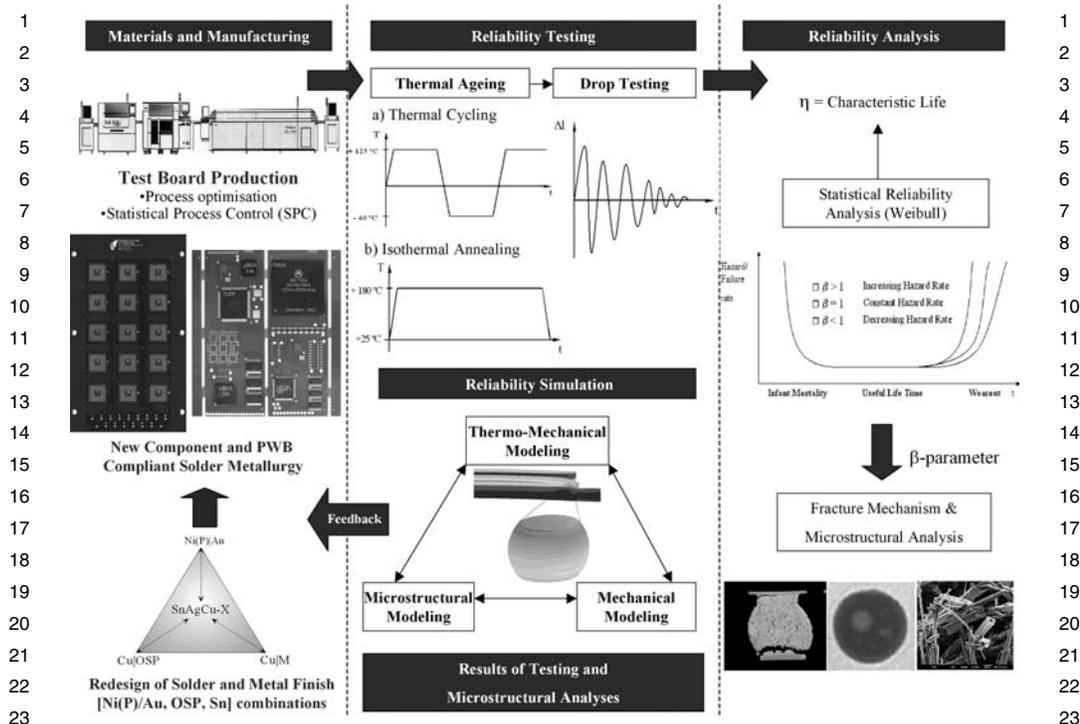


FIGURE 9.2. A schematic presentation of the reliability research procedure [1].

9.2.1.1. *Design and Manufacturing of Test Assemblies* After the electrical design of test boards, their assembly is carried out on a production-scale reflow soldering and/or wave soldering lines. It is, naturally, most important that the test assemblies are free of production related defects and therefore all the process steps—solder paste printing, component placement and, soldering—are continuously inspected and assured that they operate within their (statistically determined) control limits. However, even electrically conductive and visually acceptable interconnections can be unreliable. Inspection alone does not guarantee good reliability. Different parameters of the soldering profile, such as heating rate, activation time and temperature, time above liquidus, peak temperature, and cooling rate, all affect the quality of solder interconnections. Processing parameters of soldering determine the microstructures formed during soldering. These structures are the onset of the microstructural evolution that takes place either during the subsequent accelerated testing or service of devices. Hence, at this stage the combined thermal and thermomechanical simulations are utilized to get a better understanding and control of the solidification during reflow soldering. An example of such a simulation is presented in the next section.

9.2.1.2. *Reliability Testing* Reliability testing follows the after-reflow inspection of the test boards. Thermal cycling tests are used to study the effect of thermomechanical stresses generated by heat dissipating elements or changes in ambient temperature on the reliability of electronic equipment. Strains and stresses are produced by differences in coefficient of thermal expansion of dissimilar materials. Thermal cycling tests are typically carried out in air-to-air or fluid-to-fluid test chambers depending on the required rate of temperature change. The profile of the test is determined by values of upper and lower temperatures, dwell time, rate of change between the temperatures, and number of cycles (see Figure 9.3).

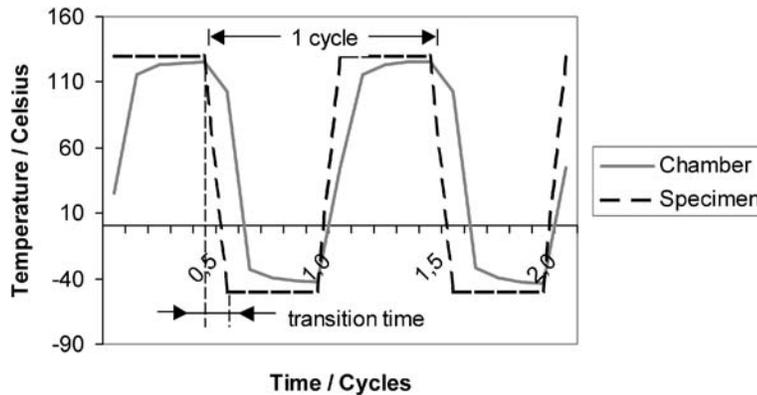


FIGURE 9.3. Typical temperature profile used in thermal cycling tests.

Since even the minimum temperatures of typical thermal cycling profiles remains above the 0.3–0.4 of the absolute melting range of almost all lead-free solder alloys, dwell time at temperature extremes allow creep processes to transform elastic strain into plastic strain. But because deformation during thermal cycling is largely elastic a change in the dwell time does not affect the severity of the test considerably. It should, however, be long enough for the temperature of the specimen to stabilize.

Because portable electronic products are more likely to be dropped than affected by changes in thermal conditions, the emphasis of the reliability research has moved, during the recent years, from thermomechanical testing to mechanical shock testing. Reliability testing of solder interconnections on printed wiring boards during high impact drop loading is studied utilizing different kinds of drop testers specially designed for this purpose. Different organizations are preparing standardized tests for mechanical shock loading of portable electronic equipment. JEDEC has recently published its own JESD22-B111 standard for handheld electronic products [24].

Drop test apparatuses are generally composed of a mechanism to drop the board repeatedly in a specified orientation and a high-speed data acquisition system to record the deacceleration condition of the test, strains on the component boards, and the drops-to-failure. The test board is typically attached to a fixture from four corners or the edges of the board. The fixture is mounted on a sledge that is dropped down on a rigid surface from a specified height in a controlled manner with the help of guiding rails. Dropping can be performed in different orientations, but it is often performed horizontally, components facing downwards. This is because the most detrimental factor for the assembly caused by dropping is not the mechanical shock itself, but the subsequent bending and vibration of the board [20,21]. Placing the component boards horizontally achieves maximum flexure of the board and onsets the natural vibrating motion. Bending causes displacement between the board and the components resulting in component, interconnection, or board failures.

The shape of the optimal deceleration pulse according to the JESD22-B111 standard is a half-sine with 0.5 ms width and G level of 1500 (see Figure 9.4), or 0.3 ms width and 2900 Gs [24]. The shape of the pulse is not only a function of the drop height but depends also on the characteristics of the strike surface: drop height determines the maximum deacceleration and the strike surface the pulse width. Real time components daisy chain measurement for failure identification requires a high-speed data acquisition system.

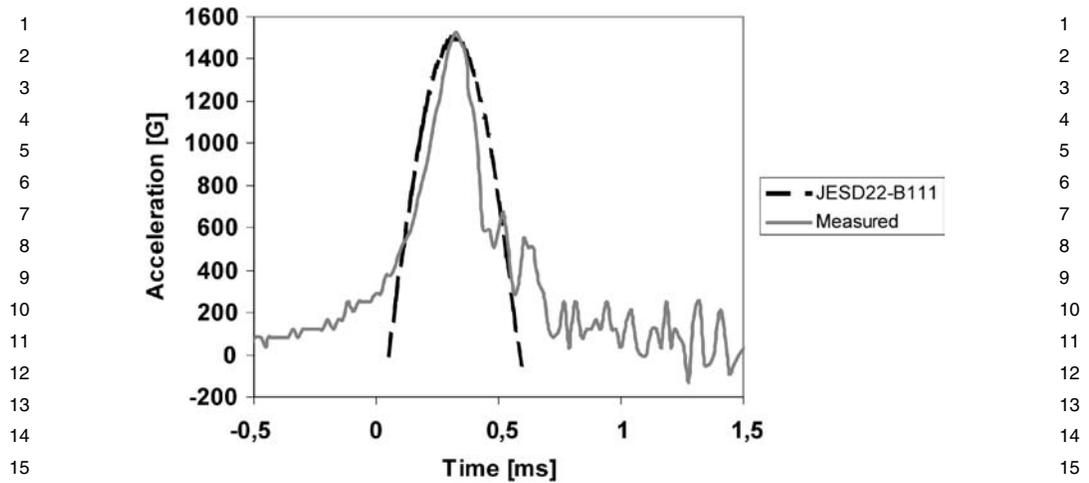


FIGURE 9.4. Strain according to the JESD22-B111 standard and that measured in the longitudinal direction of the test board [see board layout in Figure 9.18(b)].

The system should be able to detect any discontinuity of daisy chain resistance lasting for few microseconds or even less. Deacceleration of the test vehicle and strains on the component boards are also measured. Strain measurements are performed by very light strain gages attached in different parts of the test assembly in different directions. The test environment is highly accelerated because the supporting effect of the product covers and other such components in the drop impact of a functional product is neglected in such board level tests as the JESD22-B111. Furthermore, because the behavior of the test board is strongly dependent on the test board construction, dimensions, and materials, the drop test performance should be studied utilizing a standardized PWB construction. Only one type of component is used at a time. The purpose of the tests is to evaluate the reliability performance of the most common surface mounted components used in handheld electronic products and therefore component types such as ball grid arrays, land grid arrays, (wafer-level) chip scale packages, or small outline packages are used. Standardized drop tests are used mainly to compare the reliability performance of different material combinations, component structures and other product design related issues.

High deformation rate inherent in drop tests increases the strength of the solder interconnections. As the result, the brittle intermetallic layers between the solder and the metalizations become more prone to failure as the stresses in these layers increase compared to the stresses in thermal cycling tests for instance. This issue will be discussed in more detail in the following case studies.

9.2.1.3. Statistical Analysis of Reliability Test Results The amount of numerical data gathered during reliability tests is usually extensive. Therefore the use of statistical tools is indispensable. Statistical hypothesis testing is needed for making decisions whether there are statistically significant differences in reliability between certain types of assemblies. Reliability of the solder interconnections is often studied also by making use of the statistical Weibull reliability analysis. The purpose of the Weibull method is to characterize the failure distribution and to make inferences about the failure mode in operation.

In order to statistically compare and test the affects of more than one factor on the reliability, experiments have to be designed in the right manner. The factorial experiments allow examination of several factors as well as their interactions, and to determine whether the observed differences in the response i.e., the value of the measured reliability characteristic (times-to-failure or drops-to-failure) are statistically significant [25–28]. The choice of statistical method for testing hypotheses is dependent on how its failure distribution conforms to normal distribution. The test for normality can be carried out by the Shapiro-Wilk Test for instance [29]. If the data acquired conforms to normal distribution the results from the experiment can be analyzed with the Analysis of Variance (ANOVA). If the time-to-failure data fails to conform to normal distribution nonparametric methods must be used to carry out the statistical testing. Wilcoxon Rank-Sum Test procedure is perhaps the most widely used test for such purposes [26]. Tests are typically carried out at less that 5% risk level, which means that if the resulting p -value of the test is smaller that stated, it is a good indication to reject the null hypothesis and conclude that the two means are different.

Large numbers of different statistical models are available for modeling time-to-failure data. The Weibull distribution is one of the most widely used lifetime distributions in reliability engineering due to its versatility. It relates the reliability data to a failure mechanism and it can also be used with relatively small sample sizes. Depending on the values of the parameters, it can be used to model a variety of life behaviors. There are two different forms of the Weibull distributions, the two-parameter and three-parameter distribution. The two-parameter cumulative distribution is characterized by the characteristic life (η) and the shape parameter (β). The third parameter, γ , is called the failure free life. The choice of the distribution depends on the fit of the test data to the distribution in question. The three-parameter Weibull distribution can sometimes give a better fit to the data. When the γ is included in the distribution, it takes the form:

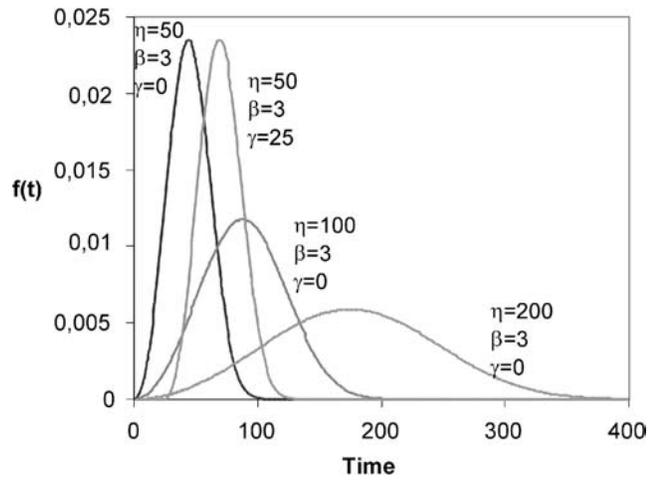
$$F(t) = 1 - \exp\left[-\left(\frac{t - \gamma}{\eta}\right)^\beta\right].$$

With different parameters, the function takes a variety of shapes as shown in Figure 9.5(a). A change in the parameter γ changes the time scale without changing the shape of the distribution. When η is increased while keeping β constant [see Figure 9.5(a)], the probability density function stretches out and decreases in height because the area under the density function is a constant value of one. The effect of the β on the probability distribution is illustrated in Figure 9.5(b).

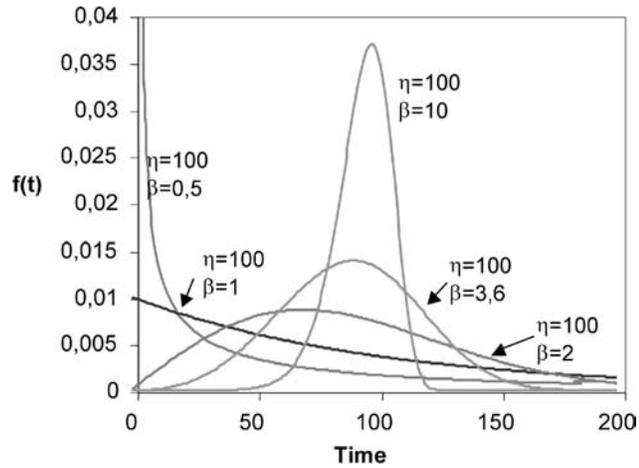
The value of β represents a certain failure rate and failures can be classified by its value to the three life-stages of the bathtub curve [30]. The relationship between the Weibull shape parameter and the bathtub curve is presented in Figure 9.6 [see also Figure 9.5(b)]. When the β value is less than unity (decreasing failure rate), the plot represents early or “infant mortality” failures. If β equals one (constant failure rate) the plot represents the intrinsic failures during the product lifespan. Values greater than one (increasing failure rate) represent the wear-out failures.

There are many methods available for the Weibull parameter estimation such as the probability paper plotting, the least squares estimation, and maximum likelihood estimation. The least squares method is a mathematical version of the probability plotting and therefore provides more objective parameter estimates. The method of least squares is often chosen instead of the maximum likelihood estimation due to its relative simplicity. The parameters are estimated with the least squares regression in the following manner:

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(a)



(b)

FIGURE 9.5. Weibull density functions with different values of: (a) η and γ (β constant), (b) β (η and γ constants).

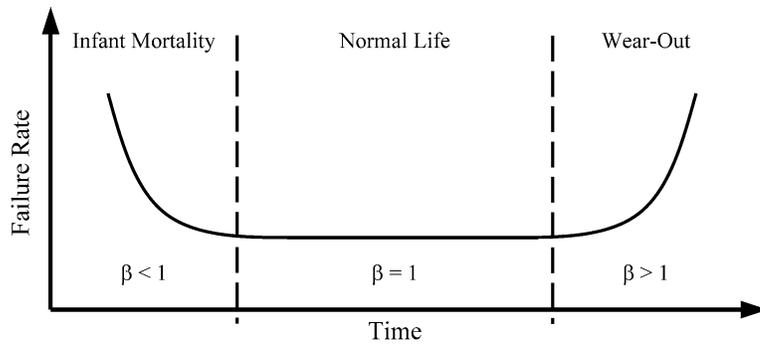


FIGURE 9.6. Relationship between the Weibull shape parameter β and the bathtub curve.

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1 a straight line is fitted to a scatter plot ($y = \log \ln[1/(1 - F(t))] = \beta \log_{10}(t) - \beta \log_{10}(\eta)$) 1
2 is linear as a function of $\log_{10}(t)$. The slope of the regression equals to β while the inter- 2
3 cept on the y -axis equals to $-\beta \log(\eta)$, where η can be calculated. The η can also be read 3
4 from the diagram at the 63.2% cumulative failure rate. 4

5 *9.2.1.4. Failure Analysis and Microstructural Characterization* The next step is the com- 5
6 prehensive failure analyses of the tested samples. Non-destructive inspection of the test 6
7 samples, which provides initial information about the failure modes, is carried out first. 7
8 This is usually done with the help of x-ray inspection or scanning acoustic microscopy. De- 8
9 tailed destructive analyses of cross-sectional samples needed for studying microstructures 9
10 are carried out with optical and scanning electron microscopy. When even higher resolu- 10
11 tions are needed the transmission microscopy will be used. The microscopes are equipped 11
12 with either energy or wave dispersive spectrometers for obtaining local chemical analyses 12
13 from the samples. 13
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15 *9.2.2. The Role of Different Simulation Tools in Reliability Engineering* 15

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17 Simulation tools are of great importance in the iterative approach because they help 17
18 us to rationalize the test results as well as to obtain better understanding about the test 18
19 conditions. For example the finite element calculations (presented in more detail in Ref. [20]) 19
20 on the effect of via-in-pads structure showed that the stresses on the component side of the 20
21 interconnections with the via-in-pad structure was one fifth higher as compared to those 21
22 without the vias. Thus the micro-via makes the PWB side more rigid and thereby increases 22
23 the stresses in upper parts of the interconnections. In the following section some central 23
24 aspects of thermal, mechanical and physical-chemical simulation will be introduced. 24

25 *9.2.2.1. Thermal Simulation of Reflow Soldered Components* As an example of the use 25
26 of simulation in the manufacturing stage, we will briefly consider a case discussed in more 26
27 details elsewhere [31,32]. The goal of the work was to study the solidification of solder 27
28 interconnections of the chip scale packaged components in a commercial forced-convection 28
29 reflow oven with the help of thermal simulation tools. The simulation work was carried out 29
30 in three consecutive steps: (i) thermal modeling of reflow oven, (ii) thermal modeling of 30
31 the component and, (iii) thermal modeling of solder interconnections. 31

32 The first step was performed with the help of the Computational Fluid Dynam- 32
33 ics technique and the other two steps were based on the Finite Element Method. Before 33
34 the simulation, temperature profiles and oven temperature were measured by using multi- 34
35 channel concurrent data logger. The measured results were adopted to optimize the thermal 35
36 model of the reflow oven. Results from the first step were used as boundary conditions for 36
37 the model in the next step. Thermal properties of SnAgCu solder were presented with the 37
38 help of thermodynamic analysis on equilibrium solidification procedure. Two fundamental 38
39 assumptions were made: solidification of solder was treated as a nearly equilibrium process 39
40 and that interconnection microstructures are homogeneous at the scale of the calculation 40
41 mesh. Both experimental data and the results from the component level calculations in- 41
42 dicated that the component is cooled faster than the board. However, the interconnection 42
43 model revealed that temperature gradient over interconnection was not likely to be large 43
44 because of high conductivity of solder. Noticeable temperature gradient inside interconnec- 44
45 tion only occurred at the final stage of solidification, when the isothermal eutectic reaction 45
46 took place. It was also suggested that inner interconnections were subjected to more uni- 46
47 form temperature field and slower solidification than outer interconnections. This provides 47
48 important information for further analysis on the mechanism of primary Sn growth. 48
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1 9.2.2.2. *Mechanical Simulation* The Finite Element Method is used to evaluate the stress 1
2 states that samples experience during testing and thereby to aid in the interpretation of the 2
3 test results. The aim of stress analysis is to calculate where in the test board layout the most 3
4 critical components are located, which interconnections are most prone to fail, and how the 4
5 stresses are distributed in the component boards as well as in the interconnection areas. The 5
6 calculations are typically carried out by utilizing the sub-modeling technique. It means that 6
7 first the displacements of the whole board are calculated with a rather rough model of the 7
8 whole assembly and then the results are used as boundary conditions to a model with more 8
9 details included and only parts of the board modeled. Typically three geometric accuracy 9
10 levels are used: (1) board level model, (2) component level model and, (3) interconnection 10
11 level model. 11

12 Mechanical simulation tools are valuable especially in analyzing results from drop 12
13 tests. As discussed above, the rapid loading during the drop makes the board bend and vi- 13
14 brate that ultimately makes the assemblies to fail. The bending of the component boards can 14
15 be regarded as a sum of different vibration modes, which are natural deformation shapes 15
16 of the structure. The board bends to each one of these natural modes with certain natural 16
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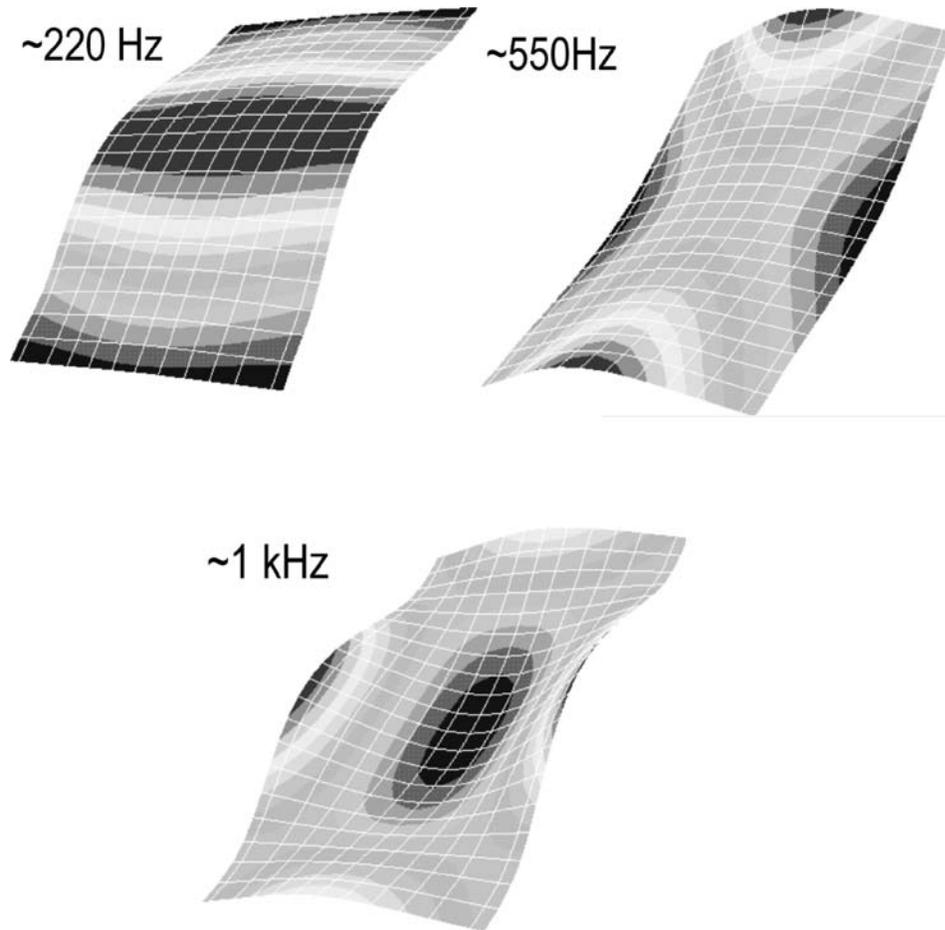


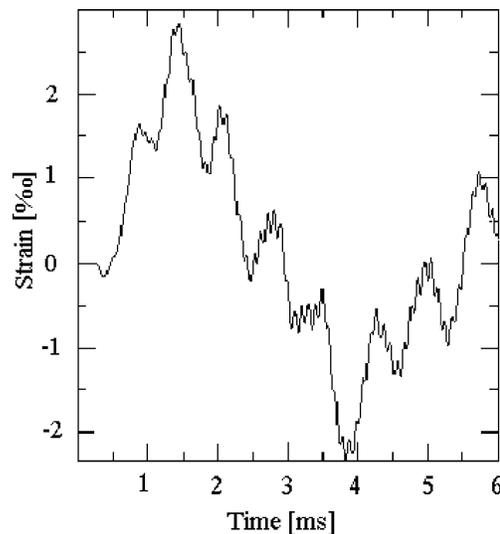
FIGURE 9.7. Three eigenforms of the drop test board (JESD22-B111) and their eigenfrequencies.

1 frequency that is characteristic to the mode. As the result the location of the maximum 1
2 stresses changes rapidly and therefore the stress states may be rather difficult to compre- 2
3 hend intuitively. 3

4 In free vibration—as in the drop test—the rule of thumb is that the lower the fre- 4
5 quency of the natural mode the greater the impact on the failure. The natural modes having 5
6 higher frequencies have smaller amplitudes and they are damped away quicker. Figure 9.7 6
7 shows three of the most important forms of the JESD22-B111 test assembly. Figure 9.8 7
8 shows the longitudinal strain on the centre of the JESD22-B111 board (board layout shown 8
9 in Figure 9.18). The strain is rather clearly a sinuous function of time. The first natural 9
10 mode is responsible for the vibration where the maximum and minimum values are about 10
11 2.3 ms apart, while the others cause the smaller and faster oscillations in the strain history. 11

12 *9.2.2.3. Simulation of Interconnection Materials* As noted earlier, manufacturing reliable 12
13 lead-free electronic products becomes even more challenging when solder interconnection 13
14 volumes are decreased while the number of reactive metals is increased [1,2,33–35]. In 14
15 addition, the microstructures formed during soldering are under continuous microstructural 15
16 evolution during the use of the devices. Thermodynamic and kinetic modeling tools can 16
17 help in determination of the potentially reliable solder, component metalization, and PWB 17
18 protective coating combinations and thereby limit the amount of experimentations needed. 18
19 Together with careful microstructural investigations these simulation tools can speed up the 19
20 R&D work and testing of new products considerably. 20

21 Thermodynamics of materials provides fundamental information on the stabilities 21
22 of phases (i.e., basically microstructures), the driving forces for chemical reactions and 22
23 diffusion processes occurring in solder interconnections during processing, testing and in 23
24 long-term use of electronic devices. Further, the thermodynamics provides us the phase 24
25 diagrams that contain information also on metastable equilibria—usually not available in 25
26 experimentally determined (stable) equilibrium diagrams. The phase equilibria in solder 26
27 or solder-substrate systems—as in any system—are computed by summing up first all 27
28 the Gibbs (free) energies of individual phases (i.e., solutions and compounds) and then 28
29



47 FIGURE 9.8. Longitudinal strain on the centre of the drop test board [JESD22-B111; see board layout in Fig- 47
48 ure 9.18(b)]. 48
49

1 minimizing—according to the second law of thermodynamics—at constant temperature 1
2 and pressure the total Gibbs energy of the n -component system. Readers interested in the 2
3 thermodynamic or diffusion kinetic modeling procedures and the calculation of phase di- 3
4 agrams are referred to vast amount of available literature, for example the review articles 4
5 and books [36–38] to begin with. 5

6 Even though the complete phase equilibrium is practically hardly ever met in solder 6
7 interconnections, the stable or metastable local equilibrium is, however, generally attained 7
8 at interfaces between dissimilar materials (or phases) in contact with each other. Since the 8
9 equilibrium is attained only at the interfaces there are activity gradients in the adjoining 9
10 phases even though the chemical potential (or activity) of a component has the same value 10
11 at the interface. These gradients determine the diffusion of components in various phases 11
12 of an interconnection region. By making use of the fundamental condition that no atom 12
13 can diffuse intrinsically against its own activity gradient as well as of the mass balance 13
14 requirement it is possible to rule out impossible reaction product sequences [36]. 14

15 It should be emphasized that phase diagrams do not contain any information on size, 15
16 shape or distribution of the phases in a material system; calculated diagrams have to be 16
17 clarified experimentally by employing different methods of microscopy. Furthermore, it 17
18 is not possible to calculate ternary or multicomponent phase diagrams solely on the basis 18
19 of the data from binary systems, since they do not include information about ternary (or 19
20 higher order) interactions or ternary compounds which are not connected to any of the 20
21 binary systems. Finally, it should be noted that even though thermodynamics provides the 21
22 basis for analyzing reactions between different materials one cannot predict the time frame 22
23 of the reactions on the basis of the phase diagrams. This is why diffusion kinetics must be 23
24 included in the analysis. 24

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27 9.3. INTERCONNECTION MICROSTRUCTURES AND THEIR EVOLUTION 27

28 It is important to know as much as possible about microstructures because they affect 28
29 the failure mechanisms in operation. The initial microstructures of the solder interconnec- 29
30 tions are generated during solidification at the cooling stage of the soldering process. This 30
31 structure establishes the starting point for the microstructural evolution that takes place 31
32 during the field service of electronic devices. 32
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35 9.3.1. *Solidification* 35

36 The majority of the lead-free solders are Sn-rich alloys with few major and mi- 36
37 nor additional elements. Therefore, the solidification behavior of solder interconnections 37
38 is dominated by Sn. At the beginning of solidification, primary grains are formed and 38
39 their morphology strongly affects the solidified microstructure. For example, in the case 39
40 of SnAgCu solders, the primary crystals can be either β -Sn, Cu_6Sn_5 or Ag_3Sn , depending 40
41 on the composition. During solidification, the primary crystals start forming wherever they 41
42 find suitable places for nucleation. Even though solidification most likely starts from either 42
43 the component or the PWB side interfaces, any oxide layer on top of molten solder inter- 43
44 connections or impurity particles in the interconnections may also act as suitable places for 44
45 heterogeneous nucleation. 45

46 Usually, when a solder alloy solidifies, a cellular or dendrite structure is formed de- 46
47 pending on the growth conditions. The most important factors affecting the solidified mi- 47
48 crostructure are solidification properties of the growing phases, temperature distribution 48
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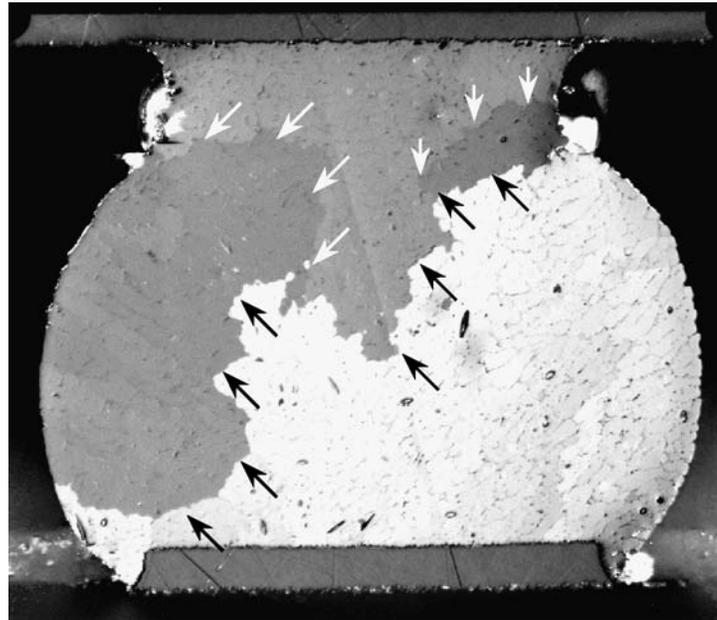
1 during solidification, and solute redistribution between liquid and solid during the cool- 1
2 ing of an alloy. Readers interested in thorough treatment of solidification are directed to 2
3 the literature [39,40]. The as-solidified microstructure in the Sn0.5Ag0.5Cu alloys used in 3
4 our experiments presented in the two case examples below is a cellular structure of tin. It 4
5 is noticeable that the interconnections seem to consist of only few colonies with different 5
6 orientation (high angle boundaries between the colonies) when investigated with polarized 6
7 light [15–19]. The areas themselves are composed of cells with angle boundary between 7
8 them (see Figure 9.9). 8

9 Another interesting point is the behavior of minor elements during solidification. 9
10 Since the last droplets of liquid that solidify are present at the high angle boundaries be- 10
11 tween the large colonies, this is also the site where most of the impurities should be located. 11
12 In fact, in our investigations gold dissolved from PWB surface finish has been observed to 12
13 enrich at the high angle boundaries as small needle-like AuSn_4 intermetallic particles [41]. 13
14 What has been stated above indicates clearly that mechanical behavior of solder intercon- 14
15 nections is most probably quite different from that of a “normal” polycrystalline material. 15
16 For example, the grain boundary cracking should not occur in the as-solidified structure 16
17 due to the absent of high angle boundaries (other than those between colonies). Therefore, 17
18 when stress is applied to interconnections having this kind of microstructure, it undergoes 18
19 microstructural evolution before fractures can propagate. A more detailed discussion on 19
20 this issue is presented below in the context of the two examples. 20

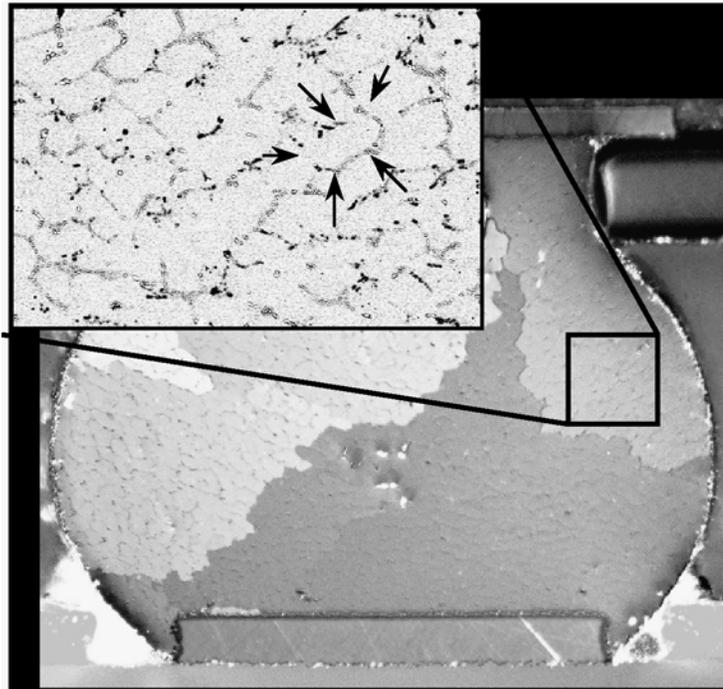
21 9.3.2. Solidification Structure and the Effect of Contact Metalization Dissolution 21

22 Under the reflow conditions typically used in lead-free soldering, solidification struc- 22
23 ture is generally cellular, where the small Cu_6Sn_5 and Ag_3Sn phases are dispersed be- 23
24 tween large primary Sn grains, as already discussed. If a protective Au metalization is used 24
25 some small needle-like AuSn_4 can also be found inside the solder matrix at the high angle 25
26 boundaries. An example of microstructure formed in the interconnections soldered with 26
27 the Sn0.5Ag0.5Cu alloy on electrochemical Ni(P) with a thin flash Au on top (denoted 27
28 Ni(P)|Au in the following) is shown in Figure 9.10. Both the Cu_6Sn_5 and the Ag_3Sn 28
29 particles are uniformly distributed around the relatively large Sn cells. Figure 9.11 shows a 29
30 micrograph taken from a sample soldered with the same alloy but this time on the boards 30
31 with Organic Solderability Preservative (OSP) on the Cu pads (noted Cu|OSP). The result- 31
32 ing microstructure seems to be different even though the same solder alloy was used: rela- 32
33 tive to Ni(P)|Au, interconnections formed on the Cu|OSP contain more and larger Cu_6Sn_5 33
34 intermetallic particles dispersed inside the solder. 34
35 35

36 Why is the resulting microstructure different? We must take into consideration what 36
37 happens during soldering. It is well known that PWB coatings and component metaliza- 37
38 tions in contact with the molten solder dissolve into the melt and thus the solder is al- 38
39 loyed further with the dissolving coatings and metalization. Too great dissolution can po- 39
40 tentially degrade the performance of solder interconnections due to the subsequent impact 40
41 on microstructures. Let us consider the differences in protective coating solidification be- 41
42 tween the Ni(P)|Au and Cu|OSP protective coatings and the implications in the microstruc- 42
43 tures. The thin layer of Au dissolves instantly and completely into the molten solder and 43
44 the Ni metalization starts dissolving next. In the case of the Cu|OSP interconnections, 44
45 the OSP partially evaporates and the rest dissolves into the solder flux during soldering 45
46 and the Cu pad that starts dissolving into the solder alloy. The dissolution rate of Cu in 46
47 Sn0.5Ag0.5Cu (wt%) is about $0.07 \mu\text{m/s}$ [15,42,43]. Based on this, the amount of Cu dis- 47
48 solution at the entire area of the soldering pad during the typical 40–45 second time above 48
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FIGURE 9.9. Optical micrograph from cross-section of the interconnection taken with polarized light: (a) colonial boundaries indicated (high angle boundaries), (b) cell boundaries indicated (small angle boundaries).

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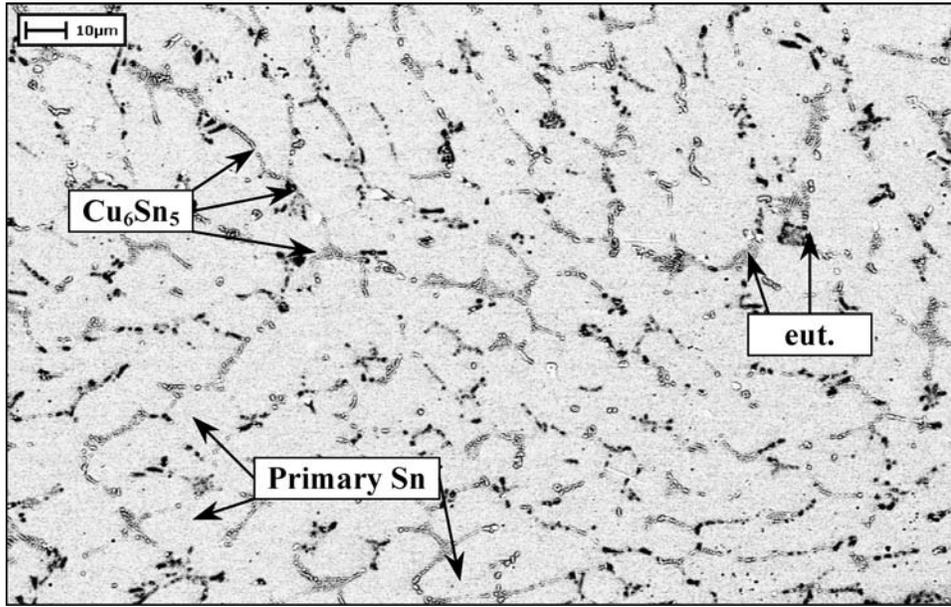


FIGURE 9.10. Microstructure of interconnections on Ni(P)|Au-coated soldering pads, where the nominal composition is Sn0.5Ag0.3Cu.

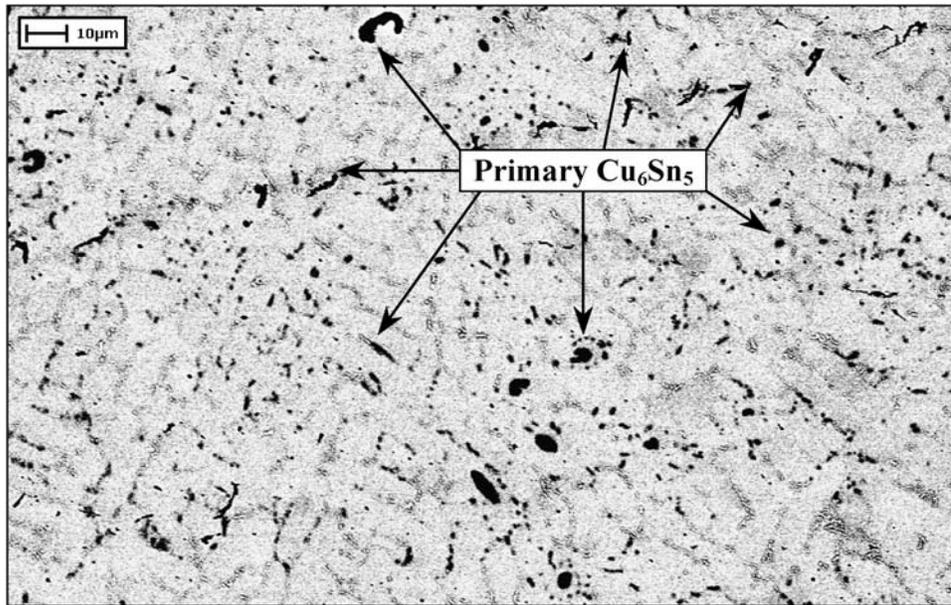


FIGURE 9.11. Microstructure of the interconnections on OSP-coated soldering pads, where the nominal composition is Sn0.5Ag1.0Cu.

217°C is enough to lift Cu concentration in the soldered interconnections close to 1 wt%, event when taking the amount of Cu bonded into the inter metallic layers on both sides of the interconnections into account. On the other hand, the dissolution rate of Ni is about 50 times smaller than that of Cu and thus, the dissolution of Ni to the solder is insignificant. All Ni that is dissolved at the interface is expected to be bonded to the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ layer. Taking into account the amount of Cu bonded to the inter metallic layers on both sides of the interconnections, the nominal composition of the interconnections soldered on the Ni(P)|Au coated pads will result in about Sn0.5Ag0.3Cu where as the final composition on the interconnection on Cu was about Sn0.5Ag1.0Cu.

An important consequence of higher Cu content is that the solidification process is different between the interconnections soldered on Ni and those soldered on Cu. When considering solidification, it is very useful to first examine the solidification of the solder interconnections with the help of equilibrium phase diagrams. It should be noted, however, that the equilibrium diagrams do not contain information about either the distribution or the morphology of the phases, as already discussed. Figures 9.13 and 9.14 present the phase fraction diagrams, where the amount of different phases in relative number of moles can be presented as a function of temperature. The interconnections soldered on Ni(P)|Au PWB have the Sn0.5Ag0.3Cu composition, whereas the interconnections soldered on Cu|OSP have the Sn0.5Ag1.0Cu.

As can be seen from Figure 9.12, the solidification of the liquid interconnections soldered on Ni(P)|Au boards starts with the formation of primary Sn phase when the interconnections are cooled down from the peak reflow temperature to below the liquidus temperature of 229°C. The Cu_6Sn_5 phase does not nucleate until below 222°C, where the composition of the liquid reaches the eutectic valley. Figure 9.13 presents the phase fraction diagram of the liquid interconnections soldered on Cu|OSP boards. In this case the solidification begins with the formation of primary Cu_6Sn_5 below 229°C. However, the nominal composition of the liquid soon meets the curve of two-time saturation, af-

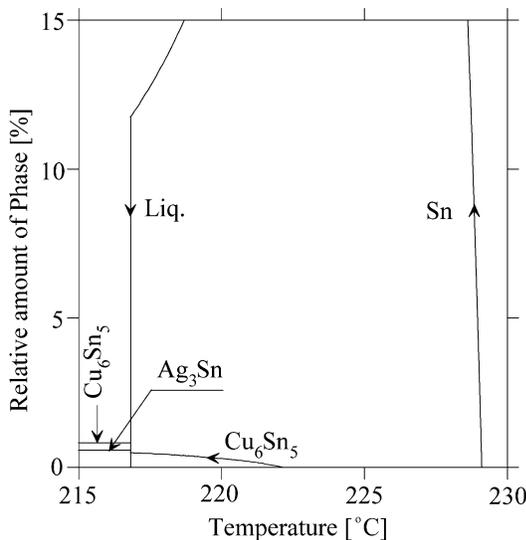
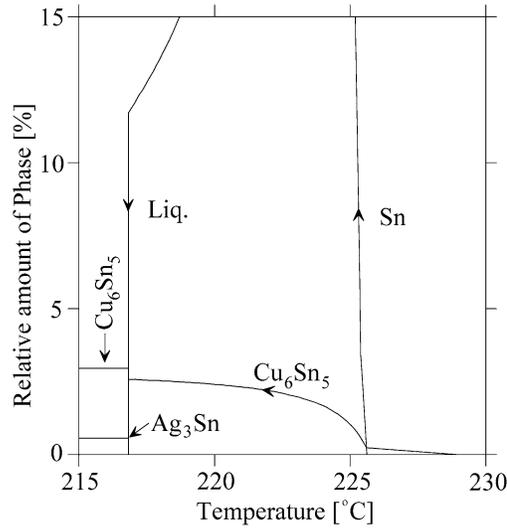


FIGURE 9.12. Phase fraction diagram of a system with nominal composition on the interconnection on the Ni(P)|Au.

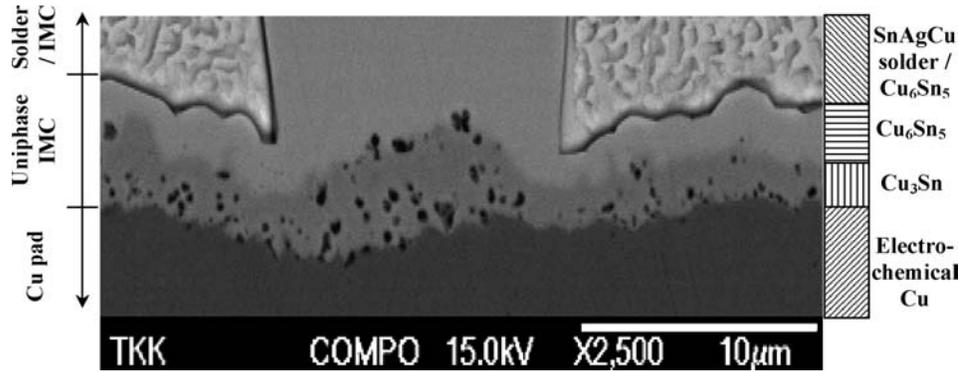
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FIGURE 9.13. Phase fraction diagram of a system with nominal composition on the interconnection on the CuOSP.

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FIGURE 9.14. Electrolytic Cu/Sn diffusion couple annealed at 125°C for 1000 hours.

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ter which the solidification of the interconnections proceeds by the binary eutectic reaction $L \rightarrow (Sn)_{eut} + (Cu_6Sn_5)_{eut}$. Below the four-phase invariant temperature, there is more than three times as much Cu_6Sn_5 in the CuOSP interconnections as in those on the Ni(P)|Au substrate and this difference is clearly visible between the microstructures in Figures 9.10 and 9.11. It should be noted, however, that the cooling rates used in reflow processes are normally much faster than the rate assumed in equilibrium considerations. Higher cooling rates will eventually evoke marked under-cooling and more refined microstructures. Hence, in practice the solidification process always departs somewhat from that of equilibrium solidification.

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9.3.3. Interfacial Reactions Products

In electronic products all the common base materials, coatings and metalizations, form intermetallic compounds (IMC) with Sn at the solder/conductor interface, and therefore these compounds must be treated as major elements of solder interconnections. A thin and continuous IMC layer(s) at the solder/conductor interfaces is an essential requirement for good wetting and bonding, and it produces distinct improvements in mechanical properties of interconnections. However, due to their inherent brittle nature too thick IMC layers may degrade the reliability of the solder interconnections. Thus, knowledge of the solder/conductor interaction and phase evolution in the solder interconnections is important not only to understand the reliability issues of the solder interconnections but also to the optimization of the soldering process from the metallurgical standpoint. The importance of knowing the properties of the IMCs in solder interconnections is clearly demonstrated in the reliability tests carried out under fast deformation rates.

Even though there are some characteristic differences between the systems met in soldering applications, the intermetallic reaction layers are formed, in principle, in three consecutive steps: the dissolution, chemical reaction, and solidification, although, the relative importance of each stage varies between the systems depending on the solubility of conductor metal in Sn [33,44]. The general sequence of events during a soldering operation can be described as follows. Immediately after the flux has removed the oxides and permits metallurgical contact of solder with the conductor metal, the contacted metal starts to dissolve into the molten solder. Initially the rate of dissolution is very high, particularly if the solder is not alloyed with the metal in question and therefore very high concentrations of solute elements can be realized locally. After a short period of time, the layer of molten solder adjacent to the contacted metal becomes supersaturated with the dissolved metal throughout the interface. At the local (metastable) equilibrium solubility, the solid IMC starts to form in this part of the interconnection. The formation of the IMC takes metal solutes out of the saturated liquid solder and causes some further dissolution of the contacted metal, especially if the intermetallic layer is not uniform on top of the substrate. Generally, after this stage the intermetallic reaction structure consists of two parts (see Figure 9.14). Next to the base metal there is a relatively thin “uniphase” layer and on top of that sometimes quite thick irregular two-phase (or solder + IMC) layer. The thickness ratio of the two parts varies strongly between different systems. What is of particular interest is that the thickness of the two-phase layer (solder + IMC) seems to increase with increasing equilibrium (stable and metastable) solubilities. During storage or in use of the assemblies, the IMCs generated during soldering grow further in thickness or increase in number, especially if the operational temperatures are well above the room temperature. Therefore, both solid/liquid and solid/solid systems must be studied to have better understanding of the reliability of soldered assemblies.

It should be noted that the local equilibrium conditions in the solder interconnections will change locally owing to the consumption of one or more of the components. This may then change the phases that can exist in local equilibrium accordingly and result in new interconnection microstructures. For a detailed discussion about the formation of IMC's in both solid/solid and solid/liquid reaction couples readers are pointed to recent review article [44].

9.3.3.1. Compounds between Cu Conductor Pads and Sn Based Solders In general, at peak temperatures typical for lead-free reflow soldering processes, i.e., around 240–250°C, Cu₆Sn₅ is the first phase to form at the liquid-tin/copper-conductor interface. The first stage of the reaction is the dissolution of Cu to liquid solder, until the solder becomes

1 supersaturated with Cu more or less uniformly at the Culliquid interface. This saturation 1
2 limit (metastable solubility) can be determined from the assessed thermodynamic data as 2
3 shown elsewhere [33,44]. 3

4 The metastable solubility indicates the largest possible amount of Cu that can dis- 4
5 solve in the liquid without precipitation. The metastable solubility is important, because it 5
6 essentially determines the dissolution rate of metal to liquid solder. The metastable solubil- 6
7 ity is typically 2–3 times higher than the stable one in metallic systems. When Cu comes 7
8 into contact with molten Sn it starts to dissolve rapidly. Initially, the dissolution is a non- 8
9 equilibrium process and locally very high concentrations of Cu can be realized in the very 9
10 vicinity of the Culliquid interface. However, the composition of the liquid at the interface 10
11 tends to decrease instantly to the metastable solubility, because extra Cu atoms are deposit- 11
12 ing back to the Cu surface. Nevertheless, since there is large driving force for the chemical 12
13 reaction between Cu and Sn atoms, the metastable composition Cu_6Sn_5 crystallites can 13
14 form very fast by the heterogeneous nucleation and growth at the Culliquid interface. In ad- 14
15 dition to more or less uniform Cu_6Sn_5 layer (uniphase) the two-phase layer ($\text{Cu}_6\text{Sn}_5 + \text{Sn}$) 15
16 can form next to the uniphase layer, most likely enhanced by the local constitutional su- 16
17 percooling of liquid. Thermodynamically there should also be a layer of Cu_3Sn between 17
18 Cu and Cu_6Sn_5 (see Figure 9.14). This layer has been experimentally observed to form in 18
19 many investigations, however, the thickness of the layer appears to be much smaller than 19
20 that of Cu_6Sn_5 layer and the formation requires rather long contact times. 20

21 *9.3.3.2. Evolution of the Sn-Cu Intermetallic Compound Layers During Use* Because Cu 21
22 is not in equilibrium with Cu_6Sn_5 , reaction in this intermetallic zone will continue through 22
23 solid state diffusion to form the layer of Cu_3Sn between the Cu pad and the Cu_6Sn_5 . The 23
24 layer of Cu_3Sn generated during soldering is very thin compared with the thickness of 24
25 Cu_6Sn_5 phase, but the thickness of both these layers increases during the solid state an- 25
26 nealing. The growth rate of the Cu_6Sn_5 phase in solid state is faster than that of the Cu_3Sn 26
27 phase over the temperature range of 60°C and 200°C but the Cu_3Sn will grow partially at 27
28 the expense of the Cu_6Sn_5 phase. The diffusion rate of Cu in Cu_3Sn is known to be as much 28
29 as three times higher than that of Sn [45]. This is why Kirkendall voids have been reported 29
30 to take place in Cu_6Sn_5 reaction couple during solid state annealing [46–48]. The authors 30
31 of this work have also detected these voids but found out that their amount depends on the 31
32 type of copper foil. In some cases voids form rather uniform plane inside the Cu_3Sn layer 32
33 or at the Cu_6Sn_5 interface where as in other cases, such as that shown in Figure 9.14, 33
34 where the $\text{Sn}/\text{Cu}_6\text{Sn}_5$ reaction couple has been annealed at 125°C for 1000 hours, it 34
35 is not possible to determine such a plane. It should be noted that the quality of copper used 35
36 in the diffusion couple experiments is very important. When using high purity Cu, only 36
37 very small sporadic voids can be observed, whereas when using electroplated/electroless 37
38 deposited copper the voids are easily seen, as shown in Figure 9.14. More discussion on 38
39 the above observation can be found in Ref. [44]. 39

40 *9.3.3.3. Other Metalization Systems* In addition to Cu also other metals, such as Ni, Au 40
41 and Ag, are used as printed wiring board and component metalization. They also react with 41
42 Sn to form intermetallic compounds. The reactions in these systems are shortly discussed 42
43 next. In general, at temperatures around 250°C Ni_3Sn_4 is the first phase to form at the 43
44 liquid tin/nickel conductor interface. The first stage of the reaction is the dissolution of 44
45 nickel into the liquid solder, until solder is supersaturated with nickel. Similar arguments 45
46 regarding the initial periods of dissolution are valid here as already discussed in the case 46
47 of Cu. After solder has been supersaturated with Ni more or less uniformly at the Nilliquid 47
48 interface, Ni_3Sn_4 nucleates at the interface and starts to grow. Dissolution rate of nickel 48
49 49

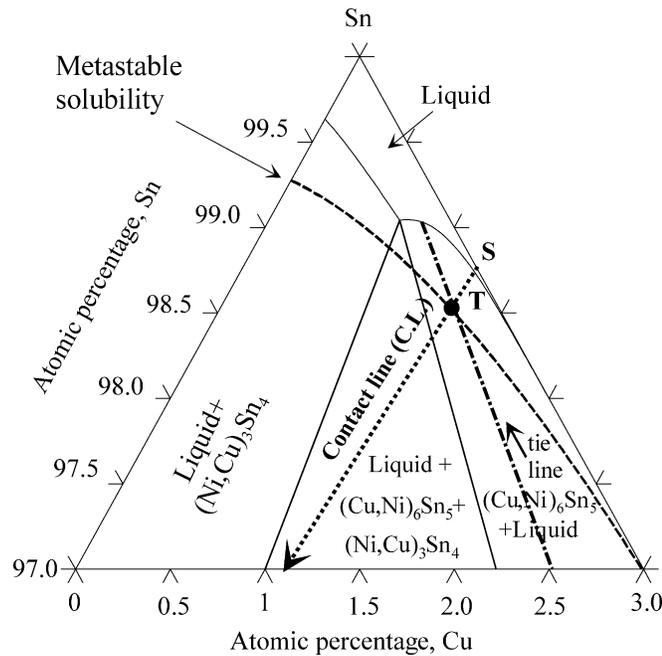


FIGURE 9.15. Enlarged corner of the Sn-Cu-Ni isotherm at 235°C.

to a liquid tin is much lower than for example that of copper [42,43]. This is reflected in the thickness of the nickel intermetallic formed during soldering that is generally much thinner than copper intermetallic compounds. Especially the $(\text{Ni}_3\text{Sn}_4 + \text{Sn})$ two-phase layer is usually absent or very thin.

What has been stated above is the general picture of events when Sn-Pb (or Sn-based solders without copper) are used. However, when using lead-free solders, which include small amounts of Cu, the situation changes and the first phase to form is Cu_6Sn_5 [or more precisely $(\text{Cu},\text{Ni})_6\text{Sn}_5$]. The formation of $(\text{Cu},\text{Ni})_6\text{Sn}_5$ on the Ni metalization can be briefly explained with the help of Figure 9.15, which shows the enlarged Sn-rich corner of the ternary Cu-Ni-Sn isotherm at 235°C. The arrow that starts from S is the contact line from the nominal composition of the SnCu solder to the Ni-corner. The evaluated ternary metastable solubility is shown with the dotted line. During the short soldering period, the composition of the molten solder changes along the contact line from the original solder composition (S) towards Ni as shown in Figure 9.15, because Ni is dissolved into the solder where the Cu/Sn ratio stays unchanged. This is owing to the fact that dissolution of Ni into liquid solder is much faster than diffusion of Cu or Sn into Ni that has to take place via solid-state mechanism. Contact line crosses the evaluated metastable liquidus inside the two-phase region (point T). This crossing point determines the absolute maximum amount of Ni in the solder. Since T is situated inside $(\text{Cu},\text{Ni})_6\text{Sn}_5 + \text{liquid}$ two-phase region, the first phase to form is $(\text{Cu},\text{Ni})_6\text{Sn}_5$. The metastable solubility is reached very quickly and therefore the formation of the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ on the Ni layer takes place rapidly. The Ni content in the first $(\text{Cu},\text{Ni})_6\text{Sn}_5$ crystals formed is determined by the tie line passing through the point T at the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ end. The composition of the liquid in local equilibrium with the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ crystals can be obtained from the other end of the tie line. It can be seen from Figure 9.15 that if Cu content of the solder is decreased, the crossing point

(T) starts to move to the left along the metastable solubility line (at constant temperature). When Cu concentration in the solder has decreased to about 1 at% (Figure 9.15) the crossing point is inside the $(\text{Ni,Cu})_3\text{Sn}_4 + (\text{Cu,Ni})_6\text{Sn}_5 + \text{Sn}$ three phase region, which means that both IMC phases will form during soldering. Finally, when Cu concentration is decreased to about 0.7 at% the connection line crosses the metastable solubility line inside the $(\text{Ni,Cu})_3\text{Sn}_4 + \text{Sn}$ two-phase region, $(\text{Ni,Cu})_3\text{Sn}_4$ is the first intermetallic compound to form during the soldering process. Thus, depending on the Cu content of the solder $(\text{Ni,Cu})_3\text{Sn}_4$, $(\text{Cu,Ni})_6\text{Sn}_5$ or both IMCs can form on top of the Ni metalization.

In a solid-state reaction only Ni_3Sn_4 out of the three stable phases grow between Ni and Sn end elements. If the other two stable IMCs grow their thickness are so small that they cannot be detected within the resolution limits of SEM even after prolonged annealing [45]. The formation of fast growing metastable NiSn_3 has also been detected at least in one investigation [50]. The temperature region where the metastable phase grows is quite restricted and additional elements present in Sn (for example Pb) suppress its growth effectively.

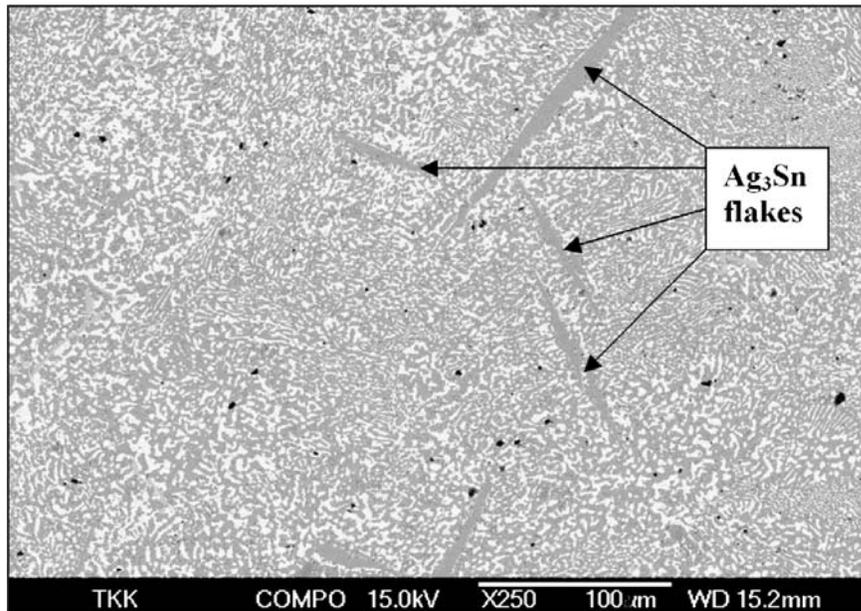
During soldering Au is the fastest metal to dissolve to Sn-rich alloys. Nevertheless, the same arguments concerning the dissolution process of Au-Sn as discussed in the case of Cu-Sn, also apply here. After solder has been supersaturated with Au more or less uniformly at the Aulliquid interface, the IMCs form out of the supersaturated melt. Results from the solderability experiments with the wetting balance show that in this system the two-phase layer (Au-Sn-IMC + Sn) tends to be very thick with respect to the uniphase IMC layer. This is expected to be related to high metastable solubility of Au in liquid Sn, which in turn indicates high dissolution rate. Thus, if the Au-layer is thin it is dissolved completely and AuSn_4 is found as randomly distributed needle-like phases inside the solder matrix after cooling. The dissolution rate of Ag is nearly as high as that of Au [42,43] and therefore during soldering tin will dissolve silver (if applied in a form of a plating) substrate rapidly. Similar arguments concerning the dissolution process with respect to time as discussed previously apply here again. After solder has been supersaturated with Ag more or less uniformly at the Agliquid interface, IMCs form by solidification out of the supersaturated melt. The intermetallic phase that has been observed to form is the orthorhombic Ag_3Sn [42,43,51]. If the silver substrate is thick enough the intermetallic forms a continuous layer on top of the original surface. Also in the Ag-Sn system the two-phase layer (Ag-Sn IMC + Sn) tends to be very thick with respect to the uniphase IMC layer. As silver (like gold) is usually used as a surface finish in electronics (i.e., in small quantities) it quickly dissolves from the original interface and forms the Ag_3Sn intermetallic into the bulk solder. The morphology of the Ag_3Sn resembles little bit that of AuSn_4 . Ag-intermetallic compounds are in the form of relatively large flakes (Figure 9.16) and can therefore cause severe problems with relatively low concentration of the compound.

9.3.4. Deformation Structures (Due to Slip and Twinning)

The familiar stress–strain diagram found practically in all the textbooks on mechanics represents the mechanical properties of metals. If the stress applied is below the yield stress (σ_y) the deformation is said to be elastic. This means that the strain induced is completely removable upon release of stress. At stress levels equal or higher than the yield stress, the metal deforms plastically. This means that deformation is not recoverable upon release of stress. Any stress above the yield stress is referred as flow stress. Solder materials are generally quite soft (under normal deformation rates) and therefore one is usually interested

1 in plastic deformation. It should be noted that in the stress–strain diagrams metal is usually 1
2 pictured to be under uniaxial loading. In reality loading is multiaxial in most of the cases. 2
3 This means that there are several tensile and shear stress components acting simultaneously 3
4 on the body. In addition, it should be noted that the tensile behavior of material can be 4
5 highly strain-rate dependent. Especially soft materials, like solders, can behave as much 5
6 stronger materials under high strain rates than they do under slow strain rates. This issue 6
7 will be further discussed in the Section 9.4.2. 7

8 Plastic deformation of metals occurs by four primary mechanisms: (1) Slip by dislo- 8
9 cations, (2) twinning, (3) grain boundary sliding and (4) diffusional creep. The importance 9
10 of each mechanism depends among other things on stress state, strain rate, temperature and 10
11 microstructure. The slip mechanism can be defined as: “The parallel movement of two ad- 11
12 jacent crystal regions relative to each other across some plane (or planes)” [52]. Slip occurs 12
13 along some specific (usually close packed) plane in definite slip direction by dislocation 13
14 movement. The combination of slip plane and slip direction defines the slip system along 14
15 which dislocation glide occurs. The amount and type of slip systems depends on the crys- 15
16 tal structure of the metal in question. In tin, the slip systems are (110) [001], (100) [001], 16
17 (10 $\bar{1}$) [101], and (121) [101] [53]. If a metal crystal possesses an insufficient number of inde- 17
18 pendent slip systems, temperature is very low or the strain rate is very high, twin modes 18
19 may be activated in some metals to provide additional deformation mechanism. Twinning 19
20 can be defined as follows “A deformation twin is a region of a crystalline body which had 20
21 undergone a homogeneous shape deformation in such a way that the resulting structure is 21
22 identical with that of the parent, but oriented differently” [54]. Examples of such twins can 22
23 be seen for example after drop testing (Section 9.4.2) where the deformation rate has been 23
24 so high that slip has not had time to occur in large scale. 24
25



48 FIGURE 9.16. Solidification structure of SnAgPb (~3.5 at% Ag) solder showing the large Ag₃Sn flakes. 48
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9.3.5. Recovery, Recrystallization and Grain Growth

During plastic deformation at a sufficiently low temperature, hardening of a metal or alloy occurs. This strain hardening is a result of a net increase in the number of dislocations and other defects in the material. If the metal is subsequently annealed, typical mechanical properties, such as yield strength and hardness, gradually return to values before the deformation. If this process takes place without changes in the grain structure, the phenomenon is called recovery. At higher temperatures or with longer annealing times, most metals will undergo a discontinuous change in grain structure, known as recrystallization. In this process new stress-free crystals grow within the deformed structure and they grow until the original grains are consumed. This primary recrystallization is followed by uniform grain growth, or by highly selective grain growth (secondary recrystallization). The driving force for the recrystallization is the increase in internal energy caused by plastic deformation. Experiments have shown that during plastic deformation only about 1–15% of energy is stored into the structure and rest is dissipated irreversibly as heat [55]. Due to the nature of the recrystallization process a minimum deformation is necessary before it can take place. The kinetics of recrystallization is dependent on a large number of variables, the most important of which are the amount of deformation, the alloying and impurity elements, stacking fault energy, and the original grain size. Naturally the rate is also dependent on time and temperature.

9.4. TWO CASE STUDIES ON RELIABILITY TESTING

In the following two case studies the component used is a lead-free Sn0.2Ag0.4Cu (wt%)-bumped chip scale packaged (CSP) component with 144 bumps (500 μm in diameter) and bump pitch of 800 μm (denoted CSP144 in the following). The heights of the bumps are 480 μm and the under-bump metallurgy consists of ~0.6–0.8 μm-thick electrochemical Ni, on top of which there originally was a thin gold layer before bumping. The structure of the component and materials used are shown in Figure 9.17.

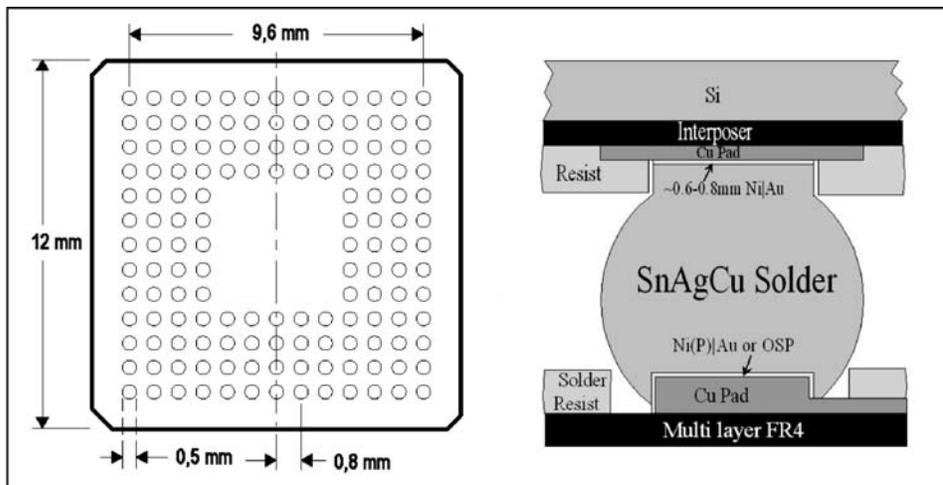


FIGURE 9.17. Structure and dimensions of the CSP144 component.

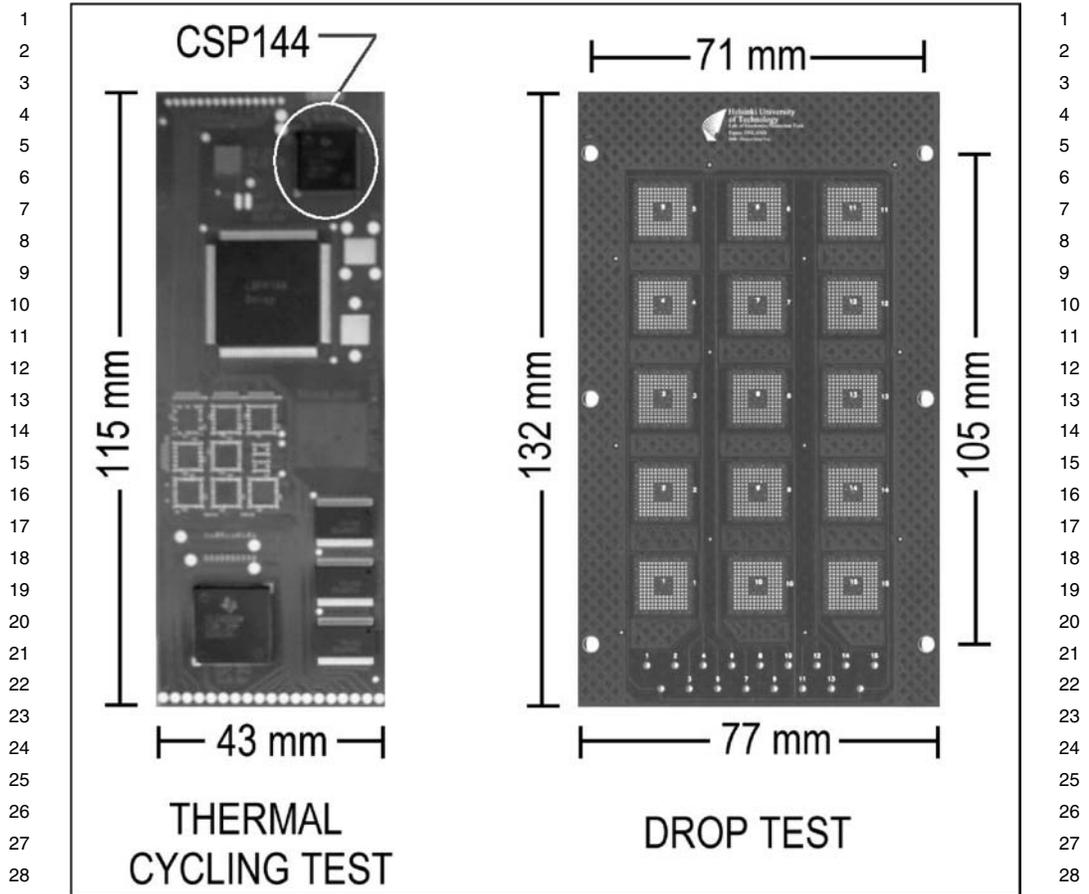


FIGURE 9.18. Layout of the test boards used in (left) thermal cycling tests, and (right) drop tests.

The protective coatings on the printed wiring boards (PWB) are the same in both case examples but the board layouts are different. The high density FR4 boards were manufactured with either electroless Ni plating containing about 9 wt% (16 at%) P with flash Au finish on top (denoted Ni(P)Au) or organic solderability preservative (denoted CuOSP) protective coating on the Cu soldering pads.

The layout and dimensions of both test boards are shown in Figure 9.18. The dimensions of the boards used in thermal cycling tests were 43 mm \times 115 mm \times 1.6 mm. The board was a double-sided four-layer FR4 board. The test assemblies were thermally cycled (Weiss TS 130) according to the IEC 68-2-14N standard (+125°C/-45°C, with 15 min dwell time) until all components had failed. The criterion for failure was defined as 20% increase in the initial resistance from that after the reflow.

The high-density circuit boards for the drop tests were designed according to the JESD22-B111 drop test standard. The PWB was a double-sided (1 + 6 + 1) stack-up multi-layer FR4 board with six inner layers in addition to the topmost resin coated copper layers. The middle component lies in the geometrical centre of the board. The pad and conductor patterning on the board is the same on the two sides except that one side of the board has micro-vias in all of the soldering pads and the other does not. Although the board is double-

1 sided, components are mounted on one side only. The weight of a fully furnished assembly 1
2 is 28.5 ± 0.3 g. The test assemblies were drop tested according to the JESD22-B111 stan- 2
3 dard (see Section 9.2.1.2). A failure was recorded when the resistance through the daisy 3
4 chain network exceeded the $1.5 \text{ k}\Omega$ threshold resistance for 200 nanoseconds three times 4
5 in a sequence of five drops. The test boards were mounted on support rods with screws at 5
6 the four corners of the board (see Figure 9.18). The components were facing downwards 6
7 during the test. The drop height was set to 82 cm in order to achieve the required peak 7
8 deceleration of 1500 G for the duration of 0.5 ms (half-sine pulse). 8
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11 9.4.1. Case 1: Reliability of Lead-Free CSPs in Thermal cycling 11

13 In this case study, the effect of solder pastes and printed wiring board protective 13
14 coatings on the reliability of the CSP144 interconnections under fatigue stressing will 14
15 be discussed. The boards were assembled using three different Pb-free no-clean solder 15
16 pastes. The solder paste compositions (wt%) were Sn4.0Ag0.5Cu, Sn3.8Ag0.7Cu, and 16
17 Sn3.5Ag0.75Cu, which will be later referred as P₁, P₂ and P₃ respectively. After assem- 17
18 bly, the test boards were inspected and subjected to thermal shock testing (IEC 68-2-14N 18
19 standard: $+125^\circ\text{C}/-45^\circ\text{C}$, dwell 15 min/15 min, up to 3000 cycles). 19

20 The experimental design included a large number of test structures assembled in 20
21 a full-scale production line to enable comprehensive statistical analysis. The reliability 21
22 test procedure was constructed as a full factorial design so that the significance on each 22
23 factor could be tested with the Analysis of Variance. The type of lead-free *solder paste* 23
24 and the *PWB coating* were the main variables studied. Results from the statistical analysis 24
25 carried out with Analysis of Variance showed that no statistically significant differences 25
26 were found between the CSP144 assemblies soldered with the different solder pastes (risk 26
27 level $< 0.1\%$). This is due to the fact that the composition of the bump is dominant; most of 27
28 the solder material composing the interconnections originates from the component bump 28
29 and only about ten percent, by volume, from the solder paste. The compositions of the 29
30 solders and the bump material, as well as the nominal interconnection compositions after 30
31 the reflow, are presented in Figure 9.19, which presents the Sn-rich corner of the SnAgCu 31
32 phase diagram with isothermal lines representing the liquidus temperatures. Letter B in the 32
33 diagram depicts the original composition the component bump. N represents the nominal 33
34 composition on the interconnections on Ni(P)|Au after the reflow and O represents Cu|OSP, 34
35 respectively (see also Section 9.3.2 of this chapter). Owing to the very small differences 35
36 in the interconnections compositions between the assemblies soldered with the different 36
37 solder pastes, the effect of different pastes was ignored in the following analyses. 37

38 The type of PWB coating material, on the other hand, was highly significant (sig- 38
39 nificant at risk level $< 0.05\%$; ANOVA): under thermo-mechanical loading the intercon- 39
40 nections on the Ni(P)|Au were more reliable than those on the Cu|OSP. The Weibull plot 40
41 drawn from the thermal cycling results is presented in Figure 9.20. The characteristic 41
42 life times (η) for the Ni(P)|Au and the Cu|OSP were 1937 and 1485 cycles, respectively. 42
43 The Weibull distribution shape parameter (β) for the Ni(P)|Au and Cu|OSP are 3.47 and 43
44 4.72 respectively. The difference in the beta values is also significant at less than 5% risk 44
45 level. 45

46 Because the only difference between the two groups of samples is the coating mate- 46
47 rial on the soldering pads, the root cause for the different reliability performance must be 47
48 related to that. As mentioned earlier in Section 9.3.2, an important consequence of higher 48
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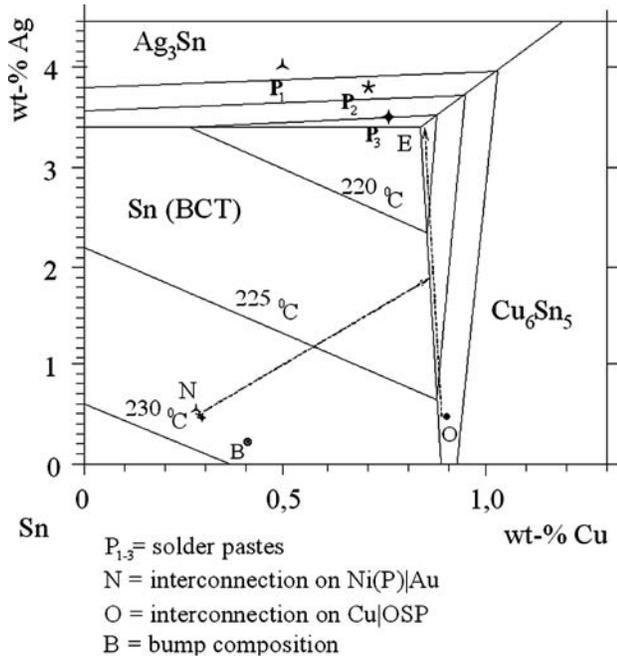


FIGURE 9.19. Compositions of different materials and the solidification path.

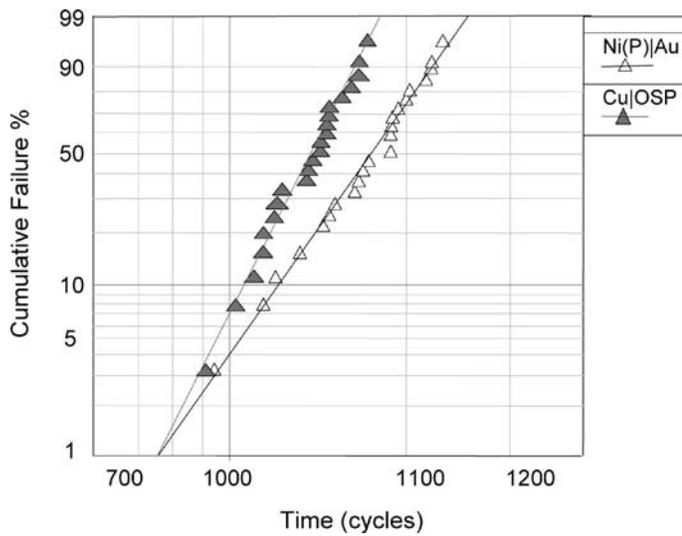


FIGURE 9.20. Weibull reliability plots of the CSP144s on different coatings.

Cu content (due to dissolution of the soldering pad) is that the solidification process and the resulting microstructure is different in these two types of interconnections: relative to Ni(P)|Au, interconnections on the Cu|OSP boards contain more and larger Cu_6Sn_5 intermetallic particles dispersed in the bulk solder. Otherwise the microstructures are very similar: The components under bump metallurgy consist of $\sim 0.6\text{--}0.8\ \mu\text{m}$ thick electro-

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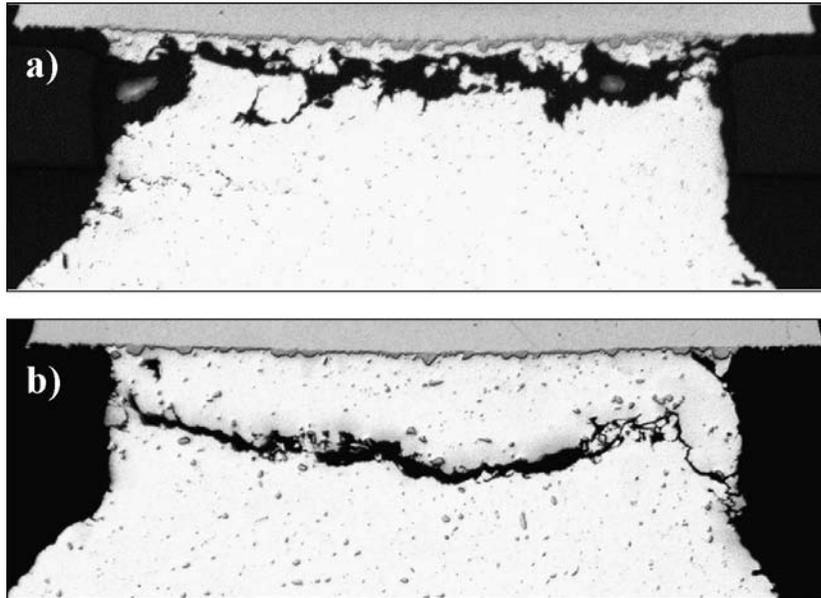


FIGURE 9.21. Crack paths in the interconnection on Ni(P)Au (a) and CuOSP (b).

chemical Ni on the top of which there has been a thin gold layer. The original gold layer had dissolved completely into the bump alloy during bumping. In the bumping stage reflow, the first phase to form is the $(\text{Cu},\text{Ni})_6\text{Sn}_5$ instead of the Ni_3Sn_4 as already discussed. The detailed analysis of the reaction can be found elsewhere [56,57]. The component side interconnection interface is thus the same in both the cases. However, the intermetallic layer on the PWB side is different: Cu_6Sn_5 in the CuOSP interconnections and $(\text{Cu},\text{Ni})_6\text{Sn}_5$ in the Ni(P)Au interconnections. The detailed fractographic studies showed that no other failure modes were operational than cracks in solder interconnections (see Figure 9.21: (a) interconnections on the Ni(P)Au, (b) interconnections on the CuOSP). Therefore to be more exact, the root cause for the different reliability performance must be related to the differences in the bulk solder and how the microstructures evolve under thermo-mechanical loading.

Micrographs in Figure 9.22 show how the microstructures evolve due to the deformation-induced recrystallization. Polarized light is useful in evaluating microstructures because the reflection is dependent on the grain orientation (asymmetric crystals) of the surface and therefore areas with different orientation are seen in different colors. The topmost micrograph shows the initial structure of a SnAgCu CSP interconnections on CuOSP after reflow soldering. The interconnections after reflow consist of relatively few colonies inside of which a cellular solidification structure is visible. The boundaries between the contrasting areas, as seen in Figure 9.9(a), are boundaries of uniformly oriented colonies of small Sn cell. The eutectic structure ($\text{Sn} + \text{Cu}_6\text{Sn}_5 + \text{Ag}_3\text{Sn}$ phases) is embedded in between the tin cells. AuSn_4 is typically seen at the boundaries between the colonies. Micrographs in the middle in Figure 9.22 exemplify how the microstructures evolve during thermomechanical loading. Recrystallization is apparent in the entire “neck region” of the interconnection even after 1000 thermal cycles, while the rest of the interconnection seems to be mostly unaffected. It seems that microstructural deformation

1 of the most highly stressed areas leads to localized recrystallization of the interconnec- 1
2 tions. 2

3 In fact, the reliability performance on the two types of assemblies is related to mi- 3
4 crostructural changes that take place during the thermomechanical loading. The difference 4
5 in the performance between the interconnections on Ni(P)Au and CuOSP reflects the 5
6 differences in bulk microstructures of the solder interconnections. Because the microstruc- 6
7 ture of the CuOSP interconnections contains numerous relatively large Cu_6Sn_5 primary 7
8 crystals, the progress of recrystallization is more rapid. These primary particles enhance 8
9 the onset of recrystallization in the CuOSP interconnections. These non-coherent high- 9
10 angle boundaries between large Cu_6Sn_5 crystals and solder matrix provide advantageous 10
11 nucleation sites for recrystallization [58,59] and therefore the rate is faster in the CuOSP 11
12 interconnections. 12
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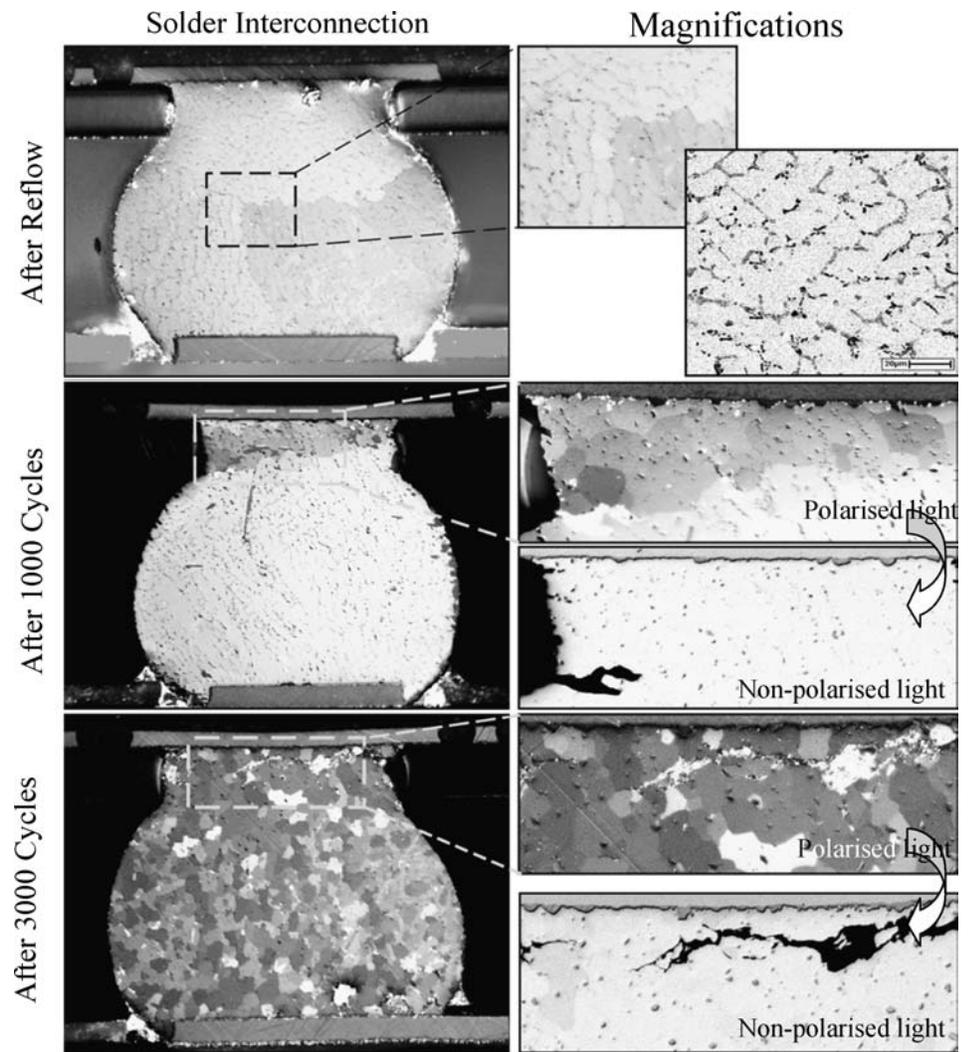


FIGURE 9.22. Evolution of microstructures in solder interconnections during thermal cycling.

The formation of high-angle boundaries between the recrystallized grains favors the nucleation and propagation of intergranular cracks in the boundaries between the recrystallized grains. The cracks do not nucleate only at the corners of the interconnections, but also at the boundary between the recrystallized grains and the non-recrystallized part [15,17–19]. Therefore, the formation of grain boundaries is a prerequisite for the cracks to propagate through the solder interconnections. Because the onset and progress of recrystallization of the interconnections on CuOSP is faster, cracks can also nucleate and propagate more rapidly and therefore interconnections on CuOSP also fail earlier.

9.4.2. Case 2: Reliability of Lead-Free CSPs in Drop Testing

Portable products are more prone to being dropped than affected by the changes in thermal conditions. Therefore over the past few years, the emphasis of the reliability research has moved from performance of assemblies under thermomechanical loading more towards mechanical shock loading, as has already been discussed. The following case study discusses some of the central issues concerning the reliability of solder interconnections under fast deformation rates.

The reliability of the same lead-free CSP144 component, as in the case study 1, is investigated under mechanical shock loading. The test boards were assembled using the Sn3.8Ag0.7Cu solder paste. After the post-reflow inspection the assemblies were drop tested according the JESD22-B111 standard. The failure mechanisms were studied from cross sections made with the standard metallographic methods. Cross sections were analyzed with the optical, scanning electron, and transmission electron microscopy. Figure 9.23 presents Weibull plot of the Ni(P)|Au and CuOSP finished assemblies.

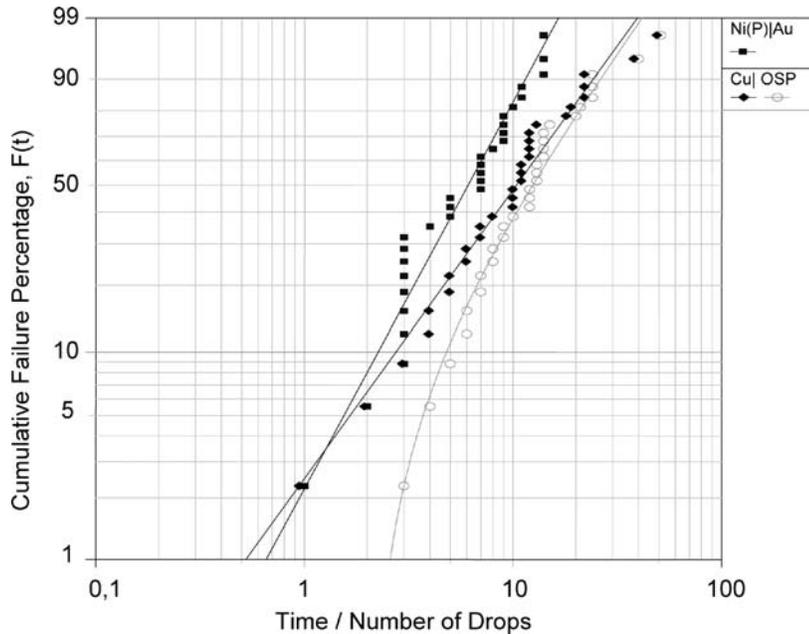


FIGURE 9.23. Weibull reliability plots for the CSP144s on different protective coatings.

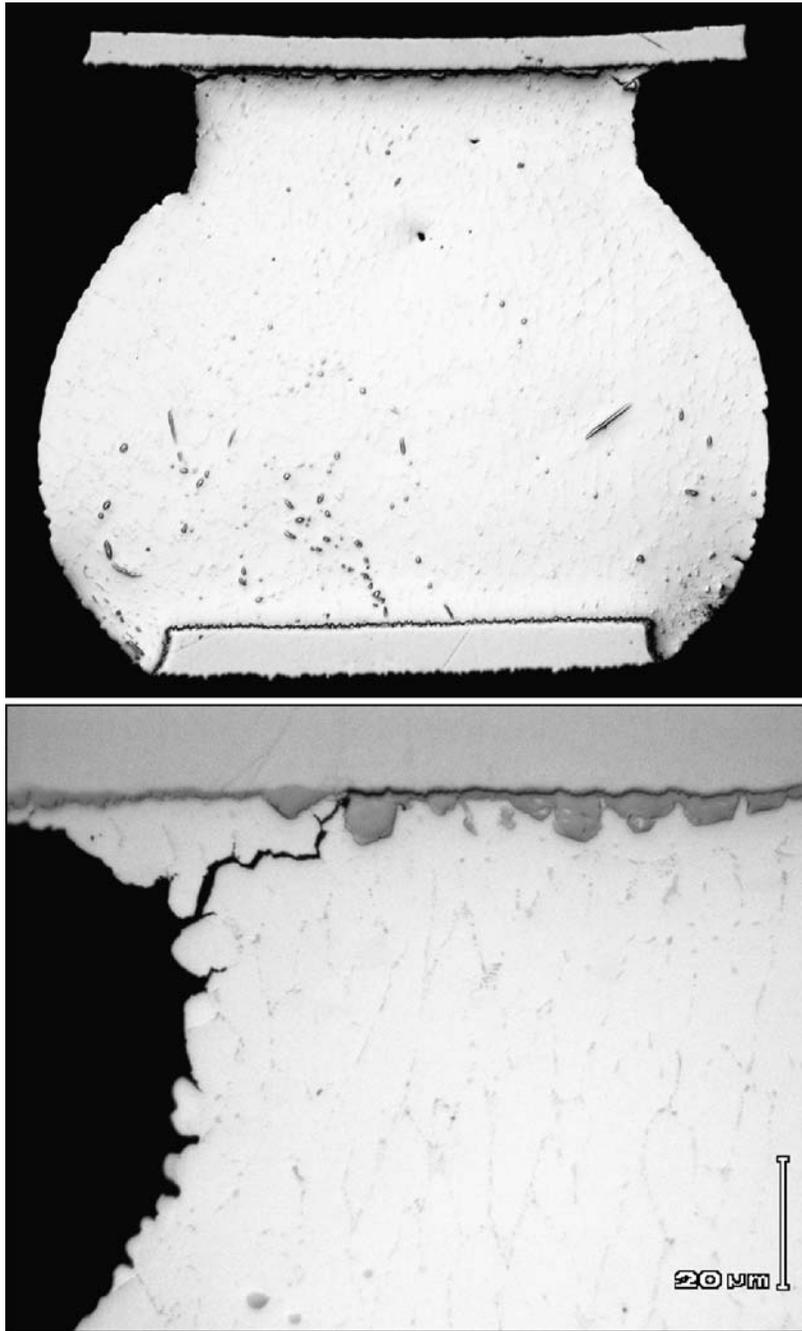
1 The characteristic life times (η) were 7 and 13 drops, and the shape parameters (β) 1
2 were 1.8 and 1.4 for Ni(P)|Au and CuOSP assemblies, respectively. The failure free life 2
3 time in the case of CuOSP is 2 drops. The decision to use either the two or three parameter 3
4 form of the Weibull distribution was based on the goodness of fit test. The reliability per- 4
5 formance between the components soldered on the Ni(P)|Au and the CuOSP coated boards 5
6 was statistically significant at less than 0.01% risk level. The significance between the beta 6
7 parameters was also statistically significant. 7

8 The β values of the drop-tested samples are considerably smaller than those typically 8
9 encountered in thermal cycling tests and, accordingly, the failure modes and mechanisms 9
10 were expected to be different. The primary failure modes investigated at the failure analy- 10
11 sis stage, were indeed different from those observed in the thermally cycled interconnec- 11
12 tions. In addition, the mechanisms were also different between the interconnections on the 12
13 Ni(P)|Au and the CuOSP. Interconnections on the CuOSP failed from the component side 13
14 interface, where cracks propagated inside the $(\text{Cu,Ni})_6\text{Sn}_5$ intermetallic compound (see 14
15 Figure 9.24), where as those on the Ni(P)|Au failed from the PWB side interface, where 15
16 cracks propagated between the $(\text{Cu,Ni})_6\text{Sn}_5$ and the Ni(P) metalization (see Figure 9.25). 16
17 Cracks in the CuOSP interconnections typically nucleate at the corner of the interconnec- 17
18 tions, safe distance away from the intermetallic compound (IMC) layers in the bulk sol- 18
19 der, but jump very quickly into the IMC layer, which obviously provides a favorable path 19
20 for the crack to propagate due to the brittle nature of the compound. The fractures in the 20
21 Ni(P)|Au interconnections propagate very close to the nickel metalizations underneath the 21
22 $(\text{Cu,Ni})_6\text{Sn}_5$ intermetallic layer as shown in Figure 9.25. The failure modes of the present 22
23 drop tested samples are very different from those observed after thermal cycling. The fail- 23
24 ure mode determined earlier in thermally cycled samples of the same material combinations 24
25 was always an intergranular fracture in the bulk solder. 25

26 What makes the crack propagate under drop test conditions inside the IMC rather 26
27 than in the bulk solder, as was typical for thermally cycled samples? The drop tests are 27
28 carried out at room temperature (~ 295 K), which is relatively high ($0.6T_m$) compared to 28
29 the melting point of the solder (~ 500 K). Therefore, the plastic behavior of the solder is 29
30 strongly strain rate dependent. As shown in Figure 9.26, the solder becomes remarkably 30
31 stronger as the strain rate increases from that used in thermal cyclic tests ($\sim 10^{-3}\%$ /s) to 31
32 that used in drop tests ($\sim 10^4\%$ /s). Thus, in drop tests, where the deformation rate is very 32
33 high, the solder interconnections are much stronger than those in thermal cycling tests. 33
34 Subsequently the magnitudes and distributions of the stresses in the solder interconnec- 34
35 tions are different under thermal cycling and drop test conditions. Finite element calcula- 35
36 tions showed that as the strain rate increases not only the stresses in solder interconnec- 36
37 tions increase but also they become more concentrated on the component side of the inter- 37
38 connections [20,21]. Due to the much higher flow stress of the solder interconnections in the 38
39 drop tests, the intermetallic compound layers will experience significantly higher stresses 39
40 than those in thermal cycling. The same calculations showed that stresses at the solder/pad 40
41 interphase on the PWB side are less than half of that on the component side. The tensile 41
42 strength of the solder increases above the fracture strength of the IMC and this ultimately 42
43 makes the fractures propagate inside the IMC layers, instead of the bulk solder. In thermal 43
44 cycling, where the strain rates are relatively low, the cyclic thermomechanical loading of 44
45 the interconnections generates plastic deformation, which ultimately leads to propagation 45
46 of fatigue fracture through the solder interconnections. 46

47 No recrystallization was observed in the drop-tested samples, even after several 47
48 months of storage at room temperature. This is because during drop testing the strength of 48
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FIGURE 9.24. Component side fracture through the $(\text{Cu,Ni})_6\text{Sn}_5$.

the solder interconnections increases and the solder does not markedly deform plastically. As the strain rate is increased twinning mechanism is activated. Twins are typically observed in the regions of the interconnections where stresses are highest [see Figure 9.27(a)].

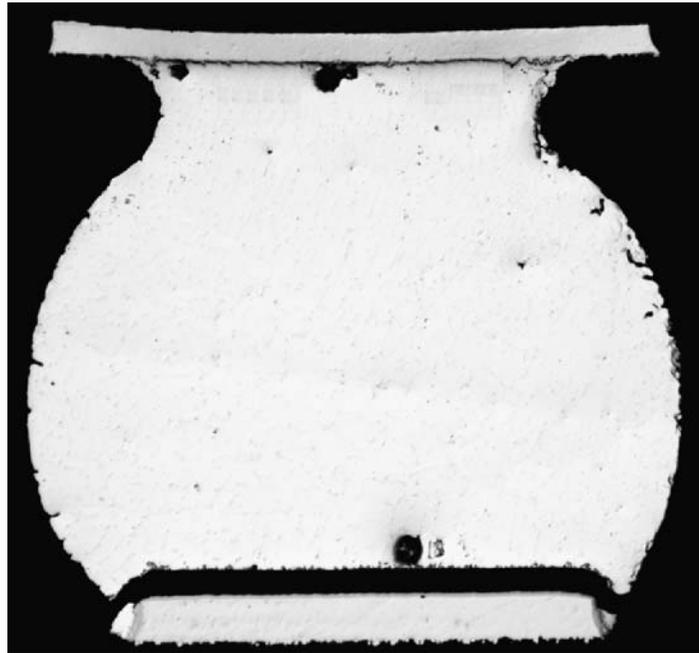


FIGURE 9.25. Failure on the PWB side below the $(\text{Cu,Ni})_6\text{Sn}_5$ ("Black Pad" \leftrightarrow Ni(P)|Au assemblies).

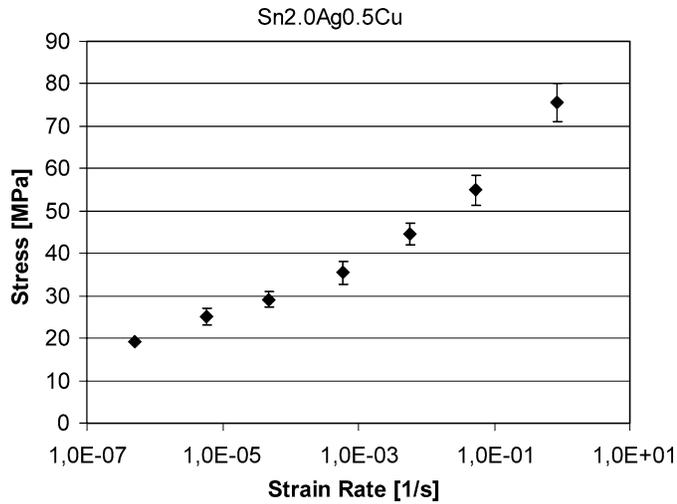


FIGURE 9.26. Flow stress vs. strain rate with standard deviations (Sn_{2.0}Ag_{0.5}Cu at room temperature).

Twins sometimes observed crossing the colonial boundaries [see Figure 9.27(b)] support the conclusion that the boundaries between the colonies are indeed high angle boundaries, as pointed out earlier.

Despite the result that the stresses at the PWB side interface are much smaller than at the component side, the primary failure mode for the interconnections soldered on

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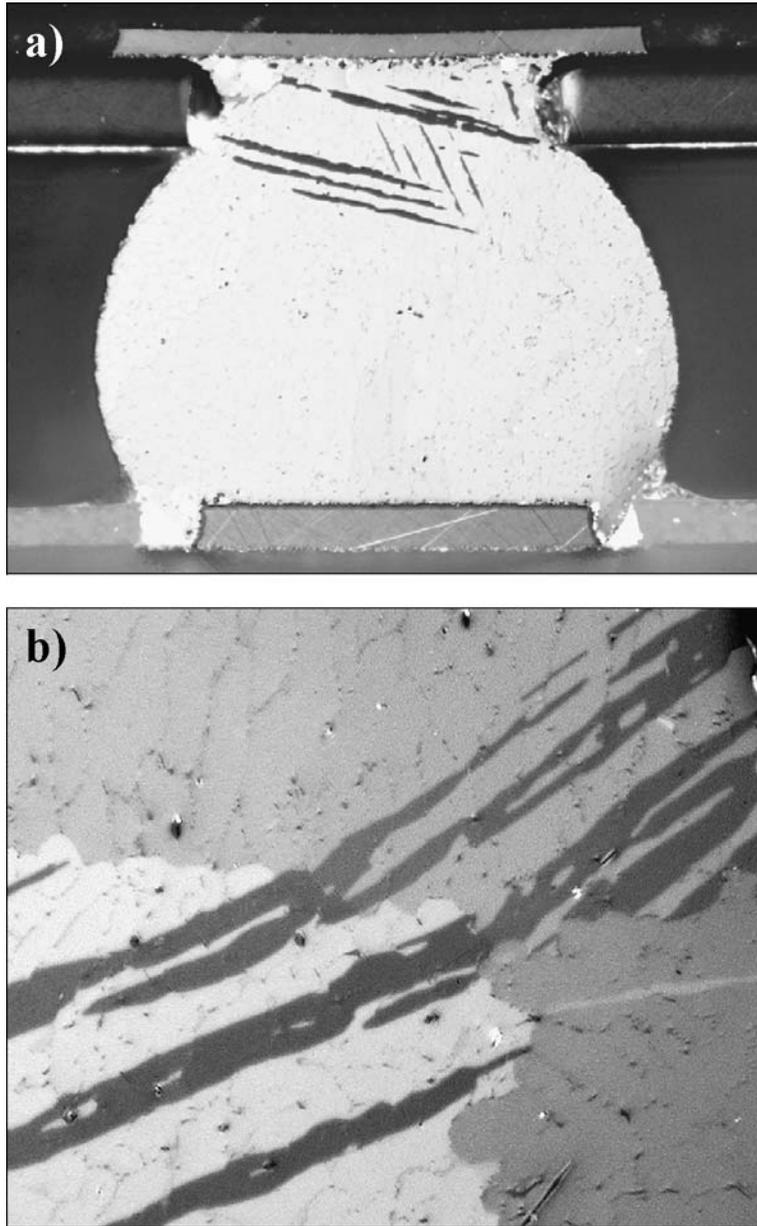


FIGURE 9.27. Structure of the bulk solder after drop test: mechanical twins.

Ni(P)/Au was a fracture on the PWB underneath the $(\text{Cu,Ni})_6\text{Sn}_5$ intermetallic layer. This emphasizes the weak nature of this interface. The fracture typically propagates completely through the solder interconnections at a single or very few impacts. The fracture path is always very smooth and straight, compared with the Cu/OSP interconnections fractures discussed above. The PWB side intermetallic layer becomes a complex multilayered structure due to the phosphorus trapped in the Ni metalization during chemical deposition. The

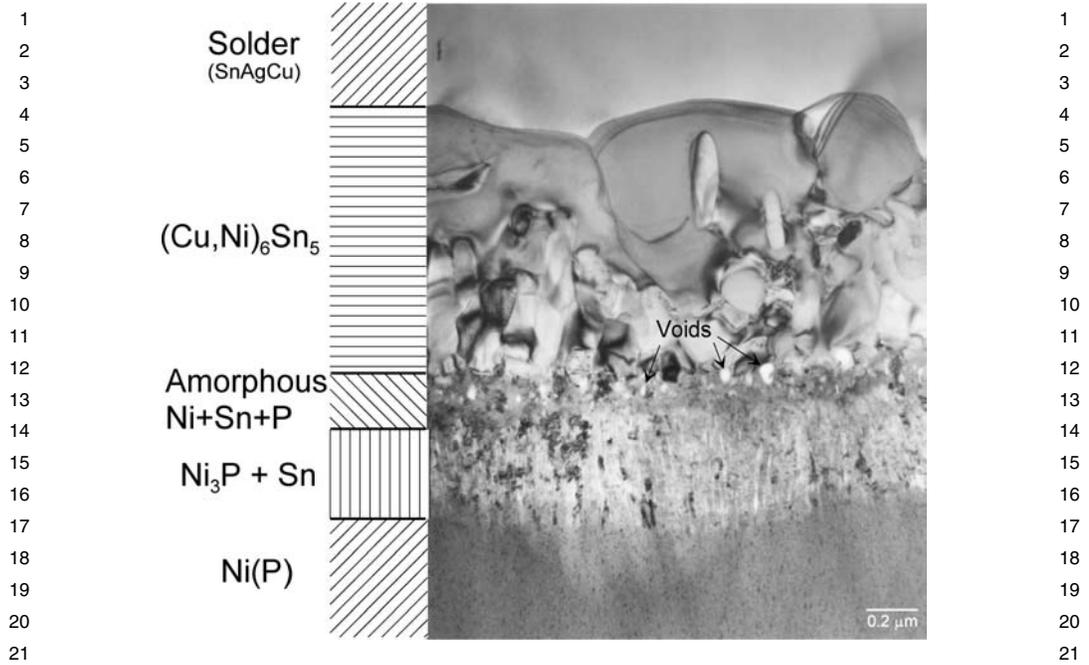


FIGURE 9.28. Transmission electron micrograph from the interfacial reaction layer in the interconnections on the Ni(P)Au metalization.

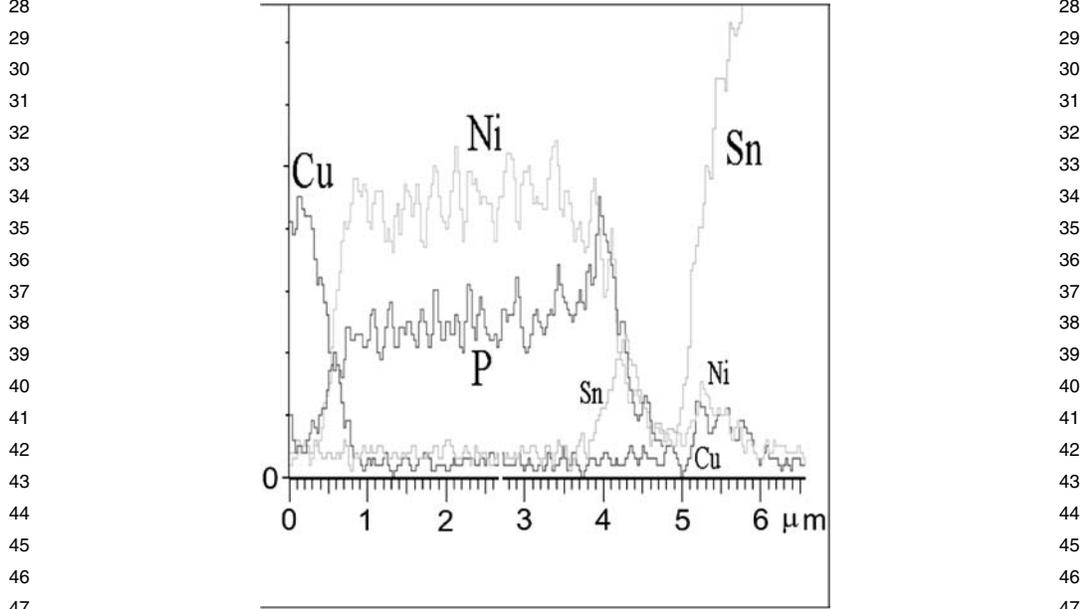


FIGURE 9.29. An energy dispersive X-ray line scan perpendicular to the fracture path.

1 phase formed next to the Ni(P) metalization is a two phase layer composed of Ni₃P and Sn. 1
2 This is a columnar layer where Sn can be found in between the Ni₃P columns. The crys- 2
3 talline nickel-phosphate contains more P than the initial electroless Ni(P). On top of that, 3
4 a thin nanocrystalline layer containing Ni, Sn, and P has been identified. The formation of 4
5 this complex reaction structure has been discussed in more detail elsewhere [60]. Micro- 5
6 graph in Figure 9.28, taken with transmission electron microscope, shows the structure of 6
7 the intermetallic layer. 7

8 Figure 9.29 shows an EDS line analysis perpendicular to the fracture path. The frac- 8
9 ture is located relative to the graphs where all the concentrations decrease considerably 9
10 (between about 4.5–5μm on the abscissa). To the left, where the amount of Ni and P in- 10
11 crease, are the PWB solder pad metalization and to the right, where the Sn concentration 11
12 increases steeply, is the solder interconnection. Relative to the fracture path layers contain 12
13 Ni, Sn and P on the board side of the fracture and Cu, Ni and Sn on the solder side. This 13
14 indicates that the fracture propagates somewhere between the (Cu,Ni)₆Sn₅ and the Ni pad 14
15 metalizations most probably in the nanocrystalline ternary phosphide layer. This type of 15
16 fracture is very common for the Ni(P)|Au. Since the stresses experienced at the PWB side 16
17 are only about half of the stresses at the component side, the fact that failure in Ni(P)|Au 17
18 cases still occurs at the PWB interface shows how strongly the phosphorus influences the 18
19 reliability. 19
20

21 9.5. SUMMARY 21

22 The ongoing trend towards ever smaller electronic products force to larger scales 22
23 of integration and to the use of smaller and finer pitch components, such as (wafer-level) 23
24 chip scale packages and flip chips. Because of the small-scale interconnections compo- 24
25 nents become closer to the printed wiring boards and subsequently the strains and stresses 25
26 experienced by solder interconnections are increased. These miniaturized interconnections 26
27 must be able to withstand sudden mechanical and thermomechanical shock loadings, local 27
28 heating of power components, and varying chemical environments. 28
29

30 Lead-free solder interconnections contain more complex intermaterial layers, which 30
31 weaken the bonding of the solder filler to boards' and components' terminations. Because 31
32 the microstructures of solder interconnections ultimately control the reliability performance 32
33 of soldered assemblies a more fundamental understanding of their formation and evolution 33
34 is needed to ensure the best possible reliability. The above-described development increases 34
35 also the importance of testing. Because testing is time consuming and expensive, all solu- 35
36 tions that can control and limit required testing time are valuable. Simulation tools can be 36
37 used to reduce unnecessary testing. However, because simulation always requires experi- 37
38 mental work to verify the results, the above-mentioned approach must be combined with 38
39 carefully executed experimental investigations. 39
40

41 Hence, understanding why the different tests yield different failure mechanisms and 41
42 ultimately different reliability performance is of utmost importance. This can only be 42
43 achieved by knowing how the stress states produced, how the materials respond to dif- 43
44 ferent types of loading, and how the microstructures of solder interconnections affect the 44
45 failure mechanisms. Therefore the emphasis in this chapter is on microstructures of sol- 45
46 der interconnections: solidification, interfacial reactions and evolution of microstructure 46
47 are central themes. An approach to study reliability of electronic is introduced. The ap- 47
48 proach presented consists of simulation, reliability testing, statistical analysis of the test 48
49

1 results, and experimental failure analysis. Furthermore, two cases of accelerated testing 1
2 (thermal cycling and drop tests) are analyzed in the form of case examples. The reasons 2
3 for the marked differences in failure mechanisms are rationalized with the help of material 3
4 scientific considerations. Failure mechanism under thermomechanical loading was found 4
5 out to be entirely different from that under drop testing. Under thermomechanical loading 5
6 nucleation and propagation of cracks is controlled by the microstructures formed during 6
7 soldering and their recrystallization behavior during use. Grain boundaries created by re- 7
8 crystallization enable cracks to propagate intergranularly in bulk solder. On the other hand, 8
9 mechanical shock impacts caused entirely different kinds of failure modes. Cracks in the 9
10 newly soldered interconnections did not propagate through the bulk solder of the intercon- 10
11 nections, but mainly in the brittle intermetallic compound layers between the bulk solder 11
12 and contact metalizations. This is primarily due to the fact that under very fast loading the 12
13 ultimate tensile strength of Sn-rich solders is strongly increased because of strain-rate hard- 13
14 ening, and therefore the stresses in the solder interconnections grow very rapidly above the 14
15 fracture strength of the intermetallic compound layers leading to intermetallic fracture. 15
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18 ACKNOWLEDGMENTS 18

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23

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