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MODULAR INTEGRATION OF CMOS AND SOI-MEMS USING "PLUG-UP" CONCEPT

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ABSTRACT

This paper reports a novel method for monolithic integration of electronics with micromechanical devices. The fabrication sequence differs from those previously described. Even though some of the elements of CMOS and MEMS fabrication are intermixed and make use of each other, they still are modular packages, which can be sequentially fabricated in separate specialized factories if both of the technologies are not available at one site. Standard or tailored SOI wafers can be used for the substrate material. Vacuum cavities are then made at predetermined regions of the buried oxide using a special technique, "Plug-up" [1]. We have demonstrated that cavity wafers of this kind can progress through the entire bipolar enhanced CMOS cycle without complications. In the end, MOS and bipolar transistors operate almost identically to reference devices on bulk silicon wafers and MEMS membranes resonate mechanically as anticipated. The proposed modular process sequence is tabulated in Fig. 1.

INTRODUCTION

Micromachined vacuum shells [2] have been studied for improving Q-values of resonators, for hermetical sealing of devices, or for realizing capacitive micromachined ultrasonic transducers [3]. The plug-up concept we have developed combines deep reactive ion etching (DRIE) of silicon [4] and SOI micromachining [5] with semipermeable polysilicon technology [2,3,6] providing a robust starting material for integrated MEMS.

There are other ways of forming buried cavities within SOI described in literature [7]. Usually they are based on making recesses on one of the wafers prior to bonding.

This approach suffers from non-uniform membrane thickness, loss of alignment marks in wafer thinning, and need for intimate discussion between wafer manufacturer and device designer.

There are some process descriptions of integrated MEMS in the literature[8,9]. Usually they suffer from compromises made between the two technologies: polysilicon MEMS is difficult to prepare over the IC, or the IC must be fabricated after making complex embedded polysilicon structures. In either case device properties are compromised or expensive process technology is needed. In our modular approach, however, there is a synergy between MEMS and IC, both MEMS and IC are made of the same material and, for example, MEMS isolation can be used also for reduction of transistor paracitic capacitances and the metallization structures are common for both.

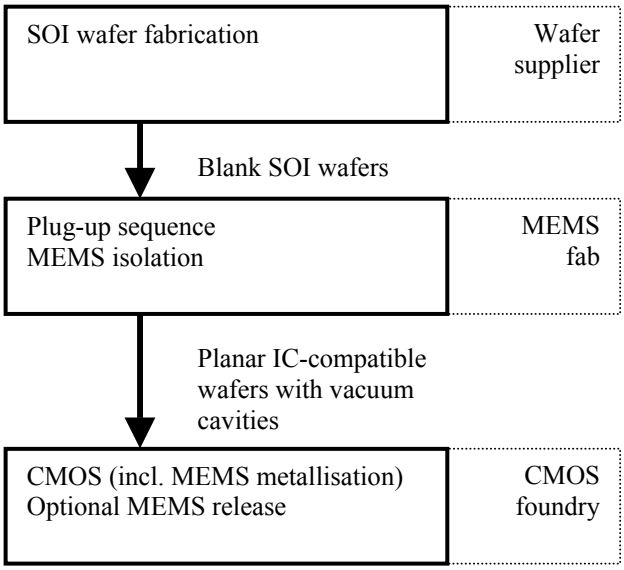

Figure 1. Simplified example of modular process flow and interfaces between fabrication sites.

SAMPLE FABRICATION

Bonded silicon on inslulator (SOI) wafers are used as starting material. The handle wafer is heavily doped p-type silicon and the resistivity of the p-type structure layer is around 10 Ωcm to accommodate conventional CMOS. Structure layer and buried oxide thicknesses are 8 μm and 1 μm, respectively. The wafer processing is mostly done at VTT Information Technology facilities.

The vacuum cavities (schematically shown in Fig. 2.) are fabricated using Plug-up sequence[1] as follows:

1. An etch-stop layer is deposited on SOI wafers.
2. An array of approximately micron-sized openings is etched through the device layer of SOI with slight overetching into the buried oxide to form antistiction bumps.
3. Semipermeable polysilicon is deposited in such a way that pinholes remain at the bottom of each well.
4. Buried oxide is locally removed through pinholes and dried with super critical carbon dioxide.
5. The wells are plugged up with conformal layer of LPCVD polysilicon film deposited at 150 mTorr. The cavities remain in vacuum.
6. After etchback, the IC-compatible, single crystal silicon surface is revealed.

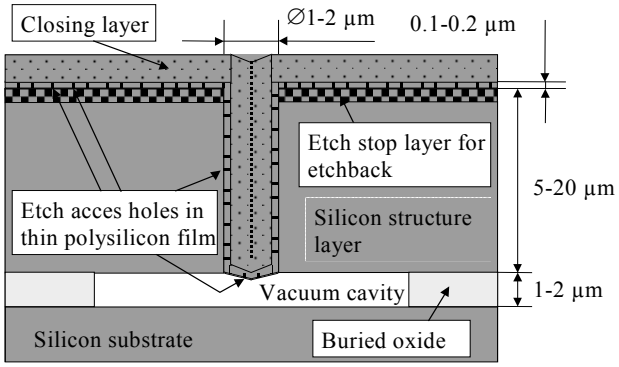

Figure 2. Schematic cross-section of a plugged-up SOI cavity before etchback with typical dimensions.

Besides the active cavities for microelectromechanical devices substrate contacts and isolation trenches are generally needed. The shematical cross-section of these sub-modules is shown in Fig. 3. In this study the integrated substrate contacts were omitted and contacts were made externally after dicing. In the future runs in-situ doped polysilicon will be used for substrate contacts. The DRIE etched isolation trenches are refilled with oxide after cavity formation, just before the formation of CMOS wells. During the cavity formation the area designated for CMOS is protected by a stack of selected thin films. The level of metallic impurity caused by the cavity forming process remained at an acceptable level which was verified by total reflection X-ray fluorescence (TXRF) measurement of test samples after deep silicon etching and super-critical carbon dioxide drying.

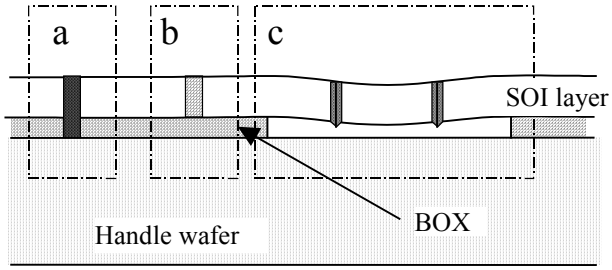

Figure 3. Breakdown of MEMS parts, a) electrical substrate contact through SOI buried oxide, b) trench isolation, c) vacuum cavity.

The top view infrared photograph of cavity test structures in shown in Fig. 4. The dark center of the hexagons indicates that the silicon membrane above the cavity is deflected by the atmospheric pressure. The light separated spots are small cavities formed from individual access holes which have not yet merged to form a continuos cavity.

The integrated circuit process selected for this demonstration is a 1 µm gate length bipolar enhanced CMOS. The BeCMOS process is optimised for analog and mixed-signal circuits. It uses a p-type substrate with triple well. Besides the standard n- and p-wells the process has a deep n-well with a shallow p-well inside it. This structure is used for isolating analog NMOS transistors and vertical pnp transistors. An extra well was added to the MEMS region to enhance the conductivity of the structure layer. The higher doping level is needed to reduce the temperature and voltage sensitivity of the anchor area of MEMS devices. Tailoring of the stucture layer doping profile by blanket implantation before wafer bonding is also an alternative to make the top electrode more conductive.

The bipolar transistors are processed before the CMOS gate process. Both npn and pnp transistors have conventional triple diffused structure with implanted emitters. CMOS portion of the process uses self-aligned molybdenum gate with 20 nm gate oxide. Molybdenum gate metal is used also as a bottom electrode for metal-insulator-metal capacitors. Stacked floating gate MOS transistors with capacitively connected control electrodes are used as EEPROM memory cells. The key properties of the processed circuit elements are tabulated in the Table 1. Most of the circuit elements are modular and they can be omitted from the fabrication process if so desired. The high voltage NMOS is an important option if electrostatic drive of capacitive elements is required.

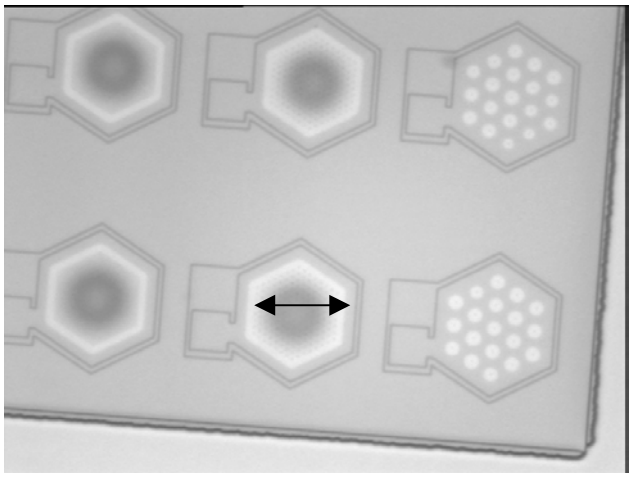

Figure 4. Near infrared photograph of hexagonal MEMS cavities with varying perforations. The marker is about 300 µm long.

RESULTS AND DISCUSSION

Modular integration using the plug-up process was demonstrated in practice. The processed NMOS, PMOS, npn, and pnp operate similarly to reference devices on plain silicon wafers. The leakage currents remained practically unaltered. The membranes within the MEMS regions are deflected downwards by ambient pressure as was verified by profilometry and near infrared microscopy. They also resonate at the expected frequency and with the expected mechanical quality factor, which proves the ability to release structures to withstand the CMOS cycle. The CV-measurement result in Fig. 5

Element	Notes
NMOS	VTH = +0.60, molybdenum gate
PMOS	VTH = -0.65, molybdenum gate
isolated NMOS	VTH = +0.60, with deep n-well isolation
vertical npn	HFE ~ 100, VA ~100
vertical pnp	HFE ~ 30, VA~50, with deep n-well isolation
EEPROM memory cells	floating NMOS/PMOS and capacitor nitride
High voltage NMOS	Breakdown voltage 40 Volt
Thin film capacitor	Metal-insulator-metal, 2 nF/(mm)^2
Thin film resistor	10 kOhm/sqr, TCR < 100 ppm/°C

Table 1. List of processed circuit elements of the modular BeCMOS

shows well behaving capacitance voltage characteristic. The apparent asymmetry is a measurement artefact of a wafer level capacitance measurement. The temperature sensitivity of the resonance frequency of the silicon membrane is governed by the temperature sensitivity of Young´s modulus of silicon. Fig. 6. shows the typical spring softening effect when the dc-bias on the resonator is increased. The approximate Q-value of such a resonator is in the range of hundreds when operated in atmospheric pressure. In vacuum the Q-value is about 1000. The mechanical losses are due to energy leakage at the edge of the device where the membrane is connected to the surroundings.

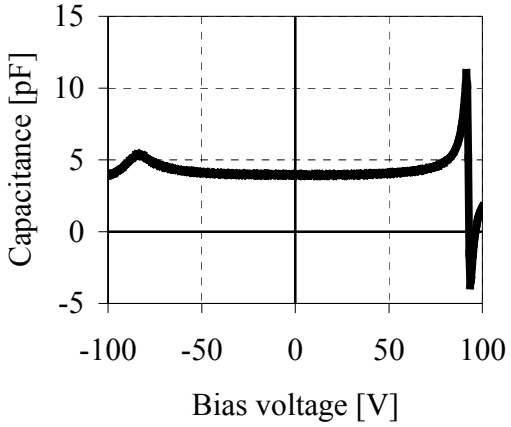

Figure 5. CV-measurement of a fabricated cavity. Mechanical resonance occurs at ± 85 V when measured at fixed 1 MHz frequency of the capacitance bridge.

Comparison of the electrical performance of SOI device with MEMS process and bulk device is shown in Fig. 7. It shows the drain leakage current in high voltage NMOS transistor with gate connected to ground. Below the breakdown voltage the current levels are the same, so the MEMS process has no adverse effecton the IC process.

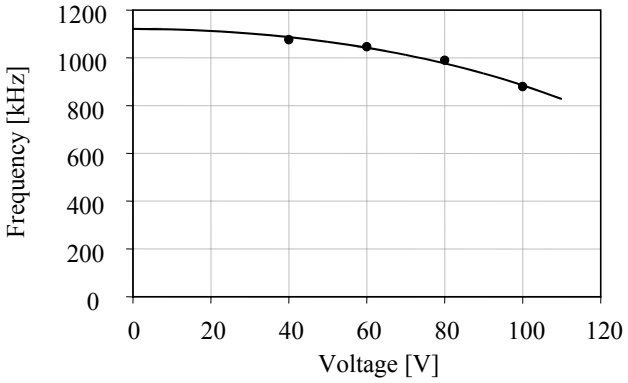

Figure 6. Resonance frequency of a hexagonal cavity resonator as a function of dc-bias voltage showing typical spring softening effect.

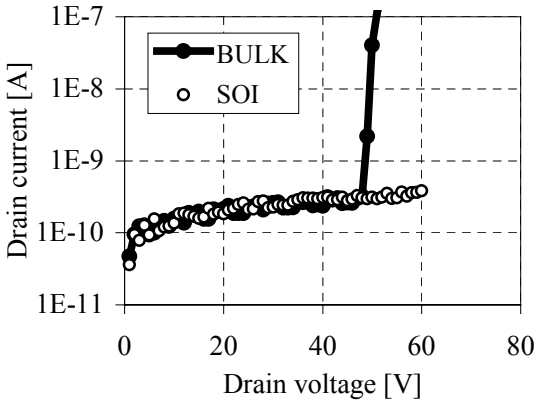

Figure 7. Drain leakage current in bulk and SOI (with MEMS) circular (outside diameter 30 μm) high voltage NMOS transistors with gate dimensions of W=27 μm and L=2.4 μm.

CONCLUSIONS

The complete analog BeCMOS was successfully processed on wafers having preprocesssed plug-up vacuum cavities. The cavity formation by plug-up sequence was shown to be CMOS compatible though effort is still needed in development of the sacrificial

etching and the super-critical carbon dioxide drying procedures.
The key advantage of the plug-up sequence is the fact, that sacrificial oxide etching using HF is done prior to all metallisation steps or gate dielectric growth. Inside of a closed cavity is clean and hermetically sealed.
This method of MEMS/CMOS integration enables modular fabrication of MEMS systems and it can act as a versatile process platform for a vast range of applications.

Acknowledgements

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References

[1] J. Kiihamäki et. al. "Plug-Up – A new concept for fabricating SOI/MEMS devices" DTIP 2003 conference.

[2] K.S. Lebouitz, et. al."Permeable Polysilicon Etch-access Windows For Microshell Fabrication", Tranducers´ 95 and Eurosensors IX, June 25-29, 1995, Vol. 1, pp. 224-227.

[3]. J. Saarilahti, M. Blomberg, A. Häärä, H. Kattelus: "A novel method for processing capacitive micromechanical ultrasonic transducers (cMUT)" to be published in Proceedings of IEEE Ultrasonics Symposium 2002.

[4] J.K. Bhardwaj, H. Ashraf, "Advanced silicon etching using high density plasma" Proc. SPIE Vol. 2639, 224 (1995).

[5] E. H. Klaassen,et. al., “Silicon Fusion Bonding And Deep Reactive Etching: A New Technology For Microstructures”, Proc Transducers’95, Stockholm, Sweden, June 1995, 556, Sensors and Actuators A 52 (1996); 132-139.

[6] Y. Kageyama, T. Tsuchiya, H. Funabashi, J. Sakata "Polycrystalline silicon thin films with hydrofluoric acid permeability for underlying oxide etching and vacuum encapsulation", J. Vac. Sci. Tech. A, vol. 18, No. 4 (2000) 1853-1858.

[7] A. Prochaska, P. Baine, S. J. N. Mitchell, H. S. Gamble, "Production of Silicon Diaphragms by Precision Grinding", Proc. SPIE, vol. 4174, (2000) 244-255.

[8] Yasaitis et. al. "A modular process for integrating thick polysilicon MEMS devices with sub-micron CMOS" Proc. SPIE, Vol. 4979 (2003) 145-154.

[9] R. Aigner, K-G. Oppermann, H. Kapels, S. Kolb, ""Cavity-Micromachining" Technology: Zero-Package Solution for Inertial Sensors", Proc. 11th Int. Conf. On Solid-state Sensors and Actuators, Munchen, Germany, June 10-14, 2001, vol.1., pp.186-189.