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A Gain Stabilization Technique for Tuned RF Low-Noise Amplifiers

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***Abstract*—A gain stabilization technique for tuned integrated low-noise amplifiers (LNAs) is presented. The proposed method regulates the *LC*-tuned load impedance of the amplifier at the operation frequency against variations of passive devices in integrated circuit (IC) process. The impedance stabilization technique is based on the excellent relative accuracy of integrated resistors. Although the absolute deviation of the integrated resistors can be as large as $\pm 20\%$, the relative deviation can be made smaller than $\pm 1\%$ provided that resistors are placed close to each other. By applying the proposed method, the voltage-gain variation of the inductively degenerated common-source LNA, which is the most popular LNA architecture, can be reduced several decibels. As a consequence, the entire radio receiver can more easily meet its specifications in the presence of IC process variations and the product yield is improved. Finally, besides the LNAs, the presented stabilization technique can also be utilized in other tuned amplifiers, filters or oscillators employing damped *LC*-tuned loads.**

***Index Terms*—Gain stabilization, low-noise amplifier (LNA), process variations, RF.**

I. Introduction

IN MODERN cellular wireless receivers, zero or low intermediate-frequency (IF) receiver architectures have become very popular [1]–[7], because in these architectures a very high level of integration can be obtained. As a consequence, a low material or component cost can be obtained. Moreover, typically, in these receiver topologies, no image filter between the low-noise amplifier (LNA) and quadrature mixers is required, and the LNA can drive the mixers directly on chip. This results also in low power consumption, because no power is wasted in buffering high-frequency signals off-chip. Moreover, the impedance level between the LNA and mixers can be set and optimized freely, which is a clear advantage in the whole RF front-end performance optimization.

In mass product applications, the radio receiver must meet its dynamic range specifications both in the nominal conditions and also in the presence of supply voltage, temperature, and process variations. Otherwise, the product yield is degraded. The lower and upper ends of the dynamic range of the radio receiver are set by the noise and intermodulation characteristics, respectively. In particular, the noise figure (NF) and input-referred third-order intercept point (IIP3) for the direct conversion presented in Fig. 1 are given as [12], [14]

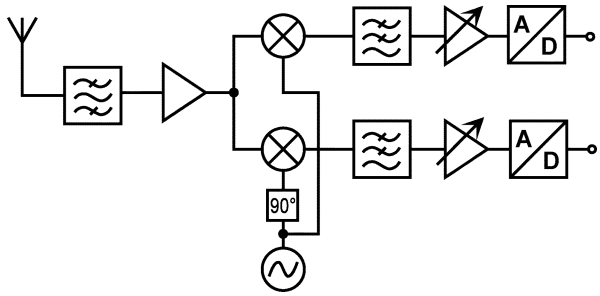

Fig. 1. Block diagram of direct conversion receiver architecture.

$$\mathrm{NF} = \mathrm{NF}_1 + \frac{\mathrm{NF}_2 - 1}{G_{a1}} + \frac{\mathrm{NF}_3 - 1}{G_{a1}G_{a2}} + \dots \quad (1)$$

$$\frac{1}{\mathrm{IIP3}} \approx \frac{1}{\mathrm{IIP3}_1} + \frac{G_{a1}}{\mathrm{IIP3}_2} + \frac{G_{a1}G_{a2}}{\mathrm{IIP3}_3} \dots \quad (2)$$

respectively. Here, NF_1, $\mathrm{IIP3}_1$, and G_{a1} are NF, IIP3, and available power gain of the LNA, respectively. Correspondingly, NF_n, $\mathrm{IIP3}_n$, and G_{an} are NF, IIP3 and available power gain of the nth block.

Equations (1) and (2) reveal the reason why it is important to stabilize the gain of the LNA. For instance, consider the case, in which the gain of the unstabilized LNA is, for some reason, smaller than in the nominal condition. Then, according to (1), the noise contributions of the following stages are suppressed less than in nominal condition and the entire receiver may fail to meet its sensitivity requirements. On the other hand, if the gain is too large in some process corner, IIP3 given by (2) is degraded and the receiver may fail to meet its intermodulation specifications. Thus, in order to maximize the yield of the receiver IC, it is very important to stabilize the gain of the LNA.

Although most of the reported wireless receivers use the inductively degenerated common-source (or common-emitter) LNA architecture shown Fig. 2(b) [1], [3]–[7], its gain stabilization techniques have not been fully examined. Biasing techniques like constant-transconductance (g_m) circuits [8] [or proportional-to-absolute temperature (PTAT) circuits [9] in the case of bipolar LNA circuits], which stabilize the LNA input device g_m against supply, temperature, and process variations, do not fully remove the gain variations. Instead, the deviation of the passive components can result to the gain variation of several decibels and in mass product applications this is not acceptable. The gain compensation technique presented in this paper [10] reduces the LNA gain variation due to the deviation of passive devices and therefore improves the yield of the

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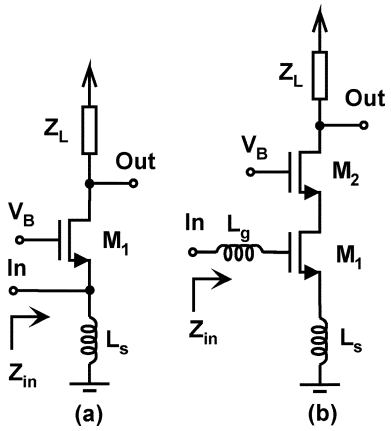

Fig. 2. (a) Common-gate LNA. (b) Inductively degenerated common-source LNA.

RFIC. Finally, the proposed technique should be used together with gain stabilization methods of active devices.

In Section II, the factors effecting to the gain stabilization of the two most popular CMOS LNA architectures, common gate and inductively-degenerated common-source amplifiers, are examined. In Section III, the drawbacks of the conventional undamped and damped *LC*-tuned loads are discussed and in Section IV, a new technique for stabilizing the damped *LC*-tuned load impedance against process variations at the operation frequency is presented. Finally, in Section V, the voltage-gain variations of the LNA using conventional and proposed damped *LC*-tuned loads are simulated and compared.

II. Gain Stabilization of Common-Gate and Inductively Degenerated Common-Source LNAs

Most of the CMOS radio receivers use either the common-gate [2], [11] or the inductively degenerated common-source LNA architectures shown in Fig. 2(a) and 2(b), respectively. Moreover, usually these topologies are realized as narrow-band circuits in order to save power and reject the out-of-band interfering signals and noise.

Typically, LNA must present a regulated input impedance (i.e. 50 Ω single ended) for the filter driving the LNA. In the case of common-gate amplifier shown in Fig. 2(a), the input impedance of the amplifier at the operation frequency f_0 can be expressed as [15]

$$Z_{\text{in}} = \frac{1}{g_m} \tag{3}$$

if

$$\omega_0^2 = \frac{1}{L_s(C_{\text{gs}} + C_p)} \tag{4}$$

Here, g_m and C_{gs} are the transconductance and gate-source capacitance of M_1, respectively, and C_p is the parasitic capacitance at the LNA input node. If the input impedance matching specifications are met, the voltage gain of the common-gate LNA at f_0 can be expressed as

$$A_v = G_m \left|Z_L(\omega_0)\right| = g_m \left|Z_L(\omega_0)\right| \tag{5}$$

where G_m is the LNA input stage transconductance (here simply g_m) and $Z_L(\omega_0)$ is the LNA load impedance at ω_0.

In order to regulate the input device g_m, the amplifier has to be biased with constant-g_m biasing technique. This regulates the LNA input impedance and input stage transconductance G_m against process, supply and temperature variations. Assume also that the constant-g_m circuit realizes g_m, which is inversely proportional to some integrated reference resistor R_{ref}. Now, if the LNA load impedance at f_0 also implemented with the same resistance material (i.e. polysilicon) as R_{ref}, the LNA voltage gain at the operation frequency is very robust against variations. As a conclusion, the gain stabilization of common-gate LNA is very straightforward.

The use of common-gate LNA is usually limited only to the applications, where the LNA NF above 3 dB is tolerable [2]. For this reason, nowadays most of the wireless receivers use the inductively degenerated common-source LNA architecture shown in Fig. 2(b). With this circuit topology, excellent input matching and NF below 3 dB can be achieved simultaneously. At the resonance frequency [14]

$$f_0 = \frac{1}{2\pi\sqrt{(L_g + L_s)C_{\text{gs}}}} \tag{6}$$

the input impedance of the LNA is purely real and can be approximated as

$$Z_{\text{in}} = r_g + \frac{g_m L_s}{C_{\text{gs}}} \approx \frac{g_m L_s}{C_{\text{gs}}}. \tag{7}$$

Again, in order to regulate the input device g_m and thus the LNA input impedance, the amplifier has to be biased with constant-g_m technique. Usually, this stabilizes the LNA input impedance [see (7)] adequately against process, supply, and temperature variations, since the other terms in (7) vary less with process than g_m. For instance, typically, the source inductance L_s is integrated, and therefore, its performance depends mainly on the device geometry, which is considered to be relatively constant from die sample to another.

At the operation frequency f_0, the transconductance of the LNA input stage is given as [14]

$$G_m = \frac{1}{\omega_0 L_s} \tag{8}$$

and then, the LNA voltage gain is simply given as

$$A_v = G_m \left|Z_L(\omega_0)\right| = \frac{\left|Z_L(\omega_0)\right|}{\omega_0 L_s} \tag{9}$$

where $Z_L(\omega_0)$ is the LNA load impedance at ω_0.

It should be noticed that if the input impedance matching conditions [see (6), (7)] are met, the LNA transconductance, given by (8), is relatively constant at the given resonance frequency f_0, since it depends only on L_s. For the same reason, the LNA voltage gain, given by (9), varies mainly along the LNA load impedance at the given frequency f_0. As a conclusion, in order to stabilize the LNA voltage gain at the operation frequency, the load impedance at the operation frequency must be stabilized against variations.

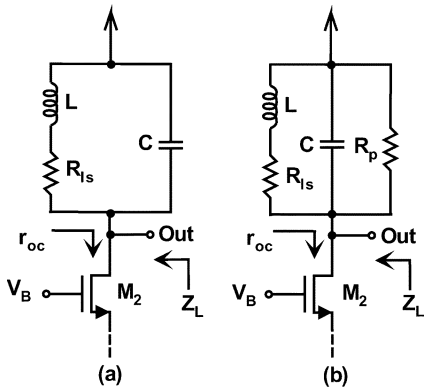

Fig. 3. Conventional parallel *LC* resonator circuits used as LNA loads. (a) Undamped *LC*-tuned load. (b) Damped *LC*-tuned load.

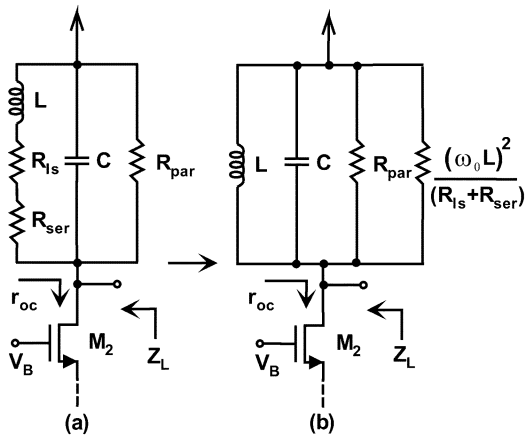

Fig. 4. Proposed parallel damped *LC* resonator circuit used as LNA load.

III. Conventional Undamped and Damped *LC*-Tuned Loads

Most of the LNAs use an *LC* resonator load to peek the gain of the amplifier at the frequency of interest and to reject the out-of-band interfering signals. A typical parallel *LC* load used in narrow-band tuned amplifiers is shown in Fig. 3(a) [1], [2], [4]–[7], [11]. Here, C includes also the input capacitances of the following $I$and Q mixers and any other parasitic capacitance presented at the LNA output node.

At the operation frequency f_0, L and C are in parallel resonance

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{10}$$

and the load impedance of the LNA is purely real [13]

$$|Z_L(\omega_0)| = R_L \approx \frac{(\omega_0 L)^2}{R_{\rm ls}} \,||r_{\rm oc} = (Q\omega_0 L)||\, r_{\rm oc} \tag{11}$$

where $R_{\rm ls}$ is the series resistance of the load inductor L, $r_{\rm oc}$ is the output impedance of the cascode amplifier, and Q is the quality (Q) factor of L. It is reasonable to assume that the Q of the whole resonator is determined by the Q factor of the integrated inductor L.

As Q factors of integrated differential inductors used in balanced LNAs are typically larger than 10, the Q of the resonator circuit shown in Fig. 3(a) is usually too high to be used as such in the LNA. That is, if the Q of the resonator is high, the bandwidth of the resonator is narrow and then, the deviation of the integrated capacitor C will spread the load resonance frequency considerably. For the same reason, the magnitude of the LNA load impedance will also vary with C at the resonance frequency. The integrated capacitors can deviate almost $\pm 20\%$ from sample to another. For this reason, an additional integrated resistance R_p is often placed in parallel with the load resonator, as shown in Fig. 3(b) [3], [16]. The shunt resistor lowers the Q of the *LC* circuit and broadens the resonator bandwidth. As a result, the magnitude of the LNA load impedance at the operation frequency varies much less with the deviation of parallel capacitance C. In addition, R_p lowers the magnitude of the LNA load impedance at the operation frequency

$$|Z_L(\omega_0)| \approx (Q\omega_0 L)||r_{\rm oc}||R_p \approx R_p \tag{12}$$

where it is assumed that, in practice, $R_p \ll r_{\rm oc}$ and $R_p \ll (Q\omega_0 L)$. Despite this, it is usually still possible to realize LNA voltage gains in the order of 20–25 dB, which are typically sufficient.

According to (12), the LNA load impedance at the resonance frequency is determined mainly by R_p. As R_p is realized as an integrated passive resistor, it can be expressed as $R_p = nR_{\rm sh}$ where $R_{\rm sh}$ is the sheet or unit resistance of the resistance material and n is the number of the sheet resistances needed to implement the desired resistance value. Moreover, as R_p is directly proportional to $R_{\rm sh}$, the LNA load impedance and also the voltage gain will deviate exactly similarly as $R_{\rm sh}$. For instance, with the tolerance of $\pm 20\%$ of integrated polysilicon resistors, the LNA voltage-gain variation due to the resistor variation only is almost $20\log 1.2 - 20\log 0.8 = 3.5$ dB. Therefore, an alternative method for reducing the Q factor of *LC*-parallel resonator must be examined in order to stabilize the LNA voltage-gain variations. It should be noticed that as the Q factor of a parallel resonator shown in Fig. 3(b) can be expressed as $Q = \omega_0 C R_p$, Q deviates exactly with the same manner as $R_{\rm sh}$.

IV. Proposed Damped *LC*-Tuned Load

A simple way of reducing the variations of the *LC* resonator Q factor with respect to the deviations of both the integrated capacitors and resistors is illustrated in Fig. 4(a). In this circuit, two resistors $R_{\rm ser}$ and $R_{\rm par}$, realized with the *same* resistance material, are used to reduce the Q of the resonator. As seen, resistor $R_{\rm ser}$ is placed in series with the inductor L, while resistor $R_{\rm par}$ is placed in parallel with the whole resonator. Moreover, $R_{\rm ser}$ and $R_{\rm par}$ can be expressed as $R_{\rm ser} = n_s R_{\rm sh}$ and $R_{\rm par} = n_p R_{\rm sh}$, respectively. To gain insight, practical design values might be $R_{\rm sh} = 100\ \Omega$, $R_{\rm ser} = 14\ \Omega$, and $R_{\rm par} = 200\ \Omega$. Moreover, it should be noticed that since both $R_{\rm ser}$ and $R_{\rm par}$ are realized with the same material, and these resistors are placed close to each other on IC, their process gradient is very similar. Thus, if the value of $R_{\rm sh}$ is for instance smaller than in nominal condition, the values of $R_{\rm ser}$ and $R_{\rm par}$ will both decrease.

To see how the circuit works, let us consider the case, in which the value of $R_{\rm sh}$ is for some reason larger than in the nominal case. Now, due to the increased $R_{\rm sh}$, the Q of the inductor L is

decreased because the value of the resistance $R_{\rm ser}$ in series with L is increased. For the same reason, the Q of the whole resonator is decreased. However, as the value of the parallel resistor $R_{\rm par}$ is increased, the Q of the whole resonator is increased. Thus, the reduction of the Q factor of L is compensated and the Q of the total resonator is left relatively unchanged. To show this analytically, $L(R_{\rm ls}+R_{\rm ser})$-series impedance is first transformed to the corresponding parallel impedance at the resonance frequency. This transformation is valid, if, for the corresponding Q factor [13]

$$\left(\frac{\omega_0 L}{R_{\rm ls}+R_{\rm ser}}\right)^2 \gg 1. \tag{13}$$

This assumption can be validated with practical design values. The resulted circuit for analyzing the load impedance Z_L is shown in Fig. 4(b). At the resonance frequency, impedance Z_L is given as

$$\begin{aligned}|Z_L(\omega_0)| &= R_L \\ &\approx \frac{(\omega_0 L)^2}{(R_{\rm ls}+R_{\rm ser})}\Big\| R_{\rm par} \\ &= \frac{R_{\rm par}(\omega_0 L)^2}{R_{\rm par}(R_{\rm ls}+R_{\rm ser})+(\omega_0 L)^2} \\ &= \frac{n_p R_{\rm sh}(\omega_0 L)^2}{n_p R_{\rm sh}(R_{\rm ls}+n_s R_{\rm sh})+(\omega_0 L)^2}.\end{aligned} \tag{14}$$

In addition

$$\frac{\partial |Z_L(\omega_0)|}{\partial R_{\rm sh}} = \frac{n_p(\omega_0 L)^2\left((\omega_0 L)^2 - n_p n_s R_{\rm sh}^2\right)}{\left(n_p R_{\rm sh}(R_{\rm ls}+n_s R_{\rm sh})+(\omega_0 L)^2\right)^2}. \tag{15}$$

From (15), it is seen that since the derivative of $|Z_L(\omega_0)|$ with respect to $R_{\rm sh}$ is not always zero regardless of the value of $R_{\rm sh}$, $|Z_L(\omega_0)|$ still varies with $R_{\rm sh}$. However, the variation is now much smaller compared to the conventional damped resonator load as will be shown. Moreover, since the Q of the resonator is usually relatively low, the deviation of the integrated capacitors leads only to a small load impedance and voltage-gain variation.

From (15), it is seen that the derivative of $|Z_L(\omega_0)|$ with respect to $R_{\rm sh}$ is zero if

$$R_{\rm sh}^2 = \frac{(\omega_0 L)^2}{n_p n_s}. \tag{16}$$

Therefore, let us select the values for n_p and n_s so that they obey the following equation

$$n_p n_s = \frac{(\omega_0 L)^2}{R_{\rm sh0}^2} \tag{17}$$

where $R_{\rm sh0}$ is the nominal value of the sheet or unit resistance. By choosing n_p and n_s this way, a given deviation (i.e $\pm 20\%$) of $R_{\rm sh}$ effects least to value of the LNA load impedance at the resonance frequency. This is because $R_{\rm sh}$ varies now in the proximity, where the derivative of $|Z_L(\omega_0)|$ with respect to $R_{\rm sh}$ is zero. Since the derivative of $|Z_L(\omega_0)|$ with respect to $R_{\rm sh}$ describes how fast $|Z_L(\omega_0)|$ varies with $R_{\rm sh}$, the variation of $|Z_L(\omega_0)|$ is its minimum in the proximity, where its derivative is zero.

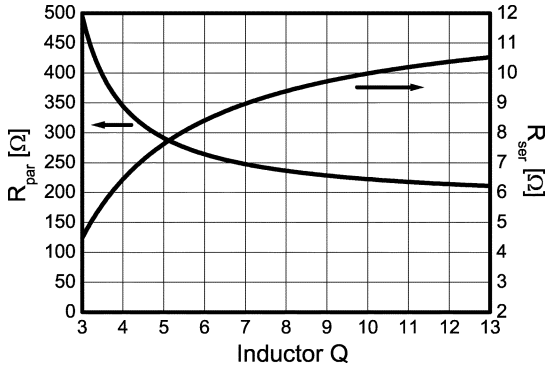

Fig. 5. Values of resistors $R_{\rm par}$ and $R_{\rm ser}$ as function of inductor Q. L = 3.75 nH, f_0 = 2 GHz, and R_L = 90 Ω.

Resistors $R_{\rm ser}$ and $R_{\rm par}$ or parameters n_s and n_p must be selected so that they realize the desired voltage gain and therefore the required parallel LNA load impedance $|Z_L(\omega_0)|$ (see (14)), and such that they obey (17). Parameters n_p and n_s can be solved from (14) and (17)

$$\begin{aligned}n_p &= \frac{R_{\rm par}}{R_{\rm sh}} \\ &= \frac{2R_L}{R_{\rm sh0}}\frac{(\omega_0 L)^2}{((\omega_0 L)^2 - R_{\rm ls}R_L)} \\ &= \frac{2R_L}{R_{\rm sh0}}\frac{Q\omega_0 L}{(Q\omega_0 L - R_L)}\end{aligned} \tag{18}$$

$$\begin{aligned}n_s &= \frac{R_{\rm ser}}{R_{\rm sh}} \\ &= \frac{1}{2R_{\rm sh0}}\left(\frac{(\omega_0 L)^2}{R_L} - R_{\rm ls}\right) \\ &= \frac{\omega_0 L}{2R_{\rm sh0}Q}\left(\frac{Q\omega_0 L}{R_L} - 1\right)\end{aligned} \tag{19}$$

where Q is the quality factor of inductor L. Since both n_p and n_s must be positive, i.e. n_p, $n_s > 0$, the inductor Q must obey the following equation in order to result realizable values for n_s and n_p

$$Q > \frac{R_L}{\omega_0 L}. \tag{20}$$

Thus, the required inductor Q depends on the desired LNA load impedance R_L and inductor impedance $\omega_0 L$ at the operation frequency.

Fig. 5 illustrates the values of $R_{\rm par}$ and $R_{\rm ser}$ given by (18) and (19), respectively, as of a function of inductor Q. It is assumed that the operation frequency is 2 GHz, L = 3.75 nH, and the desired LNA load impedance R_L is about 90 Ω. Notice that with these values, (20) requires Q of 1.9 at minimum.

From Fig. 5, it is seen that if the inductor Q is very low (i.e. in this particular case below 4), the corresponding value for the series resistor $R_{\rm ser}$ becomes impractically low. However, even with moderate values of Q, the resistors are easily realizable. Consider for instance, the case Q = 5, which requires about

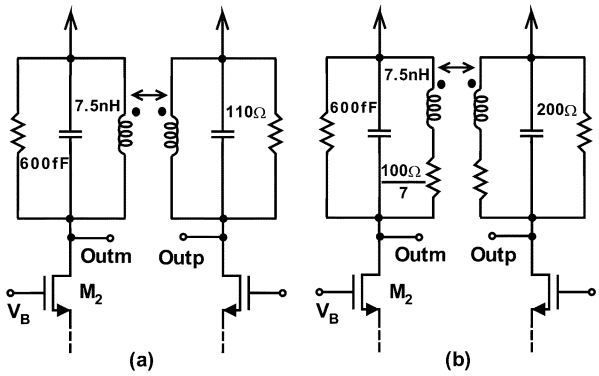

Fig. 6. Component values of a) conventional and b) proposed damped *LC* resonator circuits used as LNA loads.

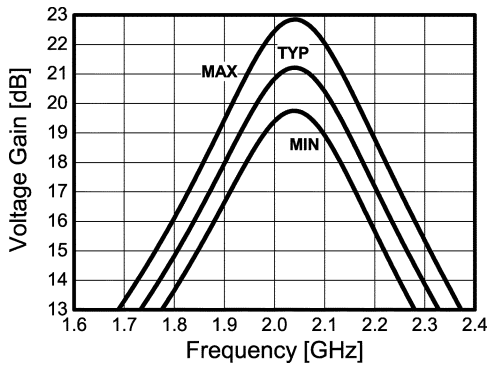

Fig. 7. LNA voltage-gain process variation due to ±20% MOM capacitor and ±13% poly resistor deviations in case of conventional damped *LC* load.

$R_{\rm par} = 300\ \Omega$ and $R_{\rm ser} = 8\ \Omega$. If $R_{\rm sh0} = 50\ \Omega$, $R_{\rm par}$ and $R_{\rm ser}$ can be implemented with six resistors in series ($n_p = 6$) and parallel ($n_s = 0.16 \approx 1/6$), respectively.

V. Process Variations of Conventional and Proposed Damped *LC*-Tuned Loads

Here, the design procedure of the *LC*-tuned LNA load impedance is demonstrated. In addition, the voltage-gain process variations of the conventional and proposed resonator circuits are simulated and compared. The LNA itself is based on the inductively degenerated common-source LNA as shown in Fig. 2(b). The amplifier operates at 2 GHz and it is implemented in 0.13-μm CMOS technology. In this technology, the deviations of the integrated metal-oxide-metal (MOM) capacitors and polysilicon resistors are about ±20% and ±13%, respectively. In order to reject the interference from substrate or supply, LNA is realized as a balanced circuit. LNA drives direct conversion I and Q mixers directly on chip.

Typically, the input stage of the LNA shown in Fig. 2(b) is designed for low noise and acceptable linearity. Moreover, the amplifier must present a regulated input impedance for the filter driving the LNA. Usually, these specifications largely determine the properties of the LNA input stage and therefore the amplifier input stage transconductance given by (8). Thus, the LNA voltage gain at the operation frequency is set to desired value by designing the load impedance accordingly. Here, it is assumed that the LNA should provide about 21 dB voltage gain at 2 GHz.

A. Conventional Damped LC Load

The design of the conventional damped *LC* load presented in Fig. 3(b) is straightforward, since there are only three parameters C, L, and R_p that need to be determined. First, L and C must resonate at 2 GHz. Here, differential inductor of 7.5 nH having Q of 11 at 2 GHz is used as shown in Fig. 6(a). This requires parallel MOM capacitance of 600 fF with parasitics to peek the gain of the amplifier at 2 GHz. Finally, parallel resistors of 110 Ω set the LNA gain to 21 dB.

The simulated LNA voltage-gain process variation due to the MOM capacitance and poly resistor deviations is presented in Fig. 7. The total LNA load impedance and voltage-gain variation is about 3.1 dB. Most of this (2.1 dB) is due to the ±13% poly sheet resistance deviation. Since the Q of the load resonator is low, the ±20% deviation of the MOM capacitors leads only to the 1-dB voltage-gain variation.

B. Proposed Damped LC Load

The design of the proposed *LC* load presented in Fig. 4(a) requires few more steps than the design of conventional resonator, since there are now five parameters C, L, $R_{\rm sh}$, n_s, and n_p that need to be determined. First, L and C must resonate at 2 GHz. Moreover, the inductor Q must be sufficiently large to ensure that the condition given by (20) is satisfied. Otherwise, the gain regulation method does not work. Since the Q of the integrated inductor at certain frequency typically increases with increasing the inductance of the inductor, it is essential to use large enough inductance for L. Here, the differential inductor of 7.5 nH having Q of 11 at 2 GHz is used as shown in Fig. 6(b). This requires parallel MOM capacitance of 600 fF with parasitics to peek the gain of the amplifier at 2 GHz.

From the design of the conventional *LC* load [see Fig. 6(a)], we know that in order to set the LNA gain to 21 dB, the LNA load impedance of $R_L = (110\ \Omega)||(11 \cdot 2\pi \cdot 2\ \text{GHz} \cdot 3.75\ \text{nH}) \approx 90\ \Omega$ at the resonance frequency is needed. Moreover, let us select the unit resistor $R_{\rm sh0}$ as 100 Ω. Then, n_p and n_s can be computed from (18) and (19), respectively. In this case, $n_p \approx 2.2$ and $n_s \approx 0.1$. Now, the values of the resistors $R_{\rm par}$ and $R_{\rm ser}$ are given as $R_{\rm par} = 2.2 \cdot 100\ \Omega \approx 2 \cdot 100\ \Omega$ and $R_{\rm ser} = 100\ \Omega/10$. It should be noticed that $R_{\rm ser}$ and $R_{\rm par}$ must be implemented with multiple units of resistors $R_{\rm sh} = 100\ \Omega$ in order to minimize their relative deviation. Calculated values for $R_{\rm ser}$ and $R_{\rm par}$ can be used for the initial design of the *LC* resonator. Further simulations indicate that the value of 200 Ω is optimal for $R_{\rm par}$, but $100\ \Omega/7$ is better for $R_{\rm ser}$ than $100\ \Omega/10$. The final component values for the resonator are summarized in Fig. 6(b).

The simulated LNA voltage-gain process variation, in the case of the compensated *LC* load, due to the MOM capacitance and poly resistor deviations is presented in Fig. 8. The total LNA load impedance and voltage-gain variation is only 0.7 dB compared to the 3.1 dB in the case of conventional damped load. Again, since the Q of the load resonator is low, the ±20% variation of the capacitors leads only to the 0.4 dB voltage-gain variation. Finally, the poly sheet resistance deviation of ±13% leads only to 0.3 dB variation in the gain, compared to the 2.1 dB in the case of simple *LC* load. The difference is even larger, if the sheet resistance of the resistor material deviates more than ±13%.

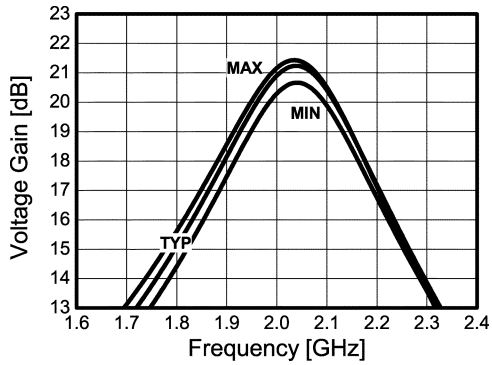

Fig. 8. LNA voltage-gain process variation due to $\pm 20\%$ MOM capacitor and $\pm 13\%$ poly resistor deviations in case of proposed damped *LC* load.

Therefore, the proposed resonator circuit greatly reduces the LNA load impedance and voltage-gain variations.

VI. Conclusion

In this paper, a gain stabilization technique for tuned integrated LNAs is presented. The proposed technique regulates the *LC*-tuned load impedance of the LNA at the resonance frequency against deviations of passive devices. The impedance stabilization technique relies on the excellent relative accuracy of integrated resistors. By applying the proposed method, the voltage-gain variation of the inductively degenerated common-source LNA can be reduced several decibels compared to the conventional resonator techniques. Although the results presented in this paper are for the CMOS LNAs, the same gain regulation technique can be used also for the bipolar or GaAs LNAs. Finally, by regulating the LNA gain, the whole radio receiver can more easily meet its specifications in the presence of IC process variations. As a result, the product yield is improved.

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