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Analysis and Optimization of Packaged Inductively Degenerated Common-Source Low-Noise Amplifiers With ESD Protection

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***Abstract*—The effects of packaging in inductively degenerated common-source low-noise amplifiers (LNAs) with electrostatic discharge (ESD) protection are studied and the performance of the packaged LNA is optimized. Equations describing the input impedance, transconductance, voltage gain, and noise figure (NF) of the packaged amplifier are derived and the effects of the LNA input matching network, package, and ESD parasitics on these amplifier quantities are highlighted. From the equations, several design guidelines for the packaged LNA are obtained and a systematic approach for the ESD-protected LNA optimization is deduced. It is also shown that, in the presence of an equivalent parallel package parasitic capacitance C_p, the NF in a well-optimized LNA is easily dominated by the losses of the input-matching network instead of the active device noise. Based on the theoretical results, a packaged inductively degenerated common-source LNA with ESD protection is designed in a 0.13-μm CMOS process. The amplifier provides a forward gain (S_{21}) of almost 18 dB at 2 GHz with an NF of 1.6 dB while consuming 8.4 mW from a 1.2-V supply.**

***Index Terms*—CMOS, electrostatic discharge (ESD) parasitics, low-noise amplifier (LNA), packaging effects, RF.**

I. Introduction

IN CONSUMER electronics applications, the integrated circuits (ICs) are almost always mounted in a package and electrostatic discharge (ESD) protection structures are required for reliability reasons. At RF frequencies, the package and ESD parasitics can have a significant effect on the circuit performance and they must be carefully taken into account in the circuit design. For the circuit simulations, accurate models for the parasitics are preferred, but analytical models are essential to develop guidelines for the circuit design and optimization.

In typical direct-conversion or low-IF receivers with an on-chip voltage-controlled oscillator (VCO) [1]–[3], the only RF off-chip interface is the low-noise amplifier (LNA) input. Thus, the package and ESD parasitics have an effect on the receiver performance only via the LNA input, assuming that a balanced LNA topology is used. Nonideal ground and supply pins have a significant effect only on the common-mode signals.

In this paper, the effects of packaging, parasitics of ESD protection structures, and the input impedance matching network on the performance of inductively degenerated common-source LNA shown in Fig. 1(a) are studied and the performance of the packaged LNA is optimized. Although most of the reported wireless receivers use this LNA architecture and the optimization of this topology has been extensively examined in the literature, the effects of the package and ESD parasitics are often, for simplicity, neglected in the analysis [4]–[8]. On the other hand, in most of the published studies, in which the effects of the package parasitics and ESD structures are considered, the LNA input impedance is assumed to be matched by employing only a series gate or base inductance [9]–[11]. Unfortunately, in the analysis of the package parasitics, this possesses a very restrictive constraint on the value of the equivalent parallel package parasitic capacitance C_p [see Fig. 1(b)], which can be tolerated while still being able to match the input impedance only by series gate inductance. Namely, if C_p is sufficiently large compared to the gate–source capacitance $C_{\rm gs}$ of the LNA input device, the impedance level at the LNA input becomes too low to be matched 50 Ω only by employing a series inductance [9]–[11]. For this reason, some of the designs using only series gate inductance have selected the LNA input impedance level lower than 50 Ω (i.e., 25-Ω single-ended) [11] or have simply accepted imperfect impedance match at the LNA input [12]. However, in mass-product applications, the last approach

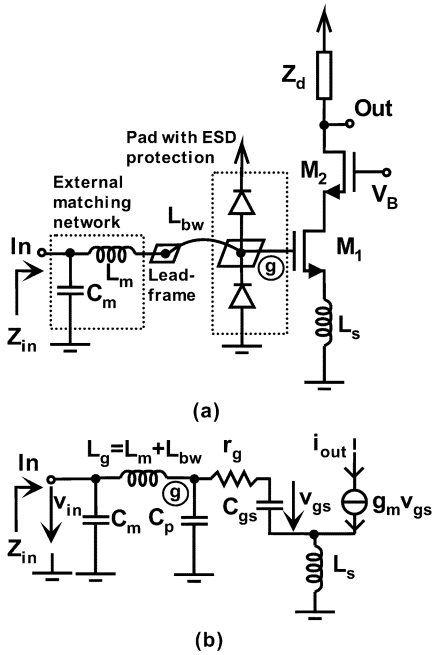

Fig. 1. (a) Single-ended equivalent circuit of packaged LNA with ESD protection. (b) Its input stage small-signal model.

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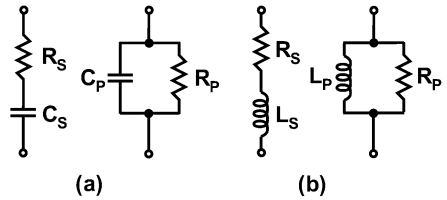

Fig. 2. Equivalent series and parallel: (a) RC and (b) RL circuits.

is not practical since the LNA must meet its input impedance-matching requirements also in the presence of process and temperature variations. If the nominal LNA S_{11} is designed to be only approximately -10 dB, the amplifier will most probably fail to meet its matching specifications in the process corners. For this reason, the equations given in this paper assume a perfect power match at the LNA input. Moreover, in this study, an LNA input-matching network consisting of two lumped elements (see Fig. 1) is considered instead of single gate series inductance. This type of matching network allows more freedom on the value of C_p since by employing two-component matching network, the impedance level at the LNA input can be more easily restored or matched to 50 Ω.

This paper is organized as follows. In Section II, the parallel-series impedance transformation technique utilized extensively in this study is revised. In Section III, the effects of the input-matching network, package, and ESD parasitics on the performance of an inductively degenerated common-source LNA are analyzed. Next, the optimization technique of the packaged LNA with ESD protection is described and an actual implementation based on the derived results is presented. Finally, the experimental results are discussed.

II. Parallel-Series Impedance-Transformation Technique

The analysis presented in this study utilizes a series of parallel-series impedance transformations at the operation frequency f_0. The parallel impedance can be replaced by a series impedance (and vice versa) if the impedances of the parallel and series versions are equal. Clearly, such a substitution cannot be valid, in general, but if the band of interest is narrow (e.g., near resonance frequency), the equivalence is reasonable [13].

The parallel-series transformation of RC circuits is illustrated in Fig. 2(a). Assuming $Q^2 = (\omega_0 C_P R_P)^2 \gg 1$, we have $C_P \approx C_S = C$ [14] and

$$R_P \approx \frac{1}{R_S(\omega_0 C)^2}. \tag{1}$$

The parallel-series transformation of RL circuits is illustrated in Fig. 2(b). In this case, the two circuits are equivalent if $Q^2 = ((\omega_0 L_S)/R_S)^2 \gg 1$ [14] and

$$R_P \approx \frac{(\omega_0 L)^2}{R_S} \tag{2}$$

where $L_P \approx L_S = L$. It is seen that in both of the RC and RL cases, the transformation keeps the values of the reactive elements C and L nearly constant.

III. LNA Analysis

The effects of the package parasitics, ESD protection diodes, and input-matching network on the LNA performance can be analyzed by considering the schematic shown in Fig. 1. Only the single-ended equivalent circuit of the packaged LNA with ESD protection is shown, but the results to be derived also apply to the balanced configuration. In actual implementation, a balanced LNA is used to reject the interference from the substrate and supply. The cascode transistor M_2 lowers the local oscillator (LO) leakage produced by the following mixer and improves the stability of the circuit. M_2 operates as a current–follower and is, therefore, neglected in the analysis. For the same reason, the output resistance $r_{\rm ds}$ of M_1 can be left out from the analysis.

As illustrated in Fig. 1, the bond pad, ESD diodes, Miller capacitance of M_1, and parasitic capacitance of bondwire introduce a parallel parasitic capacitance at the gate of the LNA input device M_1 (see node g in Fig. 1). The total parasitic capacitance can modeled as an *equivalent parallel package parasitic capacitance* C_p at the gate of M_1, as shown in Fig. 1(b), [9], [11], [12], [15], [16].

In practice, parasitic capacitance is also present in some level at the leadframe of the package. However, in this study, the leadframe capacitance $C_{\rm LF}$ is minimized by utilizing the minimum width printed circuit board (PCB) traces to route the external series inductor L_m and the leadframe, and by placing the ground layer underneath this RF trace sufficiently deep on the multilayer PCB. Thus, in this case, $C_{\rm LF} \ll C_p$ and $C_{\rm LF}$ can be neglected in the analysis.

In Fig. 1, the effects of the self-inductance of the bondwire and the inductance due to the mutual inductance between the adjacent bondwires are modeled by a series inductance $L_{\rm bw}$. Since $L_{\rm bw}$ is in series with the external matching inductor L_m, the total series gate inductance is $L_g = L_m + L_{\rm bw}$. The model for the parasitics shown in Fig. 1 can be made relatively accurate provided that the adjacent pins of RF signals are grounded or otherwise properly terminated.

In Fig. 1, L_m (or L_g) and C_m comprise an input impedance-matching network, which is required to transform upwards the equivalent impedance looking into the gate of M_1. Since the losses of this network are crucial for the LNA noise figure (NF), these components are often realized with off-chip lumped elements.

A. Input Impedance

The effects of the input-matching network, package, and ESD parasitics on the LNA input impedance can be analyzed by considering circuit shown in Fig. 3. It should be noticed that here

$$R_{\rm eq} = \frac{g_m L_s}{C_{\rm gs}} + r_g \approx \omega_T L_s \tag{3}$$

represents the real part of the LNA input impedance, which is achieved in the absence of parasitics [4] (i.e., $C_p = 0$). Moreover, in that particular case, the input-matching network is comprised only of a series inductance L_g (i.e., $C_m = 0$).

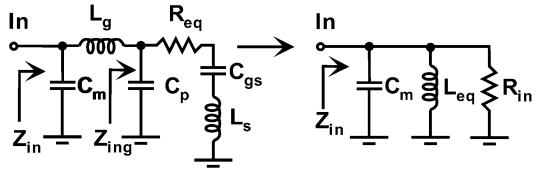

Fig. 3. LNA input impedance in the presence of parallel package parasitic capacitance C_p is analyzed by series of parallel-series conversions.

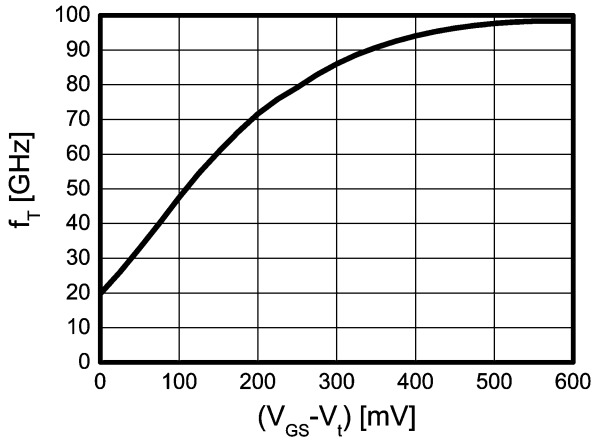

Fig. 4. Simulated unity-current gain frequency of $(\mathrm{W/L}) = (60/0.13)$ MOS device.

The unity-current gain angular frequency ω_T of the MOS transistor can be approximated as [4]

$$\omega_T \approx \frac{g_m}{C_{\mathrm{gs}}} = \frac{3}{2}\frac{\alpha\mu V_{\mathrm{eff}}}{L^2} \tag{4}$$

where $\alpha = g_m/g_{d0}$, g_{d0} is the zero bias drain conductance, μ is the electron mobility, and $V_{\mathrm{eff}} = V_{\mathrm{GS}} - V_T$ is the gate–source overdrive voltage of the MOS transistor. From (4), it is concluded that the designer can control f_T mainly via V_{GS} and channel length L.

Fig. 4 illustrates the simulated f_T of the MOS device sized as $(\mathrm{W/L}) = (60/0.13)$ as a function of V_{eff}. It is seen that for the typical overdrive voltages of 100–200 mV, f_T's in the order of 50–70 GHz are available in the applied 0.13-μm technology. In addition, since the practical values for the integrated source inductors L_s are in the order of 1–3 nH, assuming 15–25-dB LNA gain is to be implemented, the resulted values for R_{eq} are in the order of hundreds of ohms (i.e., 300–1300 Ω). These are much larger than the traditional 50 Ω considered in the older technology node 0.6 μm [4]. Finally, notice that at large V_{eff}, f_T finally saturates and ceases to increase with V_{eff}.

The parallel parasitic capacitance C_p transforms downwards the real part of the LNA input impedance. The real part of the impedance Z_{ing} looking into the gate of M_1 (see Fig. 3) at the operation frequency f_0 can be approximated by

$$\mathrm{Re}(Z_{\mathrm{ing}}) = R_{\mathrm{ing}} = \left(\frac{C_{\mathrm{gs}}}{C_p + C_{\mathrm{gs}}}\right)^2 \cdot R_{\mathrm{eq}} \tag{5}$$

where it is assumed that $\omega_0^2 C_{\mathrm{gs}} L_s \ll 1$. This assumption can easily be verified with practical design values. Thus, due to the parasitic capacitance C_p at the transistor gate, the input impedance comes down by a factor of $(C_{\mathrm{gs}}/(C_p + C_{\mathrm{gs}}))^2 \leq 1$ compared to the unpackaged LNA with given ω_T and certain size of L_s.

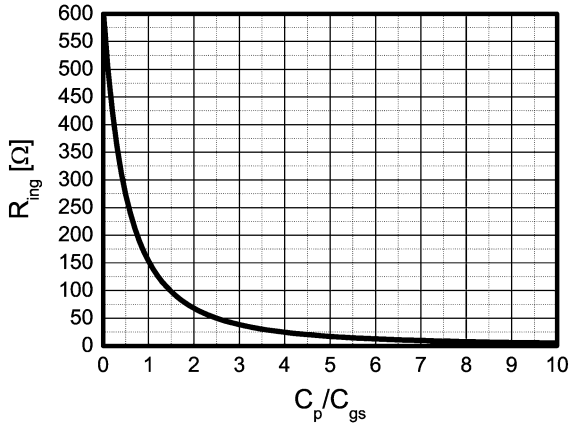

Fig. 5. Effect of package parasitic capacitance C_p on the real part of impedance Z_{ing} looking into the gate of the LNA input device M_1.

The effect of C_p on R_{ing} is illustrated graphically in Fig. 5. The component values used are $f_T = 65$ GHz, $L_s = 1.5$ nH, and $C_{\mathrm{gs}} = 100$ fF, giving $R_{\mathrm{eq}} \approx 610\ \Omega$. The values are taken from the designed LNA. As the total parallel parasitic capacitance C_p in this study is in the order of 500 fF, the resulted R_{ing} is only approximately 20 Ω. Evidently, the parallel matching capacitance C_m is needed to transform the LNA input impedance upwards to 50 Ω.

By applying a series of parallel-series conversions [16], it can be shown that the LNA input impedance at the operation frequency f_0 can be modeled as a parallel $C_m L_{\mathrm{eq}} R_{\mathrm{in}}$ impedance, as illustrated in Fig. 3. For the LNA input impedance to be purely real at the desired frequency of operation f_0 (i.e., $Z_{\mathrm{in}}(\omega_0) = R_{\mathrm{in}}$), C_m, and L_{eq} must parallel resonate at f_0

$$\omega_0^2 = \frac{1}{C_m L_{\mathrm{eq}}}. \tag{6}$$

Then

$$\begin{aligned} Z_{\mathrm{in}}(\omega_0) &= R_{\mathrm{in}} \\ &= \frac{L_{\mathrm{eq}}}{C_m}\left(\frac{C_p + C_{\mathrm{gs}}}{C_{\mathrm{gs}}}\right)^2 \cdot \frac{1}{R_{\mathrm{eq}}} \\ &= \frac{1}{(\omega_0 C_m)^2}\left(\frac{C_p + C_{\mathrm{gs}}}{C_{\mathrm{gs}}}\right)^2 \cdot \frac{1}{R_{\mathrm{eq}}} \end{aligned} \tag{7}$$

where (6) has been used. In conclusion, the value of C_m must be selected so that $R_{\mathrm{in}} = R_s$, where R_s is the source resistance (i.e., 50 Ω). Correspondingly, the value of the series inductance L_g must be chosen to satisfy (6) at the given f_0. Since the equivalent parallel inductance L_{eq} is given as

$$L_{\mathrm{eq}} = L_g - \frac{1}{(C_p + C_{\mathrm{gs}})\omega_0^2} \tag{8}$$

the series matching inductor L_g must be selected as

$$L_g = L_{\mathrm{eq}} + \frac{1}{(C_p + C_{\mathrm{gs}})\omega_0^2} = \frac{C_p + C_{\mathrm{gs}} + C_m}{C_m(C_p + C_{\mathrm{gs}})\omega_0^2} \tag{9}$$

where (6) and (8) have been used.

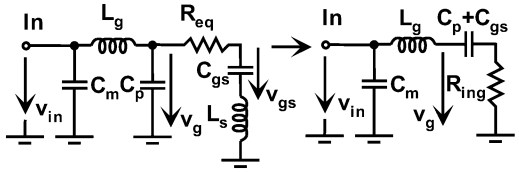

Fig. 6. Analysis of input stage transconductance G_m.

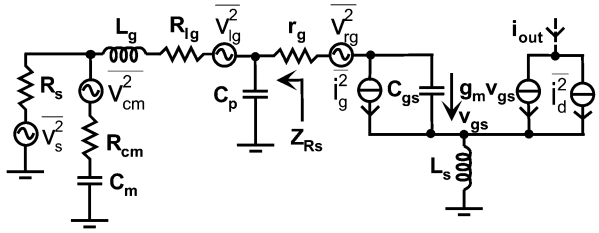

Fig. 7. Circuit model for input stage noise analysis.

B. Input Stage Transconductance

The LNA input stage transconductance at the operation frequency f_0 can also be computed with the help of the parallel-series transformation steps, as illustrated in Fig. 6. The magnitude of the input stage output current $i_{\rm out}$ can be approximated as

$$|i_{\rm out}| = g_m|v_{\rm gs}| \approx \frac{g_m|v_g|}{\sqrt{1+\omega_0^2 C_{\rm gs}^2 R_{\rm eq}^2}} \approx g_m|v_g| \tag{10}$$

where it is assumed that $\omega_0^2 C_{\rm gs}^2 R_{\rm eq}^2 \ll 1$. In addition,

$$\left|\frac{v_g}{v_{\rm in}}\right| = \frac{C_m}{C_p+C_{\rm gs}}\sqrt{\frac{1+\omega_0^2(C_p+C_{\rm gs})^2 R_{\rm ing}^2}{1+\omega_0^2 C_m^2 R_{\rm ing}^2}} \approx \frac{C_m}{C_p+C_{\rm gs}} \tag{11}$$

where (6) has been used, and it is assumed that $\omega_0^2(C_p + C_{\rm gs})^2 R_{\rm ing}^2 \ll 1$ and $\omega_0^2 C_m^2 R_{\rm ing}^2 \ll 1$. Both of these assumptions can easily be verified with practical design values. Thus, the input stage transconductance at f_0 can be approximated as

$$G_m = \left|\frac{i_{\rm out}}{v_{\rm in}}\right| = \frac{g_m C_m}{C_p+C_{\rm gs}} = \sqrt{\frac{R_{\rm eq}}{R_s}}\cdot\frac{1}{\omega_0 L_s} \tag{12}$$

where (7), (10), and (11) have been used and the LNA input impedance-matching requirement $R_{\rm in} = R_s$ is applied. Since, in practice, $R_{\rm eq}$ is designed to be larger than R_s (i.e., 50 Ω), the packaged LNA with a two-component input-matching network has a factor of $\sqrt{R_{\rm eq}/R_s}$ larger G_m compared to the unpackaged LNA, in which C_p is not present and only a series gate inductance is employed [4]. Moreover, the LNA input stage transconductance given by (12) is independent on the actual input device g_m, which is also the case in the unpackaged LNA [4]. Notice also that, in the first-order approximation, G_m does not depend on C_p, provided that the input impedance-matching requirement is met.

Assume that the LNA drives in-phase (I) and quadrature (Q) downconversion mixers directly on-chip, as usual in direct conversion and low-IF receivers. The LNA voltage gain at f_0 is then given as

$$A_v = |G_m Z_d(j\omega_0)| \approx \sqrt{\frac{R_{\rm eq}}{R_s}}\cdot\frac{|Z_d(j\omega_0)|}{\omega_0 L_s} \tag{13}$$

where $Z_d(j\omega_0)$ is the impedance at the drain of M_2 [see Fig. 1(a)]. Thus, the two-component input-matching network including the parallel parasitic capacitance C_p provides an amount of $\sqrt{R_{\rm eq}/R_s}$ voltage gain compared to the unpackaged LNA [4].

C. NF

The LNA NF at the operation frequency f_0 can be estimated by analyzing the circuit shown in Fig. 7. In this circuit, $R_{\rm cm}$ and $R_{\rm lg}$ represent the series resistances of C_m and L_g, respectively, and R_s is the source resistance. Moreover, $\overline{i_d^2}$ is the channel thermal noise including the noise due to the substrate resistance $R_{\rm sub}$, and $\overline{i_g^2}$ is the gate-induced current noise. The analysis based on the circuit shown in Fig. 7 neglects the contributions of the cascode stage and impedance Z_d at the drain of M_2. However, these noise contributions are considered separately.

The NF is computed by first calculating all the noise current contributions at the LNA output current. Moreover, all the calculations are done at the resonance frequency f_0 [see (6)] and assuming perfect power matching $R_{\rm in} = R_s$.

From Fig. 7, the noise contributions of $R_s, R_{\rm cm}$, and $R_{\rm lg}$ to the LNA output noise current can be expressed as

$$\overline{i_{n,R_s}^2} = \frac{G_m^2\overline{v_{n,R_s}^2}}{4} = G_m^2 k_B T R_s \tag{14}$$

$$\overline{i_{n,R_{\rm cm}}^2} = \frac{G_m^2\omega_0^2 C_m^2 R_s^2\overline{v_{n,R_{\rm cm}}^2}}{4} = G_m^2\omega_0^2 C_m^2 R_s^2 k_B T R_{\rm cm} \tag{15}$$

$$\overline{i_{n,R_{\rm lg}}^2} = \frac{G_m^2\omega_0^2 C_m^2 R_s^2\overline{v_{n,R_{\rm lg}}^2}}{4} = G_m^2\omega_0^2 C_m^2 R_s^2 k_B T R_{\rm lg} \tag{16}$$

respectively. Here, the input stage transconductance G_m is defined in (12).

In order to simplify the calculation of the contributions of the rest of the noise sources, the impedance Z_{R_s} looking into the generator (see Fig. 7) is first transformed to the equivalent series impedance by using a series of parallel-series conversions. It can be shown that, at the operation frequency f_0, Z_{R_s} can be expressed as an equivalent RL series impedance

$$Z_{R_s} = R_{\rm eq} + j\omega_0\frac{L_g C_m(C_p+C_{\rm gs})}{C_{\rm gs}(C_p+C_{\rm gs}+C_p)} = \omega_T L_s + \frac{j}{\omega_0 C_{\rm gs}} \tag{17}$$

where (3), (6), and (9) have been used. Consequently, by modeling Z_{R_s} with (17) and by applying a straightforward circuit analysis, the noise contributions of r_g, i_d, and i_g to the LNA output noise current can be expressed as

$$\overline{i_{n,r_g}^2} = \frac{\overline{v_{n,r_g}^2}}{4(\omega_0 L_s)^2} = \frac{k_B T r_g}{(\omega_0 L_s)^2} \tag{18}$$

$$\overline{i_{n,d}^2} = \frac{\overline{i_d^2}}{4} = k_B T\frac{\gamma}{\alpha}g_m + k_B T g_{\rm mbs}^2 R_{\rm sub} \tag{19}$$

$$\overline{i_{n,i_g}^2} = \frac{1+(g_m\omega_0 L_s)^2}{4(\omega_0^2 C_{\rm gs} L_s)^2}\overline{i_g^2} = \frac{1+(g_m\omega_0 L_s)^2}{(\omega_0 L_s)^2}\frac{k_B T\alpha\delta}{5g_m} \tag{20}$$

respectively. Here $g_{\rm mbs} = \eta g_m, \eta$ is the bias-dependent constant [17], γ is the channel current noise factor, and δ is the gate induced current noise factor [4].

Assume that the LNA utilizes an LC resonator circuit at the drain of M_2 to peek the gain of the amplifier at the frequency of

interest f_0, as usual. If the losses of this LC impedance Z_d are modeled by a parallel resistor R_d at f_0, the noise contribution of this resistor to the LNA output noise current is simply [6], [7]

$$\overline{i_{n,R_d}^2} = \frac{4k_BT}{R_d}. \tag{21}$$

Finally, the LNA NF is found by adding up the squares of the different noise current contributions while taking into account the correlation between the gate and drain noise, and by normalizing the result by the noise current $\overline{i_{n,R_s}^2}$ due to R_s

$$\begin{aligned}\mathrm{NF} = 1 &+ \left(\frac{C_p + C_{\mathrm{gs}}}{C_{\mathrm{gs}}}\right)^2 \left(\frac{R_{\mathrm{cm}}}{R_{\mathrm{eq}}} + \frac{R_{\mathrm{lg}}}{R_{\mathrm{eq}}}\right) \\ &+ \frac{r_g}{R_{\mathrm{eq}}} + \frac{\gamma}{\alpha} g_m R_{\mathrm{eq}} \left(\frac{\omega_0}{\omega_T}\right)^2 \Upsilon \\ &+ \eta^2 g_m^2 R_{\mathrm{sub}} R_{\mathrm{eq}} \left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{\alpha\delta}{5 g_m R_{\mathrm{eq}}} \\ &+ \frac{4R_{\mathrm{eq}}}{R_d} \left(\frac{\omega_0}{\omega_T}\right)^2. \end{aligned} \tag{22}$$

Here, $R_{\mathrm{eq}} = \omega_T L_s$ [see (3) and (17)] represents the real part of the impedance Z_{R_s} looking into the generator (see Fig. 7). The coefficient Υ is given by

$$\Upsilon = 1 + 2c\sqrt{\frac{\delta}{5\gamma}}\alpha + \frac{\delta\alpha^2}{5\gamma} \tag{23}$$

where c is the correlation coefficient between the gate and drain noise [4].

Now the NFs of the packaged and unpackaged LNAs are compared. Recall that in the absence of the parallel package parasitic capacitance C_p, the LNA input impedance can be matched only by a series gate inductance and the amplifier NF at the operation frequency f_0 can be written as [4], [7]

$$\begin{aligned}\mathrm{NF} = 1 &+ \frac{R_{\mathrm{lg}}}{R_s} + \frac{r_g}{R_s} + \frac{\gamma}{\alpha} g_m R_s \left(\frac{\omega_0}{\omega_T}\right)^2 \Upsilon \\ &+ \eta^2 g_m^2 R_{\mathrm{sub}} R_s \left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{\alpha\delta}{5 g_m R_s} + \frac{4R_s}{R_d} \left(\frac{\omega_0}{\omega_T}\right)^2 \end{aligned} \tag{24}$$

where R_s is the source resistance (usually 50 Ω). It is noticed that if the losses of the LNA input-matching network are neglected and R_{eq} in (22) is replaced by R_s, (22) actually becomes (24).

In a general case, the comparison of the packaged and unpackaged LNA NFs is difficult. This is, for instance, due to the fact that, in the absence of C_p, the real part of the LNA input impedance is designed so that $R_{\mathrm{in}} = \omega_T L_s = R_s = 50\ \Omega$, whereas in the presence of C_p, $R_{\mathrm{eq}} = \omega_T L_s > 50\ \Omega$, as described in Section III-A. Nevertheless, to gain insight, the NFs can be compared by assuming that, in the both unpackaged and packaged LNAs, the input devices are biased at equal V_{eff}. Thus, in both cases, the input transistors also have equal ω_T. Now, in the unpackaged case, the source inductance L_{su} is selected so that $R_s = \omega_T L_{\mathrm{su}} = 50\ \Omega$ whereas in the packaged case, $R_{\mathrm{eq}} = \omega_T L_{\mathrm{sp}} > 50\ \Omega$. Here, the subscripts u and p denote the unpackaged and packaged cases, respectively. Moreover, suppose that both of the LNAs draw an equal amount of current. Equivalently, in the both amplifiers, the input device widths W and transconductances g_m are equal. Finally, it is assumed that both of the amplifiers utilize equal impedances Z_d (and, thus, R_d) at the drain of the cascode devices.

First neglect the losses due to the matching network components L_g and C_m. With the assumptions described above, it is concluded that, in (22), the terms inversely proportional to R_{eq} contribute less to the packaged LNA NF compared to the corresponding terms inversely proportional to R_s in (24). On the contrary, the terms proportional to R_{eq} in (22) have a higher contribution to the NF compared to the corresponding terms proportional to R_s in (24). Nevertheless, it should be noticed that all the terms in (22) describing the NF of the packaged LNA can be reduced by increasing V_{eff} since both R_{eq} and ω_T increase by increasing V_{eff}. Naturally, this NF reduction is done at the expense of the power consumption, assuming the LNA input device width W is fixed.

From (22), it is seen that, as the parallel parasitic capacitance C_p increases, the noise contribution due to the LNA input-matching network increases proportional to $((C_{\mathrm{gs}}+C_p)/C_{\mathrm{gs}})^2$, worsening the LNA NF. On the other hand, from (24), it is noticed that, in the absence of C_p, the series resistance R_{lg} of the input-matching series inductance L_g contributes to the LNA NF as R_{lg}/R_s, where $R_s = 50\ \Omega$. Correspondingly, in the presence of C_p, the corresponding term is given as $(R_{\mathrm{lg}} + R_{\mathrm{cm}}) \cdot ((C_{\mathrm{gs}} + C_p)/C_{\mathrm{gs}})^2/R_{\mathrm{eq}} = (R_{\mathrm{lg}}+R_{\mathrm{cm}})(\omega_0 C_m)^2 R_s$, which is, thus, approximately a factor of $(\omega_0 C_m)^2 R_s^2$ larger than the term in the absence of C_p (notice that, in practice, $(R_{\mathrm{lg}}+R_{\mathrm{cm}}) \approx R_{\mathrm{lg}}$). For instance, in this study, the LNA input impedance matching requires that $C_m = 3.6$ pF, which, at 2 GHz, means that the noise contribution of R_{lg} is approximately five times larger compared to the LNA without C_p. In fact, in a well-optimized submicrometer LNA, the losses of the input-matching network can easily dominate the NF of the packaged LNA employing a two-component matching network.

Finally, as seen from (22), the NF of the packaged LNA directly depends on the parallel parasitic capacitance C_p only via losses of the input-matching network. In principle, the value of R_{eq} can be designed independently of C_p. However, in order to be able to match the LNA input impedance to 50 Ω, R_{eq} has to usually be designed to be larger than 50 Ω. In other words, the terms proportional to R_{eq} together with the losses of the input-matching network usually dominate the LNA NF over the rest of the terms inversely proportional to R_{eq} in (22).

IV. LNA Optimization

In modern minimum-sized CMOS devices, the shallow trench isolation (STI) substrate resistance easily dominates over the active area substrate resistance [18] and the substrate resistance is inversely proportional to the device width W. On the other hand, the input device transconductance g_m is proportional to W. Thus, from (22), it is seen that all

the other terms excluding $((C_p + C_{\rm gs})/C_{\rm gs})^2(R_{\rm cm}/R_{\rm eq} + R_{\rm lg}/R_{\rm eq}), (4R_{\rm eq})/(R_d)(\omega_0/\omega_T)^2$, and $(\alpha\delta)/(5g_mR_{\rm eq})$ increase by increasing W. On the contrary, since the terms $((C_p + C_{\rm gs})/C_{\rm gs})^2(R_{\rm cm}/R_{\rm eq}+R_{\rm lg}/R_{\rm eq})$ and $(\alpha\delta)/(5g_mR_{\rm eq})$ decrease by increasing W, an optimum input device width $W_{\rm opt}$, which minimizes the LNA NF, exists, at least in theory. However, notice that the noise due to the gate resistance can also be minimized by interdigitating the device [4].

The optimization procedure of the packaged LNA with a two-component matching network is similar with the optimization of the unpackaged LNA. First, the minimum channel length provided by the given technology is selected to maximize ω_T, given by (4), and to minimize the NF given by (22). The overdrive voltage $V_{\rm eff}$ of the LNA input device M_1 and the value of the source inductance L_s are then set to some arbitrary values. As $V_{\rm eff}$ and L_s are fixed, $R_{\rm eq}$ is also fixed [see (3)]. In the next step, the LNA input device width W is swept until an optimum NF is found. Corresponding with the each value of W, the input-matching network must be tuned accordingly to ensure that the LNA input impedance is matched. Finally, at this phase of the circuit design, it is reasonable to assume in the simulations that the cascode device M_2 has the same device width as the input device M_1.

As the optimum input device width $W_{\rm opt}$ has been found, the resulted current and power consumption must be usually checked against the power consumption constraint. If the resulted power consumption is smaller than the specification, $V_{\rm eff}$ can be increased if a smaller LNA NF is desired or required. As the increase of $V_{\rm eff}$ increases both ω_T and $R_{\rm eff}$, the NF given by (22) decreases by increasing $V_{\rm eff}$. On the other hand, if the resulted power consumption is higher than allowed, $V_{\rm eff}$ must be set to a lower value and $W_{\rm opt}$ must be re-simulated.

As $W_{\rm opt}$ and $V_{\rm eff}$ have been determined, the real part of the impedance $Z_{\rm ing}$ looking into the gate of M_1 at the operation frequency can be simulated. If the resulted $R_{\rm ing}$ is in the order of 10 Ω or smaller, larger L_s can be selected. Namely, if $R_{\rm ing}$ is only approximately 10 Ω or smaller, the input impedance matching becomes sensitive to component tolerances. If larger L_s is needed, $W_{\rm opt}$ must again be re-simulated.

It can be shown that the noise contribution of the LNA cascode device M_2, considering only channel thermal noise, to the LNA output noise current can be approximated as

$$\overline{i_{n,M_2}^2} = \frac{\overline{i_{d,M_2}^2}}{1+\left(\dfrac{g_{m2}}{\omega_0 C_{\rm ps}}\right)^2} \approx \left(\frac{\omega_0 C_{\rm ps}}{g_{m2}}\right)^2 4k_BT\frac{\gamma}{\alpha}g_{m2} \quad (25)$$

where g_{m2} is the transconductance of M_2, and $C_{\rm ps}$ is the parasitic capacitance between the drain of M_1 and the ground, respectively. Thus, the noise contribution of M_2 is minimized by minimizing the ratio $(\omega_0 C_{\rm ps})/g_{m2}$ [19]. The cascode device M_2 uses the minimum channel length to minimize $C_{\rm ps}$. Moreover, since, in practice, the LNA bias current and, thus, also the drain–source current of M_2 is determined by the optimization of the LNA input device M_1, the ratio $(\omega_0 C_{\rm ps})/g_{m2}$ can be minimized by selecting the width W_2 of M_2 accordingly. Often, the LNA NF is close to the minimum, when M_1 and M_2 are the same size, which gives the opportunity to merge them into one dual-gate field-effect transistor (FET) [20]. This elegant layout action further lowers the noise contribution of M_2 by lowering $C_{\rm ps}$.

As the sizes and bias points of M_1 and M_2 have been selected and the value of L_s has been fixed, the final component values of the matching network C_m and L_g can be determined [see (7) and (9)]. Finally, the impedance Z_d at the drain of M_2 is designed so that the LNA voltage gain at the operation frequency has the desired value [see (13)].

In practice, the optimization of the packaged LNA is an iterative process, in which the different design steps have an effect on each other. For instance, it might not be possible to set the LNA gain to the desired value simply by designing the impedance Z_d accordingly since the input stage transconductance given by (12) is too small. Thus, it might be necessary to reduce the value of L_s, and this requires, for instance, that $W_{\rm opt}$ and the component values of the matching network must be redefined. Nevertheless, the described design procedure provides guidelines for the LNA circuit design and optimization.

V. LNA Implementation

Based on theoretical results, a packaged 2-GHz inductively degenerated common-source LNA with ESD protection was designed via 0.13-μm CMOS technology. In this technology, the minimum NF of a single MOS device at 2 GHz is only in the order of 0.2 dB. The supply voltage in this process is 1.2 V. A balanced LNA is used to reject the interference from the substrate and supply. Although in direct conversion and low-IF receivers the LNA drives I and Q mixers directly on-chip, the LNA designed in this study was processed as a standalone circuit to be able to characterize the LNA performance separately. Thus, aside from the LNA input impedance, the LNA output impedance is also matched to a differential 100-Ω impedance. The LNA is mounted in a quad flat nonleaded (QFN) package and the amplifier utilizes an RF bond pad with ESD protection diodes provided by the IC vendor. In this study, the total parasitic parallel capacitance C_p (at nodes gp and gm in Fig. 8) including the capacitance due to the package parasitics, ESD protection diodes, and bond pad structure ($\sim$200 fF) is approximately 500 fF.

In the simulations, the MOS transistors were modeled by using BSIM3.v3 with parasitic gate, substrate, drain, and source resistances. The gate-induced current noise was taken into account by channel segmentation [21]. Moreover, in the simulations, the models for the PCB traces, external lumped matching components, ESD protection structures, bond pads, and package parasitics were used.

The schematic of the balanced LNA excluding the biasing details is shown in Fig. 8. At the input, the parallel matching capacitor C_m, shown in Fig. 1, is realized in a balanced LNA as a parallel component $C_{md} = C_m/2$ between the differential LNA inputs. The LNA utilizes a differential inductor L_d of 23 nH with a quality (Q) value of 8 @ 2 GHz to provide a high-impedance path between the supply voltage and the drain of M_2. The metal–oxide–metal (MOM) capacitors $C_{\rm dc}$ of 4 pF ac couple the on-chip LNA output from the matching network. Finally, the output off-chip matching network consisting of the

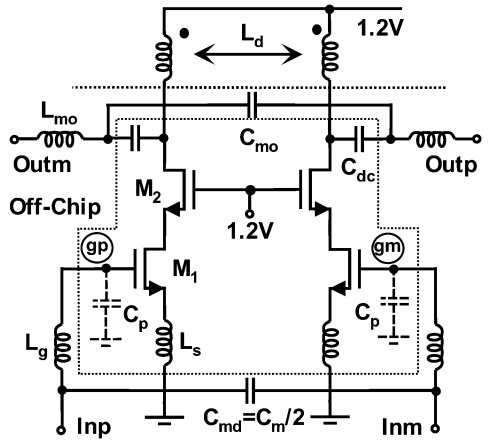

Fig. 8. Schematic of implemented LNA.

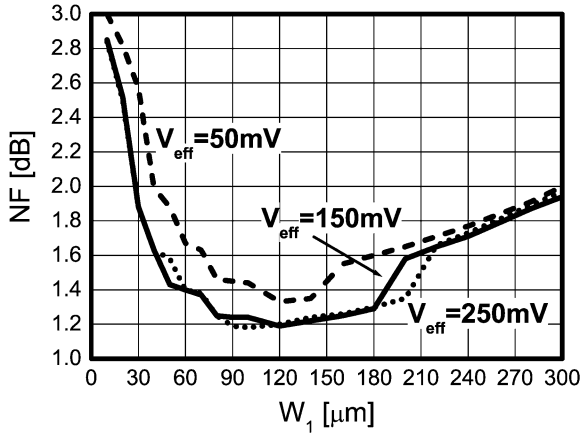

Fig. 9. Simulated LNA NF at 2 GHz as function of input device width W_1 with three different values of $V_{\rm eff}$.

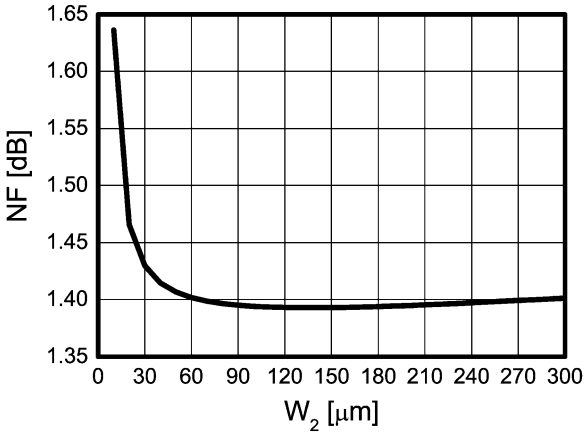

Fig. 10. Simulated LNA NF at 2 GHz as a function of cascode transistor width W_2.

series inductor $L_{\rm mo}$ and parallel capacitance $C_{\rm mo}$ complete the LNA output matching.

As described in Section IV, the design of the LNA can be started by selecting the appropriate value for the source inductance L_s. For this purpose, the input device effective gate–source voltage $V_{\rm eff} = (V_{\rm GS} - V_t)$ is set to some fixed arbitrary value, i.e., $V_{\rm eff} = 150$ mV. The input device M_1 width W_1 is then swept and the LNA NF is simulated until the optimum width is found that corresponds to the minimum NF. This can be repeated for the different values of L_s. At this phase, it is reasonable to assume that the cascode width $W_2 = W_1$. Moreover, corresponding the each value of W_1, the input and output matching networks are tuned to match the input and output at 2 GHz.

According to simulations, three different values of $L_s = 1.0, 1.5, 2.0$ nH result almost to an equal LNA noise performance at 2 GHz. On the other hand, since a low value of L_s can imply too low a value for $R_{\rm ing}$ [see (5)], while a high value of L_s can result in a too low value for G_m or LNA gain [see (12)], $L_s = 1.5$ nH is a reasonable compromise.

As the value of L_s is determined, an optimum input device width and bias $V_{\rm eff}$ can be searched. Fig. 9 illustrates the simulated LNA NF at 2 GHz with three different values of $V_{\rm eff} = 50, 150, 250$ mV as a function of the input device width W_1. Here, $L_s = 1.5$ nH, $W_2 = W_1$, and the LNA input and output are matched at each point.

From Fig. 9, it is seen that the increase of $V_{\rm eff}$ from 50 to 150 mV improves the minimum NF approximately 0.2 dB, whereas the increase of $V_{\rm eff}$ from 150 to 250 mV does not result in NF improvement. Thus, it is reasonable to choose $V_{\rm eff} = 150$ mV.

From Fig. 9, it is concluded that W_1 of 90–150 μm results in the minimum NF corresponding to $V_{\rm eff} = 150$ mV. However, since the values of 90–150 μm with $V_{\rm eff} = 150$ mV correspond to a relatively high LNA current consumption of 9.7–14.3 mA, a slightly lower value of $W_1 = 60$ μm was selected instead. This worsens the NF only by 0.2 dB and corresponds to the current consumption of 7 mA, which is tolerable on the power budget of this study.

Fig. 10 illustrates the simulated LNA NF at 2 GHz as a function of the cascode transistor width W_2. Here, $W_1 = 60$ μm, $L_s = 1.5$ nH, and $V_{\rm eff} = 150$ mV. It is seen that, for the cascode widths larger than approximately 30 μm, the NF stays relatively constant. Notice, however, that in practice, the larger cascode width implies a larger parasitic capacitance associated with the layout wires needed to connect M_1 and M_2. Since this additional capacitance increases the noise contribution of M_2 [see (25)], it is advisable to select $W_2 = W_1 = 60$ μm to simplify the layout connection of M_1 and M_2.

In order to minimize the noise contributions of the gate and substrate resistances r_g and $R_{\rm sub}$, respectively, it is important to select the number of gate fingers (n_f) accordingly [4], [21]. Fig. 11 plots the LNA NF as a function of n_f. It is assumed that both M_1 and M_2 utilize an equal amount of n_f. Moreover, it is seen that $n_f = 10$ is enough to minimize the NF. This corresponds to the gate finger width of $W_f = W_1/10 = 6$ μm. Each finger is contacted at both ends.

The final LNA utilizes the input and output matching networks with $C_{md} = 1.8$ pF, $L_g = 7.5$ nH, $C_{\rm mo} = 1.5$ pF, and $L_{\rm mo} = 9.5$ nH. At 2 GHz, the amplifier has simulated $S_{11}, S_{22} < -15$ dB, and $S_{21} = 19.1$ dB, input third-order intercept point IIP3 $= -6.5$ dBm, and NF $= 1.4$ dB. It draws approximately 7 mA from a 1.2-V supply. In this case, the highest contributions to the LNA NF have the source resistance R_s (72.0%), the series resistance $R_{\rm lg}$ of the matching inductor L_g

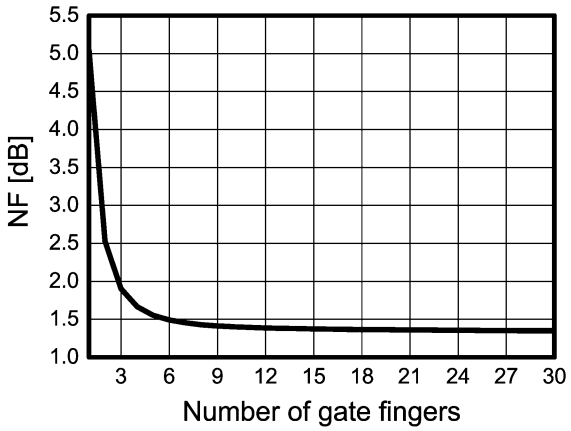

Fig. 11. Simulated LNA NF at 2 GHz as a function of the number of gate fingers.

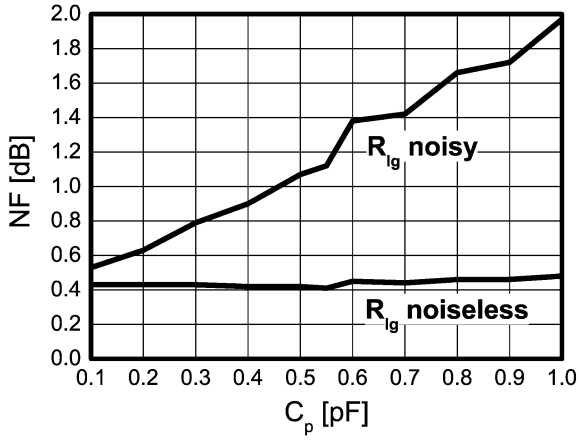

Fig. 12. Simulated LNA NF at 2 GHz as function of equivalent parallel package parasitic capacitance C_p. Matching inductor L_g series resistance $R_{\rm lg} = 1.3\ \Omega$.

(13.2%), the channel thermal noise plus gate induced current noise of M_1 (2.7%), the gate resistance r_g of M_1 (2.0%), and the series resistance $R_{\rm cm}$ of the matching capacitor C_m (1.9%). The rest of the contributions are each below 1%. Notice that since the gate current noise is modeled with the channel segmentation [21], the noise contributions of the channel thermal noise and gate induced current noise cannot be separated. It is concluded that, in this study, the noise contribution of $R_{\rm lg}$ dominates the LNA NF, as discussed in Section IV.

Consider the effect of the equivalent parallel package parasitic capacitance C_p on the LNA NF and S_{21}. Assume that the losses of the input-matching network are lumped on the equivalent series resistance $R_{\rm lg}$ of the series matching inductor L_g ($R_{\rm cm} = 0\,\Omega$). It is assumed that $R_{\rm lg} = 1.3\,\Omega$. For $L_g = 7.5$ nH, this corresponds to approximately a Q of 72 at 2 GHz, which represents a rather typical value for Q of external lumped inductors.

Fig. 12 illustrates the NF at 2 GHz as a function of the value of C_p in two cases. In the first case, the noise due to $R_{\rm lg}$ is set to zero in the simulator, while in the second case, the noise due to $R_{\rm lg}$ is considered. Again, at each point, the input and output matching networks are tuned accordingly to match the input and output impedances at 2 GHz. It is seen that, in the absence of C_p, very low LNA NFs in the order of 0.5 dB are available. Unfortunately, as C_p increases, the NF increases almost linearly in decibel scale and, finally, the noise contribution of $R_{\rm lg}$ starts to dominate the NF. It is also noticed that the value of C_p has an insignificant effect on the other LNA noise contributions since the NF with noiseless $R_{\rm lg}$ remains almost constant despite the increase of C_p. Recall that both of these conclusions can also be drawn from (22). From (22), it is seen that as C_p increases, the noise contribution of $R_{\rm lg}$ increases as $R_{\rm lg}((C_{\rm gs} + C_p)/C_{\rm gs})^2/R_{\rm eq}$, while the other contributions do not depend on C_p. Thus, the LNA NF can be reduced by reducing C_p. This can be achieved partly by selecting the LNA packet pins accordingly. Nevertheless, the lower limit of C_p is set by the ESD requirements. The noise contribution of $R_{\rm lg}$ can also be reduced by choosing larger device width and, thus, $C_{\rm gs}$ for the input device M_1. However, if the LNA current consumption is not to be increased, $V_{\rm eff}$ must be reduced to compensate for the increase of W_1. Unfortunately, this reduces ω_T and

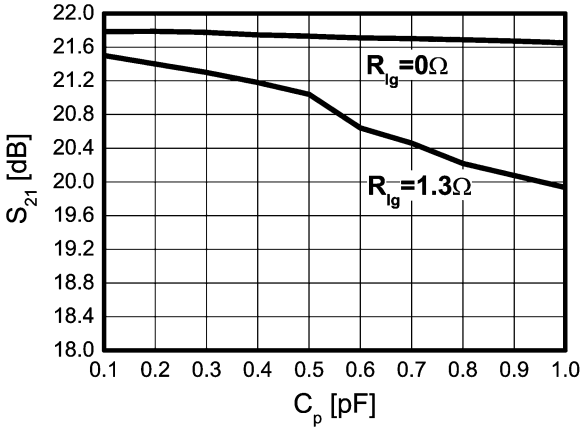

Fig. 13. Simulated LNA S_{21} at 2 GHz as a function of equivalent parallel package parasitic capacitance C_p.

$R_{\rm eq} = \omega_T L_s$ and, therefore, again, increases the noise contribution of $R_{\rm lg}$.

The effect of C_p on the LNA available power gain S_{21} at 2 GHz is depicted in Fig. 13. Again, two cases are illustrated. First, S_{21} is plotted assuming ideal series matching inductor L_g ($R_{\rm lg} = 0\,\Omega$). Next, the effect of the finite inductor series resistance ($R_{\rm lg} = 1.3\,\Omega$) is considered. It is seen that if $R_{\rm lg}$ is very small ($R_{\rm lg} \approx 0\,\Omega$), S_{21} stays almost constant despite the increase of C_p. Again, this agrees well with the theoretical derivations of Section III. Recall that according to (12), the LNA input stage transconductance G_m and, thus, the voltage and power gain, do not depend on C_p provided that $R_{\rm lg} \approx 0\,\Omega$. In practice, the finite $R_{\rm lg}$ results in a slight reduction of S_{21} as a function of a C_p increment. This can also be shown by hand calculations. Nevertheless, to keep the analysis easy to interpret, $R_{\rm lg}$ is neglected in Section III.

VI. Experimental Results

The differential LNA S-parameters were measured by using a four-port network analyzer. The results presented here correspond to the LNA input device bias $V_{\rm eff} = 150$ mV or the LNA current consumption of 7 mA.

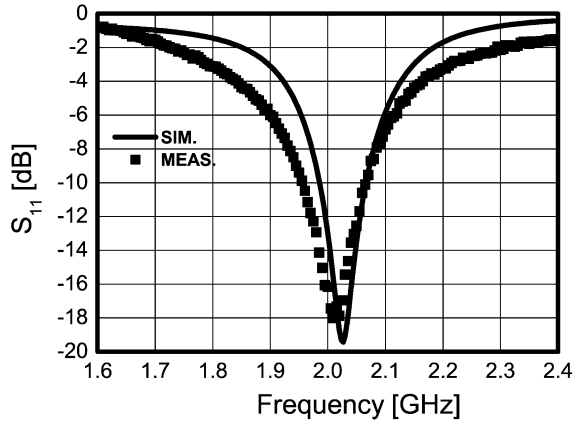

Fig. 14. Measured and simulated (solid line) LNA input impedance matching.

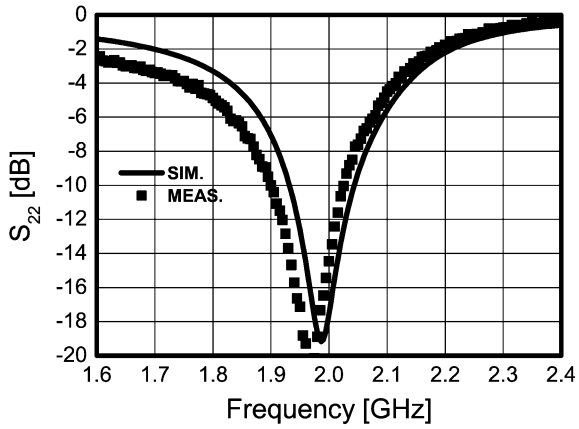

Fig. 15. Measured and simulated (solid line) LNA output impedance matching.

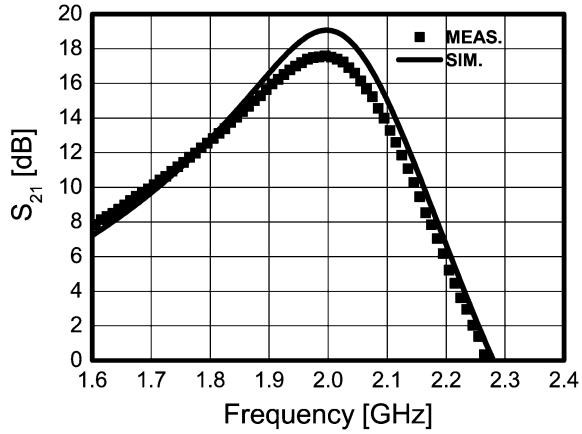

Fig. 16. Measured and simulated (solid line) LNA available power gain.

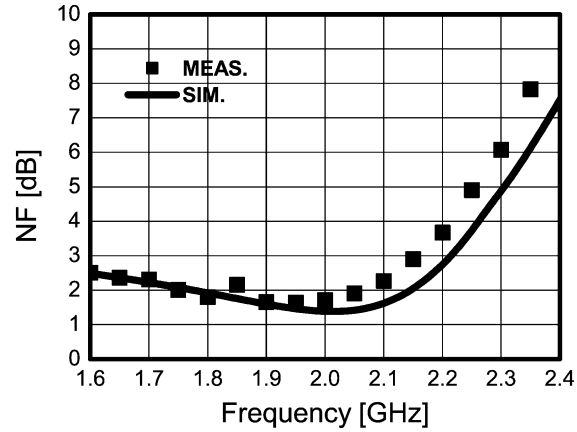

Fig. 17. Measured and simulated (solid line) LNA NF.

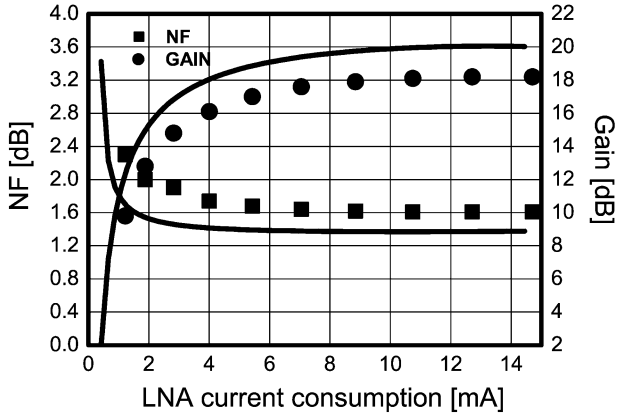

Fig. 18. Measured and simulated (solid line) LNA NF and gain.

The measured and simulated LNA input and output scattering parameters S_{11} and S_{22} are shown in Figs. 14 and 15, respectively. Moreover, the measured and simulated LNA available power gains S_{21} are illustrated in Fig. 16. The measured S_{21} at 2 GHz of 17.6 dB is approximately 1.5 dB smaller than expected or simulated (19.1 dB). The missing gain is due to the nonoptimized layout of the integrated differential inductor. Due to this layout failure, the Q value of the inductor L_d at the drain of M_2 is smaller than originally intended. If the simulations are rerun with the minimum Q corner models, the simulated LNA S_{21} is 17.8 dB, which agrees well with the measurements. The measured IIP3 is approximately -4.0 dBm, which is slightly higher than the simulated -6.5 dBm. The improved linearity is due to the missing gain.

The measured and simulated LNA NFs are plotted in Fig. 17. The measured NF at 2 GHz of 1.6 dB is approximately 0.2 dB higher than the nominal simulated (1.4 dB). It is also noticed that the simulator fails to predict the NF accurately at higher frequencies. The reason for this is uncertain.

The measured and simulated LNA NFs and forward gains as a function of the LNA current consumption are illustrated in Fig. 18. It is concluded that the NF decreases by increasing the bias current until the NF saturates at approximately 1.6 dB. This agrees well with (22). As the increase of V_{eff} or bias current at fixed device dimensions increases both ω_T and R_{eff}, the NF decreases by increasing V_{eff}. At large bias, the NF saturates due to the saturation of ω_T (see Fig. 4). For the same reason, both the LNA input stage G_m and forward gain increase first by increasing V_{eff} and ω_T [see (12)]. However, as ω_T saturates, G_m and S_{21} cease to increase with V_{eff}. Finally, it is seen that the difference between the measured and simulated NFs increase at smaller bias currents. This is due to the fact that the used MOS

noise model underestimates the bias-dependent gate resistance or gate induced current noise at the small gate bias.

VII. Conclusion

In this paper, the effects of the package and ESD parasitics on the input matching, input stage transconductance, NF, and voltage gain of the inductively degenerated common-source LNA have been examined and the performance of the packaged LNA has been optimized. The simulations, together with the theoretical derivations, agree well with the measured LNA performance. It is concluded that, in the presence of an equivalent parallel package parasitic capacitance C_p, the NF in a well-optimized submicrometer packaged CMOS LNA is easily dominated by the losses of the input-matching network instead of the active device noise. In practical applications with ESD protection, the achievable NF of a packaged LNA is, therefore, well above the theoretical minimum NF of the active device.

References

[1] B. Razavi, "A 900 MHz CMOS direct conversion receiver," in *VLSI Circuits Tech. Symp. Dig.*, 1997, pp. 113–114.

[2] A. Rofougaran, G. Chang, J. J. Rael, J. Y. C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, J. Min, E. W. Roth, A. A. Abidi, and H. Samueli, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS—Part II: Receiver design," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 535–547, Apr. 1998.

[3] S. Tadjpour, E. Cijvat, E. Hegazi, and A. A. Abidi, "A 900-MHz dual-conversion low-IF GSM receiver in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1992–2002, Dec. 2001.

[4] D. K. Shaeffer and T. H. Lee, *The Design and Implementation of Low-Power CMOS Radio Receivers*. Norwell, MA: Kluwer, 1999.

[5] B. A. Floyd, J. Mehta, C. Camero, and K. K. O, "A 900-MHz, 0.8 μm CMOS low noise amplifier with 1.2-dB noise figure," in *Proc. Custom Integrated Circuits Conf.*, 1999, pp. 661–664.

[6] G. Girlando and G. Palmisano, "Noise figure and impedance matching in RF cascode amplifiers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 11, pp. 1388–1396, Nov. 1999.

[7] P. Andreani and H. Sjöland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 9, pp. 835–841, Sep. 2001.

[8] T. K. Nguyen, C. H. Kim, G. J. Ihm, M. S. Yang, and S. G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1433–1442, May 2004.

[9] P. Leroux and M. Steyaert, "High-performance 5.2 GHz LNA with on-chip inductor to provide ESD protection," *Electron. Lett.*, vol. 37, pp. 467–469, Mar. 2001.

[10] V. Chandrasekhar and K. Mayaram, "Analysis of CMOS RF LNA's with ESD protection," in *IEEE Int. Circuits Systems Symp.*, 2002, pp. 779–802.

[11] P. Sivonen, S. Kangasmaa, and A. Pärssinen, "Analysis of packaging effects and optimization in inductively degenerated common-emitter low-noise amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 4, pp. 1220–1226, Apr. 2003.

[12] P. Leroux, J. Janssens, and M. Steyaert, "A 0.8-dB NF ESD-protected 9-mW CMOS LNA operating at 1.23 GHz," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 760–765, Jun. 2002.

[13] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge, U.K.: Cambridge Univ. Press, 1998, pp. 91–93.

[14] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998, pp. 50–53.

[15] G. Gramegna, M. Paparo, P. G. Erratico, and P. De Vita, "A sub-1-dB $\pm$2.3-kV ESD-protected 900-MHz CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1010–1017, Jul. 2001.

[16] J. Chang, "An integrated 900 MHz spread-spectrum wireless receiver in 1-μm CMOS and a suspended inductor technique," Ph.D. dissertation, Elect. Eng. Dept., UCLA, Los Angeles, CA, 1998.

[17] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. Orlando, FL: Saunders College Publishing, 1987, pp. 114–116.

[18] R. T. Chang, M. T. Yang, P. P. C. Ho, Y. J. Wang, Y. T. Chia, B. K. Liew, C. P. Yue, and S. S. Wong, "Modeling and optimization of substrate resistance for RF-CMOS," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 421–426, Mar. 2004.

[19] W. Guo and D. Huang, "Noise and linearity analysis for a 1.9 GHz CMOS LNA," in *Proc. Asia–Pacific Circuits Systems Conf.*, 2002, pp. 409–414.

[20] F. Behbahani, J. C. Leete, Y. Kishigami, A. Roithmeier, K. Hoshino, and A. A. Abidi, "A 2.4-GHz low-IF receiver for wide-band WLAN in 0.6-μm CMOS-architecture and front-end," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, Dec. 2000.

[21] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C. Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 618–632, Mar. 2003.

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