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Cancellation of Second-Order Intermodulation Distortion and Enhancement of IIP2 in Common-Source and Common-Emitter RF Transconductors

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***Abstract*—In this paper, a biasing technique for cancelling second-order intermodulation (IM2) distortion and enhancing second-order intercept point (IIP2) in common-source and common-emitter RF transconductors is presented. The proposed circuit can be utilized as an RF input transconductor in double-balanced downconversion mixers. By applying the presented technique, the achievable IIP2 of the mixer is limited by the linearity of the switching devices, component mismatches, and offsets. The proposed circuit has properties similar to the conventional differential pair transconductor in that it ideally displays no IM2 distortion. However, the presented circuit is more suitable for operation at low supply voltages because it has only one device stacked between the transconductor input and output. In the conventional differential pair, two devices consume the voltage headroom. The noise performance of the proposed transconductor is similar to the noise performance of the traditional common-source (emitter) and differential pair transconductors at given bias and device dimensions. On the other hand, the third-order intercept point (IIP3) of the presented transconductor is slightly higher than the IIP3 of the differential pair transconductor at given bias. Finally, the proposed circuit can also be employed as a current mirror, the ratio of which is very insensitive to the voltage swings at the gate or base of the current mirrored transistor.**

***Index Terms*—Biasing, common emitter, common source, degeneration, direct conversion, downconversion mixer, low voltage, RF, second-order intermodulation (IM2), second-order intercept point (IIP2), third-order intermodulation (IM3), third-order intercept point (IIP3), transconductor.**

I. Introduction

In RECENT years, direct conversion and low-IF wireless receiver architectures have become very popular [1]–[7], because in these architectures a very high level of integration can be obtained. However, one of the most severe limitations on the use of direct conversion technique and also an issue in low-IF receiver is the need for a high second-order intercept point (IIP2) [8]. In a homodyne receiver, second-order intermodulation (IM2) distortion introduces undesirable spectral components at baseband which degrade the receiver sensitivity. For instance, if two strong interferers at frequencies f_1 and f_2, close to the channel of interest, experience even-order distortion, they generate a low-frequency IM2 distortion component at frequency $f_1 - f_2$. In the RF front-end, this may happen both in the low-noise amplifier (LNA) and in the mixer. However, if the LNA and mixer are ac coupled, the low-frequency beat signal generated in the LNA is filtered out. In addition, usually the downconversion mixers utilize double-balanced topologies, which generate small amount of even-order distortion. Moreover, in an ideal mixer the low-frequency beat present at the mixer RF input is upconverted, but in reality mixers present a finite feedthrough from the RF input to the IF output, which results in finite IIP2 [9]. Finally, it is the downconversion mixer that usually determines the achievable IIP2 of the entire receiver [10].

Most of the active double-balanced mixers utilized in wireless receivers are based on the Gilbert mixer topology [11]. In general, both the RF input transconductor and switching devices contribute to the mixer nonlinearity, and the mixer IIP2 is determined by the mixer second-order nonlinearity, mismatches, and offsets. As a conclusion, in order to maximize the mixer IIP2, it is essential to develop techniques for minimizing the IM2 products generated in the mixer, since the device matching and offsets cannot be improved beyond certain limits.

To enhance the mixer IIP2, a new biasing technique for cancelling the IM2 distortion generated in the common-source or common-emitter mixer RF input transconductors is proposed. The second-order nonlinearity of the switches is not considered. The intermodulation performance of the proposed transconductor is also compared to the already existing most popular mixer RF input stages, which are the differential pair and common-source (emitter) transconductors. The characteristics of the different transconductors are compared both in the terms of IIP2 and third-order intercept point (IIP3), respectively.

This paper is organized as follows. First, the existing IM2 distortion suppression techniques in the mixer input stage are reviewed and their benefits and drawbacks are discussed. Next, the equations describing intermodulation distortion in the most used CMOS differential pair and common-source mixer RF input stages are given. In Section III-C, the operation of the proposed CMOS RF transconductor is described and analyzed by direct calculation of the nonlinear responses. In the following, the formulas predicting intermodulation distortion in the most commonly used bipolar mixer RF input stages are reviewed and the

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operation of a proposed bipolar transconductor is explained and analyzed. Next, the nonidealities of the proposed transconductor are discussed. Finally, experimental results based on circuit simulations are presented and the performances of the different RF transconductors are compared. The proposed transconductor is also simulated as part of a complete downconversion mixer.

II. IM2 Distortion Suppression Techniques in Mixer RF Input Transconductors

In a perfectly balanced mixer, stimulated and sensed differentially, the IM2 components at the mixer output are presented as common-mode signals with equal amplitude and are therefore cancelled. Unfortunately, in the presence of offsets and mismatches, the cancellation is not perfect, which results in finite mixer IIP2. If the offsets and the second-order nonlinearity of the mixer switching devices are neglected, the IIP2 of a double-balanced mixer can be approximated as [8]

$$v_{\mathrm{IIP2}} = \frac{\sqrt{2}\cdot v_{\mathrm{IIP2},g_m}}{\pi\eta_{\mathrm{nom}}} \cdot \frac{4}{(2\Delta\eta(\Delta g_m + \Delta A_{\mathrm{RF}}) + \Delta R(1+\Delta g_m)(1+\Delta A_{\mathrm{RF}}))} \tag{1}$$

where η_{nom} is the nominal value of the duty cycle in a single switch, $\Delta\eta$ is the mismatch in the duty cycles, Δg_m is the mismatch between the mixer RF input transconductances, ΔA_{RF} is the amplitude imbalance of the RF signal, ΔR is the imbalance of the mixer load resistances, and v_{IIP2,g_m} is the single-ended IIP2 of the mixer RF input transconductor, measured from the single-ended output of the transconductor. Therefore, in order to maximize entire mixer IIP2 and to minimize IIP2 sensitivity to mismatches, it is important to minimize the level of the IM2 components in the single-ended output current of the RF transconductor.

The IM2 products generated in the mixer RF input transconductor can be eliminated, or at least in practise minimized in the presence of offsets [12], [13], by a fully differential RF input stage such as a differential pair [10]. Unfortunately, as the IIP3 of the differential pair is worse than the IIP3 of the common-source (emitter) transconductor at a given bias [14], the common-source (emitter) RF input transconductor is usually preferred to the differential pair. Moreover, as supply voltage scales down with transistor technology, stacking three transistors with load resistors in a standard Gilbert cell becomes difficult or even impossible. Supply voltages in state-of-art sub-micron CMOS processes, in which the minimum channel length is 0.13 μm or even 90 nm, are only in the order of 1 V. Finally, a fully differential RF input stage utilizing *LC*-degeneration is suitable for operation at low supply voltage, but consumes large die area due to the fact that integrated inductors are required [10].

The IM2 products generated in the mixer RF input transconductor can also be eliminated by ac-coupling the RF input stage from the switches [15]. Unfortunately, the additional current sources and load resistors needed in the RF input stage increase the mixer noise figure (NF) and add additional parasitic capacitance at the common-node of the switching devices. This parasitic capacitance increases the second-order nonlinearity of the switching devices [10].

The mixer RF input transconductor proposed in this paper is based on the new biasing technique of the common-source or common-emitter circuit [16]. Similar biasing techniques have earlier been used in the context of the linear MOS transconductors based on the differential pair [17], [18]. The proposed circuit displays ideally no IM2 distortion provided that the transconductor is excited differentially and all the transistors in the circuit match with each other. Moreover, in this circuit, no extra noise sources in practical cases of interest are added in the mixer and no integrated inductors are required, which results in small die area. Finally, the presented transconductor is also suitable for operation at low supply voltages, because it has only one device stacked between the transconductor input and output. The proposed transconductor has also slightly higher IIP3 compared to the differential pair transconductor at given bias.

III. Intermodulation Distortion in CMOS RF Transconductors

In this section, the intermodulation distortion characteristics of the differential pair, common-source, and proposed common-source mixer RF input transconductors are analyzed and compared. All the transconductors are biased at equal bias current and the corresponding device sizes are also equal. Thus, all the transconductors have equal RF input stage transconductance. The effect of degeneration is not considered, because usually CMOS devices utilized in the mixer RF input transconductors are linearized simply by increasing their gate–source overdrive voltage ($V_{\mathrm{eff}} = V_{\mathrm{GS}} - V_T$) [9]. For simplicity, it is assumed that the dominant nonlinearity is the nonlinear transconductance of the MOS transistor. The effects of the high-frequency nonlinearities are taken into account by careful simulations.

A. CMOS Differential Pair RF Input Transconductor

A traditional CMOS Gilbert mixer utilizes a differential pair as its RF input transconductor to reject common-mode interference and to suppress the second-order distortion. Suppose that the MOS transistor is modeled with

$$i_{\mathrm{DS}} = \frac{K}{2}\frac{W}{L}\frac{(v_{\mathrm{GS}} - V_T)^2}{1+\theta(v_{\mathrm{GS}} - V_T)} \tag{2}$$

where θ captures how the inversion layer mobility degrades with the gate electric field [19], [20]. If the differential pair is biased by a tail current $2A \cdot I_B$, the IIP3 of the differential pair can be approximated as

$$\begin{aligned} v_{\mathrm{IIP3}} &= \frac{4}{\sqrt{3}}\frac{V_{\mathrm{eff}}(1+\theta V_{\mathrm{eff}})(2+\theta V_{\mathrm{eff}})}{\sqrt{2+\theta V_{\mathrm{eff}}(2+\theta V_{\mathrm{eff}})}} \\ &\approx 4\sqrt{\frac{2}{3}}V_{\mathrm{eff}} \\ &= 8\sqrt{\frac{AI_BL}{3KAW}} \end{aligned} \tag{3}$$

where the width and length of the input device are AW and L, respectively. The approximation holds if $\theta V_{\mathrm{eff}} \ll 1$ [21]. Moreover, ideally the single-ended output current of the differential pair does not include any even-order components, which results

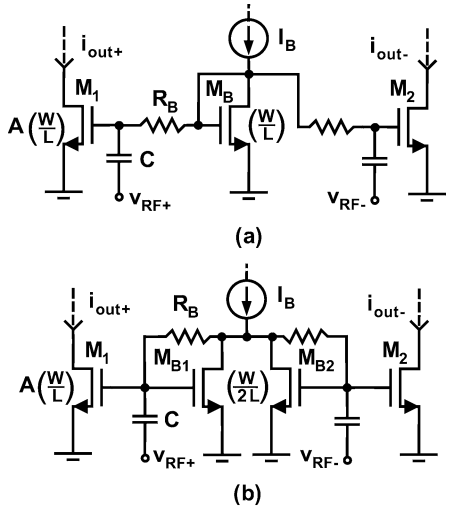

Fig. 1. (a) Traditional and (b) proposed common-source RF input transconductor.

in infinite input stage IIP2. This is a clear advantage of the differential pair RF input transconductor, as the entire mixer IIP2 is considered.

B. Common-Source RF Input Transconductor

Since the common-source transconductor biased at a given overdrive voltage $V_{\rm eff}$ exhibits smaller third-order nonlinearity than the differential pair at equal bias [14], most of the reported low-voltage CMOS downconversion mixers usually utilize the common-source transconductor as their RF input stage [see Fig. 1(a)], [2]–[5], [7], [14]. In this circuit, the main device M_1 is biased with the current mirror formed by the diode connected transistor M_b and M_1 [22]. The resistors R_B shown in Fig. 1 are assumed to be large so that the current through them can be neglected. The drawbacks of the conventional common-source circuit are its IM2 characteristics and its inability to reject common-mode interference.

Assume that the current mirror ratio is A as shown in Fig. 1(a). This states that without any RF signal present, the drain–source current of M_1 equals AI_B. The dc block capacitors C are assumed to act as short-circuits at RF. From Fig. 1(a), the bias current I_B can be expressed as

$$I_B = \frac{K}{2}\frac{W}{L}\frac{V_{\rm eff}^2}{1+\theta V_{\rm eff}} \tag{4}$$

where $V_{\rm eff} = V_{\rm GS0} - V_T$ and $V_{\rm GS0}$ is the bias voltage at the gates of $M_1 - M_2$ and M_B. Assume that the RF input signal can be expressed as

$$v_{\rm RF+}(t) = -v_{\rm RF-}(t) = v_{\rm in}(t). \tag{5}$$

By using (2) and (4), the single-ended output current $i_{\rm out+}$ of the RF input transconductor can be written as [19]

$$\begin{aligned} i_{\rm out+} &= \frac{K}{2}\frac{AW}{L}\frac{(V_{\rm eff}+v_{\rm in}(t))^2}{1+\theta(V_{\rm eff}+v_{\rm in}(t))} \\ &= AI_B\frac{(1+\beta v_{\rm in}(t))^2}{1+\alpha v_{\rm in}(t)} \end{aligned} \tag{6}$$

where

$$\alpha = \frac{\theta}{1+\theta V_{\rm eff}} \quad \beta = \frac{1}{V_{\rm eff}} \tag{7}$$

By a Taylor expansion of (6), the single-ended output current $i_{\rm out+}$ can be written as

$$\begin{aligned} i_{\rm out+} \approx AI_B + g_m v_{\rm in}(t) + \frac{K}{2}\frac{AW}{L}\frac{v_{\rm in}^2(t)}{(1+\theta V_{\rm eff})^3} \\ - \frac{K}{2}\frac{AW}{L}\frac{\theta v_{\rm in}^3(t)}{(1+\theta V_{\rm eff})^4} + \frac{K}{2}\frac{AW}{L}\frac{\theta^2 v_{\rm in}^4(t)}{(1+\theta V_{\rm eff})^5}\cdots \end{aligned} \tag{8}$$

where

$$g_m = \frac{K}{2}\frac{AW}{L}\frac{(2+\theta V_{\rm eff})V_{\rm eff}}{(1+\theta V_{\rm eff})^2} \tag{9}$$

is the RF input device transconductance.

Equation (8) reveals the drawbacks of the conventional common-source transconductor. Firstly, if the RF input signal consists of two closely spaced RF signals

$$\begin{aligned} v_{\rm in}(t) &= v_{\rm in}(\cos(\omega_1 t)+\cos(\omega_2 t)) \\ &= \frac{v_{\rm RF}}{2}(\cos(\omega_1 t)+\cos(\omega_2 t)) \end{aligned} \tag{10}$$

where $v_{\rm RF}$ is the differential RF amplitude, the dc component of the RF transconductor output current is not exactly AI_B, but it also depends on the RF input signal amplitude [21]

$$\begin{aligned} I_{\rm DC} = \Bigg(AI_B + \frac{K}{2}\frac{AW}{L}\frac{v_{\rm RF}^2}{4(1+\theta V_{\rm eff})^3} \\ + \frac{K}{2}\frac{AW}{L}\frac{\theta^2 v_{\rm RF}^4}{16(1+\theta V_{\rm eff})^5}\Bigg). \end{aligned} \tag{11}$$

This can result in additional distortion in the mixer switches, because the bias current of the switching quad also now depends on the RF signal amplitude.

The output current also includes an IM2 component due to the square term in (8). In a perfectly balanced mixer, this component is cancelled in the mixer's differential output. However, in the presence of mismatches, the cancellation is not perfect. Therefore, in the sense of the entire mixer IIP2, the presence of the IM2 component in the single-ended output current is a clear drawback of the common-source RF transconductor.

The IIP2 of the common-source RF input transconductor, measured at the single-ended output, can be approximated from (8) as [21]

$$v_{\rm IIP2} = 2V_{\rm eff}(1+\theta V_{\rm eff})(2+\theta V_{\rm eff}) \approx 4V_{\rm eff} \tag{12}$$

which represents the differential RF input voltage. Each MOS device in Fig. 1(a) experiences half of this voltage. Similarly, the IIP3 of the common-source RF input transconductor can be estimated from (8) as [21]

$$v_{\rm IIP3} = \frac{4}{\sqrt{3}}\sqrt{\frac{V_{\rm eff}(2+\theta V_{\rm eff})}{\theta}}(1+\theta V_{\rm eff}) \approx 4\sqrt{\frac{2}{3}\frac{V_{\rm eff}}{\theta}}. \tag{13}$$

The approximations in (12) and (13) hold if $\theta V_{\rm eff} \ll 1$. It is seen that the IIP3 of the common-source transconductor is by a factor of $\sqrt{1+2/(\theta V_{\rm eff}(2+\theta V_{\rm eff}))}$ higher than the IIP3 of the differential pair biased at equal $V_{\rm eff}$. If $\theta V_{\rm eff} \ll 1$, the difference

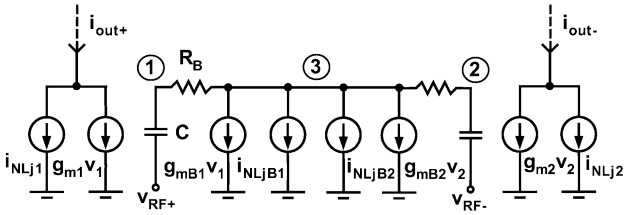

Fig. 2. Equivalent circuit model for computation of second- and third-order intermodulation products in proposed common-source RF transconductor.

is about $\sqrt{1+2/(\theta V_{\rm eff}(2+\theta V_{\rm eff}))} \approx 1/\sqrt{\theta V_{\rm eff}}$, which therefore decreases as $V_{\rm eff}$ is increased.

C. Proposed Common-Source RF Input Transconductor

Fig. 1(b) illustrates a simple biasing circuit technique for cancelling IM2 distortion in common-source transconductor. In this circuit, the original bias transistor shown in Fig. 1(a) is divided into two equal sized bias devices half the size $W/(2L)$ of the original transistor. Moreover, the differential RF input signal is also applied to the gates of the bias transistors.

To understand the operation of the proposed transconductor, the nonlinear characteristics of the circuit is now analyzed by applying the direct calculation method of nonlinear responses described in [23]. The equivalent circuit that has to be solved for the computation of IM2 and third-order intermodulation (IM3) products in the proposed common-source RF transconductor is illustrated in Fig. 2. In this model, each current source $i_{{\rm NL}jx}$ corresponds to the jth-order nonlinear current source of MOS transistor x. Moreover, it is assumed that the MOS transistor is modeled with $i_{\rm DS}-v_{\rm GS}$ relationship given by (2) and the only nonlinearity for simplicity is the nonlinear transconductance of the MOS device.

Suppose that the load of the LNA driving the I/Q mixers consists of an *LC* resonator, as usual. This implies that at low frequencies and at the harmonics of the RF signal, the LNA load can be treated as a short circuit. Equivalently, for the purpose of calculation of the corresponding IM2 products and harmonics in the circuit shown in Fig. 1(b), the nodes $v_{\rm RF+}$ and $v_{\rm RF-}$ are short-circuited to ground.

Assume that the RF input signal consists of two closely spaced signals ω_1 and ω_2 both with single-ended amplitude of $v_{\rm in}$. Thus, first-order response of the circuit is simply

$$i_{{\rm out}+,\omega_1} = -i_{{\rm out}-,\omega_1} = g_{m1}v_{\rm in} \tag{14}$$

where g_{m1} is given by (9).

Computation of Intermodulation (IM) Product at $\Delta\omega = (\omega_1-\omega_2)$: To see how the IM2 cancellation technique works, it is important to understand how the IM2 product itself is generated at the transconductor output. In general, the IM2 product at the output current of the nonlinear transconductance, such as a single MOS or bipolar transistor, is given as [23]

$$\begin{aligned} i_{{\rm out}+,\Delta\omega} &= i_{\rm NL2} + g_m v_{{\rm contr},\Delta\omega} \\ &= K_{2_{g_m}} v_{{\rm contr},\omega_1}^2 + g_m v_{{\rm contr},\Delta\omega} \\ &= \frac{1}{2}\frac{\partial g_m}{\partial v_{\rm contr}} v_{{\rm contr},\omega_1}^2 + g_m v_{{\rm contr},\Delta\omega} \end{aligned} \tag{15}$$

where g_m is the transconductance, $v_{\rm contr}$ is the voltage (i.e., $v_{\rm GS}$ of MOS device) that controls the nonlinear transconductance, and $K_{2_{g_m}}$ is the second-order nonlinearity coefficient of the nonlinear transconductance. It is seen that $i_{{\rm out}+,\Delta\omega}$ consists of two different components. The first component is due to the second-order nonlinearity coefficient $K_{2_{g_m}}$ of the transconductor. This term also depends on the value of the control voltage $v_{{\rm contr},\omega_1}$ at the fundamental frequency ω_1. On the other hand, the value of the control voltage $v_{{\rm contr},\Delta\omega}$ at $\Delta\omega$ has also effect on $i_{{\rm out}+,\Delta\omega}$ via transconductance g_m, as seen from (15). Now, if by some means the value of the control voltage $v_{{\rm contr},\Delta\omega} = -i_{\rm NL2}/g_m$ at $\Delta\omega$ can be generated, the IM2 component at the transconductor output can be cancelled. This is exactly what the bias circuit of the proposed transconductor does, as now will be shown.

With the information from the first-order response, the IM2 product at $\Delta\omega$ can be computed. For this purpose, nonlinear current sources $i_{\rm NL21}-i_{\rm NL22}$ and $i_{\rm NL2B1}-i_{\rm NL2B2}$ of order two that correspond to the transconductance of transistors M_1-M_2 and $M_{B1}-M_{B2}$, respectively, are applied and these sources are placed in parallel with the linearized equivalent transconductance, as illustrated in Fig. 2. Here

$$\begin{aligned} i_{\rm NL2B1} = i_{\rm NL2B2} &= \frac{1}{2}\frac{\partial g_{mB1}}{\partial v_{\rm GS}} v_{\rm in}^2 \\ i_{\rm NL21} = i_{\rm NL22} &= \frac{1}{2}\frac{\partial g_{m1}}{\partial v_{\rm GS}} v_{\rm in}^2. \end{aligned} \tag{16}$$

Next, the linearized network shown in Fig. 2 is solved. It should be noticed, however, that the admittance of the dc blocking capacitor C is now given as $Y_C = j\Delta\omega C$. Furthermore, since $\Delta\omega \approx 0$, capacitor C can be replaced by an open circuit. From Fig. 2, the control voltages v_1 and v_2 at nodes 1 and 2, respectively, are given simply as

$$v_1 = v_2 = -\frac{i_{\rm NL2B1}}{g_{mB1}}. \tag{17}$$

Then, the IM2 product in the single-ended output current of the proposed RF transconductor is given as

$$i_{{\rm out}+,\Delta\omega} = i_{\rm NL21} + g_{m1}v_1 = \frac{v_{\rm in}^2}{2}\left(\frac{\partial g_{m1}}{\partial v_{\rm GS}} - \frac{g_{m1}}{g_{mB1}}\frac{\partial g_{mB1}}{\partial v_{\rm GS}}\right) \tag{18}$$

where (16) and (17) have been used and g_{m1} is given in (9). Moreover, since

$$g_{mB1} = \frac{g_{m1}}{2A}, \qquad \frac{\partial g_{mB1}}{\partial v_{\rm GS}} = \frac{1}{2A}\frac{\partial g_{m1}}{\partial v_{\rm GS}} \tag{19}$$

the control voltage v_1 given by (17) can be expressed as

$$v_1 = -\frac{i_{\rm NL2B1}}{g_{mB1}} = -\frac{2A}{g_{m1}}\frac{i_{\rm NL21}}{2A} = -\frac{i_{\rm NL21}}{g_{m1}} \tag{20}$$

and thus

$$i_{{\rm out}+,\Delta\omega} = \frac{v_{\rm in}^2}{2}\left(\frac{\partial g_{m1}}{\partial v_{\rm GS}} - 2A\cdot\frac{1}{2A}\frac{\partial g_{m1}}{\partial v_{\rm GS}}\right) = 0. \tag{21}$$

Thus, the proposed bias circuit at $\Delta\omega$ generates the required control voltage, which cancels the IM2 component at the common-source transistor output.

The fact that the single-ended output current of the proposed RF input transconductor does not display any IM2 components is a clear improvement on the conventional common-source RF transconductor with respect to the IIP2 of the entire mixer. Moreover, since the IM2 product in the single-ended output current is zero, the corresponding second-order Volterra kernel $|H_2(j\omega_1, -j\omega_1)|$ also equals zero. Correspondingly, the dc component of the transconductor output current given by [23]

$$I_{\rm DC} = AI_B + \frac{1}{2}\hat{v}_{\rm in}^2|H_2(j\omega_1, -j\omega_1)| = AI_B \qquad (22)$$

does not depend on the RF input signal amplitude. Instead, the dc component is exactly AI_B, as desired. This is another advantage of the proposed transconductor compared to the conventional common-source RF transconductor, in which the dc component depends on the RF input signal amplitude [see (11)].

Computation of IM Product at $(2\omega_1 - \omega_2)$*:* By using the information from the first- and second-order response, the IM3 product can be computed. The nonlinear current sources of order three $i_{\rm NL31} - i_{\rm NL32}$ and $i_{\rm NL3B1} - i_{\rm NL3B2}$ are given as

$$\begin{aligned} i_{\rm NL3B1} &= -i_{\rm NL3B2} = \frac{i_{\rm NL31}}{2A} = -\frac{i_{\rm NL32}}{2A} \\ &= -\frac{AKW}{2L}\frac{(4+3\theta V_{\rm eff}(2+\theta V_{\rm eff}))}{4V_{\rm eff}(2+\theta V_{\rm eff})(1+\theta V_{\rm eff})^4}v_{\rm in}^3. \end{aligned} \qquad (23)$$

Notice that the circuit shown in Fig. 2 at $(2\omega_1 - \omega_2)$ is excited with current sources $i_{\rm NL3B1}$ and $i_{\rm NL3B2}$ having equal magnitude and opposite sign. Thus, these currents sum up to zero in node 3. Equivalently, no current flows through the resistors R_B and thus $v_3 = v_1 = v_2 = 0$. Therefore, the IM3 product in the single-ended output current of the proposed RF transconductor is given as

$$i_{\rm out+,(2\omega_1-\omega_2)} = g_{m1}v_1 + i_{\rm NL31} = i_{\rm NL31}. \qquad (24)$$

The IIP3 of the transconductor is found by setting the magnitudes of the fundamental response and the IM3 product in the single-ended output current as equal or $i_{\rm out+,(2\omega_1-\omega_2)} = i_{\rm NL31} = g_{m1}v_{\rm in}$. By solving $v_{\rm in}$ and by multiplying the result by two in order to represent the differential input voltage, the IIP3 of the proposed transconductor is finally given as

$$v_{\rm IIP3} = \frac{4V_{\rm eff}(1+\theta V_{\rm eff})(2+\theta V_{\rm eff})}{\sqrt{4+3\theta V_{\rm eff}(2+\theta V_{\rm eff})}} \approx 4V_{\rm eff} \qquad (25)$$

where the approximation holds if $\theta V_{\rm eff} \ll 1$.

It is seen that the IIP3 of the proposed transconductor is larger than the IIP3 of the differential pair by a factor of $\sqrt{3(2+\theta V_{\rm eff}(2+\theta V_{\rm eff}))/4+3\theta V_{\rm eff}(2+\theta V_{\rm eff})}$ when biased at equal $V_{\rm eff}$. At small $V_{\rm eff}$ $(\theta V_{\rm eff} \ll 1)$, the difference is about $\sqrt{3/2}$ i.e., 1.8 dB. However, at large $V_{\rm eff}$ $(\theta V_{\rm eff} \gg 1)$, the transconductors have approximately equal IIP3. On the other hand, compared to the conventional common-source transconductor, the proposed RF transconductor has by a factor of $\sqrt{(4+3\theta V_{\rm eff}(2+\theta V_{\rm eff}))/(3\theta V_{\rm eff}(2+\theta V_{\rm eff}))} \approx \sqrt{(2)/3\theta V_{\rm eff}}$ smaller IIP3 at given bias assuming $\theta V_{\rm eff} \ll 1$.

Although the presented transconductor has an IM2 distortion performance similar to the differential pair, it has one clear advantage. Namely, that the proposed circuit is more suitable for operation at low supply voltage. This is because the proposed RF transconductor shown in Fig. 1(b) has only one device stacked between the transconductor input and output, whereas the conventional differential pair has two devices consuming voltage headroom.

IV. Intermodulation Distortion in Degenerated Bipolar RF Transconductors

In this section, the intermodulation distortion characteristics of the resistively degenerated bipolar differential pair, common-emitter, and proposed common-emitter RF input transconductors are analyzed and compared. Resistive degeneration is considered, since typically the bipolar RF transconductors are linearized by degeneration, unlike CMOS RF transconductors. All the compared transconductors have equal bias current, equal degeneration, and equal device sizes. Thus, all the transconductors have equal RF input stage transconductance. It is assumed that the dominant nonlinearity is the nonlinear transconductance of the bipolar transistor.

A. Degenerated Bipolar Differential Pair RF Input Transconductor

As with CMOS, a traditional bipolar Gilbert mixer employs a differential pair RF input transconductor to provide common-mode rejection and to minimize second-order distortion. If the bipolar transistor is modeled with its exponential relationship

$$i_C = I_S e^{\frac{v_{BE}}{V_t}} \qquad (26)$$

and the differential pair is biased by a tail current $2A \cdot I_B$, the IIP3 of the degenerated differential pair can be expressed as [21]

$$v_{\rm IIP3} = 4V_t(1+g_mR_E)^{3/2} \qquad (27)$$

where $g_m = AI_B/V_t, R_E$ is the emitter degeneration resistance, and g_mR_E is the loop gain of the negative feedback. Again, since the single-ended output current $i_{\rm out+}$ of the differential pair transconductor does not display any second-order components, the input stage IIP2, measured from the single-ended output of the differential pair transconductor, is ideally infinite.

B. Degenerated Common-Emitter RF Input Transconductor

The conventional resistively degenerated common-emitter mixer RF input transconductance stage is illustrated in Fig. 3(a). Suppose that the current mirror ratio is A as shown in Fig. 3(a). The bias device Q_{Bb} provides base currents for the main bias device Q_b and RF devices Q_1 and Q_2.

Assume that the RF input signal of the transconductor consists of two closely spaced signals as given by (10). Then, the dc component of the degenerated common-emitter transconductor output current depends also on the RF input signal amplitude [21]. This is not desirable, because now the bias currents of the mixer switching devices also depend on the RF signal amplitude.

The single-ended output current of the degenerated common-emitter RF transconductor includes also an IM2 component,

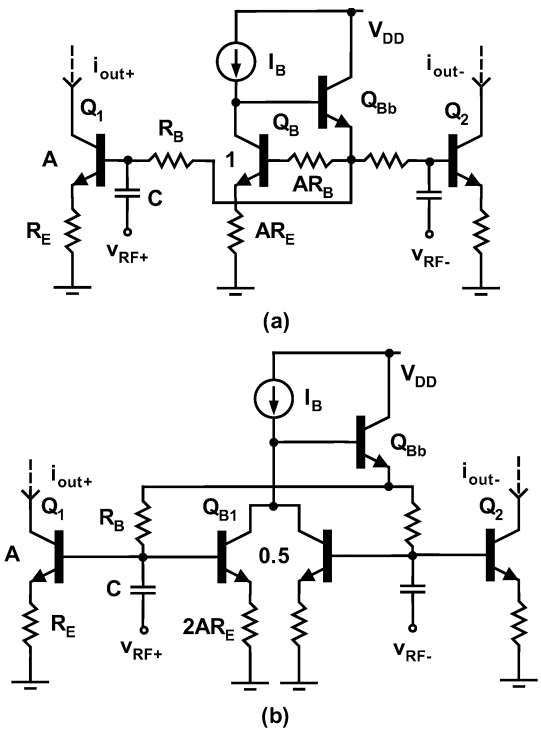

Fig. 3. (a) Traditional and (b) proposed resistively degenerated common-emitter RF input transconductor.

which is a drawback of the common-emitter RF input transconductor. The corresponding input stage IIP2, measured at the single-ended transconductor output, is given by [21]

$$v_{\mathrm{IIP2}} = 4V_t(1+g_mR_E)^2 \tag{28}$$

which represents the differential input amplitude. Feedback improves the degenerated common-emitter RF input transconductor second-order linearity compared to the transconductor without degeneration, but at the expense of the reduced input stage transconductance. Moreover, the feedback does not totally remove the IM2 distortion.

The output current of the degenerated common-emitter RF transconductor also displays a third-order intermodulation component. The corresponding input stage IIP3 can be expressed as [21]

$$v_{\mathrm{IIP3}} = 4\sqrt{2}V_t\frac{(1+g_mR_E)^2}{\sqrt{|1-2g_mR_E|}}. \tag{29}$$

The IIP3 of the degenerated common-emitter RF transconductor is higher by a factor of $\sqrt{2(1+g_mR_E))/(|1-2g_mR_E|}$ than the corresponding IIP3 of the degenerated differential pair given by (27). If $g_mR_E \gg 1$, the transconductors have approximately equal IIP3.

C. Proposed Degenerated Common-Emitter RF Input Transconductor

Fig. 3(b) shows the bipolar realization of the biasing circuit technique presented for MOS devices in Fig. 1(b). Again, the original bias transistor shown in Fig. 3(a) is divided into two

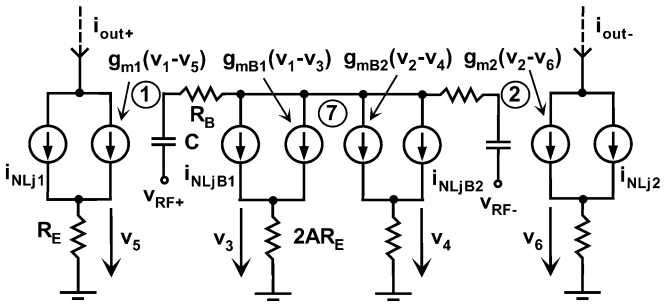

Fig. 4. Equivalent circuit model for computation of second- and third-order intermodulation products in proposed resistively degenerated common-emitter RF transconductor.

equal sized bias devices half the size of the original transistor. The values of the emitter resistances are also doubled. Notice that although the proposed bipolar transconductor is presented with degeneration, the biasing technique also applies to the common-emitter circuit without degeneration.

The proposed bipolar transconductor circuit operates exactly similarly as the CMOS counterpart. In this case, the equivalent circuit that has to be solved for the computation of second- and third-order intermodulation products in the proposed degenerated common-emitter RF transconductor is illustrated in Fig. 4.

In this case, the fundamental response of the circuit is simply

$$i_{\mathrm{out}+,\omega_1} = -i_{\mathrm{out}-,\omega_1} = \frac{g_{m1}}{1+g_{m1}R_E}v_{\mathrm{in}}. \tag{30}$$

Computation of IM Product at $\Delta\omega = (\omega_1 - \omega_2)$: The second-order nonlinear current sources $i_{\mathrm{NL21}} - i_{\mathrm{NL22}}$ and $i_{\mathrm{NL2}B1} - i_{\mathrm{NL2}B2}$ that correspond to the transconductance of transistors $Q_1 - Q_2$ and $Q_{B1} - Q_{B2}$, respectively, are given as

$$i_{\mathrm{NL2}B1} = i_{\mathrm{NL2}B2} = \frac{i_{\mathrm{NL21}}}{2A} = \frac{i_{\mathrm{NL22}}}{2A} = \frac{I_B}{4}\frac{v_{\mathrm{in}}^2}{(1+g_{m1}R_E)^2V_t^2}. \tag{31}$$

Again, the capacitor C can be replaced by an open circuit. From Fig. 4, the control voltage $(v_1 - v_5)$ is given as

$$v_1 - v_5 = v_1 = -\frac{i_{\mathrm{NL}B1}}{g_{mB1}} = -\frac{v_{\mathrm{in}}^2}{2(1+g_{m1}R_E)^2V_t}. \tag{32}$$

Finally, the IM2 product in the single-ended output current of the proposed RF transconductor is given as

$$\begin{aligned} i_{\mathrm{out}+,\Delta\omega} &= g_{m1}(v_1 - v_5) + i_{\mathrm{NL21}} \\ &= -\frac{AI_B}{V_t}\cdot\frac{v_{\mathrm{in}}^2}{2(1+g_{m1}R_E)^2V_t} \\ &\quad + \frac{AI_B}{2}\frac{v_{\mathrm{in}}^2}{(1+g_{m1}R_E)^2V_t^2} = 0 \end{aligned} \tag{33}$$

where (31) and (32) have been used.

From (33), it is seen that the single-ended output current of the proposed bipolar RF input transconductor does not have any IM2 components. Again, this is a significant improvement on the conventional common-emitter RF transconductor. Moreover, as with the proposed CMOS transconductor, the dc component of the proposed bipolar transconductor output current does not depend on the RF input signal amplitude.

Computation of IM Product at $(2\omega_1 - \omega_2)$*:* Here, the nonlinear current sources of order three $i_{\mathrm{NL31}} - i_{\mathrm{NL32}}$ and $i_{\mathrm{NL3}B1} - i_{\mathrm{NL3}B2}$ are given as

$$\begin{aligned} i_{\mathrm{NL3}B1} &= -i_{\mathrm{NL3}B2} = \frac{i_{\mathrm{NL31}}}{2A} = -\frac{i_{\mathrm{NL32}}}{2A} \\ &= -\frac{I_B}{16}\frac{v_{\mathrm{in}}^3}{(1+g_{m1}R_E)^4 V_t^3}(1+2g_{m1}R_E). \end{aligned} \quad (34)$$

As with CMOS, the circuit shown in Fig. 4 at $(2\omega_1 - \omega_2)$ is excited with current sources $i_{\mathrm{NL3}B1}$ and $i_{\mathrm{NL3}B2}$ having equal magnitude and opposite sign. Thus, these currents sum up to zero in node 7. For the same reason, $v_3 = -v_4$ and the currents $g_{mB1}(v_1 - v_3)$ and $g_{mB2}(v_2 - v_4)$ cancel each other in node 7. Equivalently, this implies that $v_7 = 0$ and thus $v_1 = v_2 = 0$. Therefore, the control voltage $(v_1 - v_5)$ is given as

$$v_1 - v_5 = -v_5 = -\frac{R_E}{1+g_{m1}R_E} i_{\mathrm{NL31}} \quad (35)$$

and the IM3 product in the single-ended output current of the proposed RF transconductor can be expressed as

$$\begin{aligned} i_{\mathrm{out}+,(2\omega_1-\omega_2)} &= -g_{m1}v_5 + i_{\mathrm{NL31}} \\ &= -\frac{AI_B}{8}\frac{v_{\mathrm{in}}^3}{(1+g_{m1}R_E)^5 V_t^3}(1+2g_{m1}R_E) \end{aligned} \quad (36)$$

where (34) and (35) have been used. By setting the magnitudes of the first-order response and the IM3 product in the single-ended output current as equal, the IIP3 of the proposed transconductor is finally given as

$$v_{\mathrm{IIP3}} = 4\sqrt{2}V_t\frac{(1+g_{m1}R_E)^2}{\sqrt{1+2g_{m1}R_E}}. \quad (37)$$

The IIP3 of the proposed degenerated common-emitter RF transconductor is higher by a factor of $\sqrt{2(1+g_mR_E))/((1+2g_mR_E)}$ than the corresponding IIP3 of the degenerated differential pair given by (27). The difference between the IIP3 of the proposed approach and differential pair transconductor is at the largest $\sqrt{2}$ i.e., 3 dB corresponding no feedback or $R_E = 0$. With a very large feedback loop gain $(g_mR_E \gg 1)$, the transconductors have approximately equal IIP3.

The IIP3 of the degenerated common-emitter RF transconductor is higher by a factor of $\sqrt{(1+2g_mR_E)/|1-2g_mR_E|}$ than the corresponding IIP3 of the presented approach. On the other hand, if $g_mR_E \ll 1/2$ or $g_mR_E \gg 1/2$, the transconductors have approximately equal IIP3. Finally, as with CMOS, the proposed bipolar transconductor is more suitable for operation at low supply voltage than the traditional bipolar differential pair.

V. Nonidealities of Proposed Transconductor

In this section, the effects of the nonidealities on the performance of the proposed transconductor are considered. The effects of the mismatch, finite output impedance of the bias circuit, noise, finite transconductor input impedance, common-mode rejection, and common-mode linearity are discussed and analyzed. Only the MOS transconductor is considered, but most of the analysis applies directly as such also to the bipolar counterpart.

Mismatch: The presented technique for the cancellation of the IM2 distortion at the common-source transconductor output relies on the matching of the main devices $M_1 - M_2$ and bias devices $M_{B1} - M_{B2}$ shown in Fig. 1. Thus, if mismatch exists i.e., between the threshold voltages V_T of the devices, residual IM2 distortion is generated. Assume that the threshold voltages of M_1 and M_{B1} are given as $V_{T1} = V_T + \Delta V_T/2$ and $V_{TB1} = V_T - (\Delta V_T)/(2)$, respectively, where ΔV_T is the mismatch in the threshold voltages of M_1 and M_{B1}. Then, it can be shown that the IM2 product in the single-ended output current of the proposed RF transconductor is given as

$$\begin{aligned} i_{\mathrm{out}+,\Delta\omega} &= \frac{v_{\mathrm{in}}^2}{2}\frac{AKW}{L}\frac{(1+2\theta V_{\mathrm{eff}})\left(3\theta^2V_{\mathrm{eff}}^2 + 6\theta V_{\mathrm{eff}} + 2\right)}{V_{\mathrm{eff}}(2+\theta V_{\mathrm{eff}})(1+\theta V_{\mathrm{eff}})^5} \\ &\times \Delta V_T \approx \frac{v_{\mathrm{in}}^2}{2}\frac{AKW}{L}\frac{\Delta V_T}{V_{\mathrm{eff}}} \end{aligned} \quad (38)$$

and the corresponding IIP2 can be approximated as

$$v_{\mathrm{IIP2}} \approx \frac{4V_{\mathrm{eff}}^2}{\Delta V_T}. \quad (39)$$

The approximations in (38) and (39) hold if $\theta V_{\mathrm{eff}} \ll 1$. The effects of the other mismatches can be analyzed similarly. From (39), it is seen that the effect of the threshold voltage mismatch on the transconductor IIP2 decreases at higher overdrive voltages V_{eff}.

Finite Output Impedance of Bias Circuit: Finite output impedances of the bias transistors $M_{B1} - M_{B2}$ and current source I_B have also effect on the cancellation of the IM2 distortion at the presented common-source transconductor output. Assume that the total parallel output impedance of the bias circuit is $R_{\mathrm{out},B}$. Then, by carrying out the analysis presented in Section III-C, it can be shown that in the presence of the finite bias circuit output impedance, the IM2 product in the single-ended output current of the proposed RF transconductor is given as

$$\begin{aligned} i_{\mathrm{out}+,\Delta\omega} &= \frac{v_{\mathrm{in}}^2}{2}\frac{A^2KW}{L}\frac{1}{(1+\theta V_{\mathrm{eff}})^3(A+g_{m1}R_{\mathrm{out},B})} \\ &\approx \frac{v_{\mathrm{in}}^2}{2}\frac{A^2KW}{L}\frac{1}{(A+g_{m1}R_{\mathrm{out},B})} \end{aligned} \quad (40)$$

and the corresponding IIP2 is then

$$\begin{aligned} v_{\mathrm{IIP2}} &= \frac{2V_{\mathrm{eff}}(1+\theta V_{\mathrm{eff}})(2+\theta V_{\mathrm{eff}})(A+g_{m1}R_{\mathrm{out},B})}{A} \\ &\approx \frac{4V_{\mathrm{eff}}(A+g_{m1}R_{\mathrm{out},B})}{A}. \end{aligned} \quad (41)$$

Noise: By applying a straightforward circuit analysis, it can be shown that the differential mean square current noise at the proposed CMOS transconductor output is given as

$$\begin{aligned} &\overline{(i_{\mathrm{out}\,n+} - i_{\mathrm{out}\,n-})^2} \\ &= 2\left(\overline{i_{d,1}^2} + g_{m1}^2R_{\mathrm{out,LNA}}^2\left(\overline{i_{g,1}^2} + \overline{i_{g,B1}^2} + \overline{i_{R_B}^2}\right)\right) \\ &= 2\cdot 4kTB\left(\frac{\gamma g_{m1}}{\alpha} + g_{m1}^2R_{\mathrm{out,LNA}}^2\left(\frac{\alpha\delta g_{m1}}{5}\left(\frac{\omega_0}{\omega_{T1}}\right)^2\right.\right. \\ &\quad \left.\left. + \frac{\alpha\delta g_{mB1}}{5}\left(\frac{\omega_0}{\omega_{TB1}}\right)^2 + \frac{1}{R_B}\right)\right) \end{aligned} \quad (42)$$

where $R_{\text{out,LNA}}$ is output resistance of the LNA, $\overline{i_{d,1}^2}$ and $\overline{i_{g,1}^2}$ are the channel thermal noise and gate-induced current noise of M_1 (and M_2), $\overline{i_{g,B1}^2}$ is the gate-induced current noise of M_{B1} (and M_{B2}), and $\overline{i_{R_B}^2}$ is the thermal noise due to R_B. Moreover, $\alpha = g_m/g_{d0}, g_{d0}$ is the zero bias drain conductance, γ is the channel current noise factor, δ is the gate induced current noise factor [22], and $\omega_{T1} = g_{m1}/C_{gs1}$ and $\omega_{TB1} = g_{mB1}/C_{gsB1}$ are the unity-current gain angular frequencies of M_1 and M_{B1}, respectively. Notice that the channel thermal noise of the bias devices does not appear at the differential output of the transconductor, since this noise voltage is seen as a common-mode voltage at gates of M_1 and M_2. Equation (42) also neglects the noise contributions of the gate and substrate resistances, since these noise contributions can be reduced to insignificant levels by choosing the number of gate fingers accordingly [24], [25].

Suppose that the proposed transconductor as well as the conventional common-source and differential pair transconductors employ equal value of resistor R_B to supply the dc voltage level for the gates of the transconductors. Actually, if the value of R_B is sufficiently large, its noise contribution is negligible. Then, it is easy to show that if the gate-induced current noise of M_{B1} and M_{B2} can be neglected, all the transconductors biased at equal current have equivalent noise performance, provided that equal device sizes are employed.

Since both M_1 and M_{B1} are biased at equal V_{eff} and their channel lengths are equal, $\omega_{TB1} \approx \omega_{T1}$ [24]. In addition, since $g_{m1} = 2Ag_{mB1}$ [see (19)], the noise contribution of $\overline{i_{g,B1}^2}$ is $2A$ times smaller than the noise contribution of $\overline{i_{g,1}^2}$. Since the current mirror ratios A of five or larger are common, the gate induced current noise of M_{B1} is at least ten times smaller than the gate induced current noise of M_1. Moreover, in submicron technologies with practical cases of interest, the frequency of operation ω_0 is much smaller than ω_T and therefore $(\omega_0/\omega_T)^2 \ll 1$. Thus, in practice the noise contributions of both $i_{g,1}^2$ and $\overline{i_{g,B1}^2}$ are negligible compared to the channel thermal noise of M_1. It can be therefore concluded that the proposed transconductor has similar noise performance as the conventional common-source and differential pair transconductors with equal bias and device dimensions.

Finite Transconductor Input Impedance: The differential input impedance of the proposed transconductor can be approximated as $Z_{\text{in}} = 2R_B/(s(C_{gs1} + C_{gsB1})R_B + 1) \approx 2/(s(C_{gs1} + C_{gsB1}))$. Thus, compared to the conventional common-source and differential pair transconductors, the proposed transconductor exhibits larger input capacitance due to C_{gsB1} of the bias devices. However, if the current mirror ratio A is reasonable, this additional input capacitance is not usually problematic. Moreover, since the load of the LNA driving the I/Q mixers usually consists of an *LC* resonator, the input capacitance of the proposed transconductor at the operation frequency can be tuned out by the inductor of the resonator.

Common-Mode Rejection: The drawback of the proposed and conventional common-source transconductor is their inability to reject common-mode signals. Thus, if the transconductor is driven by a common-mode RF signal with $v_{\text{RF}+} = v_{\text{RF}-} = v_{\text{in}}$, the single-ended transconductor output currents have equal magnitude and phase, i.e., $i_{\text{out}+} = i_{\text{out}-} = g_{m1}v_{\text{in}}$. Fortunately, if the mixer switching devices are driven by RF currents with equal phase, the switching quad does not downconvert these RF signals. Thus, although the RF input stage does not provide any common-mode rejection, the mixer core itself will reject common-mode RF currents.

Common-Mode Linearity: Consider the effect of the common-mode excitation (i.e., $v_{\text{RF}+} = v_{\text{RF}-} = v_{\text{in}}$) on the proposed transconductor linearity. It is easy to show that if the transconductor is driven by a common-mode instead of differential RF signal, the corresponding IM2 product at the single-ended transconductor output is still cancelled. This can be seen by carrying out the analysis presented in Section III.C with $v_{\text{RF}+} = v_{\text{RF}-} = v_{\text{in}}$. However, the common-mode excitation has effect on the third-order nonlinearity. This is due to the fact that in the case of common-mode excitation, the circuit shown in Fig. 2 at $(2\omega_1 - \omega_2)$ is excited with current sources $i_{\text{NL3}B1}$ and $i_{\text{NL3}B2}$ having equal magnitude and sign. This results in nonzero control voltages v_1 and v_2, which therefore have effect on the third-order nonlinearity of the main transistors M_1 and M_2. Notice that in the case of differential excitation, the control voltages at $(2\omega_1 - \omega_2)$ have no effect on the transonconductor IIP3, since $v_1 = v_2 = v_3 = 0$ (see Section III.C). Fortunately, it can be shown that by introducing a capacitance between the ground and the common-drain node of the bias devices M_{B1} and M_{B2}, the values of the control voltages v_1 and v_2 at $(2\omega_1 - \omega_2)$ can be approximated as $v_1 = v_2 \approx v_3 \approx 0$. Thus, an equal IIP3 is achieved than in the case of differential excitation. It is also easy to show that this additional capacitance does not have effect on the other properties of the circuit. Moreover, the required capacitance value is in the order of the parasitic capacitance at the common-drain nodes of M_{B1} and M_{B2}, as revealed by simulations. Thus, in practice, no extra capacitor is necessarily required.

VI. Experimental Results

A. CMOS RF Input Transconductors

In this section, the characteristics of CMOS differential pair, common-source, and proposed common-source RF input transconductors are simulated and compared. The circuits are implemented in 0.35-μm BiCMOS technology, in which the supply voltage is 2.7 V. In the simulations, the MOS transistors are modeled by using MOS Model 9 with parasitic gate, substrate, drain and source resistances. The MOS Model 9 includes also model for the gate-induced current noise. The RF input device sizes in all the transconductors are selected as $(W/L) = (50/0.35)$ and a current mirror ratio A of five is used (see Fig. 1). The current source I_B shown in Fig. 1 is implemented with pMOS transistor sized as $(W/L) = (20/0.35)$. Correspondingly, the current source employed in the differential pair is realized with nMOS device sized as $(W/L) = (100/0.35)$.

In the simulations, the different transconductors are biased at equal current. Thus, their transconductances and input referred noise voltages are also equal for fair comparison, as verified by simulations. All the results are presented as input power in

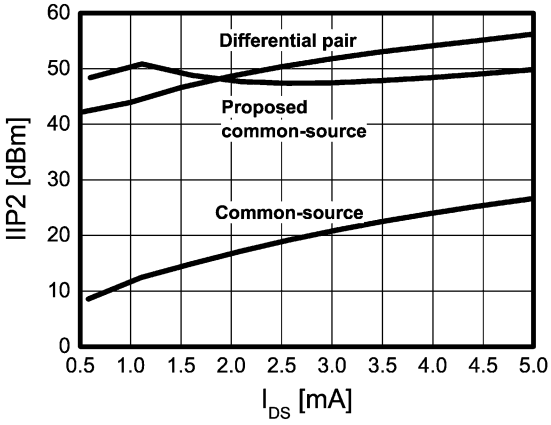

Fig. 5. Single-ended IIP2s of CMOS differential pair, common-source, and proposed common-source RF input transconductors.

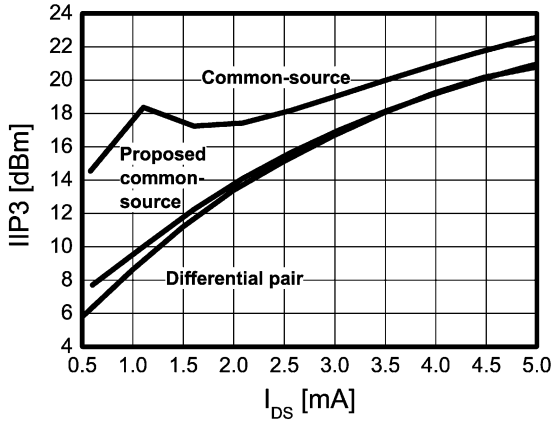

Fig. 6. IIP3s of CMOS differential pair, common-source, and proposed common-source RF input transconductors.

dBm and the differential RF input voltage is referred to a 100-Ω impedance. The simulations are performed at 2 GHz.

The single-ended IIP2s, i.e., measured at the single-ended transconductor output, of the differential pair, common-source, and proposed common-source RF input transconductors are plotted in Fig. 5 as a function of the input device drain–source current $I_{\rm DS}$. It is seen that the proposed common-source and differential pair transconductors exhibit very small IM2 distortion, whereas the single-ended IIP2 of the conventional common-source transconductor is relatively poor compared to the other transconductors. This agrees well with the theoretical derivations of Section III. It can also be seen that the common-source IIP2 can be improved by increasing its $V_{\rm eff}$ or $I_{\rm DS}$ at fixed device dimensions (W/L), as also predicted by (12).

The IIP3s of the differential pair, common-source, and proposed common-source RF input transconductors as a function of the input device $I_{\rm DS}$ are plotted in Fig. 6. It can be seen that the conventional common-source transconductor exhibits less third-order nonlinearity than the other transconductors. However, since the typical requirements for the downconversion mixer IIP3s are in the order of $+5 \ldots +15$ dBm, depending on the radio system and block partitioning, the IIP3s of the proposed common-source and differential pair transconductors shown in Fig. 6 are also sufficient for most applications, assuming that the entire mixer IIP3 is dominated by the RF input stage third-order nonlinearity. Nevertheless, in order to obtain a given IIP3 at fixed device size, the conventional common-source transconductor requires the smallest bias current. It is also noticed that IIP3 of the common-source circuit shows a peaking in the moderate inversion region [26].

It is seen that at low $V_{\rm eff}$ the proposed common-source transconductor has about 1.4 dB larger IIP3 than the differential pair transconductor. This is close to the theoretical value of $\sqrt{3/2}$ or 1.8 dB, as anticipated by comparing (3) and (25) when $\theta V_{\rm eff} \ll 1$. On the other hand, at large $V_{\rm eff}$, the proposed transconductor and differential pair have practically equal IIP3, as predicted with $\theta V_{\rm eff} \gg 1$. It can also be seen that the difference between the IIP3s of the conventional and proposed common-source transconductors decreases as $V_{\rm eff}$ or $I_{\rm DS}$ is increased. This can be understood by comparing (13) and (25).

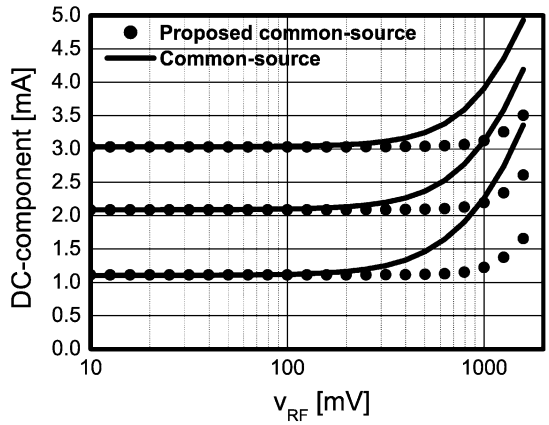

Fig. 7. Output current dc component of common-source and proposed common-source RF transconductors. $I_B = 200, 400$, and $600\ \mu$A and current mirror ratio $A = 5$.

Since the proposed RF transconductor has a smaller IIP3 by a factor of $\sqrt{(4+3\theta V_{\rm eff}(2+\theta V_{\rm eff}))/(3\theta V_{\rm eff}(2+\theta V_{\rm eff}))} \approx \sqrt{(2)/(3\theta V_{\rm eff})}$ than the IIP3 of the common-source transconductor at given bias, the difference between the transconductor IIP3s decreases as $V_{\rm eff}$ is increased. Finally, all the transconductors can be linearized with respect to third-order intermodulation distortion by increasing their $V_{\rm eff}$ or $I_{\rm DS}$ for a given device size.

Fig. 7 illustrates how the dc component of the conventional and proposed common-source transconductor output currents vary, as the differential RF input voltage is applied on the gates of the current mirrored transistors M_1 and M_2. Naturally, it is desired that the dc component does not depend on the level of the RF input signal. The results are presented with a current mirror ratio A of five and three values of bias currents, $I_B = 200$, 400, and 600 μA. The dc component of the transconductor output current without any RF signal present is not exactly AI_B, since the drain–source voltages of the main and bias devices are not exactly equal.

From Fig. 7, it is seen that the RF signal has negligible effect on the dc component of the conventional common-source transconductor output current provided that the RF input amplitude is smaller than 200 mV. However, if the RF input amplitude

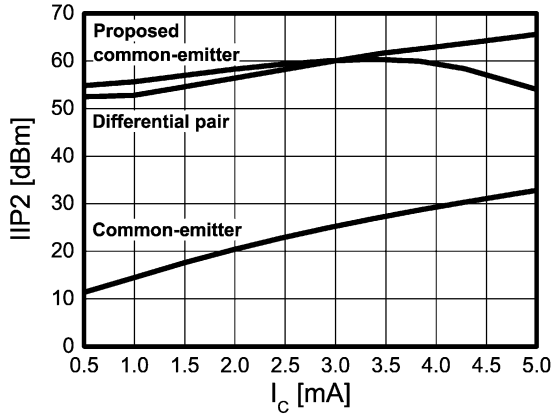

Fig. 8. Single-ended IIP2s of degenerated bipolar differential pair, common-emitter, and proposed common-emitter RF input transconductors.

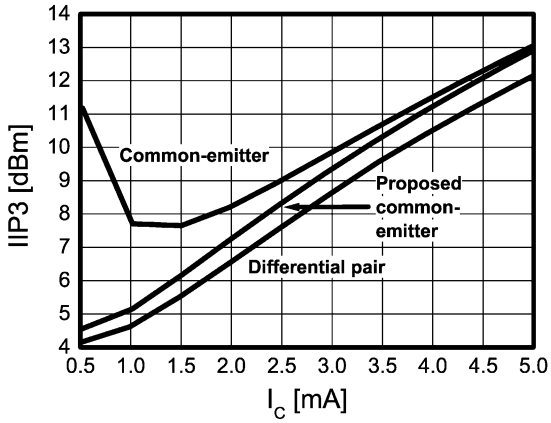

Fig. 9. IIP3s of degenerated bipolar differential pair, common-emitter, and proposed common-emitter RF input transconductors.

of 200 mV or larger is applied, the dc component is seen to depend on the level of the RF signal. On the contrary, the dc component of the proposed common-source transconductor output current is seen to remain very constant even in the presence of RF input amplitudes as large as 800 mV. For the RF amplitudes larger than 800 mV, the dc component also depends much less on the level of the RF input signal compared to the conventional common-source transconductor with equal RF amplitude. This proves that the proposed circuit provides a more stable bias current for the mixer switches, since the dc component is very insensitive to the level of the RF input amplitude. This is important, for instance, in case of blocking, when relatively large RF input signals can be present at the mixer input.

B. Bipolar RF Input Transconductors

In this section, the characteristics of resistively degenerated bipolar differential pair, common-emitter, and proposed common-emitter RF input transconductors are compared by simulations. Again, the transconductors are realized in 0.35-μm BiCMOS technology, in which the supply voltage is 2.7 V. The RF input devices in all the circuits are implemented with bipolar devices with six emitters, two collectors, and emitter length of 10 μm. Each RF transistor has ten transistors in parallel and the current mirror ratio A is five (see Fig. 3). The different transconductors are biased at equal current and their transconductances and differential input referred noise currents and voltages are also equal for fair comparison. This is verified by simulations. All the circuits have resistive degeneration of 30 Ω. As with CMOS, the current source I_B shown in Fig. 3 is implemented with pMOS transistor sized as $(W/L) = (20/0.35)$ whereas the current source employed in the differential pair is realized with nMOS device sized as $(W/L) = (100/0.35)$. The simulations are performed at 2 GHz.

Fig. 8 illustrates the single-ended IIP2s of the degenerated differential pair, common-emitter and proposed common-emitter RF input transconductors as a function of input device collector current I_C. As with MOS, it is seen that the proposed degenerated common-emitter and differential pair transconductors exhibit very small IM2 distortion, whereas the single-ended IIP2 of the conventional degenerated common-emitter transconductor for $I_C < 4$ mA is over 30 dB worse than the IIP2 of the other transconductors. This agrees well with the theoretical derivations of Section IV. It can also be seen that the IIP2 of the degenerated common-emitter transconductor increases rapidly as I_C is increased. As I_C is increased, the input device transconductance g_m is increased and IIP2 is increased proportional to $(1 + g_m R_E)^2$ (see (28)).

The IIP3s of the degenerated differential pair, common-emitter, and proposed common-emitter RF input transconductors are plotted in Fig. 9 as a function of the input device I_C. The difference between the IIP3s of the different transconductors with practical collector currents (i.e., $I_C > 1$ mA) is seen to be much smaller than in the MOS case. It is also seen that the proposed degenerated common-emitter transconductor has slightly larger IIP3 than the degenerated differential pair transconductor. On the other hand, with large values of I_C or $g_m R_E$, the proposed transconductor has equal IIP3 to the traditional degenerated common-emitter transconductor. This was also anticipated by comparing (29) and (37) with large values of loop gain $g_m R_E$. Actually, with large values of I_C or $g_m R_E$, all the different transconductors have almost equal IIP3, as predicted with (27), (29), and (37) with large $g_m R_E$. All the transconductors can be linearized with respect to third-order distortion by increasing their I_C (or R_E). This can be attributed to the increased feedback loop gain, which improves the third-order linearity, as predicted by theoretical derivations.

Fig. 10 illustrates how the dc component of the degenerated common-emitter and proposed common-emitter transconductor output currents vary, as the differential RF input voltage is applied on the base of the current mirrored transistors Q_1 and Q_2 (see Fig. 3). The results are presented with a current mirror ratio A of five and three values of bias currents, $I_B = 200$, 400, and 600 μA.

From Fig. 10, it can be seen that provided that the RF input amplitude is smaller than about 150 mV, the level of the RF signal has negligible effect on the dc component of the degenerated common-emitter output current. However, if the RF amplitude of 150 mV or larger is applied, the dc component depends on the level of the RF signal. On the contrary, it is seen that the dc component of the proposed degenerated common-emitter

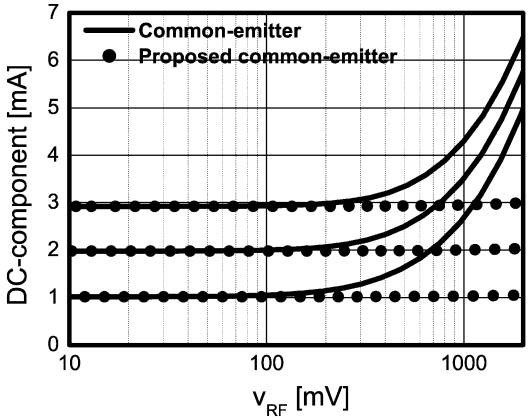

Fig. 10. Output current dc component of degenerated common-emitter and proposed common-emitter RF transconductors. $I_B = 200, 400$, and $600\ \mu$A and current mirror ratio $A = 5$.

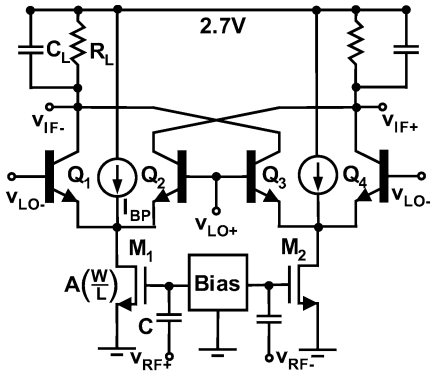

Fig. 11. Schematic of BiCMOS downconversion mixer.

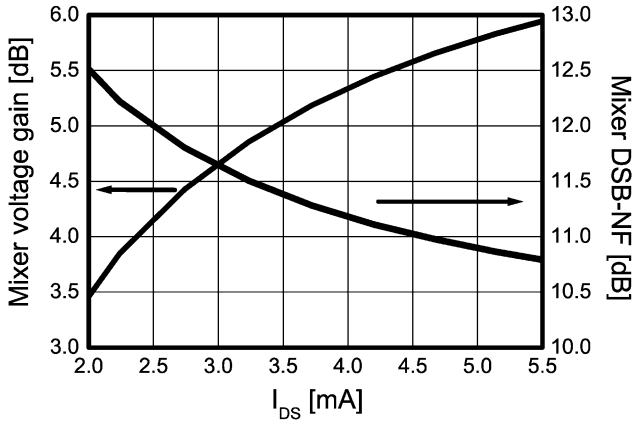

Fig. 12. Voltage conversion gain and DSB-NF of BiCMOS downconversion mixer with conventional and proposed common-source RF input stages.

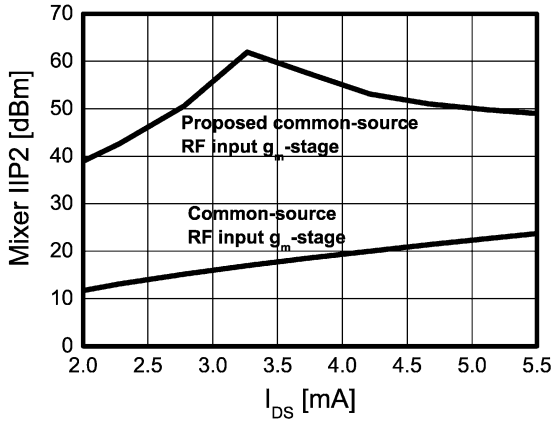

Fig. 13. Single-ended IIP2 of BiCMOS downconversion mixer with conventional and proposed common-source RF input stages.

transconductor output current has negligible dependence on the level of the RF signal, even in the presence of very large RF voltage swings. Thus, again the proposed circuit provides more stable bias current for the mixer switches, since the dc component depends very little on the level of the RF input amplitude.

C. BiCMOS Downconversion Mixer

In this section, the performance of the traditional and proposed common-source RF input transconductors are simulated and compared in an actual downconversion mixer implemented in 0.35-μm BiCMOS technology. The schematic of the mixer is shown in Fig. 11. The same size of RF input and bias devices are used as in Section VI.A. Bipolar transistors $Q_1 - Q_4$ are employed as mixer switches and the LO-voltage swing driving the switching quad is 1.2 V_{PP} differential. The mixer load consists of a first-order low pass filter which attenuates the upper sideband at the output. Here, $R_L = 350\ \Omega$ and capacitor $C_L =$ 20 pF. The current sources I_{BP} allow different bias currents for the RF input stage and switching transistors [27], [28]. In the simulations, the switches in all cases are biased at the constant bias current of 0.75 mA. Thus, the dc current through the single load resistor R_L is 1.5 mA. The simulations are performed at 2 GHz.

Fig. 12 illustrates the mixer voltage conversion gain and double-sideband NF (DSB-NF) at 100 kHz IF frequency as a function of the RF input device drain–source current $I_{\rm DS}$. It is seen that the curves of the different mixers are top on each other. Thus, it is concluded that the mixers utilizing the conventional and proposed common-source RF input transconductors have equal voltage conversion gain and DSB-NF. Moreover, it can be deduced that the proposed RF input transconductor has equivalent noise performance as the traditional common-source transconductor at given bias and device dimensions.

The single-ended IIP2s, i.e., measured at the single-ended mixer output, of the mixers employing traditional and presented common-source RF input stages are shown in Fig. 13 as a function of the RF input device $I_{\rm DS}$. It is seen that the mixer utilizing the proposed RF transconductor has 20–40 dB higher IIP2 than the mixer employing the conventional common-source stage.

Fig. 14 illustrates how the IIP2 of the mixer utilizing the proposed common-source RF input transconductor varies in the presence of mismatches. In the histogram, both the single-ended and differential IIP2s are shown. In this Monte Carlo mismatch simulation, the RF transconductor is biased at $I_{\rm DS} = 3.5$ mA and the simulation has been performed for 1000 samples. The mismatches in MOS devices, bipolar transistors, resistors, and capacitors are considered. Based on this simulation, the mean value (μ) of the single-ended IIP2 is 55.8 dBm, standard deviation (σ) is 5.3 dBm, the minimum IIP2 is 42.5 dBm, and the maximum IIP2 is 129.1 dBm. The corresponding values for the differential IIP2 are $\mu = 97.2$ dBm, $\sigma = 9.3$ DBm, $\mathrm{IIP2}_{\min} =$

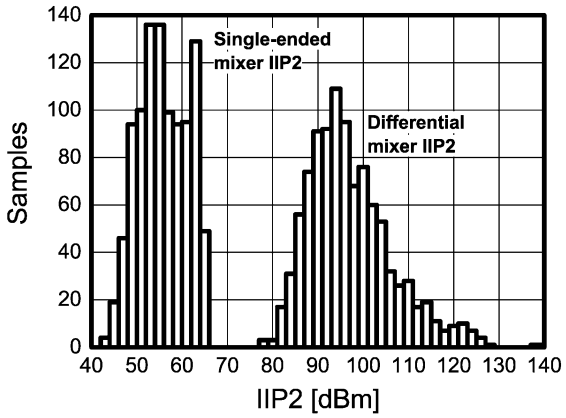

Fig. 14. Effect of device mismatches on IIP2 of mixer utilizing proposed common-source RF input transconductor. In histogram, both single-ended and differential IIP2s are shown.

77.8 dBm, and $\mathrm{IIP2}_{\max} = 139.6$dBm, respectively. Thus, 95% of the differential IIP2 samples are between 97.2 dBm $\pm\, 2\sigma$ or $78.6 \ldots 115.8$ dBm.

The same Monte Carlo mismatch simulation was also performed for the mixer utilizing the traditional common-source RF input stage. In that particular case, the values for the single-ended mixer IIP2 are given as μ =18.6 dBm, $\sigma = 0.2$, $\mathrm{IIP2}_{\min}$ =18.1 dBm, and $\mathrm{IIP2}_{\max}$ =19.1 dBm. Correspondingly, the values for the differential IIP2 are μ =81.3 dBm, σ =9.3 dBm, $\mathrm{IIP2}_{\min}$ =64.2 dBm, and $\mathrm{IIP2}_{\max} = 129.1$ dBm, respectively. Therefore, 95% of the differential IIP2 samples are between 81.3 dBm $\pm\, 2\sigma$ or $62.7 \ldots 99.9$ dBm.

From the mismatch simulations of the mixer under question, it is concluded that the proposed technique enhances the single-ended and differential mixer IIP2 by 37 and 16 dB, respectively. Moreover, since the requirements for the IIP2s of the mixers utilized in direct conversion receivers are in the order of 70 dBm [29], some of the IIP2 samples of the downconversion mixer employing traditional common-source RF stage do not meet the IIP2 specifications. On the contrary, even the minimum differential IIP2 of the mixer utilizing the proposed RF transconductor is larger than the required IIP2 of 70 dBm. Thus, it is concluded that the proposed approach increases the yield of the entire radio receiver by improving the IIP2 of the downconversion mixer.

VII. Conclusion

In this study, a biasing technique for cancelling IM2 distortion and improving IIP2 in common-source and common-emitter RF transconductors is presented. The proposed circuit can be employed as an RF input transconductor in double-balanced downconversion mixers. It is shown that the proposed approach increases the yield of the entire radio receiver by enhancing the mixer IIP2. The presented transconductor has properties similar to the conventional differential pair in the sense that it ideally displays no IM2 distortion, provided that the transconductor is excited differentially and all the transistors in the circuit match with each other. However, as in the conventional differential pair, in the presence of offsets and mismatches, a small residual IM2 is generated. The proposed circuit is also very suitable for operation at low supply voltage, because it has only one device stacked between the transconductor input and output. In the conventional differential pair two devices consume the voltage headroom. The noise performance of the proposed transconductor is similar to the noise performance of the traditional common-source (emitter) and differential pair transconductors with equal bias and device dimensions. On the other hand, the IIP3 of the proposed transconductor is slightly better than the IIP3 of the differential pair transconductor at given bias. The dc component of the proposed transconductor output current is also very insensitive to the level of the RF input amplitude. Thus, the presented circuit can be utilized as a current mirror, whose current mirror ratio is very insensitive to the voltage swings at the gate or base of the current mirrored transistor.

References

[1] B. Razavi, "A 900 MHz CMOS direct conversion receiver," in *Proc. Symp. VLSI Circuits*, 1997, pp. 113–114.

[2] A. Rofougaran, G. Chang, J. J. Rael, J. Y. C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, J. Min, E. W. Roth, A. A. Abidi, and H. Samueli, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS-part II: Receiver design," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 535–547, Apr. 1998.

[3] A. Pärssinen, J. Jussila, J. Ryynänen, L. Sumanen, and K. A. I. Halonen, "A 2 GHz wide-band direct conversion receiver for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1893–1903, Dec. 1999.

[4] M. S. J. Steyaert, J. Janssens, B. De Muer, M. Borremans, and N. Itoh, "A 2-V CMOS cellular transceiver front-end," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1895–1907, Dec. 2000.

[5] T. P. Liu and E. Westerwick, "5-GHz CMOS radio transceiver front-end chipset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1927–1933, Dec. 2000.

[6] R. Magoon, A. Molnar, J. Zachan, G. Hatcher, and W. Rhee, "A single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-N synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1710–1720, Dec. 2002.

[7] W. Sheng, B. Xia, A. E. Emira, C. Xin, A. V. Valero-Lopez, S. T. Moon, and E. Sanchez-Sinencio, "A 3-V, 0.35-μm CMOS bluetooth receiver IC," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 30–42, Jan. 2003.

[8] K. Kivekäs, A. Pärssinen, and K. A. I. Halonen, "Characterization of IIP2 and DC-offsets in transconductance mixers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 34, no. 12, pp. 1893–1903, Dec. 1999.

[9] B. Razavi, *RF Microelectronics*: Prentice Hall PTR, 1998.

[10] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order distortion mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394–406, Mar. 2003.

[11] B. Gilbert, "The MICROMIXER: A highly linear variant of the Gilbert mixer using a bisymmetric class-AB input stage," *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1412–1423, Sept. 1997.

[12] D. Coffing and E. Main, "Effects of offsets on bipolar integrated circuit even-order distortion terms," *IEEE Trans. Microwave Theory Tech.*, vol. 49, no. 1, pp. 23–30, Jan. 2001.

[13] A. A. Abidi, "General relations between IP2, IP3, and offsets in differential circuits and the effects of feedback," *IEEE Trans. Microwave Theory Tech.*, vol. 51, no. 5, pp. 1610–1612, May 2003.

[14] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2178–2185, Dec. 1998.

[15] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 44, no. 6, pp. 428–435, June 1997.

[16] A. Vilander and P. Sivonen, "Cancellation of Second-Order Distortion and Enhancement of IIP2 in Common-Source and Common-Emitter Transconductance Circuits," U.S. Patent Application, Feb. 2004.

[17] A. Nedungadi and T. R. Viswanathan, "Design of linear CMOS transconductance elements," *IEEE Trans. Circuits Syst.*, vol. CAS-31, no. 10, pp. 891–894, Oct. 1984.

[18] K. Kuo and A. Leuciuc, "A linear MOS transconductor using source degeneration and adaptive biasing," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 10, pp. 937–943, Oct. 2001.

[19] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1023–1036, Jul. 1998.
[20] A. Rofougaran, J. Y. C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 880–889, Jul. 1996.
[21] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 3, pp. 315–325, Mar. 1999.
[22] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.
[23] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*. Norwell, MA: Kluwer, 1998.
[24] D. K. Shaeffer and T. H. Lee, *The Design and Implementation of Low-Power CMOS Radio Receivers*. Norwell, MA: Kluwer, 1999.
[25] R. T. Chang, M. T. Yang, P. P. C. Ho, Y. J. Wang, Y. T. Chia, B. K. Liew, C. P. Yue, and S. S. Wong, "Modeling and optimization of substrate resistance for RF-CMOS," *IEEE Trans. Electron. Devices*, vol. 51, no. 4, pp. 421–426, Mar. 2004.
[26] B. Toole, C. Pleitt, and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, pp. 319–328, Feb. 2004.
[27] W. M. C. Sansen and R. G. Meyer, "An integrated wide-band variable-gain amplifier with maximum dynamic range," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 8, pp. 159–166, Aug. 1974.
[28] J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, and K. A. I. Halonen, "A dual-band RF front-end for WCDMA and GSM applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1198–1204, Aug. 2001.
[29] E. E. Bautista, B. Bastani, and J. Heck, "A high IIP2 downconversion mixer using dynamic matching," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1934–1941, Dec. 2000.

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