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A 1.2-V RF Front-End With On-Chip VCO for PCS 1900 Direct Conversion Receiver in 0.13-μm CMOS

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***Abstract*—In this paper, a 1.2-V RF front-end realized for the personal communications services (PCS) direct conversion receiver is presented. The RF front-end comprises a low-noise amplifier (LNA), quadrature mixers, and active RC low-pass filters with gain control. Quadrature local oscillator (LO) signals are generated on chip by a double-frequency voltage-controlled oscillator (VCO) and frequency divider. A current-mode interface between the downconversion mixer output and analog baseband input together with a dynamic matching technique simultaneously improves the mixer linearity, allows the reduction of flicker noise due to the mixer switches, and minimizes the noise contribution of the analog baseband. The dynamic matching technique is employed to suppress the flicker noise of the common-mode feedback (CMFB) circuit utilized at the mixer output, which otherwise would dominate the low-frequency noise of the mixer. Various low-voltage circuit techniques are employed to enhance both the mixer second- and third-order linearity, and to lower the flicker noise. The RF front-end is fabricated in a 0.13-μm CMOS process utilizing only standard process options. The RF front-end achieves a voltage gain of 50 dB, noise figure of 3.9 dB when integrated from 100 Hz to 135 kHz, IIP3 of -9 dBm, and at least IIP2 of $+30$ dBm without calibration. The 4-GHz VCO meets the PCS 1900 phase noise specifications and has a phase noise of -132 dBc/Hz at 3-MHz offset.**

***Index Terms*—Active filter, direct conversion, dynamic matching, low-noise amplifier (LNA), low voltage, mixer, personal communications services (PCS), radio frequency (RF), radio receiver, RF CMOS, RF front-end, voltage-controlled oscillator (VCO).**

I. Introduction

INTEGRATION of RF transceiver functions on standard digital CMOS technology paves the way to the realization of a single-chip radio modem. A digital baseband and RF transceiver in the same technology increases the level of integration and reduces the bills of material (BOM). In addition, radio on CMOS offers a potential for cost reduction, since the mask count in pure CMOS technology is typically smaller than in the corresponding BiCMOS technology [1].

Recently, RF CMOS has become a dominant integrated circuit (IC) technology for noncellular wireless applications such as Bluetooth [2], Global Positioning System (GPS) [3], and wireless local area network (WLAN) [4]. Moreover, most of these wireless receivers utilize zero- or low-IF architectures, because with these receiver topologies a very high level of integration can be obtained. As a consequence, a low material and component cost is achievable.

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In this paper, a 1.2-V analog RF front-end with on-chip voltage-controlled oscillator (VCO) for the PCS 1900 direct conversion receiver fabricated in standard digital 0.13-μm CMOS process is presented. The implemented RF front-end utilizes only standard devices available in 0.13-μm CMOS process. Thus, no expensive process options such as dual-gate-oxide MOS transistors, metal–insulator–metal (MIM) capacitors, or high-resistivity poly (HIPO) resistors are employed.

This paper is organized as follows. Section II highlights the rationale behind the direct conversion RF front-end architecture. In Section III, the RF front-end circuit design is covered in detail and in Section IV, the experimental results are presented. Next, Section V discusses the effect of the receiver gain on the noise and DC offset performance, and finally in Section VI, conclusions are given.

II. CMOS RF Front-End for PCS 1900 Direct Conversion Receiver

Low-frequency flicker noise is of particular concern in CMOS direct conversion receivers [5]. In wideband communication systems such as wideband code division multiple access (WCDMA), the realization of a zero-IF receiver with CMOS technology is feasible, since the large-signal bandwidth makes the system less sensitive to flicker noise. For instance, part of the signal energy near zero-frequency and thus flicker noise can be high-pass filtered without significantly deteriorating the signal-to-noise ratio (SNR) [6], [7]. However, in narrowband systems, such as global system for mobile communications (GSM) or personal communications services (PCS), high-pass filtering is not possible since most of the signal energy is located near DC. For this reason, most of the reported CMOS receivers for GSM or PCS have usually been implemented either with heterodyne [8], [9] or low-IF architectures [10]–[14]. Unfortunately, in a superheterodyne receiver, several expensive external filters are required and power is wasted in buffering high-frequency signals off-chip. On the other hand, in a low-IF receiver, the image must be sufficiently rejected [10]. Accordingly, the requirements for the amplitude (ΔA) and phase imbalance $(\Delta\phi)$ between the I and Q paths are more stringent compared to the direct conversion receiver. In a GSM or PCS low-IF receiver, it is necessary that the image-rejection ratio is at least 32 dB or equivalently $\Delta A \leq 0.3$ dB and $\Delta\phi \leq 2^\circ$ [10], whereas in a direct conversion receiver, it is usually sufficient if $\Delta A \leq 1$ dB and $\Delta\phi \leq 5^\circ$. In addition, in a low-IF receiver, on-chip analog image rejection requires a passive [15] or active [3] polyphase filter, which increases the complexity and power

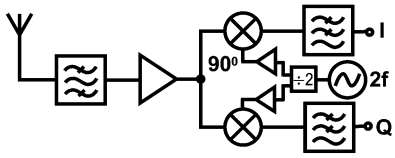

Fig. 1. Block diagram of direct conversion receiver architecture.

consumption. Finally, notice that an active low-pass filter (for instance, a channel filter) at zero-IF always obtains a given dynamic range with lower power than a bandpass filter with the same passband centered at some nonzero-IF [16].

Recently, GSM or PCS direct conversion receivers manufactured in CMOS technology have also been reported [17]–[19]. However, although the RF parts of the receiver [17] operate at 1.5 V, the baseband operational amplifiers (op-amps) utilize supply voltage of 2.5 V and thus complicate the supply voltage management of the RFIC. Moreover, the use of dual-gate-oxide transistors and MIM capacitors increase the processing mask count and thus the cost of the receiver [17]. The direct conversion receiver reported in [18] utilizes the cascade of two downconversion mixer stages at RF signal path to reduce DC offsets and flicker noise. Unfortunately, the use of cascade mixer downconversion architecture complicates the design and increases the power consumption, since two complex local oscillator signals are required. Finally, the transceiver [19] is implemented with an older technology node (0.25 μm) and higher supply voltage (2.8 V), which makes the single-chip realization with the state-of-the-art digital baseband difficult.

The block diagram of the direct conversion RF front-end implemented in this study is illustrated in Fig. 1. The front-end is targeted to be used together with a high-resolution delta-sigma analog-to-digital converter ($\Delta\Sigma$ ADC) having dynamic range of approximately 80 dB over a bandwidth of 100 kHz. These types of $\Delta\Sigma$ modulators have already been reported to be manufactured in 0.13-μm CMOS [20], [21]. It is assumed that the sample rate of the $\Delta\Sigma$ ADC is significantly larger than the receive bandwidth of the PCS 1900 system, i.e., 60 MHz (1930–1990 MHz). Accordingly, the duplex filter preceding the LNA also provides anti-aliasing filtering for the $\Delta\Sigma$ ADC. With these assumptions, a simple second-order analog active low-pass RC filter (see Fig. 1) with a 160-kHz passband prior $\Delta\Sigma$ ADC is sufficient to attenuate the blocking signals and to provide anti-aliasing filtering.

High analog-to-digital (A/D) conversion dynamic range $\Delta\Sigma$ ADCs allow for reduced analog amplification [14], [17], [22]. Accordingly, in this work the analog RF front-end voltage gain (from the LNA input to the low-pass filter output) preceding the ADCs is about 50 dB. Relatively low amplification prior the ADCs makes DC offsets also less of a problem in the direct conversion receiver [17], [22]. For instance, in this work the offsets of the analog baseband op-amps experience only about 6–10-dB voltage gain to the RF front-end output. Thus, in this work it is assumed that the DC offsets are digitized by the ADCs and removed in the digital domain.

Low supply voltage (i.e., 1.2 V) and low-frequency flicker noise present in submicron CMOS processes pose challenges for the design of a PCS 1900 direct conversion RF front-end.

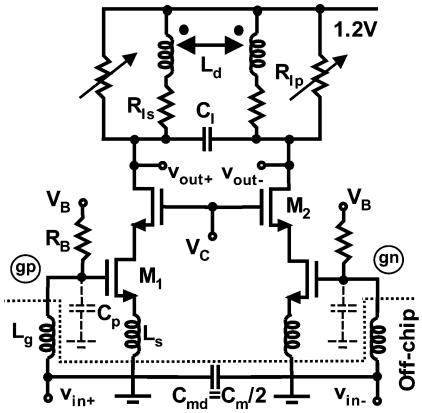

Fig. 2. Low-noise amplifier.

The approach adopted in this work alleviates these problems by utilizing a current-mode interface between the downconversion mixer output and analog baseband input together with a dynamic matching technique. The current-mode interface simultaneously enhances the mixer linearity at low supply voltage, allows the reduction of flicker noise contribution of the mixer switching devices, and minimizes the noise contribution of the analog baseband. The dynamic matching technique is used to suppress the flicker noise of the common-mode feedback (CMFB) circuit utilized in the current mode interface, which otherwise would dominate the mixer low-frequency noise.

III. RF Front-End Circuit Design

All circuits described here operate from a 1.2-V power supply. Moreover, all the circuits utilize balanced topologies to reject the interference from substrate or supply.

A. Low-Noise Amplifier

The LNA is based on the most commonly used topology, i.e., an inductively degenerated common-source amplifier [23], as shown in Fig. 2. In mass product applications, the integrated circuits are almost always mounted in a package and electrostatic discharge (ESD) protection structures are required for reliability reasons. At the LNA input, ESD protection diodes, the bond pad plate structure, Miller capacitance of the LNA input device M_1, and parasitic capacitance of bondwire introduce a parallel parasitic capacitance at the gate of the LNA input transistors M_1 (see nodes "gp" and "gn" in Fig. 2). The total parasitic capacitance can modeled as an *equivalent parallel package parasitic capacitance* C_p at the gate of M_1, as shown in Fig. 2 [24], [25]. It is a well-known fact that if C_p is sufficiently large compared to the gate-source capacitance C_{gs} of the LNA input device M_1, the impedance level at the LNA input becomes too low to be matched 100-Ω differential impedance only by employing a series gate inductance. In this work, $C_p \approx 5 \times C_{gs}$, which implies that LNA input impedance matching network comprising of parallel capacitor C_{md} and series gate inductor L_g (see Fig. 2) is needed to transform upwards the equivalent impedance looking into the gate of M_1. Since the losses of the input impedance matching network are crucial for the LNA noise figure (NF), these components are realized with off-chip lumped elements.

If the noise contributions of the cascode transistors are neglected and the LNA input impedance is assumed to be perfectly matched at the operation frequency f_0, the LNA NF at f_0 can be approximated as [24]

$$\begin{aligned}\mathrm{NF} = 1 &+ \left(\frac{C_p + C_{gs}}{C_{gs}}\right)^2 \left(\frac{R_{cm}}{R_{eq}} + \frac{R_{lg}}{R_{eq}}\right) \\ &+ \frac{r_g}{R_{eq}} + \frac{R_{eq}}{R_B} + \frac{1}{g_m^2 R_B R_{eq}} \left(\frac{\omega_T}{\omega_0}\right)^2 \\ &+ \frac{\gamma}{\alpha} g_m R_{eq} \left(\frac{\omega_0}{\omega_T}\right)^2 \Upsilon + \eta^2 g_m^2 R_{\mathrm{sub}} R_{eq} \left(\frac{\omega_0}{\omega_T}\right)^2 \\ &+ \frac{\alpha\delta}{5 g_m R_{eq}} + \frac{4R_{eq}}{R_{lp,eq}} \left(\frac{\omega_0}{\omega_T}\right)^2 \end{aligned} \tag{1}$$

where

$$R_{eq} = \frac{g_m L_s}{C_{gs}} + r_g \approx \omega_T L_s \tag{2}$$

and R_{cm} and R_{lg} represent the series resistances of C_m and L_g, respectively, r_g is the gate resistance, R_B is the bias resistor used to supply the LNA bias voltage V_B, $\alpha = g_m/g_{d0}$, g_{d0} is the zero bias drain conductance, γ is the channel current noise factor, δ is the gate induced current noise factor [23], η is a bias-dependent constant, R_{sub} is the substrate resistance, and $R_{lp,eq}$ is the equivalent parallel load resistance. The coefficient Υ is given by

$$\Upsilon = 1 + 2c\sqrt{\frac{\delta}{5\gamma}}\alpha + \frac{\delta\alpha^2}{5\gamma} \tag{3}$$

where c is the correlation coefficient between the gate and drain noise [23].

The optimum values (i.e., for the minimum LNA NF) for the input device and cascode device widths, their biasing currents, source inductance L_s, and input impedance matching components (L_g and C_m) can be found as described in [24], in which the optimization procedure of the packaged common-source LNA with ESD protection is discussed.

The LNA achieves NF of 1.5 dB, input-referred third-order intercept point (IIP3) of -4 dBm (at maximum gain), and it draws about 8 mA from 1.2-V supply. In this case, the highest contributions to the LNA NF have the 50-Ω source resistance R_s (70.3%), the series resistance R_{lg} of the matching inductor L_g (14.6%), the bias resistor R_B (3.4%), the gate resistance r_g of M_1 (2.1%), the channel thermal noise plus gate induced current noise of M_1 (1.6%), and the equivalent parallel load resistance $R_{lp,eq}$ of the LNA (1.6%). The rest of the contributions are each below 1%.

In this work, the noise due to the series resistance R_{lg} of the gate inductor L_g dominates the LNA NF. This might not be expected, since off-chip inductors and capacitors in general have high quality factor (Q), i.e., in this work in the order of 80 and 300@2 GHz, respectively. Notice also that in practice $R_{lg} + R_{cm} \approx R_{lg}$. However, from (1) it is seen that the noise contribution of R_{lg} to the LNA NF depends on the ratio of C_p to C_{gs}. Thus, if the parallel parasitic capacitance C_p due to the ESD and package parasitics is increased, the noise contribution of R_{lg} is increased proportional to $((C_{gs} + C_p)/C_{gs})^2$ worsening the LNA NF. Moreover, since in this work $C_p \approx 5 \times C_{gs}$, the noise due to R_{lg} is indeed noticeable especially as the minimum NF of a single MOS device itself in the utilized 0.13-μm CMOS technology is only about 0.2 dB@2 GHz. In practical applications with ESD protection, the achievable NF of the packaged LNA is therefore well above the theoretical minimum NF of the active device.

To improve the RF front-end linearity with high signal levels, the LNA has two gain steps, which are 12 dB and 15 dB. The corresponding voltage gains are -7 dB, 8 dB, and 20 dB. The gain control is implemented adjusting the value of the resistor R_{lp} in parallel with the LC resonator accordingly [26].

A tuned load peaks the gain of the amplifier at the PCS 1900 band. The load utilizes a differential inductor L_d resonating with the parallel capacitance realized with interdigital metal–oxide–metal (MOM) capacitor C_l and parasitics. The resistance R_{ls} in series with L_d, realized with the same resistance material as R_{lp}, regulates the LC-tuned LNA load impedance at the narrow PCS frequency band against variations of passive devices in IC process [27], [28]. By selecting the values of R_{ls}, R_{lp}, and L_d as described in [28], the voltage gain variation of the LNA can be reduced several decibels compared to the conventional resonator techniques. The LNA and mixers are AC-coupled with 4-pF interdigital MOM capacitors.

B. Downconversion Mixer

Fig. 3 illustrates the schematics of the LC-folded cascode downconversion mixer [9] and active RC low-pass filter. Since the common-source transconductor biased at a given overdrive voltage $V_{\mathrm{eff}} = V_{\mathrm{GS}} - V_t$ exhibits smaller third-order nonlinearity than the differential pair at equal bias [29], the downconversion mixer shown in Fig. 3 employs the common-source transconductor as its RF input stage. RF input devices M_{RF} are biased at V_{eff} of about 300 mV for an IIP3 of $+14$ dBm and each RF input device draws about 3 mA. Nonminimum channel lengths are employed to further improve the input stage linearity.

An LC-folded cascode downconversion mixer is ideally suited for low-voltage operation since, for instance, at the mixer RF input stage only one active device is stacked between the supply rails. Differential inductor L_{md} parallel resonating with interdigital MOM capacitor C_{mp} and parasitics provide a high-impedance at the desired RF frequency ω_{RF} and a low impedance at the second-harmonic frequency $2\omega_{\mathrm{RF}}$ and $2\omega_{\mathrm{LO}}$ as well as at the low-frequency $\Delta\omega = \omega_{\mathrm{RF1}} - \omega_{\mathrm{RF2}}$ [30]. Thus, the LC resonator simultaneously improves the mixer RF input stage IIP3 and filters out the second-order intermodulation (IM2) distortion components $\Delta\omega$ generated at the mixer RF input stage.

Switches in an active mixer contribute flicker noise to the mixer output in two different ways [31]. In the direct mechanism, flicker noise modulates the time instants of mixer switching. In this design, the direct mechanism is lowered by providing a large local oscillator (LO) voltage swing (almost rail-to-rail) driving the mixer switches M_{sw} by employing CMOS inverters as LO buffers. Correspondingly, the indirect mechanism is suppressed by tuning out the tail capacitance

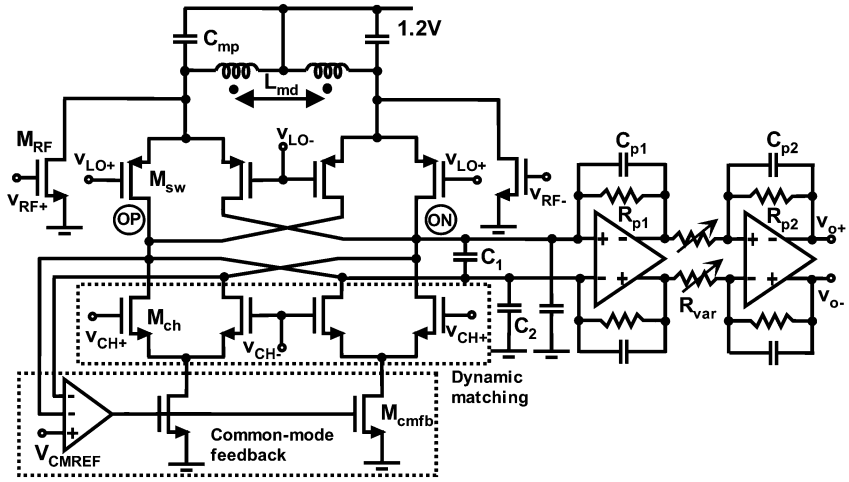

Fig. 3. Downconversion mixer and active RC low-pass filter.

at the common-source node of the switching devices by the differential inductor L_{md} [32]. Finally, both of the mechanisms are minimized by utilizing pMOS instead of nMOS switching transistors, since the flicker noise in pMOS devices is lower than in nMOS devices due to buried channel conduction induced by the threshold adjust implant [31]. Switch FET's M_{sw} also have relatively large gate area $W \times L$ to lower flicker noise further.

The mixer–analog baseband interface utilizes a current-mode signal processing. The differential-mode output current of the mixer is driven to the feedback loop of the RC integrator (transimpedance amplifier), whereas the common-mode current is sinked by the CMFB current source devices $M_{\rm cmfb}$. The transimpedance amplifier low-pass filters the mixer differential-mode output current and converts it back to voltage. High-gain op-amps shown in Fig. 3 can swing rail-to-rail at minimum distortion. Moreover, the transimpedance amplifier has a high common-mode rejection. This is essential in a direct conversion receiver because after downconversion the common-mode IM2 distortion generated in the mixer must be blocked before it becomes differential as a result of device mismatch at baseband [33].

The op-amp in the negative feedback loop [10] provides a virtual ground at the mixer output (see nodes "OP" and "ON" in Fig. 3). Thus, ideally there is no voltage swing present at the mixer output. Moreover, since there is no voltage swing at the drain of the switching devices M_{sw}, the nonlinearity due to the switches is minimized. Accordingly, the bias current of the switches can be scaled down to reduce their flicker noise [34] without deteriorating the mixer linearity.

The current-mode interface needs a CMFB circuit to operate properly. Unfortunately, without the dynamic matching technique, the CMFB transistors $M_{\rm cmfb}$ add uncorrelated flicker noise at the mixer output, which in practice can dominate the mixer low-frequency noise. For the same reason, the use of entire current-mode interface is often disqualified. Scaling up the FET gate area $W \times L$ lowers the flicker noise, but this increases the gate-source capacitance of $M_{\rm cmfb}$ and worsens the stability of the CMFB circuit.

In this work, the flicker noise of transistors $M_{\rm cmfb}$ is suppressed by applying a dynamic matching or chopper stabilization technique [35], [36]. Earlier, the dynamic matching, in the context of downconversion mixers, was used to reduce the flicker noise generated in the actual mixer core [37]. Effectively, one mixer preceding and a second one following the main mixer core have been used to boost the second-order intercept point (IIP2) and to lower the flicker noise of the main mixer core. On the contrary, here the dynamic matching technique is used to reduce the flicker noise of the mixer common-mode load and not directly the mixer core itself.

In this work, dynamic matching is utilized as follows. Transistors M_{ch} (see Fig. 3), operating as switches, are driven by a rail-to-rail signals $v_{\rm CH+}$ and $v_{\rm CH-}$ in antiphase at the chopper frequency of $f_{\rm CH} = f_{\rm LO}/16$ ($\sim$122.5 MHz). Signals $v_{\rm CH+}$ and $v_{\rm CH-}$ are generated from the LO signal by frequency division. Thus, transistors M_{ch} essentially form an upconversion mixer, which upconverts the flicker noise of CMFB transistors $M_{\rm cmfb}$ at the chopper frequency and thus outside the signal band of interest. Moreover, since the differential-mode interference signals at the mixer output do not flow through the CMFB circuit, the switching quad M_{ch} does not downconvert the interference signals to the signal band of interest. In addition, since the switches M_{ch} are driven by a large amplitude square wave at the relatively low frequency to a deep triode region, their voltage headroom consumption and noise contribution is insignificant. Finally, notice that without dynamic matching, the mismatch in transistors $M_{\rm cmfb}$ would directly effect the RF front-end IIP2 and DC offset. However, by applying chopper stabilization, both of these effects due to the mismatch in $M_{\rm cmfb}$ are suppressed.

Consider the effect of the dynamic matching on the white noise contribution of the CMFB transistors $M_{\rm cmfb}$ to mixer output noise. Notice that without the chopper stabilization, the CMFB transistors $M_{\rm cmfb}$ add uncorrelated white noise of $\overline{i^2_{d,M_{\rm cmfb}}} = 4kT\gamma g_{\rm cmfb}$ at the mixer output or transimpedance amplifier input. On the other hand, if the chopper stabilization is applied and the commutation of the switching devices M_{ch} is assumed square-wave-like, the chopper frequency and its odd harmonics will downconvert the respective components of

wideband white noise current $\overline{i^2_{d,M_{\rm cmfb}}}$ to the IF. After including the conversion gain $2/\pi$, the noise at the mixer output due to $\overline{i^2_{d,M_{\rm cmfb}}}$ is [31]

$$\begin{aligned}\overline{i^2_{{\rm on},M_{\rm cmfb}}} &= n\times\left(\frac{2}{\pi}\right)^2\overline{i^2_{d,M_{\rm cmfb}}}\\ &= \frac{\pi^2}{4}\times\left(\frac{2}{\pi}\right)^2\overline{i^2_{d,M_{\rm cmfb}}}\\ &= \overline{i^2_{d,M_{\rm cmfb}}}\end{aligned}\tag{4}$$

where the factor n represents accumulated noise after aliasing. For the harmonic amplitudes of the square wave, $n=\pi^2/4$ [31]. It is concluded that the dynamic matching has no effect on the white noise contribution of the CMFB transistors $M_{\rm cmfb}$ to the mixer output noise.

C. Low-Pass Filter

In order to minimize the silicon area, -3-dB corner frequency of the low-pass filter in an integrated direct conversion receiver should be as large as possible. In this work, the blocker signal at the offset frequency of 600 kHz from the desired signal sets the required filter order and corner frequency. As already depicted, in this work a simple second-order analog active low-pass RC filter (see Fig. 3) with a 160-kHz passband prior $\Delta\Sigma$ ADC is sufficient to attenuate the blocking signals and to provide anti-alias filtering for the $\Delta\Sigma$ ADC. It is assumed that the $\Delta\Sigma$ ADC has a sample rate of significantly larger than 60 MHz (i.e., PCS 1900 receive bandwidth) and dynamic range of approximately 80 dB over a bandwidth of 100 kHz. The low-pass filter provides five steps of gain control via a switchable resistor $R_{\rm var}$ (see Fig. 3).

The active filter very often contributes the largest noise of all the building blocks in an integrated direct conversion receiver [38]. In this work, the noise contribution of the filter is minimized by utilizing a filter with a current-mode input stage (i.e., transimpedance amplifier). If the input-referred noise voltage of the op-amp in the transimpedance amplifier shown in Fig. 3 is $v_{n,{\rm in}}$, its output noise voltage at the filter passband is given as $v_{n,{\rm out}}=(1+R_{p1}/R_{{\rm out},m})\times v_{n,{\rm in}}$ where $R_{{\rm out},m}$ is the parallel output impedance of the mixer and CMFB circuit. If $R_{p1}\ll R_{{\rm out},m}$, $v_{n,{\rm out}}\approx v_{n,{\rm in}}$. Thus, the input-referred noise voltage of the op-amp experiences no voltage gain from the op-amp input to the op-amp output. On the contrary, in a filter with a voltage-mode input stage, the corresponding noise voltage gain can be significant.

At the low supply voltage (i.e., 1.2 V), the condition $R_{p1}\ll R_{{\rm out},m}$ dictates that the mixer must be terminated with an active common-mode load instead of a simple resistive load. Due to the voltage headroom limitations at low supply voltage, the value of the passive resistive load and thus $R_{{\rm out},m}$ cannot be chosen to be arbitrarily large.

The current-mode interface between the mixer output and analog baseband input is also very beneficial regarding the offset voltage of the op-amp in the transimpedance amplifier. Similarly, as the input-referred noise voltage, the input-referred offset voltage of the op-amp in the transimpedance amplifier experiences no voltage gain to the op-amp output. Again, in a filter with a voltage-mode input stage, the corresponding gain can be significant. Finally, since the second stage of the low-pass filter provides at maximum about 6 dB voltage gain, the input-referred offset voltages of the first and second op-amps shown in Fig. 3 experience at maximum only about 6 dB and 10 dB voltage gain, respectively, to the RF front-end output. Accordingly, these offset voltages can be digitized by the ADC.

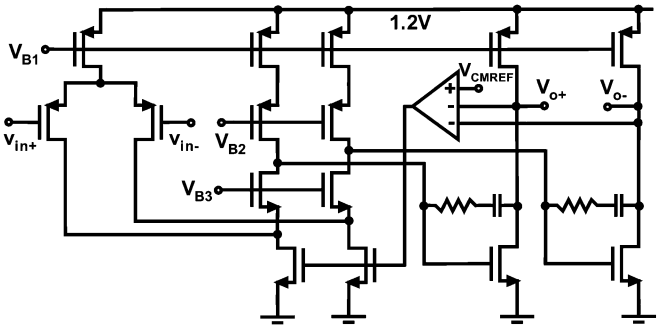

Fig. 4. Operational amplifier.

As described above, the differential-mode mixer output current is injected to the feedback loop of the first RC integrator. Ideally, the differential-mode input impedance $Z_{{\rm in},ta}$ of the transimpedance amplifier should be as small as possible to ensure a maximum transfer of current from the mixer output to the transimpedance amplifier output. However, $Z_{{\rm in},ta}$ is small only in the frequency range where the open loop gain of the first op-amp shown in Fig. 3 is high [39]. The op-amp must therefore be designed for high-frequency operation. The blocker signals at the frequencies beyond the op-amp gain-bandwidth product (GBW) are attenuated by the capacitors C_1 and C_2 at the mixer output. In addition, they prevent the op-amp from slewing due to the high-frequency mixer output signals. Finally, capacitors C_2 determine the dominant pole of the CMFB circuit.

The filter uses two-stage op-amps with a folded cascode input stage (Fig. 4). The input stage utilizes pMOS transistors for lower flicker noise. Each op-amp shown in Fig. 3 drains about 10 mA and gives 70 dB DC gain with a GBW of about 500 MHz. Most of the current consumption of the first op-amp is due to the large parasitic capacitance associated with the interdigital MOM capacitor C_{p1} utilized in the feedback loop. This parasitic capacitance is in the order of 10% of C_{p1}. For stability issues, the nondominant pole of the first op-amp, set by the parasitic capacitance of C_{p1}, has to be placed at a sufficiently high frequency. Unfortunately, this requires relatively high current consumption at the op-amp output stage. The output stage current consumption could significantly be scaled down, if MIM capacitors instead of interdigital MOM capacitors were utilized. At given capacitance density, MIM capacitors have much less parasitics compared to the interdigital MOM capacitors. Simulations indicate that with MIM capacitors the op-amp current consumption could be lowered from 10 mA to 5 mA. However, interdigital MOM capacitors are standard CMOS compatible and do not need any extra processing step, as is the case with special MIM capacitors. Finally, since in this work the second op-amp drives the off-chip measurement circuitry, the second

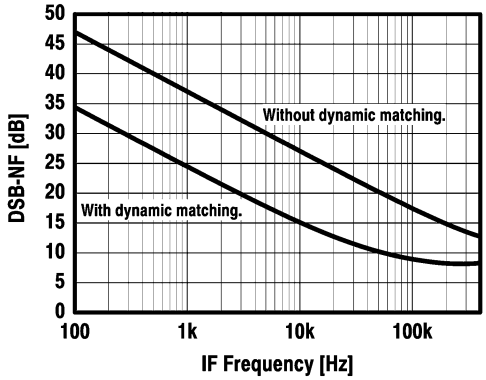

Fig. 5. Simulated spot DSB-NF of cascaded mixer–low-pass filter block with respect to noise in 100-Ω differential resistor.

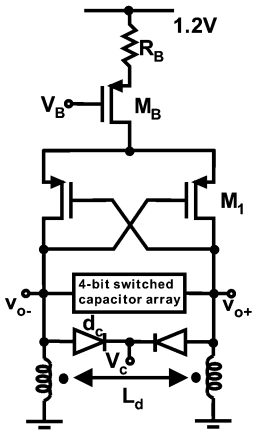

Fig. 6. Voltage-controlled oscillator.

op-amp also draws 10 mA to provide sufficient driving capability for the off-chip load. In actual application, however, the second op-amp drives the ADC on-chip, implying the second op-amp current consumption can be scaled down significantly.

The cascaded mixer–low-pass filter block provides gain of 31 dB, IIP3 of +12 dBm, and double-sideband noise figure (DSB-NF) of 12 dB with respect to the noise in 100-Ω differential resistor. The DSB-NF is integrated from 100 Hz to 135 kHz.

The effect of the dynamic matching on the spot DSB-NF of the cascaded mixer–low-pass filter block is illustrated in Fig. 5. It is seen that the dynamic matching lowers the spot DSB-NF about 12 dB by lowering the low-frequency flicker noise contribution of the CMFB transistors $M_{\rm cmfb}$ (see Fig. 3).

D. LO Circuitry

The double-frequency VCO (Fig. 6) consists of a cross-coupled pMOS pair M_1 with a pMOS current source M_B at the tail. A recent study has shown that an all-PMOS topology with a ground referenced LC tank shown in Fig. 6 is the most appropriate LC VCO architecture for the lowest phase noise [40].

PMOS transistors lower the flicker noise in the cross-coupled pair M_1. Differential pair FETs also employ nonminimum channel lengths to suppress flicker noise further. A pMOS instead of nMOS tail current source also reduces the flicker noise in the tail current. In addition, to lower the flicker noise further, the tail current $W\times L$ is scaled up while keeping W/L constant. A long-channel FET at the current source also lowers the flicker noise which upconverts into close-in phase noise around the oscillation frequency [41]. Finally, resistive degeneration (R_B) suppresses the flicker noise due to M_B. Without degeneration, M_B introduces a noisy current (considering only 1/f noise) of

$$\overline{i_{n,M_B}^2} = g_{mB}^2\overline{v_{n,M_B}^2} = (2\mu_p I_B K_f)/(fL^2)$$

at the common-source node of the cross-coupled pair M_1. Here μ_p is the hole mobility, I_B is the drain-source current of M_B, K_f is the flicker noise coefficient of the PMOSFET, L is the channel length of M_B, and f is the frequency. Correspondingly, with degeneration the noise current is reduced to

$$\begin{aligned}\overline{i_{n,M_B}^2} &= (g_{mB}^2\overline{v_{n,M_B}^2})/(1+g_{mB}R_B)^2\\ &= (2\mu_p I_B K_f)/((fL^2)(1+g_{mB}R_B)^2).\end{aligned}$$

Thermal noise in the current-source drain current is lowered by biasing M_B at large $V_{\rm GS}-V_t$ [11].

A 4-bit switched capacitor array [42] in parallel with a pn-junction varactor tunes the oscillation frequency. The VCO has a continuous tuning range of 1.7% whereas the discrete tuning scheme extends the total tuning range to 13.3%. With the differential inductor (L_d) Q of 15@4 GHz, the VCO output swing is about 1.2 $V_{\rm p\text{-}p}$ (single-ended) at 10 mA bias current. The source-follower couples the VCO to the frequency divider.

The VCO achieves a phase noise of -132.3 dBc/Hz at 3-MHz offset from 4 GHz and thus complies with GSM or PCS phase noise requirements. Notice that the phase noise reduces by 6 dB after frequency division by two.

A pair of source-coupled D flip-flops in a ring clocked by the double-frequency VCO realizes divide-by-two and produces the desired LO frequency with quadrature phases. In this work, the tail current source in conventional source-coupled logic (SCL) design is omitted to ease 1.2-V operation. Each flip-flop swings about 1 $V_{\rm p\text{-}p}$ at the output and the entire divide-by-two draws an average current of 2.4 mA from the supply.

In order to drive relatively large gate area mixer switching transistors, LO buffering is needed. Each LO buffer consists of a two-stage CMOS inverter chain. In addition, each LO buffer consumes an average current of 1.4 mA and the LO voltage swing driving the mixers is about 0.8 $V_{\rm p\text{-}p}$.

IV. Experimental Results

The front-end was fabricated in 0.13-μm CMOS and all the circuits operate on 1.2-V supply. The RF front-end is mounted in a quad flat nonleaded (QFN) package and all the pads are ESD protected. Fig. 7 shows the microphotograph of the RF front-end. Its area is 4.2 mm^2. In the layout of the VCO circuit, there are two differential inductors shown. The other inductor is part of the buffer, which is used to enable the VCO measurements. If the RF front-end utilized MIM capacitors and HIPO resistors instead of standard MOM capacitors and poly resistors, the silicon area of the low-pass filter and the entire RF front-end would be about 20% and 10% smaller, respectively.

The measured performance of the RF front-end is summarized in Table I. Several samples have been measured in order

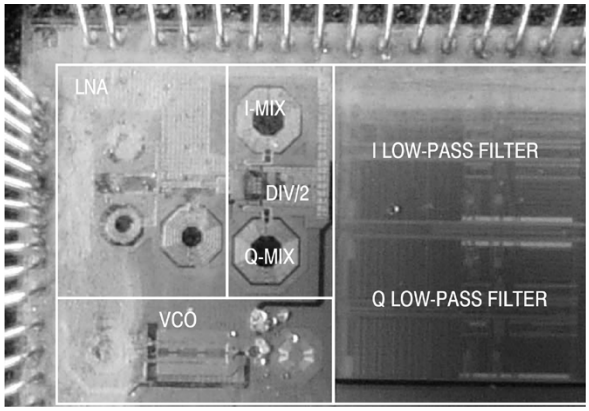

Fig. 7. Microphotograph of RF front-end.

TABLE I
SUMMARIZED PERFORMANCE OF PCS 1900 RF FRONT-END

Parameter	Measured	Unit
Receive band	1930-1990	MHz
S_{11} (balanced 100 Ω)	$\leq$ -12	dB
Voltage gain (max.)	50	dB
DSB-NF @ gain max	3.9	dB
IIP3 @ gain max	-9	dBm
IIP2 @ gain max	$\geq$ +30	dBm
I/Q gain imbalance	0.4	dB
I/Q phase imbalance	3	deg
LO at RF input	-94	dBm
DC offset at baseband output	$<$ 50	mV
VCO tuning range	13.3	%
VCO phase noise	-132 @ 3 MHz	dBc/Hz
Supply voltage	1.2	V
Power consumption	105	mW

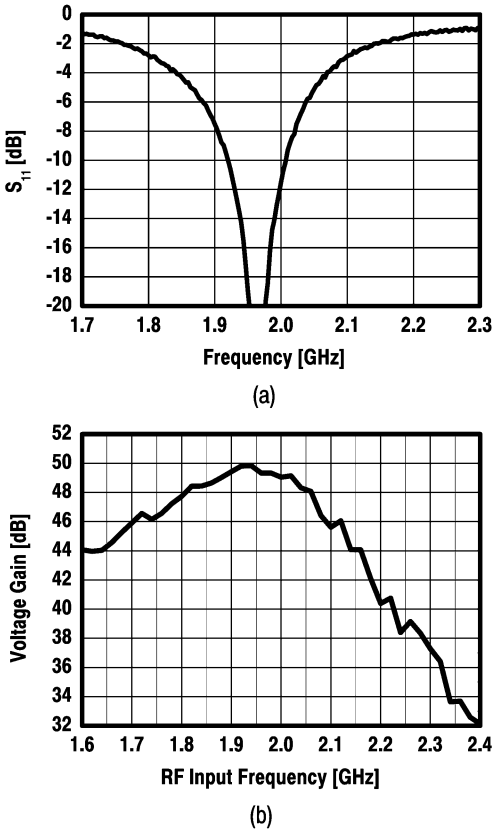

Fig. 8. (a) Measured LNA input reflection coefficient S_{11}. (b) Measured receiver frequency response.

to achieve reliability in the measurements. The measured LNA input impedance matching and maximum voltage gain of the RF front-end are illustrated in Fig. 8(a) and (b), respectively. The input reflection coefficient S_{11} is better than -12 dB in the PCS 1900 band. The peak conversion voltage gain is about 50 dB.

The measured DC offset is below 50 mV at the RF front-end output in all measured samples. The offset voltages at that range can be digitized by the ADC having a dynamic range of 80 dB without overloading. Accordingly, the DC offset cancellation can be fully be achieved in the digital baseband processor.

The RF front-end achieves a DSB-NF of 3.9 dB, when integrated from 100 Hz to 135 kHz. The flicker noise corner frequency lies approximately at 8 kHz. If the noise is integrated from 500 Hz to 135 kHz, the DSB-NF reduces to 3.4 dB.

The correct lower integration limit of noise in direct conversion receivers depends on the signal detection at the baseband and always relates to a specific solution. Therefore, the sensitivity is finally defined as a combination of the receiver NF and the bandwidth of the detector. When the DC offset removal in the analog front-end is not necessary due to the low front-end gain as discussed in Sections II and V, the DC offset removal can be optimized in the baseband algorithm design as done for example in [43] and [44]. On the other hand, this fact obviously causes difficulties, for instance, how to fairly compare the noise performance of different reported RF front-ends [17]–[19]. Hence, an accurate performance comparison would necessitate exactly the same noise integration limits or the information about the flicker noise corner frequency and the level of the thermal noise of the circuit. Only with that information can different implementations be fairly compared using the analysis given in [45].

In the implemented RF front-end, the gain of the small wanted signal is compressed by 1 dB with a blocker of $-30/-22/-18$ dBm at 0.6/1.6/3.0-MHz offset, respectively. At the blocker offset frequencies of 3–100 MHz, the compression characteristics of the front-end remain constant (i.e., the gain of the small wanted signal is compressed by 1 dB with a blocker of -18 dBm). On the other hand, from 100 to 200 MHz, the RF front-end blocking performance improves from -18 dBm to -12 dBm. The performance improvement is due to the fact that the blocker signals at the frequencies beyond 100 MHz are attenuated by the capacitors C_1 and C_2 at the mixer output (see Fig. 3) and by the duplex filter. Moreover, according to the measurements, the rejection of the blocker signal at the chopper frequency (i.e., 122.5 MHz) is always more than 70 dB. Ideally, the rejection is infinite, because the differential blocker signals do not flow through the CMFB or chopper circuit (see Fig. 3). Instead, they are filtered by the capacitors C_1 and C_2 at the mixer output.

The IIP3 and IIP2 are measured with 800-kHz and 1.6-MHz, and 6.00- and 6.05-MHz downconverted signals, respectively.

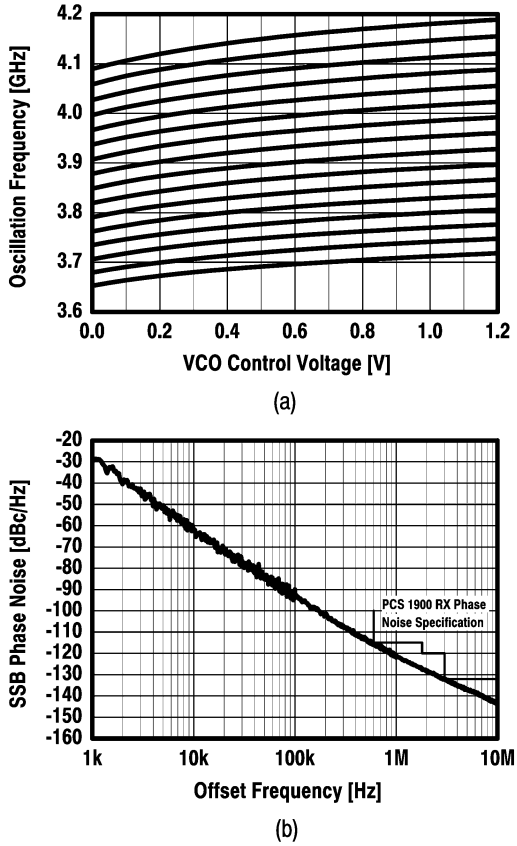

Fig. 9. Measured VCO (a) tuning range and (b) phase noise.

The measured IIP3 of the RF front-end is about -9 dBm. The worst IIP2 values were found to be $+30$ dBm, while the highest were $+45$ dBm without any calibration. Thus, some samples do not have sufficient IIP2 performance to pass the AM suppression test. To further improve the second-order intermodulation characteristics of the RF front-end, well-known calibration techniques can be utilized [46]. The IIP2 performance can be improved by inserting a controllable additional resistive load in parallel to the positive and negative resistors R_{p1} (see Fig. 3).

The RF front-end I/Q gain and phase imbalance is about 0.4 dB and 3°, respectively. The phase imbalance $\Delta\phi$ is deduced by measuring the gain imbalance ΔA and image-rejection ratio (IMRR), and by calculating $\Delta\phi$ once ΔA and IMRR are known [15]. It is concluded that the I/Q gain and phase imbalance are sufficient for the direct conversion PCS receiver, but not for the low-IF PCS receiver [10].

The VCO tuning range, as shown in Fig. 9(a), is 13.3%. The measured VCO phase noise at 4 GHz is shown in Fig. 9(b). The VCO meets the PCS 1900 phase-noise requirements at all offset frequencies [47], [48]. At offset frequencies of 0.6, 1.8, and 3.0 MHz, the measured phase noise is -115.5, -127.6, and -132.3 dBc/Hz, respectively.

During the initial phase of the circuit design, the accurate information on the level of the interdigital MOM capacitor parasitics were not available. For this reason, op-amps utilized in the active RC low-pass filter were over-designed to make a safe design. However, according to measurements, the power consumption of the analog baseband can be reduced about 23 mW without significantly effecting the RF front-end gain, NF, or intermodulation performance. Moreover, if further analog baseband power consumption reduction is desired, interdigital MOM capacitors can be replaced by MIM capacitors, which lowers the analog baseband power consumption about 50%. Finally, notice that the power consumption reported in Table I also includes the op-amp driving the off-chip measurement circuitry. In an actual direct conversion receiver with integrated ADC, the current consumption of the corresponding op-amp can be scaled down significantly.

V. Discussion of Effect of Receiver Gain on Noise and DC Offset Performance

The implemented RF front-end has been designed to be compatible with a $\Delta\Sigma$ ADC having dynamic range of 80 dB over a bandwidth of 100 kHz. Moreover, the RF front-end employs only about 50 dB voltage gain to ensure that the DC offset cancellation can be fully be achieved in the digital baseband processor. Low receiver gain also promotes operation at 1.2-V supply voltage and reduces the analog filtering requirements.

If the RF front-end is combined with the $\Delta\Sigma$ ADC having a dynamic range of 80 dB, the total NF of the receiver is about 4.4 dB (when integrated from 100 Hz to 135 kHz). If the noise is integrated from 500 Hz to 135 kHz, the receiver NF reduces to 4.0 dB.

If it is desired to reduce the noise contribution of the ADC to the receiver NF, the RF front-end voltage gain or the dynamic range of the ADC must be increased, or the analog baseband must be implemented by utilizing dual-gate-oxide MOS transistors. First, assume that the RF front-end voltage gain is increased by increasing the analog baseband gain, i.e., by 6 dB. Unfortunately, this increases the offset voltage by a factor of two resulting in offset voltages at maximum in the order of 100 mV at the baseband output. Moreover, if the additional 6 dB gain is implement in the first or second RC integrator (see Fig. 3), the in-band blockers and interferes will saturate the corresponding op-amps. Accordingly, the analog baseband must be implemented by dual-gate-oxide transistors [17] and by utilizing 2.7-V supply voltage. Nevertheless, assume that the analog baseband utilizes 2.7-V supply and the 6 dB extra gain is implemented in the first RC integrator. Then, the RF front-end DSB-NF improves from 3.9 dB to 2.7 dB, when integrated from 100 Hz to 135 kHz. Correspondingly, the receiver NF improves from 4.4 dB about to 2.9 dB.

If the baseband is to be implemented utilizing only 1.2-V supply voltage, the additional baseband 6 dB gain must be implemented by inserting one additional RC integrator with 6 dB gain at the baseband output. The additional RC integrator is needed to filter in-band blockers and interferers, which otherwise would saturate the corresponding op-amp and overload the ADC. The integrator must also be designed for lower noise than the equivalent input-referred noise of the ADC. Otherwise, the receiver NF is not improved by this approach. Nevertheless, increasing the baseband gain by 6 dB by this method reduces the receiver NF from 4.4 dB at best close to 4 dB. Moreover, the maximum DC offset voltage at the baseband output increases by a factor of two, or from 50 mV to 100 mV.

The receiver NF can also be improved by increasing the LNA gain. System simulations indicate that if the LNA gain is increased by 2 dB or from 20 dB to 22 dB, the RF front-end DSB-NF improves from 3.9 dB to 3.2 dB, when integrated from 100 Hz to 135 kHz. Correspondingly, the receiver NF improves from 4.4 dB to about 3.6 dB. The 2 dB gain increase in the LNA can be implemented simply by increasing the LNA load impedance level at frequency band of interest [28]. Naturally, due to the increased LNA gain, the RF front-end IIP3 and IIP2 both decrease about 2 dB. However, the resulting IIP3 of about -11 dBm is still higher than the IIP3s of the corresponding state-of-the-art CMOS GSM or PCS receivers [12], [13], [19]. Moreover, the 2 dB additional LNA gain does not require additional analog baseband filtering or increase the DC offset voltage contribution of the mixer or analog baseband at the RF front-end output.

Finally, the noise contribution of the ADC to the receiver NF can be reduced by increasing the dynamic range of the ADC. For instance, if ADC with dynamic range of 82 dB instead of 80 dB is used and the RF front-end gain is increased slightly from 50 dB to 51 dB, the ADC increases the receiver NF only by 0.2 dB and the resulted receiver NF is 4.1 dB (integrated 100 Hz–135 kHz). This is a feasible solution because the state-of-the art $\Delta\Sigma$ ADC achieves a dynamic range of 84 dB over a bandwidth of 100 kHz [20]. If the 1 dB gain increase is implemented at the analog baseband, the maximum DC offset voltage at the RF front-end output increases only from 50 mV to 56 mV. This is tolerable by the ADC.

The above discussion addresses several means which can be easily applied to the design to boost the performance with relatively small changes to the original design. Those are needed when all the available capabilities of the technology are utilized to improve the sensitivity of the receiver. The use of a state-of-the art ADC avoids several other constraints related to re-partitioning of filtering and gain and also allows even more headroom for the DC offset generated in the receiver. Thus, the recent advances in $\Delta\Sigma$ ADC performance can be effectively utilized in the system design of an RF front-end having reduced gain and overall complexity.

VI. Conclusion

A 1.2-V RF front-end with on-chip VCO for a PCS 1900 direct conversion receiver is presented in this paper. A current-mode interface between the downconversion mixer output and analog baseband input improves the RF front-end performance in several ways. Firstly, since there is no voltage swing at the mixer output, the nonlinearity due to the mixer switching devices is minimized. For the same reason, the bias current of the switches can be scaled down to reduce their flicker noise without deteriorating the mixer linearity. The current-mode interface also minimizes the noise contribution of the analog baseband in such a way, which requires only a moderate voltage gain (or transconductance) in the LNA and mixer. Both of these issues are out of importance when operating at 1.2-V supply voltage. To operate properly, the current-mode interface requires a CMFB circuit. A drawback of a conventional CMFB circuit is its large flicker noise, which in practice can dominate the entire mixer low-frequency noise and prevent the use of the current-mode interface. In this work, the dynamic matching technique is used to suppress the flicker noise of the CMFB circuit and to enable the use of the current-mode interface. The RF front-end is fabricated in a digital 0.13-μm CMOS process utilizing only standard process options for low cost. The measured performance includes a voltage gain of 50 dB, noise figure of 3.9 dB, IIP3 of -9 dBm, and minimum IIP2 of $+30$ dBm without calibration. The 4-GHz VCO achieves a phase noise of -132 dBc/Hz at 3-MHz offset.

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