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Espoo 2006

DESIGN, ANALYSIS, AND OPTIMIZATION OF RADIO FREQUENCY FRONT-ENDS FOR INTEGRATED WIRELESS RECEIVERS

Doctoral Dissertation

Pete Sivonen

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Department of Electrical and Communications Engineering
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Dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the Department of Electrical and Communications Engineering for public examination and debate in Auditorium S5 at Helsinki University of Technology (Espoo, Finland) on the 27th of October, 2006, at 12 noon.

Helsinki University of Technology
Department of Electrical and Communications Engineering
Electronic Circuit Design Laboratory

Teknillinen korkeakoulu
Sähkö- ja tietoliikennetekniikan osasto
Piiritekniikan laboratorio

Distribution:
Helsinki University of Technology
Department of Electrical and Communications Engineering
Electronic Circuit Design Laboratory
P.O. Box 3000
FI - 02015 TKK
FINLAND
URL: http://www.ecdl.tkk.fi
Tel. +358-9-451 2271
Fax +358-9-451 2269
E-mail: pete.sivonen@nokia.com

ISBN 951-22-8366-2
ISBN 951-22-8367-0 (PDF)
ISSN 1795-2239
ISSN 1795-4584 (PDF)
URL: http://lib.tkk.fi/Diss/2006/isbn9512283670/

TKK-DISS-2172

Otamedia Oy
Espoo 2006

HELSINKI UNIVERSITY OF TECHNOLOGY P. O. BOX 1000, FI-02015 TKK http://www.tkk.fi	ABSTRACT OF DOCTORAL DISSERTATION

Author Pete Sivonen

Name of the dissertation

Design, analysis, and optimization of radio frequency front-ends for integrated wireless receivers

Date of manuscript 13th of September, 2006	Date of the dissertation 27th of October, 2006

☐ Monograph ☒ Article dissertation (summary + original articles)

Department	Department of Electrical and Communications Engineering
Laboratory	Electronic Circuit Design Laboratory
Field of research	Electronic Circuit Design
Opponent(s)	Doctor Jan Crols
Supervisor	Professor Kari Halonen
(Instructor)	Doctor in Science (Technology) Aarno Pärssinen

Abstract

This thesis consists of six publications and an overview of the research topic, which is also a summary of the work. The research described in this thesis is focused on the design, analysis, and optimization of RF front-ends for wireless zero- and low-IF receivers. The main interest of the work is in the 1-4 GHz range and in CMOS and BiCMOS technologies. Often, the RF front-end limits the performance of the entire direct conversion or low-IF radio receiver.

The emphasis in this work is on the challenges posed by mass production for the design of integrated RF circuits. Thus, the effects of packaging and ESD protection on the LNA performance are analyzed and circuit optimization and design methods for the packaged LNAs are examined. This thesis also studies circuit techniques for the stabilization of the RF front-end performance against process and temperature variations. For this purpose, a gain stabilization technique for tuned LNAs is proposed. By applying the proposed method, the voltage gain variation of the inductively degenerated LNA, which is the most popular LNA architecture, is shown to be reduced several decibels. As a consequence, the radio receiver can more easily meet its specifications in the presence of IC process variations and the product yield is thereby improved. To improve the IIP2 of the mixer, a circuit technique for the cancellation of the second-order intermodulation distortion in downconversion mixer RF input stages is proposed. The presented method is shown to improve the yield of the radio receiver by reducing the IIP2 sensitivity to mismatches and offsets.

Low supply voltage and low-frequency flicker noise present in sub-micron CMOS processes pose challenges for the design of direct conversion RF front-ends, especially for narrow-band systems such as GSM. However, since the development of low-voltage CMOS analog and RF circuits is economically advantageous, the design and optimization of low-voltage CMOS RF front-ends are studied in this work.

The work summarizes the design, analysis, and optimization of several RF front-ends, LNAs, and mixers. One of the implemented RF front-ends is integrated with an on-chip VCO as a part of larger direct conversion receiver chip. One is realized with an on-chip VCO as a standalone RF front-end. Also, a standalone CMOS LNA has been characterized.

Keywords radio frequency, radio receiver, direct conversion, low-noise amplifier, downconversion mixer

ISBN (printed) 951-22-8366-2	ISSN (printed) 1795-2239
ISBN (pdf) 951-22-8367-0	ISSN (pdf) 1795-4584
ISBN (others)	Number of pages 97 p. + app. 51 p.

Publisher Electronic Circuit Design Laboratory

Print distribution Electronic Circuit Design Laboratory

☒ The dissertation can be read at http://lib.tkk.fi/Diss/2006/isbn9512283670/

TEKNILLINEN KORKEAKOULU PL 1000, 02015 TKK http://www.tkk.fi	VÄITÖSKIRJAN TIIVISTELMÄ

Tekijä Pete Sivonen

Väitöskirjan nimi

Radiotaajuusetupäiden suunnittelu, analyysi ja optimointi integroiduissa radiovastaanottimissa

Käsikirjoituksen jättämispäivämäärä 13.9.2006	Väitöstilaisuuden ajankohta 27.10.2006

☐ Monografia ☒ Yhdistelmäväitöskirja (yhteenveto + erillisartikkelit)

Osasto	Sähkö- ja tietoliikennetekniikan osasto
Laboratorio	Piiritekniikan laboratorio
Tutkimusala	Piiritekniikka
Vastaväittäjä(t)	Tohtori Jan Crols
Työn valvoja	Professori Kari Halonen
(Työn ohjaaja)	Tekniikan tohtori Aarno Pärssinen

Tiivistelmä

Väitöskirja koostuu kuudesta julkaisusta ja tutkimustyön yleiskatsauksesta. Väitöskirjassa on tutkittu suoramuunnos- ja matalanvälitaajuuden radiovastaanottimien radiotaajuusetupäiden suunnittelua ja optimointia. Radiotaajuusetupäiden ominaisuuksia on myös analysoitu laajasti. Työn pääpaino on taajuusalueessa 1-4 GHz sekä CMOS- ja BiCMOS-integrointiteknologioissa. Käytännössä radiotaajuusetupäät usein rajoittavat suoramuunnos- ja matalanvälitaajuuden radiovastaanottimien suorituskykyjä.

Tutkimustyö keskittyy mikropiirien massatuotannon integroitujen radiotaajuuspiirien suunnittelulle aiheuttamiin haasteisiin. Paketoinnin ja ESD-suojauksen vaikutuksia matalakohinaisien vahvistimien ominaisuuksiin analysoidaan ja paketoitujen vahvistimien suorituskykyjen optimointia käsitellään. Tapoja vähentää radiotaajuusetupäiden suorituskykyjen vaihteluita prosessi- ja lämpötilavaihteluiden seurauksena tutkitaan. Esitetään tekniikka, jolla matalakohinaisien vahvistimien jännitevahvistuksien vaihteluita voidaan huomattavasti pienentää. Tapa alassekoittimien toisen kertaluvun leikkauspisteiden parantamiseksi esitetään. Käyttämällä hyväksi tutkimuksen tuloksia radiovastaanottimien saantoja voidaan parantaa, koska vastaanottimet voivat helpommin saavuttaa niille asetetut vaatimukset prosessi- ja lämpötilavaihteluista huolimatta.

Lyhyen viivanleveyden CMOS-prosessien alhainen käyttöjännite ja matalataajuinen $1/f$-kohina ovat ongelmallisia radiotaajuusetupäiden suunnittelussa, etenkin kapeakaistaisissa radiojärjestelmissä. Koska radiotaajuuspiirien integrointi digitaali-CMOS-teknologioilla on kuitenkin taloudellisesti kannattavaa, tutkitaan tässä työssä alhaisen käyttöjännitteen CMOS-radiotaajuusetupäiden optimointeja ja toteutuksia.

Tutkimustyössä on suunniteltu, analysoitu ja toteutettu useita radiotaajuusetupäitä, vähäkohinaisia vahvistimia ja alassekoittimia. Yksi radiotaajuusetupäistä on integroitu jänniteohjatun oskillaattorin kanssa samalle piirillle osana suoramuunnosvastaanotinta. Yksi radiotaajuusetupää on toteutettu erillisenä integroituna piirinä jänniteohjatun oskillaattorin kanssa. Myös erillinen integroitu vähäkohinainen CMOS-vahvistin on karakterisoitu.

Asiasanat radiotaajuus, radiovastaanotin, suoramuunnos, vähäkohinainen vahvistin, alassekoitin	
ISBN (painettu) 951-22-8366-2	ISSN (painettu) 1795-2239
ISBN (pdf) 951-22-8367-0	ISSN (pdf) 1795-4584
ISBN (muut)	Sivumäärä 97 s. + liit. 51 s.

Julkaisija Piiritekniikan laboratorio

Painetun väitöskirjan jakelu Piiritekniikan laboratorio

☒ Luettavissa verkossa osoitteessa http://lib.tkk.fi/Diss/2006/isbn9512283670/

Preface

The research for this thesis has been carried out at Nokia between 2002 and 2005. I want to express my gratitude to all my present and former colleagues for their help and contributions to this work.

I would like to thank my supervisor, Prof. Kari Halonen, for giving me the opportunity to work on this thesis with a large degree of independence. I also warmly thank Prof. Asad Abidi and Prof. Francesco Svelto for reviewing my thesis and for their valuable comments and suggestions. I wish to express my gratitude to D.Sc. Aarno Pärssinen for instructing me throughout my post-graduate studies and for his expert advice.

During my thesis work, I was lucky enough to belong to a powerful research team. I am extremely grateful to my colleague Ari Vilander for his excellent ideas, advice, and comments in the field of integrated RF circuits. I also wish to thank Seppo Kangasmaa for his instruction and numerous discussions. In addition, I would like to thank Jussi-Pekka Tervaluoto for fruitful discussions and advice, and for letting me benefit from his expertise in the design of integrated radio receivers and analog baseband circuits. Finally, I would like to express my gratitude to all my present and former superiors, Mikael Svärd, Helena Pohjonen, Jarkko Posti, and Ph.D. Petteri Alinikula for their positive attitude towards my post-graduate studies and for giving me the opportunity to study for this thesis while working full time in industry.

The research for this thesis has been completely carried out while working full time in industry. Thus, finding the motivation, time, and energy to write the articles and to complete the thesis by working during evenings and weekends only has not always been easy. However, now, almost at the end of this work, I have no doubt about its significance to me. I have been able to learn a significant number of new and interesting things, I have learnt how to conduct academic research, and, most of all, I have learnt a scientific way of thinking.

Big thanks go to all of my friends for various leisure-time activities. When lacking motivation to write, there was always something else to do. My parents, Raili and Pertti, deserve my gratitude for supporting me throughout my studies.

Pete Sivonen
Helsinki, September 2006

Contents

List of symbols and abbreviations

Symbols

β_0	low-frequency current gain of bipolar transistor
δ	gate induced current noise factor
ΔA	amplitude imbalance
$\Delta\eta$	mismatch in duty cycle
Δg_m	mismatch between transconductances
$\Delta\phi$	phase imbalance
ΔR_L	imbalance of load resistances
η	bias dependent constant
η_{nom}	nominal value of duty cycle
γ	channel current noise factor
γ_N	NMOS channel current noise factor
γ_P	PMOS channel current noise factor
μ	electron mobility
τ_F	base transit time in forward direction
Θ	inversion layer mobility degradation factor
ω	angular frequency
ω_T	unity-current gain angular frequency
A	base-emitter area
A_{LO}	local oscillator amplitude
A_v	voltage gain
c	correlation coefficient between gate and drain noise
C	capacitor
C_π	base-emitter capacitance
C_b	base-charging capacitance
C_{gs}	gate-source capacitance
C_{je}	base-emitter depletion layer capacitance
C_{LF}	leadframe capacitance
C_m	matching capacitance
C_{md}	differential matching capacitance
C_{ox}	oxide capacitance
C_p	equivalent parallel package parasitic capacitance
C_{par}	parasitic capacitance
C_{ps}	parasitic capacitance at source of cascode transistor
D/A	digital-to-analog
f	frequency
F	noise factor
f_0	operation frequency
f_T	unity-current gain frequency

G	control voltage
g_{d0}	zero bias drain conductance
g_m	transconductance
G_m	transconductance
I	dc current
I	in-phase
I_B	bias current
i_C	collector current
I_C	collector bias current
$\overline{i_b^2}$	mean-square shot noise in base current
$\overline{i_c^2}$	mean-square shot noise in collector current
i_{DS}	drain-source current
I_{DS}	drain-source bias current
$\overline{i_d^2}$	mean-square thermal noise in channel current
$\overline{i_g^2}$	mean-square gate-induced current noise
i_{in}	input current
$\overline{i_n^2}$	mean-square current noise
$\overline{i_{on}^2}$	mean-square output current noise
i_{out}	output current
I_{PTAT}	PTAT bias current
I_{ref}	reference bias current
I_{SW}	switching pair bias current
I_T	tail current
k_B	Boltzmann's constant $1.38 \cdot 10^{-23} J/K$
K_f	flicker noise coefficient
$K_{2_{gm}}$	second-order nonlinearity coefficient
L	inductor
L	channel length
L_b	base inductance
L_{bw}	parasitic bondwire inductance
L_e	emitter inductance
L_g	gate inductance
L_m	matching inductance
L_s	source inductance
M	mutual inductance
M	multiplying factor
n_f	number of gate fingers
NF_{DSB}	double-sideband noise figure
n_s	number of sheet resistances
n_p	number of sheet resistances
q	charge of electron $1.6 \cdot 10^{-19} C$

Q	quadrature-phase
Q	quality factor
Q_{ind}	inductor quality factor
R	resistor
R_{eq}	equivalent resistor
r_b	base resistance
R_{cm}	series resistance of matching capacitance
R_E	emitter resistance
r_g	gate resistance
R_g	real part of impedance looking into gate
R_{in}	input resistance
R_L	equivalent load resistance
R_{lb}	series resistance of base inductance
R_{lg}	series resistance of gate inductance
R_{ls}	series resistance of inductance
r_{oc}	output resistance of cascode amplifier
R_p	shunt resistance
R_{par}	parallel resistance
R_{ref}	reference resistor
R_s	source resistance
R_{ser}	series resistance
R_{sh}	sheet resistance
R_{sub}	substrate resistance
S	slope of LO signal
S_{11}	scattering parameter
t	time
T	absolute temperature
T	impedance transformation ratio
T	LO period
T_0	standard temperature 290 K
V	DC voltage
v_π	base-emitter voltage
V_{DD}	supply voltage
V_B	bias voltage
v_{BE}	base-emitter voltage
V_{BE}	base-emitter bias voltage
v_c	control voltage
V_{eff}	gate-source overdrive bias voltage
V_{GS}	gate-source bias voltage
v_{IIP2}	differential input second-order intercept point voltage amplitude
v_{IIP3}	differential input third-order intercept point voltage amplitude

v_{in}	input voltage
v_{LO}	LO voltage amplitude
v_{out}	output voltage
$\overline{v_{on}^2}$	mean-square output voltage noise
v_{RF}	RF signal
v_s	source voltage
V_t	thermal voltage
V_T	threshold voltage
W	channel width
Z_b	impedance looking into base
Z_g	impedance looking into gate
Z_{in}	input impedance
Z_L	load impedance
Z_{R_s}	impedance looking into generator

Abbreviations

ADC	analog-to-digital converter
$BiCMOS$	bipolar complementary metal oxide semiconductor
BJT	bipolar junction transistor
BOM	bills of material
$CDMA$	code division multiple access
$CMFB$	common-mode feedback
$CMOS$	complementary metal oxide semiconductor
dc	direct current
DR	dynamic range
DSB	double-sideband
DSB-NF	double-sideband noise figure
DSP	digital signal processing
ECL	emitter coupled logic
ESD	electrostatic discharge
FET	field effect transistor
GBW	gain-bandwidth product
GPS	global positioning system
GSM	global system for mobile communications
IC	integrated circuit
ICP	input compression point
IF	intermediate frequency
$IIP2$	input second-order intercept point
$IIP3$	input third-order intercept point
IM	intermodulation
IM_2	second-order intermodulation

IM_3	third-order intermodulation
LNA	low-noise amplifier
LO	local oscillator
MOS	metal oxide semiconductor
$MOSFET$	metal oxide semiconductor field effect transistor
NF	noise figure
$NMOS$	N-channel metal oxide semiconductor transistor
PA	power amplifier
PCB	printed circuit board
PLL	phase-locked loop
$PMOS$	P-channel metal oxide semiconductor transistor
$PTAT$	proportional-to-absolute temperature
QFN	quad flat non-leaded package
RF	radio frequency
$RFIC$	radio frequency integrated circuit
SCL	source coupled logic
SNR	signal-to-noise ratio
SOC	system-on-a-chip
$SSB\text{-}NF$	single-sideband noise figure
STI	shallow trench isolation
VCO	voltage-controlled oscillator
$WCDMA$	wide-band code division multiple access
$WLAN$	wireless local area network

List of Publications

I. P. Sivonen, S. Kangasmaa, and A. Pärssinen, "A SiGe RF front-end with on-chip VCO for a GPS receiver," in *Proceedings of the European Solid-State Circuits Conference*, pp. 435-438, Florence, Italy, Sep. 2002.

II. P. Sivonen, S. Kangasmaa, and A. Pärssinen, "Analysis of packaging effects and optimization in inductively degenerated common-emitter low-noise amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 1220-1226, Apr. 2003.

III. P. Sivonen, A. Vilander, and A. Pärssinen, "A gain stabilization technique for tuned RF low-noise amplifiers," *IEEE Transactions on Circuits and Systems-I:Regular Papers*, vol. 51, pp. 1702-1707, Sep. 2004.

IV. P. Sivonen and A. Pärssinen, "Analysis and optimization of packaged inductively degenerated common-source low-noise amplifiers with ESD protection," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, pp. 1304-1313, Apr. 2005.

V. P. Sivonen, A. Vilander, and A. Pärssinen, "Cancellation of second-order intermodulation distortion and enhancement of IIP2 in common-source and common-emitter RF transconductors," *IEEE Transactions on Circuits and Systems-I:Regular Papers*, vol. 52, pp. 305-317, Feb. 2005.

VI. P. Sivonen, J. Tervaluoto, N. Mikkola, and A. Pärssinen, "A 1.2-V RF front-end with on-chip VCO for PCS 1900 direct conversion receiver in 0.13-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 384-394, Feb. 2006.

Throughout the overview, these papers will be referred to by Roman numerals.

Author's Contribution

As a general guideline, in each paper of which I was the first author, the main responsibility for the manuscript has been mine.

In Paper I, I carried out the circuit design, analysis, simulations, and measurements of all the circuits in the RF front-end, excluding the VCO, which was completely designed and measured by Seppo Kangasmaa. The system partitioning was done together with Seppo Kangasmaa. I was responsible for the top-level RF simulations. The paper itself was completely written by the author and revised by Seppo Kangasmaa and Aarno Pärssinen.

In Paper II, I had the responsibility for the theoretical analysis, circuit design, and simulations. I was also responsible for the LNA and RF front-end measurements. Seppo Kangasmaa and Aarno Pärssinen were involved in this work as instructors. The manuscript itself was entirely written by the author and revised by Seppo Kangasmaa and Aarno Pärssinen.

The gain stabilization technique presented in Paper III was developed in co-operation with Ari Vilander. I was responsible for all the theoretical work presented in this paper. I derived the design equations for the gain stabilization technique and also presented the necessary conditions for the technique to operate properly. In addition, I was responsible for the LNA and LC-tuned load simulations presented in this paper. The paper was completely written by the author and revised by Aarno Pärssinen.

I carried out the theoretical analysis, circuit design, and simulations in Paper IV. I was also responsible for the LNA measurements. The paper was entirely written by the author and revised by Aarno Pärssinen.

The IIP2 enhancement circuit proposed in Paper V was invented by myself together with Ari Vilander. In the paper, I was responsible for all the theoretical work. In addition, I performed all the simulations and wrote the paper completely. Aarno Pärssinen gave valuable comments for the manuscript and he revised the paper.

In Paper VI, I carried out the circuit design of LNA, I and Q mixers, frequency dividers, and LO buffers. Niko Mikkola designed and measured the VCO, while Jussi Tervaluoto designed the analog baseband circuitry. I performed the top-level simulations together with Jussi Tervaluoto. We also co-operated in the design of the interface between the mixer and analog baseband. The system partitioning work was mainly done by Jussi Tervaluoto. Jukka Kuivalainen and Tuomas Leinonen provided significant assistance in the RF front-end measurements. Finally, I was responsible for writing the paper, although Jussi Tervaluoto and Aarno Pärssinen gave valuable comments and suggestions for the manuscript.

1 Introduction

1.1 Background

The mobile wireless communications market has been growing very rapidly in recent years. The rapid growth has been aided by low-power, low-cost, and high-performance radio frequency integrated circuits (RFICs). Increasing the level of integration has been the major target in the design of transceivers for wireless applications. Highly integrated RFIC reduces the printed circuit board (PCB) area and complexity while lowering the component cost.

In recent years, direct conversion and low-intermediate frequency (IF) wireless radio receiver architectures have gained increasing attention [1]- [7], because in these topologies a very high level of integration can be obtained. Moreover, radio transceivers and complete systems-on-a-chip (SOC) realized in pure complementary metal oxide semiconductor (CMOS) technology are rapidly appearing in a wireless market that for years was dominated by bipolar and BiCMOS implementations [8]. RF CMOS has already become the dominant IC technology for non-cellular wireless applications such as Bluetooth [7], Global Positioning System (GPS) [9], and wireless local area network (WLAN) [10]. However, most of the commercial transceivers for cellular applications such as global system for mobile communications (GSM) [11], [12], [13], wide-band code division multiple access (WCDMA) [14], [15], and CDMA [16], [17], [18] are currently implemented in BiCMOS technology.

Development work for mass production applications poses challenges for the design of integrated RF circuits. Firstly, in order to maximize the product yield, the circuit performance must be stabilized against process, temperature, and supply voltage variations. For this purpose, appropriate circuit techniques and biasing methods must be utilized. Secondly, the power consumption, size and cost of the component parts must be minimized. In consumer electronics applications, these requirements are met by maximizing the level of integration while minimizing the number of external components and silicon area. The power consumption is also minimized by making intelligent decisions at both the architectural and circuit-design levels, and by careful system and circuit co-design. Next, commercial RFICs must also be mounted in a package to protect the circuits from mechanical stress and to ease the automatic soldering of chips to PCB. In addition, for reliability reasons, off-chip interfaces must be protected by electrostatic discharge (ESD) protection structures. Unfortunately, at RF frequencies, the package and ESD parasitics cannot be neglected and they must be carefully taken into account in the circuit design. Finally, the fact that the supply voltage of integrated RF circuits must scale down with transistor technology poses additional challenges for the analog and RF circuit design. The challenge is how to achieve a large dynamic range and meet the RF specifications, which do not relax. Low supply voltage limits the upper end of the dynamic range and prevents the stacking of several devices.

1.2 Objectives of the work

The research described in this thesis focuses on the design, analysis, and optimization of RF front-ends for wireless zero- and low-IF receivers. Both CMOS and BiCMOS implementations are discussed. Often, the RF front-end limits the performance of the entire direct conversion or low-IF receiver. The emphasis is on the challenges posed by the mass production to the design of integrated RF circuits. Thus, the effects of packaging and ESD protection on the performance of low-noise amplifiers (LNAs) are analyzed and circuit optimization methods for the packaged LNAs are studied. Also, circuit techniques for the stabilization of the RF front-end performance against process and temperature are presented. In addition, a biasing circuit technique for the cancellation of the second-order intermodulation distortion in downconversion mixer RF stages is proposed. The presented approach is shown to improve the yield of the entire zero- or low-IF radio receiver by improving the second-order intercept point (IIP2) of the mixer. Finally, this thesis also concentrates on the design and optimization techniques for 1.2-V low-voltage RF front-ends realized in pure digital CMOS.

1.3 Contents of the thesis

This thesis is divided into two parts. In the first part, an overview of the monolithic RF front-end design issues for direct conversion or low-IF receivers is given to summarize the technical work that has been carried out. In the technology aspects, the overview is focused on CMOS and BiCMOS processing technologies. In Chapter 2, the direct conversion and low-IF receiver architectures are discussed and the factors influencing the choice of the integration technology are emphasized. Next, typical requirements given for the RF front-end in wireless receivers are discussed. A detailed description of the design of LNAs and active downconversion mixers are given in Chapters 3 and 4, respectively. In Chapter 5, the RF front-end interface issues are considered. The second part of the thesis contains the published papers.

2 Highly Integrated Radio Architectures for Wireless Receivers

Nowadays most of the reported wireless receivers are based either on direct conversion or low-IF architectures, because these receiver topologies allow a very high level of integration and low cost. Zero- and low-IF receivers also reduce radio complexity by removing the need for off-chip IF filters and multiple local oscillator (LO) signals. Often, only a single external filter, which is the RF band-selection filter, is required. The channel selection filtering, either in analog or digital domain, can be performed on silicon. Thus, since in zero- or low-IF receivers there is no need to drive impedance-matched off-chip nodes, the needed chip pin count is reduced and the impedance levels between the different blocks can be optimized for maximal dynamic performance. Finally, direct conversion and low-IF architectures permit efficient integration of multimode receivers. In general, the selection of the radio receiver architecture between the zero- or low-IF topology is made on the basis of the radio system requirements and on the integration technology available.

2.1 Direct conversion receiver

A block diagram of the direct conversion receiver is shown in Fig. 1(a). The antenna feeds the received RF signal to a bandpass filter that performs the preselection of the received RF band. The LNA, which is usually the first integrated block of the receiver, amplifies the RF signal in order to reduce the noise contributions of the following stages. The LNA can be connected directly (or through an external filter) to the downconversion mixers. The mixers drive the analog baseband containing low-pass filters and gain stages.

A direct conversion receiver downconverts the band of interest directly to a zero frequency and utilizes low-pass filtering to reject nearby interference signals. An analog or digital low-pass filter can also be employed to select the desired channel and to reject all adjacent channels. The direct conversion architecture avoids the image suppression problem because the image consists of the channel itself at zero IF [19]. For the same reason, typical gain mismatches and phase errors in the two I and Q branches cause only a small loss in the detected signal-to-noise ratio (SNR). Thus, typically it is sufficient to reject the image by, say, 15-20 dB or so and this is easily obtained with conventional quadrature conversion [20]. However, the direct conversion architecture has several well-known problems such as dc offset, flicker noise, and even-order distortion, which must be considered in the design [3], [19], [21]. In wide-band communication systems such as WLAN, CDMA, and WCDMA, the realization of the zero-IF receiver becomes viable, because the large-signal bandwidth makes the system less sensitive to dc offset and $1/f$ noise. Accordingly, both CMOS and BiCMOS direct conversion receivers for WLAN, CDMA, and WCDMA applications have been proposed in the recent past [22], [23], [16], [18], [24], [3], [25]. On the other hand, since CMOS zero-IF receivers, in general, suffer from much higher flicker noise than their bipolar or BiCMOS counterparts, the direct conversion receivers for narrow-band systems, such as GSM, can be more easily implemented in BiCMOS technologies [26]. Nevertheless, GSM zero-IF receivers manufactured in CMOS technology have also been reported recently [27], [Paper VI].

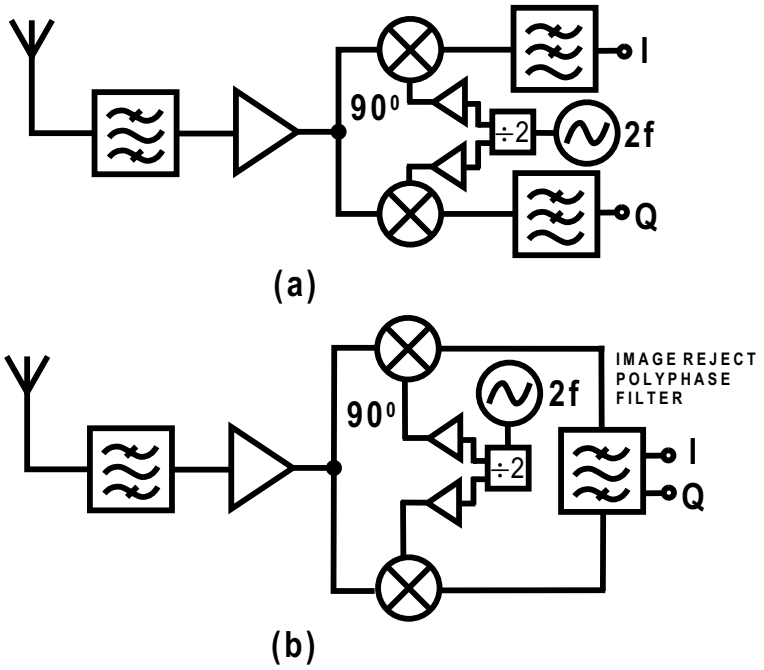

Figure 1: Block diagram of (a) direct conversion receiver and (b) low-IF receiver, assuming analog image rejection. In the case of digital image rejection, (a) also represents a block diagram of a low-IF receiver.

2.2 Low-IF receiver

In a zero-IF receiver, dc offset and flicker noise cannot be easily eliminated without removing valuable spectral energy around the dc in the downconverted spectrum [20]. On the contrary, in low-IF receivers, the band of interest is translated to a near-zero-IF frequency in such a way that the dc offset can be easily removed and $1/f$ noise has less impact on receiver sensitivity [28]. The intermediate frequency of a low-IF architecture is usually chosen in such a way that the image channel is the adjacent channel, in which the maximum allowed signal power is kept much lower than in the other channels. This solution keeps the image-rejection requirement within affordable levels. Nevertheless, in general, the requirements for the amplitude (ΔA) and phase imbalance $(\Delta\phi)$ between the I and Q paths are more stringent compared to the direct conversion receiver. For instance, in a GSM low-IF receiver, it is necessary that the image-rejection ratio is at least 32 dB or, equivalently, $\Delta A \leq 0.3$ dB and $\Delta\phi \leq 2^o$ [4], whereas in a direct conversion receiver it is usually sufficient if $\Delta A \leq 1$ dB and $\Delta\phi \leq 5^o$. Without tuning, the repeatable image rejection of a simple quadrature mixer is limited to about 40 dB [20]. The image channel may be rejected by mixing the RF with the quadrature phases of the LO, and filtering the result with a Hilbert or polyphase filter at the IF, as shown in Fig. 1(b). Unfortunately, compared to the zero-IF architecture, on-chip analog image rejection with a passive [29] or active [9] polyphase filter increases the complexity and power consumption of the receiver. An active low-pass filter (for instance, a channel filter) at zero-IF always obtains a given dynamic range with lower power than a band-pass filter with the same passband

centered at some nonzero-IF [30]. Finally, although it is possible to reject the image in a digital signal processing (DSP) by digitizing separate I and Q paths after the mixer, the analog-to-digital converter (ADC) must digitize the image as well and therefore must have higher dynamic range (DR) [4], [31]. As a conclusion, the use of low-IF receiver architecture is feasible when the mirror image suppression requirements are moderate, as, for instance, in reported low-IF CMOS receivers for GPS [32], [9], Bluetooth [7], or GSM [4].

2.3 Choice of integration technology

Most of the modern wireless radio receivers are implemented either by using CMOS or BiCMOS technologies. In this section, the benefits, drawbacks and trade-offs of these technology options are discussed.

In designs where time to market is critical, the availability of accurate simulation models is essential. Fortunately, at the moment, the existing temperature, high-frequency small-signal and noise models for both bipolar junction transistors (BJTs) and MOS devices are adequate for predicting accurately the performance of RF circuits. For instance, the RF performance of MOS transistors can be modeled accurately by using MOS Model 11, BSIM3, or BSIM4 with model extrinsic parasitic gate, substrate, drain and source resistances. On the other hand, the non-quasi-static RF model, based on the channel segmentation, is capable of predicting both the drain and gate-induced current noise accurately [33].

Generally, to achieve comparable noise factors and transconductances, bipolar topologies require less current than MOS versions due to the better g_m/I ratio [34], [35], thus making it easier to save power. However, the two types of transistors offer a roughly comparable dynamic range at a given bias [30], [36]. For instance, when designed for equal linear full scale, a degenerated bipolar differential pair gives the same transconductance per unit bias current as the corresponding MOSFET transconductor [36]. In general, the dynamic range is limited at the lower end by the noise spectral density integrated across the channel bandwidth, and at the upper end by the large signal swing that distorts gain and defines the intercept point.

The performance of bipolar RF circuits can be easily and effectively stabilized against temperature, supply and process variations by employing biasing techniques such as Proportional-to-Absolute Temperature (PTAT) or bandgap circuits [37], [38]. On the other hand, although similar biasing techniques, such constant-transconductance (g_m) circuit [39], for CMOS circuits exist, the design of robust RF MOS circuits is usually a more difficult task due to the complicated parameter variations of MOS devices with temperature and process [40]. As a result, open loop small-signal RF MOS circuits, such as amplifiers and mixers, experience larger process and temperature variations than their bipolar counterparts.

In general, BJTs provide better matching and lower flicker noise than CMOS devices. For, these reasons, the realization of a direct conversion receiver with BiCMOS tech-

nology, especially for narrow-band applications such as GSM, is easier than with pure CMOS technology. For instance, the use of BJTs as switches in active mixer and possibly in some parts of analog baseband (i.e. at the input stage of op-amps) results in lower low-frequency noise than with MOS devices only [6], [41]. Moreover, better matching due to the use of BJTs in appropriate circuits results in better second-order intermodulation (IM2) performance, which is essential in direct conversion and also in low-IF receivers [28], [42]. The availability of BJTs in BiCMOS technology should not, however, preclude the use of CMOS in those RF applications where CMOS is superior, for example in voltage controlled oscillators (VCOs) [6], [8].

Although BiCMOS technology provides some benefits over the pure CMOS technology in circuit design, and, possibly, performance wise, radio on pure CMOS offers a potential for cost reduction, since the mask count in pure CMOS technology is typically smaller than in the corresponding BiCMOS technology [43]. Moreover, integration of RF transceiver functions on standard digital CMOS technology paves the way to the realization of a single-chip radio modem. A digital baseband and RF transceiver in the same technology increases the level of integration and reduces the bills of material (BOM). CMOS technology has also the ability to operate at lower supply voltage (e.g., 1-2 V) than the BiCMOS technology. This is due to the fact, that, typically each BJT has a turn-on voltage of approximately 0.7-0.8 V and thus the absolute minimum supply voltage for BJT circuits is about 1.4-1.6 V (assuming, at maximum, two stacked transistors) [44]. On the contrary, the turn-on voltages of MOS devices can be significantly affected by doping and therefore in modern CMOS processes several different threshold voltages (V_T), such as high-, standard- and low-V_T are available. For instance, transistors with low-V_T can be utilized in analog or digital circuits, where speed is important. On the other hand, devices with high-V_T are useful when the low power consumption of the digital parts due to the leakage currents is critical.

Currently, RF CMOS technology dominates IC technology for non-cellular wireless applications such as Bluetooth and WLAN whereas most of the transceivers for cellular applications such as GSM and WCDMA are implemented in BiCMOS technology. However, all-CMOS radio transceivers are already making inroads into the cellular wireless market [8]. The challenges of CMOS technology are overcome by careful architectural decisions and by appropriate circuit-design techniques. Wherever possible, the availability of high-density logic should be exploited by pushing the design complexity into the digital domain [45]. Nevertheless, while a higher transistor unity-current gain frequency (f_T) and the consequent speed is welcome in fine-line CMOS with gate lengths of 0.13 μm or below, the lower supply voltage of 1.2 V or below poses additional challenges.

2.4 Requirements for RF front-end

In this section, typical requirements given for the direct conversion or low-IF receiver RF front-end are discussed. In this thesis, the RF front-end refers to the LNA, I and Q mixers, and LO quadrature generation circuit excluding the VCO and phase-locked loop (PLL). The LNA and mixer together determine the front-end performance. Thus, an optimum performance can only be obtained by co-designing the front-end circuits. Moreover, in practice, the RF front-end dominates the linearity and noise performance of the entire zero- or low-IF receiver.

As seen from Fig. 1, the RF front-end architecture in both zero- and low-IF receiver topologies is the same. Actually, if the image rejection is performed in the digital domain, Fig. 1(a) also represents the block diagram of both receiver topologies. In general, the requirements given for the zero- and low-IF receiver RF front-end for certain applications are also very similar. However, the requirements nevertheless usually differ at least in terms of I and Q balance, dc offset, low-frequency noise, and second-order nonlinearity.

The RF front-end of a wireless receiver must simultaneously meet several requirements [46]. First, as shown in Fig. 1, an RF front-end is practically always preceded by an off-chip filter. Accordingly, the RF input impedance of the front-end has to be designed to match the characteristic impedance, e.g., 50 Ω, of the filter. If the terminating impedances of the RF preselection filter differ from the specified characteristic impedance, the results may be a large ripple in the passband and a poorer transition band of the filter. Secondly, the input-referred noise, and thus the noise factor (F) of the front-end, must be sufficiently low to enable detection of weak input signals. In particular, the noise factor for the direct conversion presented in Fig. 1(a) is given as [47], [2]

$$F = F_1 + \frac{F_2 - 1}{\left(\frac{A_{v1}}{2}\right)^2} + \frac{F_3 - 1}{\left(\frac{A_v1}{2} \times A_{v2}\right)^2} + ... \tag{1}$$

where A_{vi} represents the voltage gain of the i^{th} block and F_1, F_2, and F_3 are the noise factors of the LNA, mixer, and low-pass filter, respectively. F_2 and F_3 are defined as the input-referred noise voltage of each circuit scaled to the noise in a hypothetical 50-Ω resistor [30]. The first two terms in Eq. (1) represent the noise factor of the RF front-end itself. Moreover, from Eq. (1) it is seen that the front-end gain $(A_{v1} \times A_{v2})$ must be sufficiently high to overcome the noise contributions of the following circuits (i.e. the low-pass filter shown in Fig. 1(a)), which may otherwise degrade the receiver sensitivity. Typically, the maximum voltage gain of the RF front-end is in the range of 20 dB to 40 dB. However, depending on the mixer-analog baseband interface, the RF front-end can utilize current- instead of voltage-mode signal processing at the mixer output [4], [Paper VI]. Thus, in that particular case, the front-end gain is expressed more conveniently in terms of transconductance instead of voltage gain. Finally, to improve the receiver linearity with high RF input signal levels, the gain of the RF front-end is often variable.

Flicker noise at zero or low IF can be troublesome, particularly in CMOS receivers. The noise factor of CMOS mixers, baseband amplifiers, and filters may be much higher at low

frequencies than those based on estimates of thermal noise alone. Accordingly, besides the low level of thermal noise, the $1/f$ noise corner frequency of the RF front-end must be located at a sufficiently low frequency to ensure that the flicker noise does not worsen the integrated noise factor more than is tolerable [48]. Given the particular integrated noise factor target and level of thermal noise, the RF front-end for a zero-IF receiver must naturally provide a lower $1/f$ corner frequency than for a corresponding low-IF receiver.

Due to the third-order nonlinearity of the RF front-end, two large undesired signals at the adjacent channels can create a third-order intermodulation (IM3) product at the desired channel [49]. If the energy of the IM3 product is sufficiently large, it can overlap and corrupt the weak desired signal. Accordingly, the front-end must have a sufficiently large third-order intercept point (IIP3) to withstand this effect. In particular, the IIP3 for the direct conversion receiver presented in Fig. 1(a) is given as [2]

$$\frac{1}{IIP3} = \frac{1}{IIP3_1} + \frac{A_{v1}^2}{IIP3_2} + \frac{(A_{v1} \times A_{v2})^2}{IIP3_3} ... \tag{2}$$

where $IIP3_i$ is the IIP3 of the i^{th} block measured in terms of the input signal power dissipated in a reference 50-Ω resistor. Again, the first two terms in Eq. (2) represent the IIP3 of the RF front-end itself. From Equations (1) and (2) it is seen that, although a high front-end gain reduces the noise contributions of the downstream stages, the gain can not be arbitrarily large, because, otherwise, the receiver linearity is degraded.

In addition to IIP3, the RF front-end must have a sufficiently high input compression point (ICP) to tolerate large blocking or interference signals. A strong signal can reduce the front-end small-signal gain when the front-end is receiving a weak desired signal, or it can cause a rise in the noise level [50].

One of the most severe limitations on the use of direct conversion techniques, and also an issue in a low-IF receivers, is the need for a very high second-order intercept point (IIP2) [42]. In the RF front-end, the second-order intermodulation introduces undesirable spectral components at the baseband, which degrade the receiver sensitivity. For instance, if two strong interferers at frequencies f_1 and f_2 close to the channel of interest experience even-order distortion, they generate a low-frequency interference signal at the frequency $f_1 - f_2$. Again, to withstand this effect, the IIP2 of the RF front-end must be high enough.

In a zero-IF receiver, the downconverted band extends to a zero frequency. Accordingly, extraneous offset voltages can corrupt the signal. Thus, in order to prevent the baseband circuits or ADC from saturating, the dc offset voltage at the RF front-end output must be sufficiently low. Compared to the zero-IF architecture, low-IF topology is less susceptible to dc offset [4]. In addition to dc offset, the LO leakage to the front-end RF input must not exceed a certain level. The leakage of the LO signal to the antenna can create radiation interference in the band of other users using the same or nearby channel [21].

Amplitude imbalance (ΔA) and phase error $(\Delta\phi)$ between the I and Q paths of the RF front-end can corrupt the downconverted signal constellation and raise the bit rate [21].

As discussed in Section 2.2, in general, the specifications for the ΔA and $\Delta\phi$ between the I and Q paths are more stringent in the low-IF architecture compared to the zero-IF topology.

Product development for consumer electronics applications pose additional requirements for the RF front-end circuit design. To maximize the product yield, the above listed front-end requirements must also be met in the presence of process, temperature, and supply voltage variations. In addition, the RF front-end power consumption, silicon area, and number of off-chip components must be minimized and the RF front-end off-chip interfaces, in practice the front-end RF input, must be protected by ESD protection structures. Finally, usually the front-end circuits must be realized with differential topologies to increase the immunity to common-mode interference from substrate or supply perturbations.

As an example, Table 1 lists some typical requirements given for the direct conversion receiver RF front-end (from the LNA input to the mixer output) for WCDMA applications [51], [52], [53].

Table 1: Typical requirements for the RF front-end of a WCDMA direct conversion receiver.

Parameter	Specification	Unit
Receive band	2110-2170	MHz
S_{11}	$\leq$ -10	dB
Voltage gain (max.)	33	dB
DSB-NF @ gain max	3	dB
IIP3 @ gain max	-8	dBm
IIP2 @ gain max	+42	dBm
I/Q gain imbalance	1	dB
I/Q phase imbalance	3	deg
LO at RF input	-60	dBm

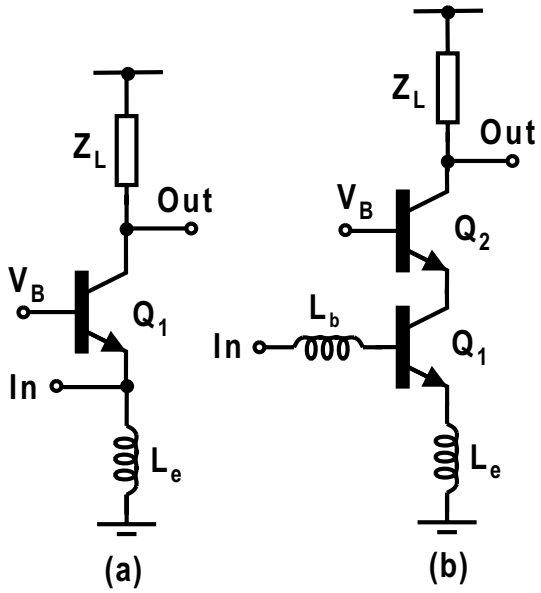

Figure 2: (a) Common-base LNA. (b) Inductively degenerated common-emitter LNA.

3 Low-Noise Amplifier Design

In wireless receivers, an LNA is typically the first amplifying stage. Thus, it is responsible for providing signal amplification while not degrading SNR, and its noise factor sets a lower bound on the noise factor of the entire receiver IC. Moreover, as seen from Eq. (1), the gain of the LNA has to be large enough to suppress the noise contributions of the following mixer and baseband. However, too large gain can overload the mixer and compromise the receiver linearity (see Eq. (2)). Typically, the LNA gain is in the range of 15-25 dB. The LNA must also have sufficient linearity to prevent the intermodulation products of a strong interferer from overwhelming the weak desired signal. Nevertheless, usually in a well-designed RF front-end, it is the downconversion mixer that limits the front-end linearity.

As described already in Section 2.4, the input impedance of the LNA has to be designed to match the characteristic impedance, e.g., 50 Ω, of the duplex filter. The output matching is also required if the LNA is followed by an external filter. In addition, the LNA must provide sufficient reverse isolation to reduce the amount of LO signal that leaks from the mixer to the antenna [40].

3.1 LNAs for CMOS and BiCMOS technologies

Most of the modern radio receivers use either the common-base (gate) [2], [35] or the inductively degenerated common-emitter (source) [3], [54], [55] LNA architectures shown in Figures 2(a) and 2(b), respectively. Moreover, usually these topologies are realized as narrow-band circuits in order to save power and reject the out-of-band interfering signals

and noise. Unfortunately, typically the use of common-base and common-gate LNAs is limited only to applications, where the LNA noise figure ($NF = 10\log(F)$) of 2-3 dB, or above, is tolerable. Nevertheless, a common-base LNA utilizing feedback is capable of achieving NF below 2 dB [56]. Unfortunately, in feedback-type LNAs, the realization of variable gain (or discrete values of gain) becomes complicated, because the LNA input impedance depends on the voltage gain of the amplifier. On the other hand, if the variable gain is implemented in a mixer instead of an LNA [56], the mixer must have higher linearity. For these reasons, nowadays, most of the wireless receivers use the inductively degenerated common-emitter or common-source LNA architectures. With these circuit topologies, excellent input matching and NF below 2 dB can be achieved simultaneously. For this reason, this thesis concentrates only on the inductively degenerated common-emitter and common-source LNA circuits.

3.2 Impacts of packaging and ESD protection

In consumer electronics applications in which mass production is used, the integrated circuits are almost always mounted in a package to protect the circuits from being damaged. In addition, off-chip interfaces must be protected against ESD. In the circuit design for RF frequencies, the package and ESD parasitics can have a significant effect on the circuit performance. Moreover, in general, these parasitics do not scale down with technology [30]. For these reasons, the package and ESD parasitics must be carefully modeled and considered during the circuit design phase, since they are a vital part of the circuit. For the circuit simulations accurate models for the parasitics are preferred, but analytical models are essential to develop guidelines for circuit design and optimization.

Typically, in zero- or low-IF receivers with an on-chip VCO (see Fig. 1), the only RF off-chip interface is the LNA input. Thus, the package and ESD parasitics have effect on the RF front-end performance only via the LNA input, as the differential signal processing is considered. Non-ideal ground and supply pins have effect only on the common-mode signals.

Although most of the reported wireless receivers use the common-emitter (source) LNA architecture and the optimization of this topology has been extensively examined in the literature, the effects of the package and ESD parasitics are often for simplicity neglected in the analysis [54], [55], [57], [58], [59]. However, as the off-chip parasitics are part of the LNA, the models for the parasitics are necessary to predict the LNA performance.

In the following, the effects of packaging, parasitics of ESD protection structures, and the input impedance matching network on the performance of inductively degenerated common-emitter and common-source LNAs are studied and the performance of the packaged LNAs are optimized. It is shown that the package and ESD parasitics have effect on the LNA input impedance, input stage transconductance, voltage gain, noise factor, and linearity. The presented equations provide design guidelines and insight for the optimization principles and fundamental limitations of the packaged common-emitter and common-source LNAs.

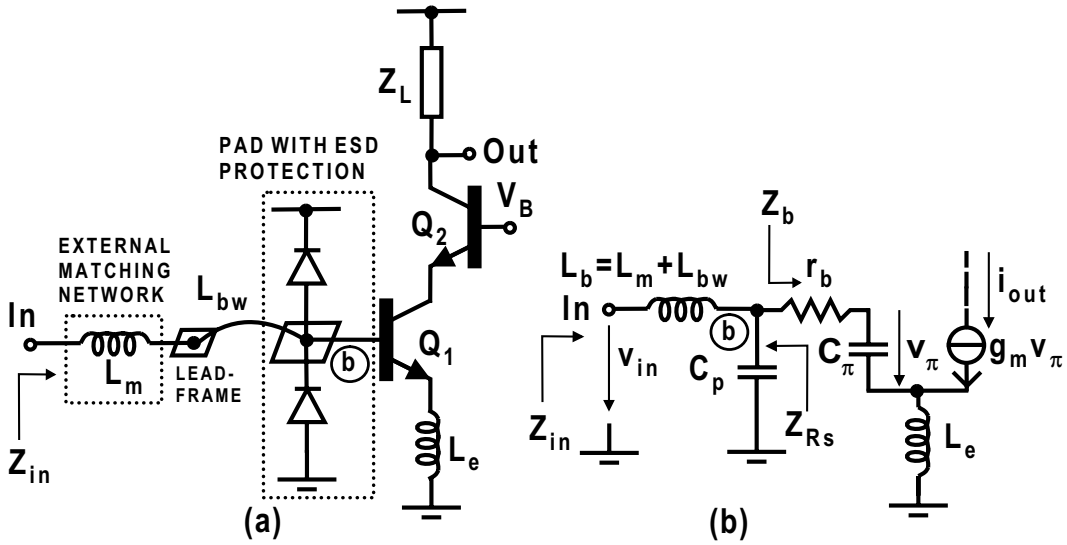

Figure 3: (a) Single-ended equivalent circuit of packaged inductively degenerated common-emitter LNA with ESD protection and (b) its input stage small-signal model.

The effects of the package parasitics and ESD protection diodes on the inductively degenerated common-emitter LNA performance can be analyzed by considering the schematic shown in Fig. 3. Only the single-ended equivalent circuit of the packaged amplifier with ESD protection is shown, but the results to be presented apply also to the balanced configuration. As shown in Fig. 3, the bonding pad, ESD diodes, Miller capacitance of Q_1, and parasitic capacitance of bondwire introduce a parallel parasitic capacitance at the base of the LNA input device Q_1 (see node 'b' in Fig. 3). The total parasitic capacitance can be modeled as an *equivalent parallel package parasitic capacitance* C_p at the base of Q_1, as shown in Fig. 3(b) [34], [60], [61], [62], [Paper II], [Paper IV]. In Fig. 3, the effects of the self inductance of the bondwire and the inductance due to the mutual inductance between the adjacent bondwires are modeled by a series inductance L_{bw}. Since L_{bw} is in series with an external matching inductor (L_m), the total series base inductance (L_b) is $L_m + L_{bw}$. The model for the parasitics shown in Fig. 3 can be made relatively accurate provided that the adjacent pins of RF signals are grounded or otherwise properly terminated, as described in detail below.

Although the model for the package and ESD parasitics shown in Fig. 3 uses only two circuit elements, it will still give a clear and accurate insight into how the properties of the LNA are modified by the parasitics. Moreover, the model shown is convenient for hand calculation purposes. In simulations, however, a detailed model shown in Fig. 4(a) can be used.

If a balanced LNA topology is employed and the differential input signal pins of the amplifier are selected so that the adjacent pins are ground pins, each coupling capacitance

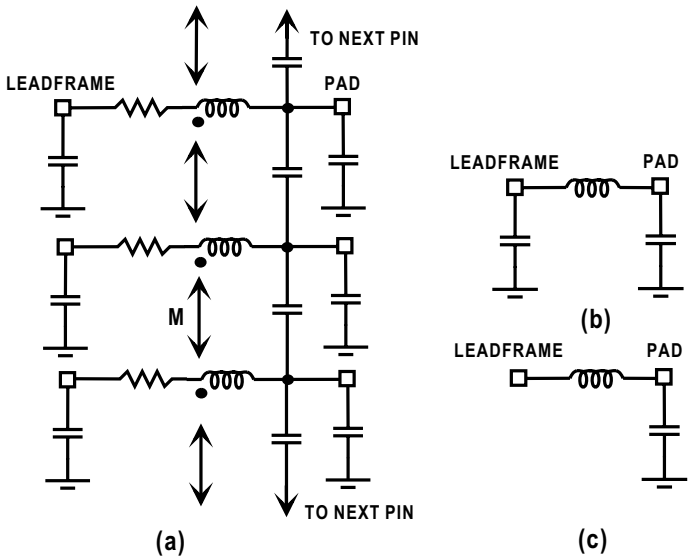

Figure 4: (a) Detailed model for the package and ESD parasitics. (b)-(c) Simplified models for the parasitics.

shown in Fig. 4(a) between the signal pin and adjacent ground pin also becomes a parallel capacitance between the signal pin and ground. The resistance in series with the bondwire is negligible in practice. Thus, the package model for the both differential LNA input signal pins is reduced to the π-network shown in Fig. 4(b).

In practice, parasitic capacitance is always present at some level at the leadframe of the package. However, the leadframe capacitance can be minimized to negligible levels by utilizing the minimum-width PCB traces to route the leadframe and the external base inductor, and by placing the ground layer underneath this RF trace sufficiently deeply in the multilayer PCB. Thus, in that particular case the leadframe capacitance is much smaller than the parasitic capacitance at the pad side, and the leadframe capacitance can be neglected in the analysis. Thus, the model for the package and ESD parasitics shown in Fig. 4(c) can be used.

3.3 Packaged inductively degenerated common-emitter LNA with ESD protection

The parallel parasitic capacitance C_p affects the input impedance (Z_{in}) (see Fig. 3) of the inductively degenerated common-emitter LNA by transforming the real part of Z_{in} downwards. Nevertheless, here it is assumed that the input impedance of the amplifier can still be matched to the source impedance (R_s) by employing only a series base inductance as shown in Fig. 3.

The effects of the package and ESD parasitics on the LNA input impedance matching can be analyzed by using a parallel-series transformation technique [39], [62]. At the

operation frequency, the real part of Z_{in} can be approximated by [Paper II]

$$Re(Z_{in}) = R_{in} = \left(\frac{C_\pi}{C_p + C_\pi}\right)^2 \cdot R_{eq} = k^2 \cdot R_{eq} \tag{3}$$

where

$$R_{eq} = \frac{g_m L_e}{C_\pi} + r_b \approx \omega_T L_e \tag{4}$$

and

$$k = \frac{C_\pi}{C_p + C_\pi} \tag{5}$$

Here R_{eq} represents the real part of the impedance Z_b looking into the base of Q_1. Moreover, R_{eq} is the real part of the LNA input impedance, which is achieved in the absence of parasitics [32] (i.e. $C_p = 0$). In addition, the input impedance matching requires that $R_{in} = R_s$. Here L_e is the emitter inductance, C_π is the base-emitter capacitance, g_m is the transconductance, r_b is the base resistance, and $\omega_T \approx g_m/C_\pi$ is the unity-current gain angular frequency of Q_1, respectively. The value of L_b must be selected to tune the input impedance to the frequency of interest (f_0) [Paper II]

$$L_b = \frac{1}{(C_p + C_\pi)\omega_0^2} \tag{6}$$

Figure 5 illustrates the simulated f_T of a bipolar transistor in a 0.35-μm BiCMOS technology for different base-emitter areas ($A = 1, 2, ...7\times$), and as a function of collector bias current (I_C). The unit NPN transistor has two base contacts and an emitter size of 0.4 x 10 μm^2. It is seen that, if the base-emitter junction area is increased, for instance, to reduce r_b, the BJT has to be biased at a larger I_C to obtain a certain f_T. The decline in f_T at high collector currents (clearly seen in Fig. 5 for $A = 1$) is due to an increase in the base transit time in the forward direction (τ_F) caused by high-level of injection and Kirk effect at high currents [37].

From Eq. (3) it is concluded that, because of the parasitic capacitance at the transistor base, the LNA input impedance comes down by a factor of $k^2 \leq 1$ compared to the unpackaged amplifier with a given ω_T and a certain size of L_e. Accordingly, in general, to achieve a comparable LNA input impedance level, a packaged amplifier requires a larger L_e for a given sized input device (i.e. C_π) and I_C ($g_m = I_C/V_t$) than the corresponding unpackaged LNA (i.e. $C_p = 0$). At 29°C, $V_t = k_B T/q$ =26mV where q is the electron charge, k_B is the Bolzmann's constant, and T is absolute temperature, respectively.

Figure 6 illustrates the effect of C_p on the single-ended LNA input impedance at the resonance frequency. In this example, f_0=1.575 GHz, $I_c = 1.1$ mA, $L_e = 1.1$ nH, $C_\pi = 575$ fF, and $r_b = 5\ \Omega$ giving $R_{eq} \approx 89\ \Omega$. The values represent rather typical values for the LNA designed in a 0.35-μm BiCMOS technology for GPS applications [Paper II]. Moreover, in the 0.35-μm BiCMOS technology utilized in this work, the total parasitic parallel capacitance C_p including the capacitance due to the quad flat nonleaded (QFN) package parasitics, ESD protection diodes, and bonding pad structure is about 600 fF [Paper II].

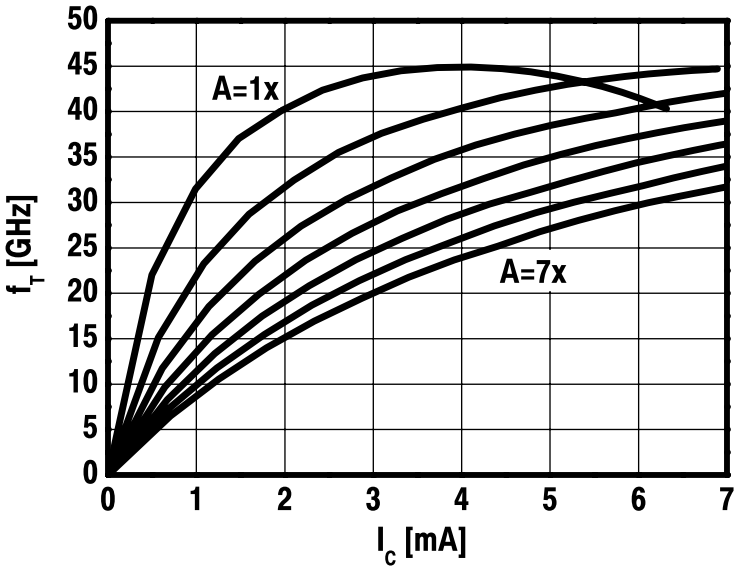

Figure 5: Simulated unity-current gain frequency of BJT in 0.35-μm BiCMOS technology for different base-emitter junction areas. A unit NPN transistor has two base contacts and an emitter size of 0.4 x 10 μm^2.

Thus, in the 0.35-μm BiCMOS technology with an LNA mounted in a QFN package, C_p might easily be in the same order of magnitude as the base-emitter capacitance of the practically sized and biased input device of the amplifier, i.e. $C_\pi \approx C_p$. Moreover, with given component values, Eq. (3) predicts $R_{in} \approx 21.4\,\Omega$, which is only in the order of a few tens of ohms, instead of 50 Ω traditionally used.

It is possible to scale up the R_{in} of the packaged LNA to some extent by scaling up L_e, but, in practice, this might make it difficult to obtain enough voltage gain from the amplifier. On the other hand, if $C_\pi < C_p$, R_{in} can be made larger by increasing C_π. In practice, $C_\pi = C_b + C_{je}$ can be made larger by scaling up the base-emitter area or biasing the input device at a larger I_C, which increases the base-charging capacitance $C_b = \tau_F g_m$ [37]. Here, C_{je} is the emitter-base depletion layer capacitance. Unfortunately, it is easy to show that for a given C_p, R_{in} can be scaled up by increasing C_π only up to $C_\pi = C_p$. Further increase of C_π will actually decrease R_{in}. Finally, a higher I_C results also in a higher device ω_T (see Fig. 5), and thus a larger R_{eq} and R_{in}, but a higher I_C increases the power consumption of the amplifier.

The input impedance level of the packaged amplifier can also be transformed upwards by utilizing an external impedance transformation network. However, this solution increases the cost, since an additional off-chip component is required. In addition, the higher the impedance transformation scale factor at the LNA input is, the larger is the required quality (Q) factor of the matching circuit. In fact, when scaling impedance by a large fac-

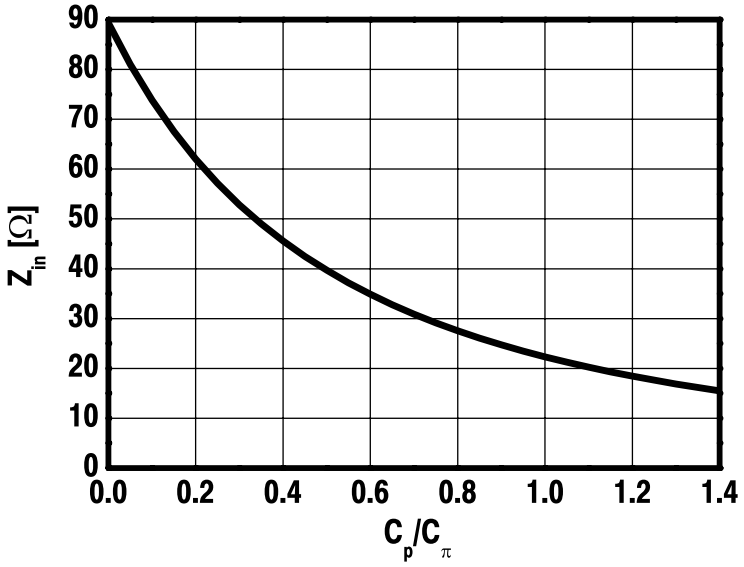

Figure 6: Effect of package parasitic capacitance on LNA input impedance.

tor, the required Q factor of the matching circuit grows quadratically and the LNA input matching becomes sensitive to parasitics, process and component variations [36]. On the other hand, by employing only a series base inductance for the matching, the Q value of the input network is only moderate and the LNA input impedance matching is very tolerant against variations.

Due to the reasons discussed above, it can in some cases be reasonable to select the input impedance level of the packaged LNA to be lower than the typically employed 100 Ω differential, for instance 50 Ω [Paper II]. This is also possible from the practical point of view, since low-loss external baluns or preselection filters are available for an impedance transformation ratio of 1:1.

The input stage transconductance (G_m) of the packaged LNA with ESD protection at the operation frequency f_0 can also be computed in a straightforward manner with the help of the parallel-series transformation steps, or by treating the network formed by L_b and C_p as a lossless reciprocal impedance matching network [36]. Either way, assuming perfect impedance matching $R_{in} = R_s$, G_m at ω_0 is given by [Paper II]

$$G_m = \left|\frac{i_{out}}{v_{in}}\right| = \sqrt{\frac{R_{eq}}{R_s}} \cdot \frac{1}{\omega_0 L_e} \cdot \frac{1}{\sqrt{1+\omega_0^2 C_\pi^2 R_{eq}^2}} \approx \sqrt{\frac{R_{eq}}{R_s}} \cdot \frac{1}{\omega_0 L_e} = \sqrt{\frac{\omega_T}{L_e R_s}} \cdot \frac{1}{\omega_0} \quad (7)$$

According to Eq. (7), G_m depends on the value of C_p. For instance, if C_p is increased at constant collector current I_C and thus ω_T, L_e must be scaled up to preserve the LNA input impedance match (see Eq. (3)). As a result, G_m is decreased. On the other hand,

in order to preserve both the input impedance and G_m of the amplifier in their original values, both L_e and ω_T must be scaled up if C_p is increased.

Assuming that the LNA drives I and Q downconversion mixers directly on-chip, as is usual in direct conversion and low-IF receivers, the voltage gain of the packaged amplifier can be expressed as [Paper II]

$$A_v = |G_m Z_L(j\omega_0)| \approx \sqrt{\frac{R_{eq}}{R_s}} \cdot \frac{|Z_L(j\omega_0)|}{\omega_0 L_e} \tag{8}$$

where $Z_L(j\omega_0)$ is the LNA load impedance at ω_0.

The calculation of the noise factor of the packaged LNA with ESD protection can be significantly simplified if the impedance Z_{R_s} looking into the generator (see Fig. 3) is first transformed to the equivalent series impedance at the operation frequency f_0. The complex conjugate impedance matching requires that $Z_{R_s} = Z_b^*$, where Z_b is the impedance looking into the base of Q_1. Accordingly,

$$Z_{R_s} = Z_b^* \approx \left(\omega_T L_e + \frac{1}{j\omega_0 C_\pi} + j\omega_0 L_e\right)^* \approx \omega_T L_e + \frac{j}{\omega_0 C_\pi} \tag{9}$$

Thus, by calculating all the noise current contributions at the LNA output current, and by assuming perfect power matching $R_{in} = R_s$, it can be shown that the noise factor of the packaged amplifier at f_0 is given by [Paper II]

$$F_{LNA} = 1 + \frac{R_{lb}}{k^2 R_{eq}} + \frac{r_b}{R_{eq}} + \frac{g_m R_{eq}}{2\beta_0} + \frac{1}{2 g_m R_{eq} \beta_0}\left(\frac{\omega_T}{\omega_0}\right)^2 + \frac{g_m R_{eq}}{2}\left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{4R_{eq}}{R_L}\left(\frac{\omega_0}{\omega_T}\right)^2 \tag{10}$$

where β_0 is the low-frequency current gain of Q_1. The first and second terms are the thermal noise due to the series resistance (R_{lb}) of L_b and r_b, respectively. The third and fourth terms account for the shot noise in the base current $\overline{i_b^2} = 2qI_C\Delta f/\beta_0$, the fifth is due to the shot noise in the collector current $\overline{i_c^2} = 2qI_C\Delta f$, while the last term is the thermal noise due to the equivalent load resistor (R_L). Eq. (10) neglects the noise contribution of the cascode transistor to the LNA noise factor. This, however, is a reasonable assumption [Paper II]. Since $R_{eq} = R_s/k^2$, Eq. (10) can also be written as

$$F_{LNA} = 1 + \frac{R_{lb}}{R_s} + \frac{r_b k^2}{R_s} + \frac{g_m R_s}{2\beta_0 k^2} + \frac{k^2}{2 g_m R_s \beta_0}\left(\frac{\omega_T}{\omega_0}\right)^2 + \frac{g_m R_s}{2k^2}\left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{4R_s}{k^2 R_L}\left(\frac{\omega_0}{\omega_T}\right)^2 \tag{11}$$

If Eq. (11) is compared with the equation describing the noise factor of the unpackaged LNA [55], it can be seen that, excluding the noise due to R_{lb}, the equation for the noise factor of the packaged amplifier is obtained from the unpackaged case by replacing R_s by $R_{eq} = R_s/k^2$. This is also intuitively reasonable, since in packaged LNA, R_{eq} represents the real part of the impedance Z_{R_s} looking into the generator at impedance match.

To validate Eq. (11) by means of circuit simulation, Figure 7 plots the simulated NF $(10\log(F_{LNA}))$ of the packaged LNA in 0.35-μm BiCMOS with ESD protection at 1.575 GHz

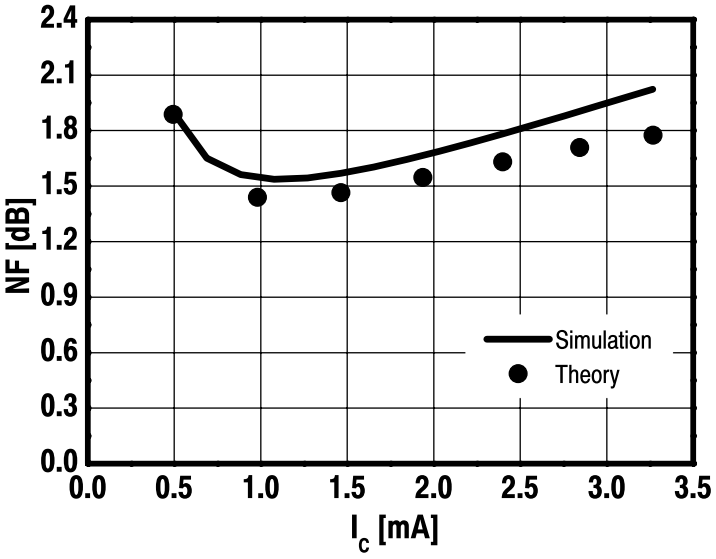

Figure 7: Theoretical (dots) and simulated (solid line) NF at 1.575 GHz versus collector current, for the packaged inductively degenerated common-emitter LNA.

as a function of input device I_C together with theoretical values calculated by using Eq. (11). In this example, the unit NPN transistor has two base contacts and an emitter size of 0.4 x 10 μm^2, and the input BJT employs four unit transistors in parallel. Moreover, in this simulation, $C_p = 600$ fF. Corresponding to each value of I_C, the input impedance in the simulation is matched to a 25 Ω [Paper II] (instead of 50 Ω) by tuning L_e and L_b accordingly. The other component values used are $R_{lb} = 2.2\ \Omega$, $R_L = 90\ \Omega$, $\beta_0 = 80$, and $r_b = 10\ \Omega$. In theoretical calculations, r_b includes also the component due to the parasitic emitter resistance (r_e), since r_e contributes to the LNA NF exactly similarly as r_b [55]. According to Fig. 7, the deviation between simulated and calculated noise figures is smaller than 0.25 dB. Accordingly, a good agreement between the theory and simulation is found.

From Eq. (11) it is concluded that, since k is lower than unity, C_p due to the package and ESD parasitics affects the LNA noise factor by reducing the noise contributions of r_b and $\overline{i_b^2}$ (in practice the fourth term due to $\overline{i_b^2}$ always dominates over the third term). This can also be understood by noticing that, in the presence of C_p, $R_{eq} = \omega_T L_e$ can be designed to be larger than R_s without violating the input matching constraint of the amplifier. (For instance, for a given ω_T, the packaged LNA must utilize a larger emitter inductance to realize a given input impedance level than the corresponding unpackaged amplifier biased at equal I_C to obtain equal ω_T.) For the same reason, the input BJT in the packaged LNA sees a larger impedance looking into the generator than in an unpackaged amplifier. A similar effect can be achieved by introducing an additional capacitor C_{BE}

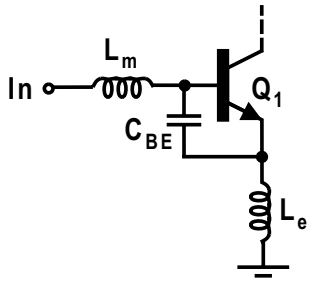

Figure 8: Inductively degenerated common-emitter LNA with parallel-series matching network. Capacitor C_{BE} reduces noise contributions of r_b and $\overline{i_b^2}$.

between the base and emitter of the LNA input BJT [55] (see Fig. 8). The resulting mixed parallel-series input matching network reduces the noise contributions of the LNA input circuit (i.e. r_b and $\overline{i_b^2}$) [55]. Unfortunately, again as in an LNA with a mixed parallel-series input matching network [55], packaging increases the frequency-dependent terms due to $\overline{i_c^2}$ and R_L (see Eq. (11)). These terms, however, can be lowered by biasing the BJT at higher ω_T.

From Eq. (11) it is seen that the noise contributions of $\overline{i_c^2}$ and R_L decrease while increasing the collector current I_C. On the other hand, since the terms due to r_b and $\overline{i_b^2}$ increase with I_C (k increases with I_C), an optimum value for I_C, corresponding to the minimum LNA noise factor, exists. Moreover, the LNA input BJT must utilize a base-emitter area A that is sufficiently large to reduce the noise due to r_b. However, since a larger area requires a higher I_C to obtain a given ω_T, the device area cannot be selected to be arbitrarily large without violating the power consumption constraint of the amplifier.

The IIP3 of the LNA shown in Fig. 3 can be approximated as [36]

$$v_{IIP3,LNA} \approx \frac{v_{IIP3,BJT}}{|v_\pi/v_{in}|} = \sqrt{\frac{R_s}{R_{eq}}}(g_m\omega_0 L_e)v_{IIP3,BJT} = \sqrt{\frac{L_e R_s}{\omega_T}}(g_m\omega_0)v_{IIP3,BJT} \quad (12)$$

where $v_{IIP3,BJT} = 2\sqrt{2}V_t$ is the IIP3 of the input BJT Q_1 [79] and the passive input network amplifies the input voltage across Q_1 by $|v_\pi/v_{in}| = \sqrt{R_{eq}/R_s}/(g_m\omega_0 L_e)$. If the value of C_p is increased, L_e must be scaled up to preserve the LNA input impedance match at constant I_C and ω_T, as described earlier. Simultaneously, the voltage swing across the base-emitter junction of Q_1 is reduced and the IIP3 of the amplifier is improved.

In the following, the noise optimization of the packaged LNA is considered. Since the downconversion mixer in practice often dominates the linearity of the RF front-end (naturally this is not always the case), the linearity optimization of the LNA is not considered here. Nevertheless, from Eq. (12) it is seen that the IIP3 of the amplifier can be improved by scaling up I_C or L_e.

The minimum noise factor of the packaged LNA with ESD protection can be found for in-

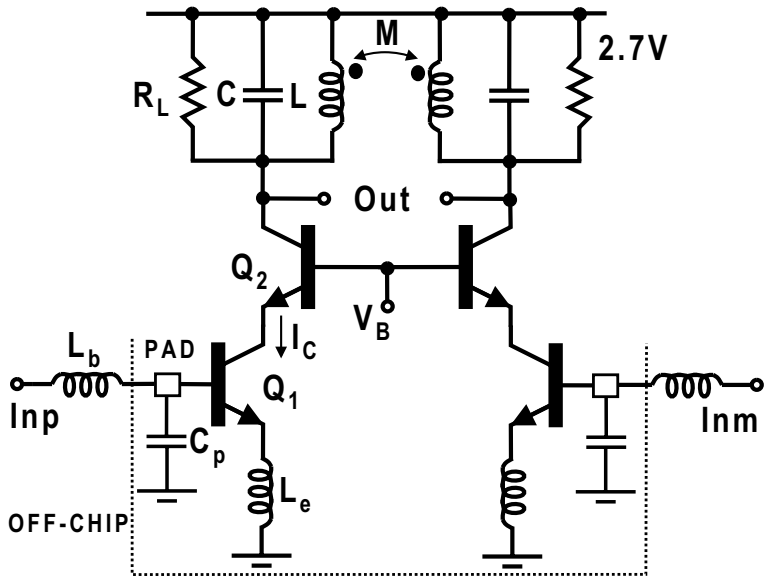

Figure 9: Packaged 1.575-GHz inductively degenerated common-emitter LNA with ESD protection in 0.35-μm BiCMOS.

stance as follows. First, the base-emitter junction area A is fixed to a certain value. Next, I_C is swept until the minimum LNA noise factor is found. Corresponding to each value of I_C, the value of L_e is scaled to ensure that $Re(Z_{in}) = R_s$ (see Eq. (3)). In addition, the value of L_b is chosen to tune the input impedance to the frequency of operation f_0 (see Eq. (6)). In the next step, the base-emitter area is increased or set to another value and the procedure is repeated until an optimum value for I_C, which corresponds to the minimum noise factor with the given power consumption constraint, is found. Finally, the voltage gain of the amplifier can be set to the desired value by designing the load impedance accordingly (see Eq. (8)) [Paper III].

Figure 10 plots the simulated NF $(10\log(F_{LNA}))$ of the packaged differential LNA (see Fig. 9) with ESD protection, realized in a 0.35-μm BiCMOS technology with a supply voltage of 2.7 V, at 1.575 GHz as a function of input device I_C with different values of base-emitter areas of Q_1 ($A_1 = 1, 2, ...7\times$). Again, the unit NPN transistor has two base contacts and an emitter size of 0.4 x 10 μm^2. Moreover, in this example, $C_p = 600$ pF. Corresponding to each value of I_C, the input impedance is matched to a differential impedance of 50 Ω [Paper II] (instead of 100 Ω) by tuning L_e and L_b as described above. The LNA load impedance, consisting of a damped LC resonator, is tuned to 1.575 GHz and R_L is scaled to obtain approximately 22 dB peak voltage gain. From Fig. 10, it is seen that, if A_1 is $4\times$ or larger, the minimum NF remains relatively constant. However, a larger A_1 requires a higher I_C to obtain the minimum NF. Thus, it can be advantageous to select, for instance, $A_1 = 4$, i.e. four transistors parallel, for which the minimum NF of 1.7 dB is obtained at $I_C = 1.1$ mA. Thus, the total current consumption of the amplifier is 2.2 mA. The emitter and base inductors of 1.1 nH and 8.2 nH, respectively, complete the input matching. The amplifier achieves a simulated IIP3 of about -11 dBm.

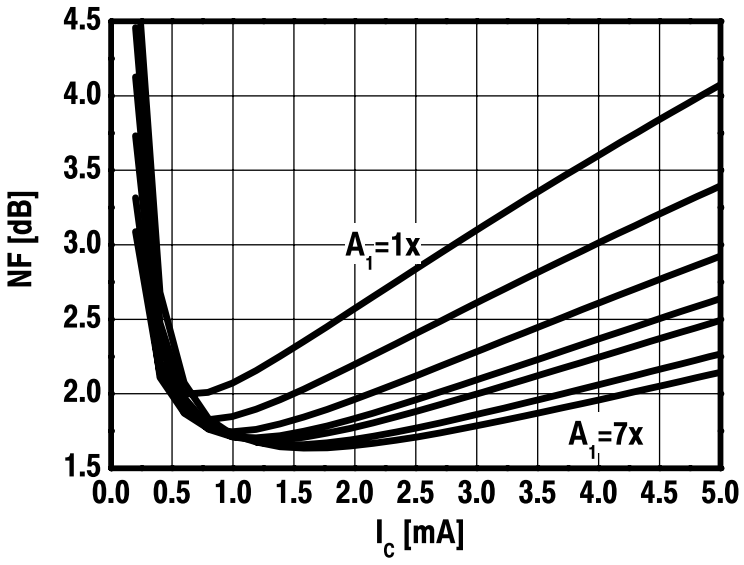

Figure 10: NF of packaged LNA at 1.575 GHz for different input transistor base-emitter areas.

Figure 11 illustrates the simulated NF of the amplifier shown in Fig. 9 at 1.575 GHz as a function of the cascode transistor area (A_2). Here, $A_1 = 4\times$, $L_e = 1.1$ nH, $L_b = 8.2$ nH, and $I_C = 1.1$ mA. It is seen that, in this case, the cascode transistor area has small effect on the LNA NF. In general, however, the noise contribution of the cascode device Q_2 is minimized by minimizing the parasitic capacitance at the emitter of Q_2.

In Fig. 12, the NF of the packaged LNA shown in Fig. 9 is plotted as a function of the input device I_C and with different values of C_p due to the package and ESD structures ($C_p = 0.2, 0.3, ...1.2$ pF). Again, at each point, the input impedance of the amplifier is matched to a differential impedance of 50 Ω by tuning L_e and L_b accordingly. Moreover, in this example, $A_1 = 4\times$ and $A_2 = 1\times$. From Fig. 12 it is seen that as C_p is increased, the LNA NF is improved first due to the fact that the noise contributions due to r_b and $\overline{i_b^2}$ are reduced, as also predicted theoretically. Accordingly, C_p reduces the noise due to the LNA input circuit similarly to a parallel capacitance C_{BE} connected between the base and emitter of the LNA input BJT [55] (see Fig. 8). In this case, the optimum value of C_p is about 0.7-0.8 pF, which results in NF of 1.6 dB. Nevertheless, if C_p is about 0.5-1.2 pF, the minimum LNA NF remains almost constant ($\sim$1.6-1.7 dB). However, the larger value of C_p calls for a higher value of I_C to obtain the minimum NF. Again, this agrees well with theoretical derivations. Since the larger C_p implies a smaller value of k (see Equations (5) and (11)), the larger C_p increases the noise contributions of $\overline{i_c^2}$ and R_L. However, these noise contributions can be reduced to the original levels by scaling up I_C, which results in higher values for both k and ω_T. As a result, the higher value of C_p requires a

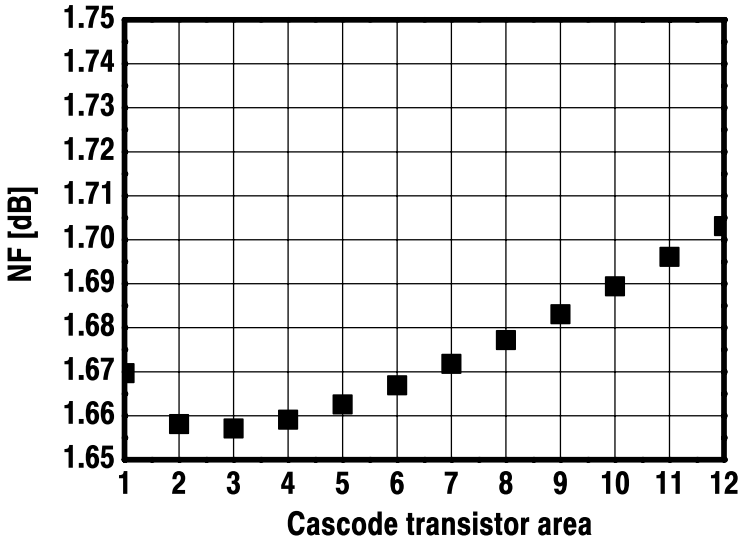

Figure 11: NF of packaged LNA at 1.575 GHz for different cascode transistor base-emitter areas.

higher I_C to obtain the minimum NF. However, if C_p is sufficiently large, in this example larger than 1.2 pF, the LNA input impedance becomes too low to be matched even to a differential impedance of 50 Ω by utilizing only a base inductor. Eventually, a separate impedance matching network is required.

3.4 Packaged inductively degenerated common-source LNA with ESD protection

Figure 13(a) illustrates the schematics of the packaged inductively degenerated common-source LNA with ESD protection. As in bipolar LNA, the bonding pad, ESD diodes, Miller capacitance of M_1, and parasitic capacitance of bondwire introduce a parallel parasitic capacitance at the gate of the LNA input FET M_1 (see node 'g' in Fig. 13). Again, the total parasitic capacitance is modeled as an equivalent parallel package parasitic capacitance C_p at the gate of M_1, as shown in Fig. 13(b) [34], [60], [61], [62], [Paper II], [Paper IV].

As in the previous chapter and in most of the published studies, in which the effects of the package parasitics and ESD structures are considered, the LNA input impedance is assumed to be matched by employing only a series gate or base inductance [60], [63], [Paper II]. However, in the analysis of the package parasitics, this imposes a very restrictive constraint on the value of C_p, which can be tolerated while still being able to match the input impedance only by series base or gate inductance. Namely, if C_p is sufficiently large compared to the gate-source capacitance (C_{gs}) of the LNA input FET, the impedance level

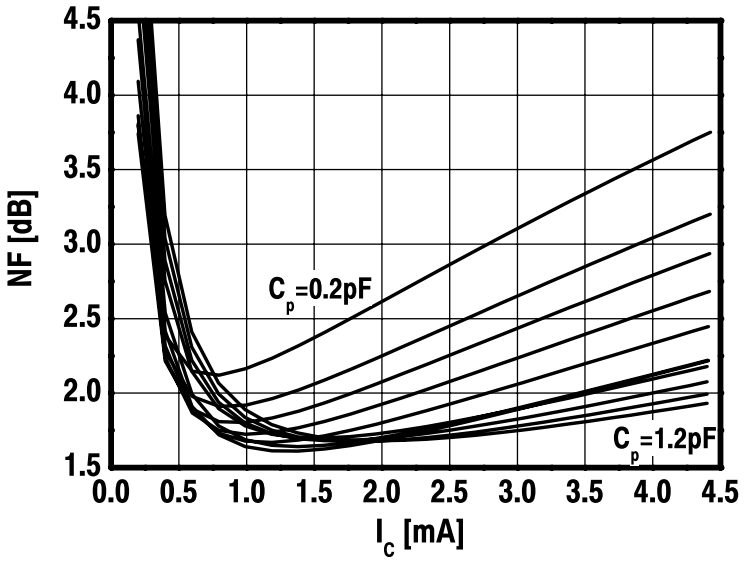

Figure 12: NF of packaged LNA at 1.575 GHz for different values of parallel parasitic capacitance.

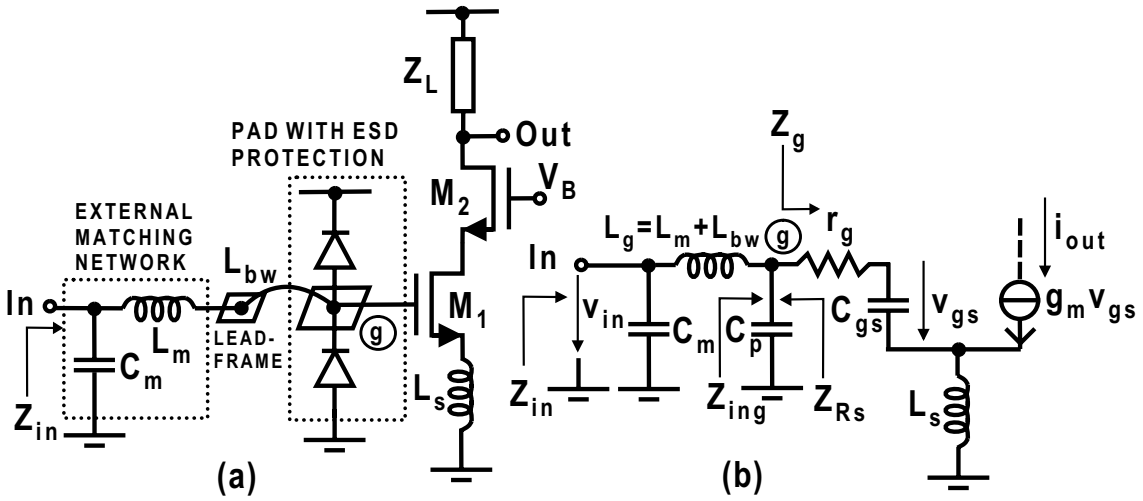

Figure 13: (a) Single-ended equivalent circuit of packaged inductively degenerated common-source LNA with ESD protection and (b) its input stage small-signal model.

at the amplifier input becomes too low to be matched to 50 Ω only by employing a series inductance [60], [63], [Paper II]. For this reason, and as proposed in the previous chapter, some of the designs using only a series base or gate inductance have selected an LNA input impedance level lower than 50 Ω (i.e. 25 Ω single-ended) [Paper II] or have simply accepted a non-perfect impedance match at the amplifier input [61]. However, in mass product applications, the last approach is not practical, since the LNA must also meet its input impedance matching requirements in the presence of process and temperature variations. If the nominal S_{11} is designed to be only about -10 dB, the amplifier will most probably fail to meet its matching specifications in the process corners. For this reason, the equations given throughout this thesis assume a perfect power match at the amplifier input. Moreover, in the following, an LNA input matching network consisting of two lumped elements L_m (or L_g) and C_m (see Fig. 13) is considered instead of single gate series inductance. This type of matching network allows more freedom for the value of C_p, since, by employing a two-component matching network, the impedance level at the amplifier input can be more easily restored or matched to 50 Ω. Since the losses of the input matching network are crucial for the LNA noise factor, these components are often realized with off-chip lumped elements, as shown in Fig. 13.

As in the bipolar LNA, C_p transforms downwards the real part of the CMOS LNA input impedance. The real part of the impedance Z_{ing} looking into the LNA on-chip input (see Fig. 13) at the operation frequency can be approximated by [Paper IV]

$$Re(Z_{ing}) = R_{ing} = \left(\frac{C_{gs}}{C_p + C_{gs}}\right)^2 \cdot R_{eq} \tag{13}$$

where

$$R_{eq} = \frac{g_m L_s}{C_{gs}} + r_g \approx \omega_T L_s \tag{14}$$

represents the real part of the LNA input impedance, which is achieved in the absence of parasitics [32] (i.e. $C_p = 0$). Moreover, in that particular case, the input matching network comprises only a series inductance L_g. Here, L_s is the source inductance, C_{gs} is the gate-source capacitance, g_m is the transconductance, r_g is the gate resistance, and $\omega_T \approx g_m/C_{gs}$ is the unity-current gain angular frequency of M_1, respectively. Thus, due to the parasitic capacitance at the transistor gate, the input impedance comes down by a factor of $(C_{gs}/(C_p + C_{gs}))^2 \leq 1$ compared to the unpackaged amplifier with given ω_T and a certain size of L_s. Moreover, if C_p is very large compared to C_{gs}, R_{ing} becomes low compared to R_s and the LNA input impedance matching becomes sensitive to parasitics and process variations.

The unity-current gain angular frequency of FET can be approximated as [32]

$$\omega_T \approx \frac{g_m}{C_{gs}} = \frac{3}{2}\frac{\alpha \mu V_{eff}}{L^2} \tag{15}$$

where $\alpha = g_m/g_{d0}$, g_{d0} is the zero bias drain conductance, μ is the electron mobility, and $V_{eff} = V_{GS} - V_T$ is the gate-source overdrive voltage of FET. From Eq. (15) it is

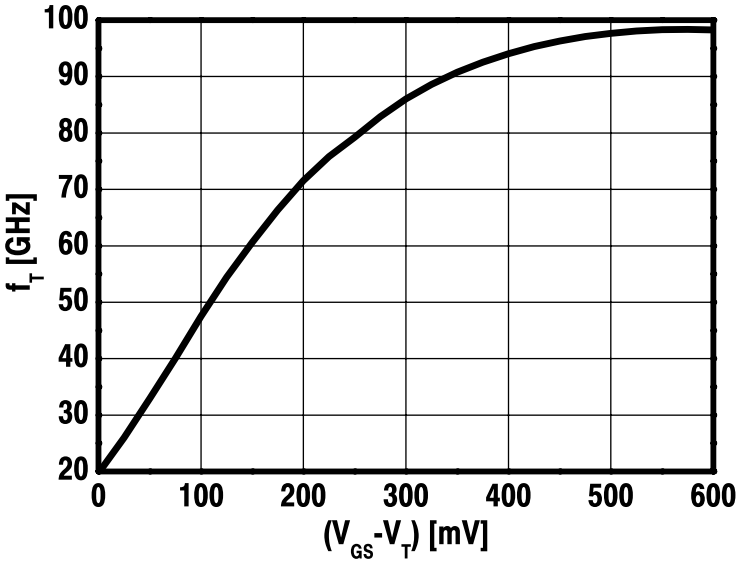

Figure 14: Simulated unity-current gain frequency of $(W/L) = (60/.13)$ FET in 0.13-μm CMOS technology.

concluded that the designer can control the f_T mainly via V_{GS} and channel length (L). Figure 14 illustrates the simulated f_T of FET sized as $(W/L) = (60/.13)$ as a function of V_{eff} in a 0.13-μm CMOS technology. It is seen that, for the typical overdrive voltages of 100-200 mV, f_Ts in the order of 50-70 GHz are available in the 0.13-μm technology utilized in this thesis. Moreover, since the practical values of L_s are typically in the order of 1-3 nH, assuming that a 15-25 dB LNA voltage gain is to be implemented (at 2 GHz), the resulting values for R_{eq} are in the order of hundreds of ohms (i.e. 300-1300 Ω).

The effect of C_p on R_{ing} is illustrated graphically in Fig. 15. The component values used are $f_T = 65$ GHz, $L_s = 1.5$ nH, and $C_{gs} = 100$ fF giving $R_{eq} = 612\ \Omega$. The values represent rather typical values for LNA designed in the 0.13-μm CMOS technology for PCS 1900 applications [Paper IV], [Paper VI]. Moreover, in the 0.13-μm CMOS technology utilized in this work, the total parasitic parallel capacitance including the capacitance due to the QFN package parasitics, ESD protection diodes, and bonding pad structure is about 500 fF [Paper II]. (This is almost the same value as $C_p = 600$ fF in the 0.35-μm BiCMOS technology with a QFN package in the previous chapter. Accordingly, the ESD and package parasitics do not significantly scale down with IC process technology.) With given component values, the resulting R_{ing} is only about 17 Ω. Evidently, if the LNA input impedance is to be matched to $50\ \Omega$, a matching network is needed to transform the input impedance of the amplifier upwards.

By applying a series of parallel-series conversions it can be shown that, at the operation frequency f_0, the input impedance of the LNA shown in Fig. 13 is given by [Paper

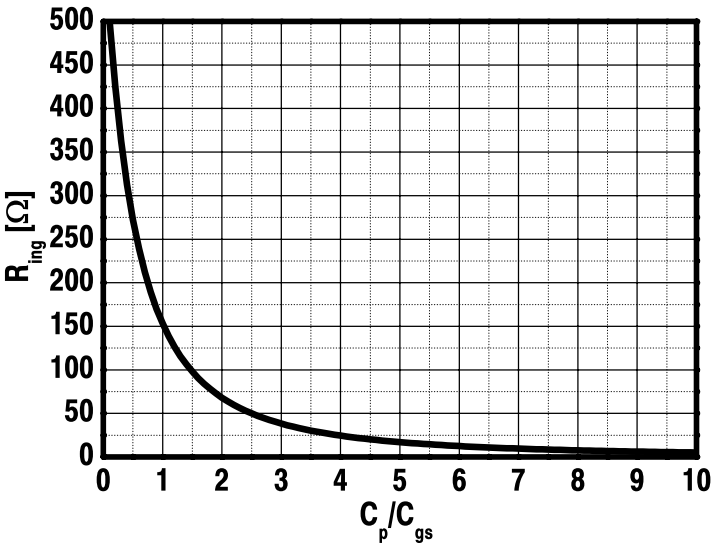

Figure 15: Effect of package parasitic capacitance C_p on the real part of impedance Z_{ing} looking into LNA on-chip input.

IV]

$$Z_{in}(\omega_0) = R_{in} = \frac{1}{(\omega_0 C_m)^2}\left(\frac{C_p + C_{gs}}{C_{gs}}\right)^2 \cdot \frac{1}{R_{eq}} \tag{16}$$

In conclusion, the value of C_m must be selected so that $R_{in} = R_s$, where R_s is the source resistance (i.e. 50 Ω). Correspondingly, the value of L_g must be selected to tune the input impedance to the desired frequency or [Paper IV]

$$L_g = \frac{C_p + C_{gs} + C_m}{C_m(C_p + C_{gs})\omega_0^2} \tag{17}$$

Provided that at the frequency of operation the LNA input impedance matching requirement $R_{in} = R_s$ is met, the input stage transconductance G_m of the packaged amplifier shown in Fig. 13 is given by [Paper IV]

$$G_m = \left|\frac{i_{out}}{v_{in}}\right| = \sqrt{\frac{R_{eq}}{R_s}} \cdot \frac{1}{\omega_0 L_s} \tag{18}$$

It is seen that G_m is independent of the actual input device g_m, which is also the case in the unpackaged amplifier [32]. In addition, provided that, a lossless input matching is considered, G_m does not depend on the value of C_p. Nevertheless, usually this is a reasonable assumption provided that an off-chip matching network with high-Q components is employed, as shown in Fig. 13. Moreover, in an amplifier with a two-component matching network shown in Fig. 13, the value of L_s, and thus R_{eq}, can be in principle selected independently of the value of C_p, since the real part of the LNA input impedance

can be tuned to the desired value by selecting the value of the matching capacitance (C_m) accordingly, as shown by Eq. (16). On the contrary, if only a gate inductance is used for the impedance matching, L_s, and thus R_{eq}, must be selected to ensure that $Re(Z_{in}) = R_s$. Then, G_m does depend on the value of C_p (see Eq. (7)).

If the finite insertion loss of the input matching network is taken into account, it can be shown that the G_m of the LNA shown in Fig. 13 depends weakly on C_p. Assume for this purpose that the losses of the input matching network are lumped on the equivalent series resistance (R_{lg}) of L_g. Then, it can be shown that, if $\omega_0 C_{gs}^2 R_{eq} \ll (C_p + C_{gs})$ (which can be easily verified with practical component values at 2 GHz), G_m can be approximated as

$$G_m = \sqrt{\frac{R_{eq}}{R_s}} \cdot \frac{1}{\omega_0 L_s} \cdot \frac{1}{\sqrt{1 + \frac{1}{R_s R_{eq}} \left(\frac{C_{gs} R_{eq}}{(C_p + C_{gs})} + \frac{(C_p + C_{gs}) R_{lg}}{C_{gs}} \right)^2}} \tag{19}$$

It is seen that, if the value of C_p is increased, G_m is decreased.

The voltage gain of the packaged LNA with ESD protection at f_0 is given as

$$A_v = \sqrt{\frac{R_{eq}}{R_s}} \frac{|Z_L(j\omega_0)|}{\omega_0 L_s} \frac{1}{\sqrt{1 + \frac{1}{R_s R_{eq}} \left(\frac{C_{gs} R_{eq}}{(C_p + C_{gs})} + \frac{(C_p + C_{gs}) R_{lg}}{C_{gs}} \right)^2}} \approx \sqrt{\frac{R_{eq}}{R_s}} \frac{|Z_L(j\omega_0)|}{\omega_0 L_s} \tag{20}$$

where $Z_L(j\omega_0)$ is the impedance at the drain of M_2 (see Fig. 13(a)).

As in the case of the bipolar LNA, the calculation of the noise factor of the packaged CMOS LNA with ESD protection can be significantly simplified if the impedance Z_{R_s} (see Fig. 13) looking into the generator is first transformed into the equivalent series impedance at the operation frequency f_0. Again, the complex conjugate impedance matching requires that $Z_{R_s} = Z_g^*$ where Z_g is the impedance looking into the gate of M_1. Thus

$$Z_{R_s} = Z_g^* \approx \left(\omega_T L_s + \frac{1}{j\omega_0 C_{gs}} + j\omega_0 L_s \right)^* \approx \omega_T L_s + \frac{j}{\omega_0 C_{gs}} \tag{21}$$

Moreover, assuming perfect power matching $R_{in} = R_s$, it can be shown that the noise factor of the packaged LNA at f_0 is given by [Paper IV]

$$\begin{aligned} F_{LNA} &= 1 + \left(\frac{C_p + C_{gs}}{C_{gs}} \right)^2 \left(\frac{R_{cm}}{R_{eq}} + \frac{R_{lg}}{R_{eq}} \right) + \frac{r_g}{R_{eq}} + \frac{\gamma}{\alpha} g_m R_{eq} \left(\frac{\omega_0}{\omega_T} \right)^2 \Upsilon \\ &\quad + \eta^2 g_m^2 R_{sub} R_{eq} \left(\frac{\omega_0}{\omega_T} \right)^2 + \frac{\alpha\delta}{5 g_m R_{eq}} + \frac{4 R_{eq}}{R_L} \left(\frac{\omega_0}{\omega_T} \right)^2 \end{aligned} \tag{22}$$

where γ is the channel current noise factor, η is a bias dependent constant [64], R_{sub} is the substrate resistance of M_1, and δ is the gate induced current noise factor [32]. The coefficient Υ is given by

$$\Upsilon = 1 + 2c \sqrt{\frac{\delta}{5\gamma}} \alpha + \frac{\delta \alpha^2}{5\gamma} \tag{23}$$

where c is the correlation coefficient between the gate and drain noise [32]. In Eq. (22), the first, second, and third terms are the thermal noise produced by the series resistances R_{lg} and R_{cm} of the input matching components L_g and C_m, respectively, and r_g, respectively. The fourth term is due to the channel thermal noise $\overline{i_d^2} = 4kT\gamma g_m \Delta f$, gate-induced current noise $\overline{i_g^2} = (4kT\delta\omega_0^2 C_{gs}^2 \Delta f)/(5g_{d0})$, and correlation between the gate and drain noise. The fifth and seventh terms are the thermal noise in R_{sub} and in equivalent load resistor (R_L). Finally, the sixth term is again due to $\overline{i_g^2}$. Eq. (22) neglects the noise contribution of the cascode transistor M_2 to the LNA noise factor. However, in the following, the noise contribution of M_2 is considered separately.

Again, if Eq. (22) is compared to the equation describing the noise factor of the unpackaged LNA [32], it can be seen that, excluding the noise due to the input matching network components R_{lg} and R_{cm}, the equation for the noise factor of the packaged amplifier is obtained from the unpackaged case by replacing R_s with R_{eq}. As in the BJT LNA, this is intuitively reasonable, since in the packaged amplifier, R_{eq} represents the real part of the impedance Z_{R_s} looking into the generator at impedance match.

To verify Eq. (22) by means of circuit simulation, Figure 16 plots the simulated NF of the packaged LNA in 0.13-μm CMOS with ESD protection at 2 GHz as a function of input FET width W together with theoretical values calculated by using Eq. (22). In this simulation, the input FET employs the channel length of 0.13 μm, the FET is biased at $V_{eff} = 200$ mV, and the estimated total parasitic capacitance C_p due to the ESD and package parasitics is about 500 fF. Corresponding to each value of W, the LNA input impedance in the simulation is matched to a 50 Ω by tuning L_m and C_m accordingly. The other component values used are $R_{cm} = 1\ \Omega$, $R_{lg} = 1.5\ \Omega$, $L_s = 1.6$ nH, and $R_L = 200\ \Omega$. In addition, parameters γ and δ for a 0.13-μm NMOSFET are estimated from [33] as $\gamma = 1.1$ and $\delta = 4.0$, respectively. From Fig. 16 it is concluded that the simulated noise figures fit well with the theoretical ones. At largest, the deviation between the simulated and calculated noise figures is about 0.3 dB.

In the unpackaged LNA (i.e. $C_p = 0$), the real part of the LNA input impedance is designed so that $R_{in} = \omega_T L_s = R_s = 50\ \Omega$. On the other hand, in a packaged amplifier where C_p is present, R_{eq} is, in practice, designed to be much larger than $50\ \Omega$. Thus, from Eq. (22) it is concluded that, for instance, for given ω_T, packaging affects the LNA noise factor by increasing the noise contributions of the terms proportional to R_{eq}, whereas it decreases the noise contributions of terms inversely proportional to R_{eq}. Fortunately, very high values of ω_T available in sub-micron CMOS processes (i.e. 0.13-μm CMOS technology utilized in this thesis) suppress the noise contributions proportional to R_{eq} significantly, since these terms are also inversely proportional to ω_T. The noise factor of the packaged LNA depends directly on C_p only via losses of the input matching network (i.e. R_{lg} and R_{cm}). Thus, in practice, in a packaged amplifier the terms proportional to R_{eq} together with the losses of the input matching network usually dominate the LNA noise factor over the rest of the terms inversely proportional to R_{eq}.

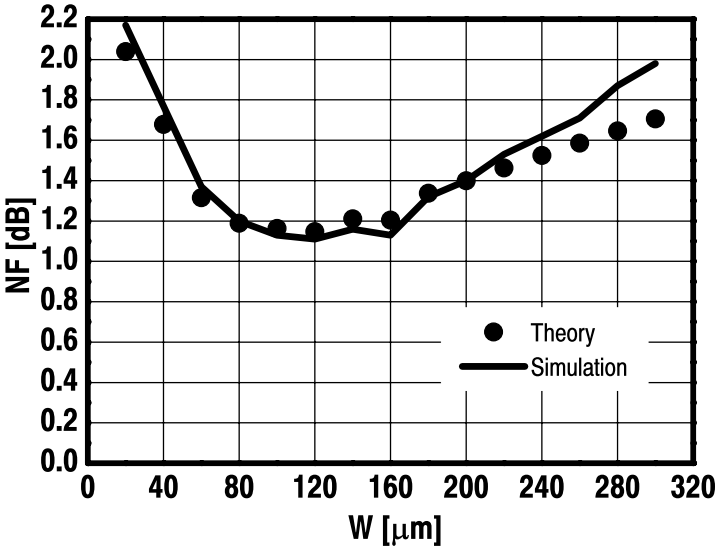

Figure 16: Theoretical (dots) and simulated (solid line) NF at 2 GHz versus input FET width, for the packaged inductively degenerated common-source LNA.

The IIP3 of the LNA shown in Fig. 13 can be approximated as [36]

$$v_{IIP3,LNA} \approx \frac{v_{IIP3,FET}}{|v_{gs}/v_{in}|} = \sqrt{\frac{R_s}{R_{eq}}}(g_m\omega_0 L_s)v_{IIP3,FET} \tag{24}$$

where $v_{IIP3,FET} \approx 2\sqrt{2V_{eff}/(3\theta)}$ is the IIP3 of the LNA input FET M_1 [Paper V], θ captures how the inversion layer mobility degrades with the gate electric field [2], and the passive matching network amplifies the input voltage across M_1 by $|v_{gs}/v_{in}| = \sqrt{R_{eq}/R_s}/(g_m\omega_0 L_s)$.

In the following, the noise optimization of the packaged FET LNA is considered. Again, since the downconversion mixer usually dominates the RF front-end linearity, the linearity optimization of the LNA is not considered here. Nevertheless, from Eq. (24) it is seen that the IIP3 of the FET LNA can be scaled up by reducing the voltage gain in the matching network by biasing the FET at larger V_{eff}, scaling up L_s, and by scaling the FET width up. Scaling up the FET channel length also improves the IIP3 of the amplifier by improving the intrinsic FET linearity, since θ is inversely proportional to the channel length.

In modern minimum-sized CMOS devices, the shallow trench isolation (STI) substrate resistance easily dominates over the active area substrate resistance [65] and the substrate resistance is inversely proportional to the device width (W). On the other hand, the input device g_m is proportional to W. Thus, from Eq. (22) it is seen that, since the terms

$(1 + C_p/C_{gs})^2 (R_{cm} + R_{lg}) / R_{eq}$ and $(\alpha\delta)/(5g_m R_{eq})$ decrease by increasing W, while the other terms excluding the noise due to R_L increase by increasing W, an optimum input device width W_{opt}, which minimizes the LNA noise factor, exists, at least in theory. However, the noise due to r_g can also be minimized by interdigitating the device [32]. If each gate finger is contacted at both ends, r_g can be approximated as $r_g = (WR_{sh})/(12Ln_f^2)$, where n_f is the number of gate fingers and R_{sh} is the sheet resistance of the gate material [32].

The minimum noise factor of the packaged CMOS LNA with ESD protection can be found, for instance, as follows. First, the minimum, or at least sufficiently low, channel length provided by the given technology is selected to provide high enough ω_T given by Eq. (15) and to minimize the noise factor given by Eq. (22). Then, the overdrive voltage V_{eff} of the LNA input FET M_1 and the value of L_s are set to some arbitrary values. As V_{eff} and L_s are fixed, R_{eq} is also fixed (see Eq. (14)). In the next step, the width W of M_1 is swept until an optimum noise factor is found. Corresponding to each value of W, the input matching network must be tuned accordingly to ensure that the LNA input impedance is matched. Finally, in this phase of the circuit design, it is reasonable to assume in the simulations that the cascode FET M_2 has the same device width (W_2) as M_1.

Figure 18 plots the simulated NF $(10\log(F_{LNA}))$ of the packaged differential LNA with ESD protection shown in Fig. 17, realized in the 0.13-μm CMOS technology with a supply voltage of 1.2 V, at 2 GHz with three different values of $V_{eff} = 50, 150, 250$ mV and as a function of the input FET width (W_1). Here $L = 0.13$ μm, $L_s = 1.5$ nH, $W_2 = W_1$, and at each point the LNA input impedance is matched to a differential impedance of 100 Ω. Moreover, in this example, $C_p = 500$ fF. The LNA load impedance, tuned to 2 GHz, is designed to obtain approximately 21 dB peek voltage gain.

From Fig. 18, it is seen that the increase of V_{eff} from 50 mV to 150 mV improves the minimum NF by about 0.2 dB, whereas the increase of V_{eff} from 150 mV to 250 mV does not result in NF improvement. Thus, a reasonable choice is $V_{eff} = 150$ mV. From Fig. 18, it is also concluded that a W_1 of 90-150 μm results in the minimum NF corresponding to $V_{eff} = 150$ mV. However, since the values of 90-150 μm with $V_{eff} = 150$ mV correspond to a relatively high LNA current consumption of 10-14 mA, a slightly lower value of $W_1 = 60$ μm can be selected instead. This worsens the NF by only 0.2 dB and corresponds to the LNA current consumption of 7 mA. In order to minimize the noise contributions of r_g and R_{sub}, respectively, the LNA input FET utilizes 10 gate fingers and each finger is contacted at both ends. The input matching network consisting of $L_g = 7.5$ nH and $C_{md} = 1.5$ pF completes the input matching (see Fig. 17). The amplifier achieves an IIP3 of about -5 dBm.

The noise contribution of the LNA cascode FET M_2, considering only channel thermal noise, to the LNA output noise current can be approximated as [Paper V]

$$\overline{i_{n,M_2}^2} = \frac{\overline{i_{d,M_2}^2}}{1 + \left(\frac{g_{m2}}{\omega_0 C_{ps}}\right)^2} \approx \left(\frac{\omega_0 C_{ps}}{g_{m2}}\right)^2 4k_B T \frac{\gamma}{\alpha} g_{m2} \Delta f \tag{25}$$

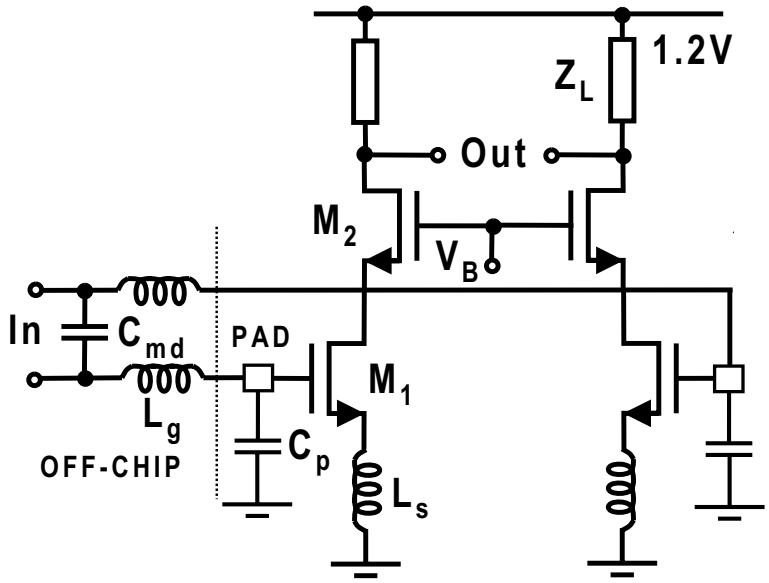

Figure 17: Packaged 2-GHz inductively degenerated common-source LNA with ESD protection in 0.13-μm CMOS.

where g_{m2} is the transconductance of M_2 and C_{ps} is the parasitic capacitance between the drain of M_1 and ground, respectively. Thus, the noise contribution of M_2 is minimized by minimizing the ratio $(\omega_0 C_{ps})/g_{m2}$ [66]. To minimize C_{ps}, it is wise to employ the minimum channel length for M_2. Moreover, since, in practice, the LNA bias current and thus also the drain-source current of M_2 is determined by the optimization of the LNA input FET M_1, the ratio $(\omega_0 C_{ps})/g_{m2}$ can be minimized by selecting the width W_2 of M_2 accordingly. Often, the LNA noise factor is close to the minimum, when M_1 and M_2 have the same size. Figure 19 illustrates the simulated NF of the LNA shown in Fig. 17 at 2 GHz as a function of W_2. Here $W_1 = 60$ μm, $L_s = 1.5$ nH, and $V_{eff} = 150$ mV. It is seen that for W_2 larger than about 30 μm, NF stays relatively constant. Thus, it is reasonable to select, for instance, $W_2 = W_1 = 60$ μm.

In the following, the effect of the equivalent parallel package parasitic capacitance C_p on the NF and voltage gain of the LNA shown in Fig. 17 is considered. It is assumed that the losses of the input matching network are lumped on the equivalent series resistance R_{lg} of the series matching inductor L_g (i.e. $R_{cm} = 0\ \Omega$). It is assumed that $R_{lg} = 1.3\ \Omega$. For $L_g = 7.5$ nH, this corresponds to about Q of 72 at 2 GHz, which represents a rather typical value for Q of external lumped inductors. Moreover, in the following example, $W_2 = W_1 = 60$ μm, $L_s = 1.5$ nH, and $V_{eff} = 150$ mV.

Figure 20 illustrates the simulated NF of the packaged LNA, shown in Fig. 17, at 2 GHz, as a function of the value of C_p in two cases. In the first case, an ideal input matching network with no insertion loss is assumed (i.e. the noise due to R_{lg} is set to zero in the simulator), while in the second case, the finite insertion loss is considered (i.e. the noise due to R_{lg} is considered). Again at each point, the input matching network is tuned ac-

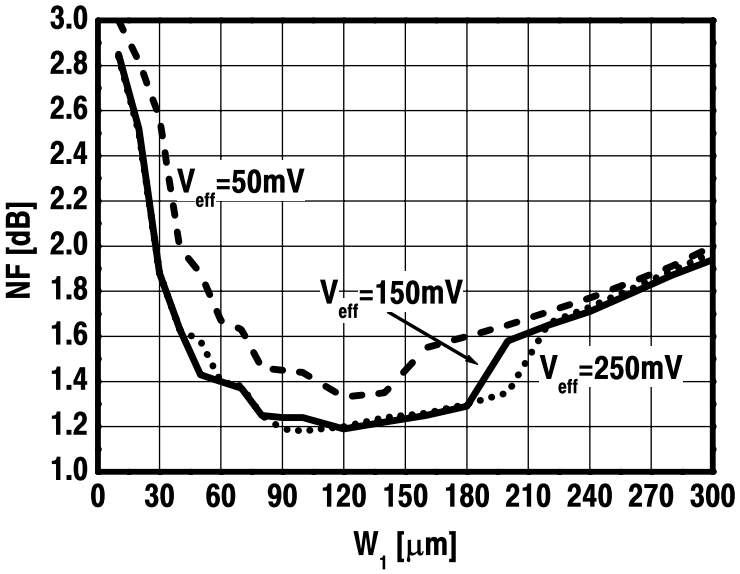

Figure 18: Simulated LNA NF at 2 GHz as a function of input FET width with three different values of V_{eff}.

cordingly to match the input impedance at 2 GHz. It is seen that, in the absence of C_p, very low LNA noise figures in the order of 0.5 dB are available. This can be attributed to the very high values of ω_T available in the employed 0.13-μm CMOS technology. From Fig. 14, it is seen that a FET with a minimum channel length of 0.13 μm and biased at $V_{eff} = 150$ mV achieves almost 60 GHz of f_T. Unfortunately, as seen from Fig. 20, as C_p increases, NF increases almost linearly on the dB-scale and finally the noise due to the insertion loss of the input matching network (i.e. R_{lg}) starts to dominate the NF. It is also noticed that the value of C_p has insignificant effect on the other LNA noise contributions, since the NF with an ideal matching network remains almost constant despite the increase of C_p. Recall that both of these conclusions can also be drawn from Eq. (22). From Eq. (22) it is seen that, as C_p increases, the noise due to the insertion loss of input matching network increases proportionally to $(1 + C_p/C_{gs})^2 R_{lg}/R_{eq}$ while the other contributions do not depend on C_p. As a conclusion, the LNA NF can be lowered by reducing C_p. This can be achieved partly by selecting the packet pins of the amplifier accordingly. Nevertheless, the lower limit for C_p is set by the ESD requirements and capacitance due to the bonding pad. The noise contribution of R_{lg} can also be lowered by scaling up the input device width W and length L with a constant ratio of W/L, since this scales up the input FET C_{gs}. However, larger L results in lower ω_T, which in turn increases the LNA NF. Finally, the noise due to R_{lg} can be reduced by biasing the input FET at larger V_{eff}, which results in higher ω_T, and thus R_{eq}, but this increases the power consumption of the circuit.

The effect of C_p on the voltage gain of the packaged LNA, shown in Fig. 17, at 2 GHz is

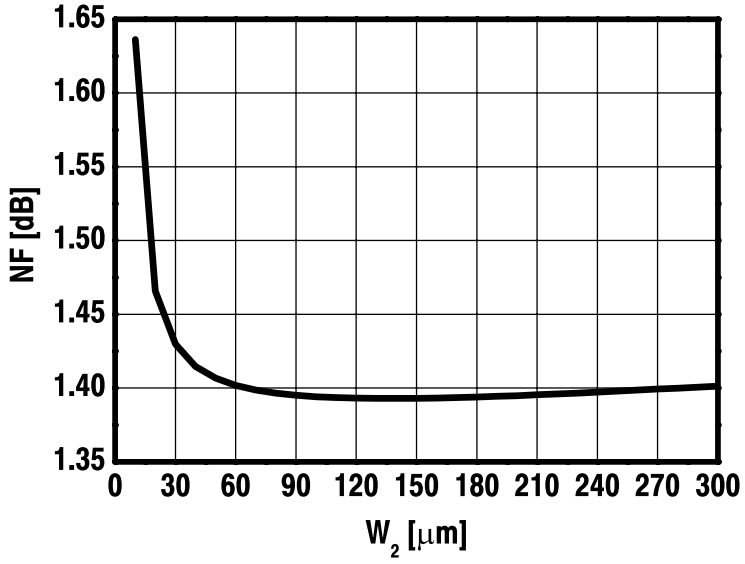

Figure 19: Simulated LNA NF at 2 GHz as a function of cascode FET width.

depicted in Figure 21. Again, two cases are illustrated. First, the voltage gain is plotted assuming an ideal input matching network with no loss (i.e. $R_{lg} = 0\ \Omega$). Next, the effect of the finite insertion loss (i.e. $R_{lg} = 1.3\ \Omega$) is considered. It is seen that, if R_{lg} is very small ($R_{lg} \approx 0\ \Omega$), the voltage gain stays almost constant despite the increase of C_p. Again, this agrees well with the theoretical derivations. Recall that, according to Eq. (18), the input stage transconductance and thus the voltage gain of the amplifier, do not depend on C_p provided that $R_{lg} \approx 0\ \Omega$. In practice, the finite R_{lg} results in a slight reduction of G_m, and thus voltage gain, as a function of the C_p increment, as predicted by Equations (19) and (20).

Based on the analysis and discussion presented above, it is concluded that in the presence of an equivalent parallel package parasitic capacitance C_p, noise factor in well-optimized sub-micron packaged CMOS LNA is easily dominated by the losses of the input matching network, instead of active device noise. In practical applications with ESD protection, the achievable noise factor of the packaged LNA is therefore well above the theoretical minimum noise factor of the active device.

3.5 LC-tuned load of LNA

In practice, the radio receiver must meet its dynamic range specifications in nominal conditions and also in the presence of temperature and process variations. In general, the dynamic range of the radio receiver is at the lower end limited by the noise floor and at the upper end by the receiver nonlinearity. Moreover, in order to reduce the variations of the receiver dynamic range due to the temperature and process variations, it is important

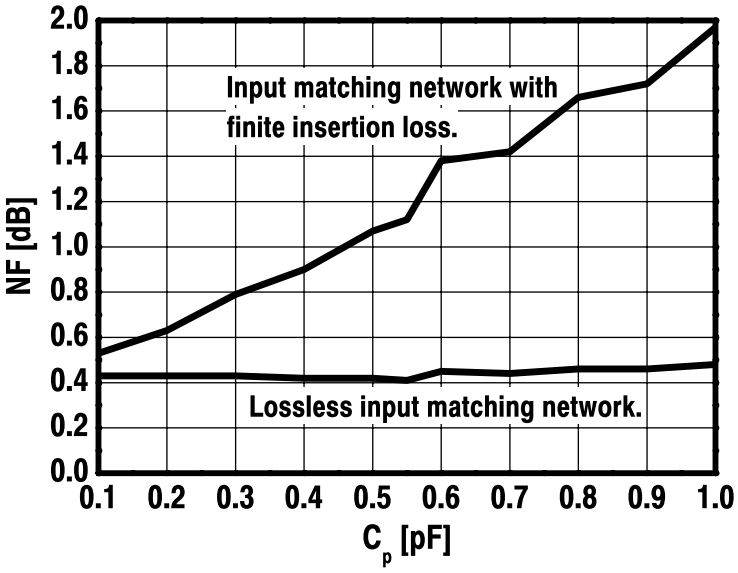

Figure 20: Simulated NF of packaged LNA at 2 GHz as a function of equivalent parallel package parasitic capacitance. Two cases are shown: Input matching network 1) with no insertion loss ($R_{lg} = 0$) and 2) with finite insertion loss ($R_{lg} = 1.3\ \Omega$).

to stabilize the gain of the LNA. To understand this, consider the case in which the gain of the unstabilized LNA is for some reason smaller than in the nominal condition. Then, according to Eq. (1), the noise contributions of the downstream circuits such as mixer and analog baseband are suppressed less than in the nominal condition and the entire receiver may fail to meet its sensitivity requirements. On the other hand, if the LNA gain is too large in some process corner, IIP3 given by Eq. (2) is degraded and the receiver may fail to meet its intermodulation specifications. Therefore, in order to maximize the yield of the receiver IC, it is very important to regulate the LNA gain.

In order to stabilize the input impedance Z_{in} (see Equations (3) and (16)) and the input stage transconductance G_m (see Equations (7) and (18)) of the inductively degenerated common-emitter or common-source LNA against process and temperature variations, the LNA has to be biased with a PTAT or constant-g_m biasing technique [37], [39], respectively. Usually, this stabilizes $\omega_T \approx g_m/C_\pi$ of the input BJT or $\omega_T \approx g_m/C_{gs}$ of the input FET, and thus Z_{in} and G_m adequately against variations, since the other terms in Equations (3), (16) and (7), (18) vary less with process than g_m and thus ω_T. Moreover, in that particular case, the LNA voltage gain, given by Equations (8) and (20), varies mainly along the magnitude of the LNA load impedance $|Z_L(\omega_0)|$ at the given frequency f_0. As a conclusion, in order to stabilize the voltage gain of the amplifier at the operation frequency, $|Z_L(\omega_0)|$ of the inductively degenerated LNA must be regulated against variations.

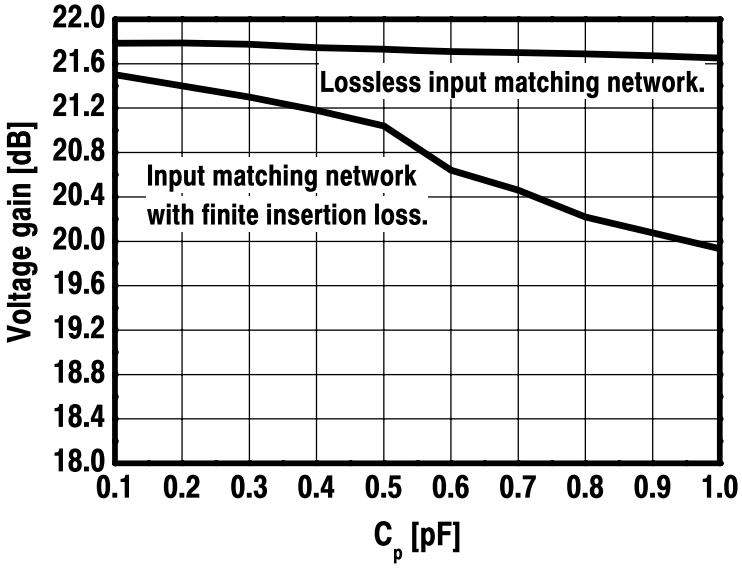

Figure 21: Simulated LNA voltage gain at 2 GHz as a function of equivalent parallel package parasitic capacitance. Two cases are shown: Input matching network 1) with no insertion loss ($R_{lg} = 0$) and 2) with finite insertion loss ($R_{lg} = 1.3\ \Omega$).

Most of the LNAs use an LC-tuned load to peek the gain of the amplifier at the frequency of interest and to reject the out-of-band interfering signals. A typical parallel LC circuit used in narrow-band tuned amplifiers is shown in Fig. 22(a) [3], [Paper I], [Paper II], [Paper VI]. Here C includes also the input capacitances of the I and Q mixers and any other parasitic capacitance presented at the LNA output. The shunt resistor (R_p) lowers the Q factor of the LC circuit and widens the resonator bandwidth. As a result, the magnitude of the amplifier load impedance varies much less at the operation frequency with the deviation of C. At the operation frequency f_0, L and C are in parallel resonance $f_0 = 1/(2\pi\sqrt{LC})$ and Z_L is purely real $|Z_L(\omega_0)| = R_L \approx (Q_{ind}\omega_0 L)||r_{oc}||R_p \approx R_p$. Here, R_{ls} is the series resistance of the load inductor L, $Q_{ind} = (\omega_0 L)/R_{ls}$ is the Q factor of L, and r_{oc} is the output impedance of the cascode amplifier. Unfortunately, as the LNA load impedance at the resonance frequency is mainly determined by R_p, $|Z_L(\omega_0)|$ and also the LNA voltage gain will deviate similarly as R_p. For instance, with the tolerance of $\pm 20\%$ of integrated polysilicon resistors, the gain variation due to R_p variation only is almost $20\log 1.2 - 20\log 0.8$ =3.5 dB.

A simple technique for regulating the magnitude of an LC-tuned LNA load impedance at the operation frequency against deviations of both the integrated capacitors and resistors is illustrated in Fig. 22(b) [Paper III], [67]. In this circuit, two resistors, R_{ser} and R_{par}, realized with the *same* resistance material, are employed to reduce the resonator Q.

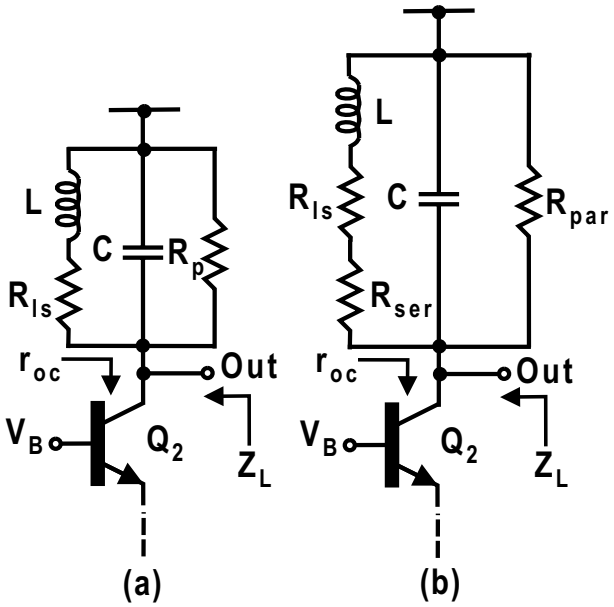

Figure 22: LC-tuned circuits for LNA load. (a) Conventional and (b) proposed damped parallel LC-resonator.

Assume that R_{ser} and R_{par} are expressed as $R_{ser} = n_s R_{sh}$ and $R_{par} = n_p R_{sh}$, respectively, where R_{sh} is the sheet or unit resistance of the resistance material (i.e. polysilicon). Since both R_{ser} and R_{par} are realized with the same material and these resistors are placed close to each other on silicon, their process gradient is very similar. To understand how the proposed circuit operates, consider the case in which the value of R_{sh} is for some reason smaller than its nominal value. Now, due to the decreased R_{sh}, the Q of the inductor L is increased because the value of the resistance R_{ser} in series with it is decreased. For the same reason, the Q of the whole resonator is increased. However, as the value of the parallel resistor R_{par} is decreased, the Q of the whole resonator is decreased. As a result, the increase in the Q factor of L is compensated and the Q of the entire resonator is left relatively unchanged.

It can be shown that if the values of resistors R_{ser} and R_{par}, or parameters n_s and n_p, are related as [Paper III]

$$n_p n_s = \frac{(\omega_0 L)^2}{R_{sh0}^2} \tag{26}$$

a given deviation (i.e. $\pm 20\%$) of R_{sh} has minimum effect on the magnitude of the LNA load impedance $|Z_L(\omega_0)| = R_L$ at the resonance frequency f_0. Thus, R_{ser} and R_{par}, or n_s and n_p, respectively, must be selected so that they realize the desired LNA voltage gain (see Eq. (8)) and therefore the required $|Z_L(\omega_0)| = R_L$, and such that they obey Eq. (26). Accordingly, it can be shown that, in that particular case, n_p and n_s must be chosen as [Paper III]

$$n_p = \frac{R_{par}}{R_{sh}} = \frac{2R_L}{R_{sh0}} \frac{Q_{ind}\omega_0 L}{(Q_{ind}\omega_0 L - R_L)} \tag{27}$$

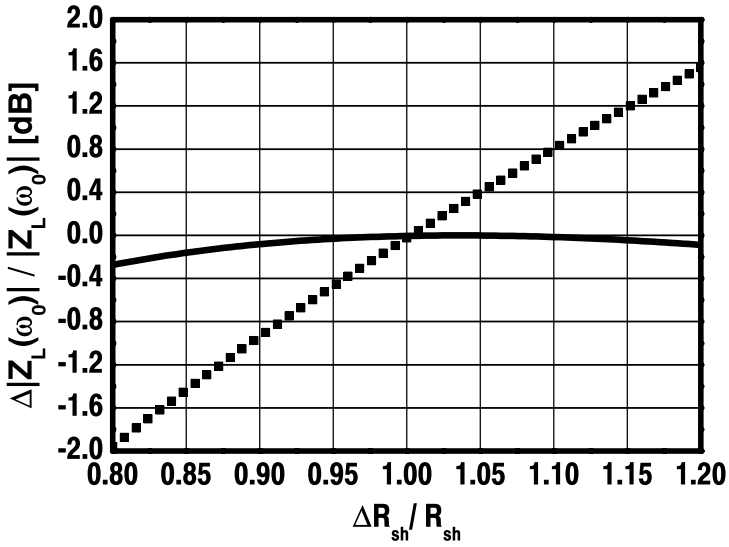

Figure 23: Effect of sheet resistance variation on the magnitude of conventional (scattered line) and proposed (solid line) LC-tuned LNA load impedance at the resonance frequency.

$$n_s = \frac{R_{ser}}{R_{sh}} = \frac{\omega_0 L}{2R_{sh0}Q_{ind}}\left(\frac{Q_{ind}\omega_0 L}{R_L} - 1\right) \tag{28}$$

In order to result realizable values for n_s and n_p, the inductor Q must satisfy the following equation

$$Q_{ind} > \frac{R_L}{\omega_0 L} \tag{29}$$

The effect of the R_{sh} deviation on the magnitude of both the conventional (see Fig. 22(a)) and proposed LC-circuit impedance (see Fig. 22(b)) at the resonance frequency is illustrated graphically in Fig. 23. It is seen that the proposed technique reduces the LNA load impedance and therefore the voltage gain variations several dBs compared to the conventional techniques.

3.6 Variable gain in LNAs

The requirements for the receiver linearity and noise factor determine the maximum gain of the LNA in the presence of received input signals near the sensitivity level. However, in modern wireless receivers, the power of the desired signal at the receiver input may vary from -110 dBm to -20 dBm [68]. In order to improve the receiver linearity and to prevent the receiver from saturating in the presence of high signal levels, it may be necessary to have variable gain in the LNA. The lower LNA gain, and therefore the higher receiver noise factor, may be tolerated, if the received signal is not at the sensitivity level [69]. In practice, the variable gain in the receiver is usually implemented both in the RF and

baseband circuits.

Nowadays, most of the reported RF front-ends and LNAs utilize digital instead of analog gain control, which means that the RF front-end provides only discrete values of voltage gain. The drawback of the analog gain control is the need for a digital-to-analog (D/A) converter in the gain tuning engine to produce the analog control voltage or current. On the contrary, in the digital tuning scheme, the receiver gain can be altered without D/A converters.

The voltage gain of the inductively degenerated LNA can be altered by, for instance, employing current steering, by utilizing separate signal paths [69], by adjusting the input stage transconductance G_m or the load impedance Z_L. Unfortunately, as the gain control via altering G_m usually heavily affects the input impedance, input stage linearity, and noise factor of the amplifier, the other listed methods are preferred.

Figure 24 illustrates three possible ways of controlling the voltage gain of the inductively degenerated LNA. All the techniques shown provide a constant LNA input impedance in different gain modes. In the first approach, the gain step of the amplifier is implemented by connecting resistor R_{gp} in parallel with the LC resonator by closing the switch M_p to reduce the Q value of the resonator [70], [71]. Thus, in high-gain mode, the control voltage G_p is high and only a resistor R_p is connected in parallel with the resonator. In low-gain mode, G_p is low and both R_p and R_{gp} are active. Accordingly, in high-gain mode, the magnitude of the LNA load impedance at the resonance frequency is given by $|Z_{L,H}(\omega_0)| = (Q_{ind}\omega_0 L)||R_p$ whereas in low-gain mode $|Z_{L,L}(\omega_0)| = (Q_{ind}\omega_0 L)||R_p||R_{gp} \approx R_p||R_{gp}$. Unfortunately, as the gain step $|Z_{L,H}(\omega_0)|/|Z_{L,L}(\omega_0)|$ depends on the Q value of the inductor (i.e. Q_{ind}), the gain step does not necessarily remain constant in the presence of process variations [69]. In general, the value of the sheet resistance (R_{sh}) of the resistance material used to realize R_p and R_{gp} do not track with Q_{ind}, which depends, for instance, on the losses of the metal interconnect layers employed to realize the inductor.

In the second gain control approach shown in Figure 24(b), the gain of the amplifier is altered by steering the output current of the LNA input stage (i_{in}) to the resistor chain formed by R_1-R_3 [72]. For instance, in high-gain mode, the control voltage G_H is high and all the other control voltages are low. Thus, in high-gain mode, i_{in} is injected to the LNA output node, which has the highest resistance in the resistor chain. The other gain modes operate similarly. The benefit of the resistor-chain gain-control technique is its robustness against process variations. Since the gain steps depend on the resistance ratios of R_1, R_2, and R_3, the gain steps remain constant, even in the presence of process variations. For instance, if the ratio is $R_1 : R_2 : R_3 = 2 : 1 : 1$, the gain step between the successive gain modes is 6 dB. Finally, the impedance looking into the common-source node of the cascode devices (which is given by $1/g_{mc}$ where g_{mc} is the transconductance of the cascode transistor) remains constant in all gain modes. Thus, since the impedance $1/g_{mc}$ seen at the drain of the LNA input device remains constant despite the gain mode, the input matching of the amplifier remains constant in different modes of operation.

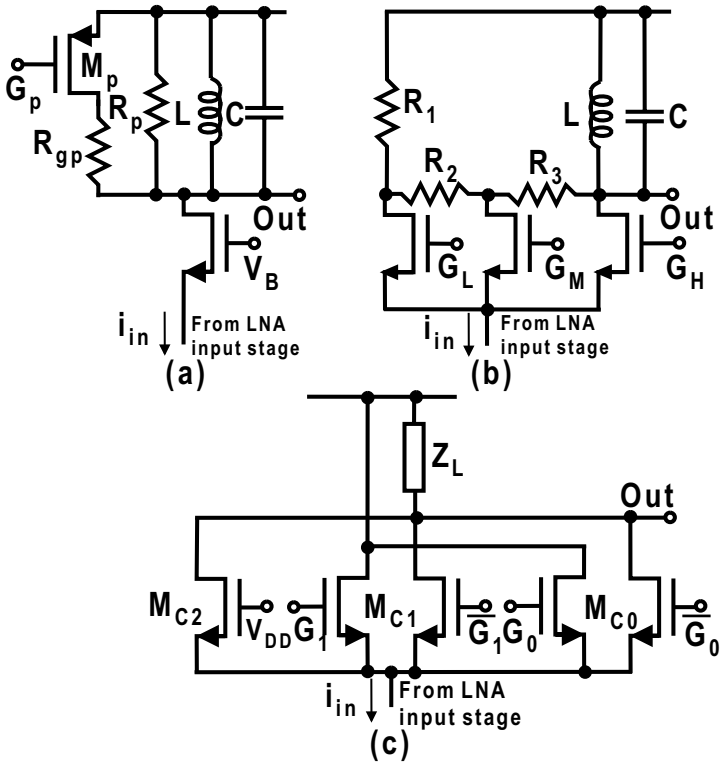

Figure 24: Three possible ways to implement digital gain control for inductively degenerated LNA. (a) Adjustment of LC-tuned load. (b) Resistor-chain gain-control technique. (c) Digitally controlled current steering circuit.

In the last technique, shown in Figure 24(c), the gain of the amplifier is altered by utilizing digitally controlled current steering in the cascode branch [73]. For instance, in high-gain mode, the control voltages $\overline{G_0}$ and $\overline{G_1}$ are high and i_{in} is steered totally to the LNA output node. In other modes of operation, a certain amount of i_{in} is steered to the supply voltage. Since the gain steps are based on the ratio of the W/L ratio of the cascode devices, a well-defined gain step, which remains constant in the presence of process variations, is produced. Finally, again this gain control technique provides constant impedance, given by $1/(g_{mc0} + g_{mc1} + g_{mc2})$, looking into the common-source node of the cascode devices. Accordingly, the LNA input matching remains constant in different modes of operation.

3.7 Biasing techniques

As described earlier, in order to stabilize the input impedance Z_{in} (see Eq. (3)), the input stage transconductance G_m (see Eq. (7)), and the voltage gain of the inductively degenerated common-emitter LNA against process and temperature variations, $g_m = I_C/V_t = (qI_C)/(kT)$ of the LNA input BJT has to be stabilized against variations. This can be accomplished by employing a PTAT biasing technique [37].

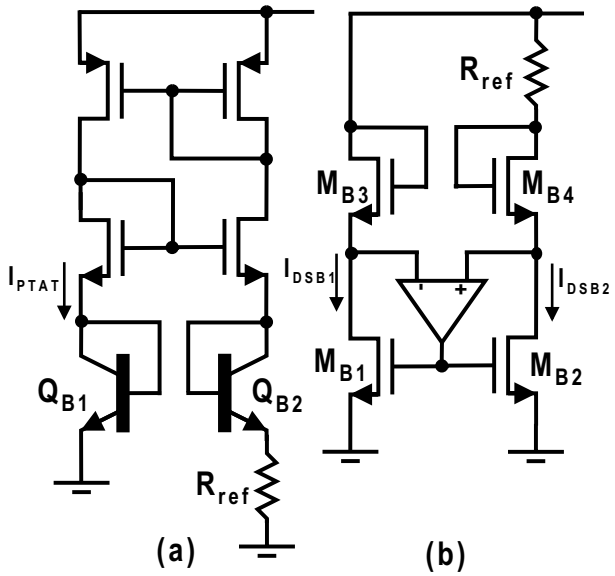

Figure 25: (a) PTAT reference circuit. (b) Constant-g_m circuit.

Figure 25(a) illustrates a typical PTAT reference circuit realized in BiCMOS technology. Although not shown, the bias circuit must use a start-up network to guarantee that the circuit ends up in the desired state. The PTAT circuit operates as follows. The NMOS and PMOS current mirrors with current mirror ratios of 1:1 force the collector currents of Q_{B1} and Q_{B2} to be equal. Therefore, the voltage across the reference resistor (R_{ref}) is the voltage difference between the base-emitter voltages of Q_{B1} and Q_{B2}. Thus, the current through R_{ref} is given by

$$I_{PTAT} = \frac{V_{BE1} - V_{BE2}}{R_{ref}} = \frac{V_t}{R_{ref}} \ln\left(\frac{A_2}{A_1}\right) = \frac{kT}{qR_{ref}} \ln\left(\frac{A_2}{A_1}\right) \tag{30}$$

where A_1 and A_2 are the base-emitter areas of Q_{B1} and Q_{B2}, respectively. Thus, if this reference current (I_{PTAT}) is mirrored by a multiplying factor of M to the collector current of the LNA input device (Q_1), g_m of Q_1 is given by $g_m = (MI_C)/V_t = (M/R_{ref}) \cdot \ln(A_2/A_1)$, which is seen to depend only on the geometry and on the value of R_{ref}, as desired.

Similarly, as with a BJT LNA, Z_{in} (see Eq. (16)), G_m (see Eq. (18)), and the voltage gain of the inductively degenerated common-source LNA can be regulated against process and temperature variations by stabilizing g_m of the LNA input FET against variations. In CMOS technology, this can be achieved by utilizing a constant-g_m biasing method [39].

One possible way to realize the constant-g_m circuit is shown in Figure 25(b) [39]. Again, the start-up network is omitted. If the FET is modeled with its square-law relationship

$$i_{DS} = \frac{\mu C_{ox}}{2} \frac{W}{L} (v_{GS} - V_T)^2 = \frac{K}{2} \frac{W}{L} (v_{GS} - V_T)^2 \tag{31}$$

and the sizes of the transistors $M_{B1} - M_{B4}$ are chosen as $(W/L)_{B1} = (W/L)_{B2} = (W/L)_{B3} = (W/L)$ and $(W/L)_{B4} = S \cdot (W/L)$, the drain-source currents of M_{B1} and M_{B2} are given as

$$I_{DSB1} = I_{DSB2} = \frac{L}{KWR_{ref}^2} \left(\frac{\sqrt{S} - 1}{\sqrt{S}} \right)^2 \tag{32}$$

Accordingly, the transconductance of M_{B1} and M_{B2} is

$$g_{mB1} = g_{mB2} = \frac{\sqrt{2}}{R_{ref}} \left(\frac{\sqrt{S} - 1}{\sqrt{S}} \right) \tag{33}$$

Thus, for instance, by biasing the LNA input FET by the gate-source voltage of M_{B1} and M_{B2}, the g_m of the LNA input FET can be made to depend only on the geometry and on the value of R_{ref}.

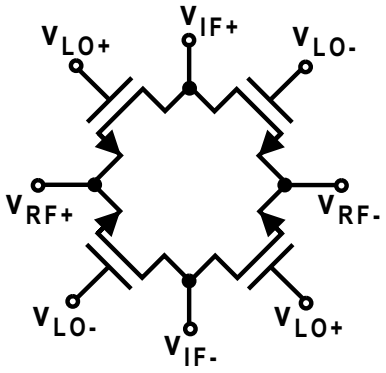

Figure 26: Passive mixer.

4 Downconversion Mixer Design

Typically, an RF front-end for a wireless receiver must provide approximately 25-35 dB voltage gain to limit the noise contribution of the analog baseband [53]. In addition, since practical voltage gains of the single-stage LNAs (i.e. inductively degenerated LNAs) are in the order of 15-25 dB, active mixers, which can provide conversion voltage gain, are often employed to provide the rest of the required voltage gain.

A passive commutating mixer, consisting of four FETs as analog switches (Fig. 26), is often considered to be superior to its active counterpart in the sense of flicker noise and linearity [74]. Since a passive mixer does not need a bias current and thus there is no dc current flowing through the switching FETs, it is essentially free of flicker noise [30]. A passive mixer requires large LO voltage swings, in practice, rail-to-rail, to work properly. This, however, can be accomplished by, for instance, employing CMOS inverters as LO buffers.

The serious drawback of passive mixers operating in voltage mode is their non-unilateral nature [75]. This means that the baseband circuit after the mixer may significantly load the LNA driving the mixer switching quad and thus degrade the gain of the LNA [30]. Moreover, in a direct conversion and low-IF receiver, it is important that the gain of the RF front-end (i.e. the cascade of LNA and mixer) is sufficient to overcome the noise of the baseband circuits (see Eq. (1)). Unfortunately, since passive mixers exhibit conversion loss (typically at least 3-5 dB), a prohibitively larger gain is required in the LNA. In practice, voltage gain in the order 30 dB has to be implemented at RF before the passive mixer. Unfortunately, this amount of voltage gain at RF can easily lead to problems like instability and degradation of linearity. For these reasons, active mixers are more suitable for direct conversion and low-IF receivers. Accordingly, in the following, only active downconversion mixers are considered.

A downconversion mixer for a zero- or low-IF receiver has to fulfill several requirements. First, as described above, the downconversion mixer should provide sufficient gain to re-

duce the noise contribution of the analog baseband circuits [76]. Next, a mixer with a low noise factor is desirable to relax the LNA gain requirement. Notice also that, in general, if the LNA gain can be reduced, the receiver linearity can be improved (see Eq. (2)).

A downconversion mixer aliases both the main and image responses at the output. Accordingly, this must be considered when the mixer noise factor is specified and the noise is referred to the mixer input. If the mixer output noise is referred to one or both input sidebands, the single-sideband (SSB) noise factor or double-sideband (DSB) noise factor is considered, respectively. The SSB noise factor is applicable to the superheterodyne receiver, in which only one of the input sidebands (i.e. the RF band) is converted to the IF and the image band is rejected [76]. On the other hand, in a direct conversion receiver, the LO signal is centered in the desired channel. Thus, both the desired signal energy and noise occupy both upper and lower sidebands, and there is no idle sideband to be filtered [2]. Moreover, since the direct conversion receiver keeps the images of signal and noise in separate quadrature channels, the DSB noise factor is applicable to zero-IF architecture [46].

Often, in a well-designed RF front-end, the mixer linearity dominates the entire front-end linearity. In a downconversion mixer, third-order intermodulation (IM3) may cause two large adjacent-channel signals to generate IM3 products at spurious frequencies coincident with a weak desired channel. Accordingly, the IIP3 of the mixer has to be sufficiently high to mitigate against this effect. In addition to IIP3, the downconversion mixer for a zero- or low-IF receiver has to have adequate ICP to tolerate large blocking or interference signals, which may reduce the front-end small-signal gain or increase the noise factor.

If two strong signals at the frequencies of f_1 and f_2, which are located at the passband of the preselection filter of the receiver, are exposed to a second-order nonlinearity, unwanted spurious baseband responses are generated. These are the dc offset component and the baseband IM2 component at $f_1 - f_2$ [77]. In the RF front-end, this may happen both in the LNA or in the mixer. However, if the LNA and mixer are ac-coupled (which is a common practice), the dc offset and low-frequency beat signal generated in the LNA are filtered out. Therefore, it is the downconversion mixer that usually determines the achievable IIP2 of the entire receiver [28]. Thus, a downconversion mixer with high IIP2 is required to protect a zero- or low-IF receiver from unwanted dc offsets and IM2 products, and to minimize the effect of the second-order nonlinearity on the receiver performance.

The mixers utilized in integrated homodyne or low-IF receivers are practically always based either on single- or double-balanced circuit topologies [42]. If a mixer operates with a differential LO signal and single-ended RF signal, it is called single-balanced. However, if a mixer accommodates both differential RF and LO signals, it is called double-balanced. The double-balanced configurations generate less even-order distortion and provide better port-to-port isolation than the single-balanced mixers. In addition, the single-balanced topologies are more susceptible to noise in LO signal [40]. For these reasons, this thesis concentrates only on double-balanced topologies.

In the following, the design and optimization of bipolar and BiCMOS active downconversion mixers is discussed first. Next, low-voltage circuit design techniques for CMOS mixers are presented. Then, methods and techniques for suppressing IM2 distortion in mixer RF input stages are discussed and the benefits and drawbacks of different techniques are analyzed. It should be noticed that in order to maximize the mixer IIP2 and to minimize the IIP2 sensitivity to mismatches, it is important to minimize the level of the common-mode IM2 components in the output current of the mixer RF transconductor. Finally, the characteristics of different RF transconductors are compared both in terms of IIP2 and IIP3.

The purpose of the following discussion is to provide design guidelines and insight into the design and optimization principles of active downconversion mixers and the whole RF front-end. As already mentioned, in practice, the mixer IIP3 often limits the RF front-end linearity and the mixer IIP2 determines the IIP2 of the entire zero- or low-IF receiver. Finally, since the mixer in practice is preceded only by 15-25 dB voltage gain in the LNA (limited by the receiver linearity requirements), the effect of the mixer noise to the receiver noise is not usually negligible. Thus, besides of the mixer linearity, circuit and optimization techniques must be utilized to minimize mixer noise.

4.1 Bipolar and BiCMOS downconversion mixers

Most of the active double-balanced mixers utilized in wireless receivers are based on the Gilbert mixer topology shown in Fig. 27 [78]. The Gilbert mixer employs a differential pair Q_1-Q_2 as its RF input transconductance stage to convert the differential voltage-mode RF signal to a differential current. The current-mode RF signal is then fed through the current-steering cell Q_3-Q_6 driven by the LO signal. The IF output is also produced as a current-mode and is converted to the voltage at the IF load R_{L1}-R_{L2}. If instantaneous switching of the switching quad is assumed (i.e. that the current-mode RF signal is multiplied by the square wave toggling at the LO frequency), the mixer voltage conversion gain is given by [30]

$$A_v = \frac{2}{\pi} g_m R_L \tag{34}$$

where g_m is the transconductance of Q_1 (and Q_2). Often, the load of the mixer consists of a first-order RC low-pass filter (i.e. of a capacitor in parallel with a load resistor), which improves the mixer out-of-band blocking characteristics and relaxes the linearity requirements of the following baseband circuits.

The noise and linearity of the mixer RF input stage are crucial to the mixer performance. Often the linearity of the Gilbert mixer is mainly determined by the RF input stage and is quite poor in the basic Gilbert mixer due to the limitations in the linearity of the BJT differential pair [78]. If the bipolar transistor is modeled with its exponential relationship

$$i_C = I_S e^{\frac{v_{BE}}{V_t}} \tag{35}$$

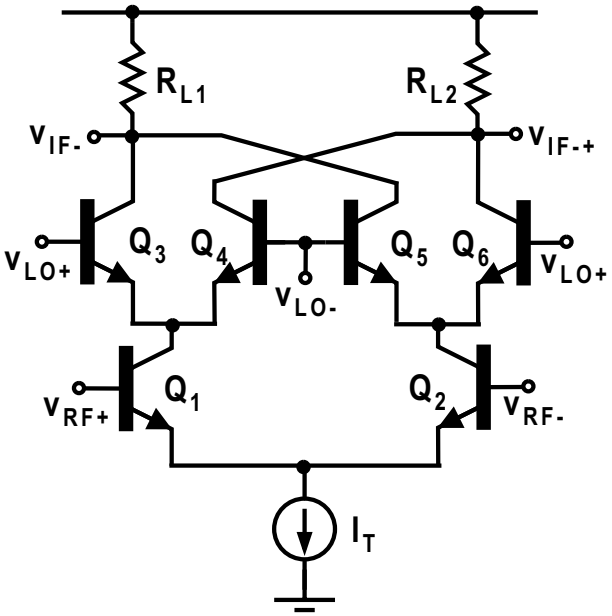

Figure 27: Gilbert mixer.

where I_S is the collector saturation current and the differential pair is biased by a tail current $I_T = 2A \cdot I_B$, the IIP3 of the differential pair can be approximated as [79]

$$v_{IIP3} = 4V_t \tag{36}$$

which represents the differential RF input amplitude. Thus, the IIP3 of the BJT differential pair is fixed approximately to a value of $v_{IIP3} = 4 \times 26$ mV=104 mV at room temperature [79]. The linearity of the RF input stage can be improved by, for example, utilizing an inductive or resistive emitter degeneration [80]. Inductive degeneration results in lower noise than resistive degeneration, but, unfortunately, it increases silicon area and cost significantly, because, in I and Q mixers four integrated inductors (or two differential inductors) are required. With resistive degeneration, the IIP3 of the differential pair improves to [79]

$$v_{IIP3} = 4V_t(1 + g_m R_E)^{3/2} \tag{37}$$

where $g_m = (AI_B)/V_t$, R_E is the emitter degeneration resistance, and $g_m R_E$ is the loop gain of the negative feedback.

As supply voltage scales down with transistor technology, the stacking of four devices in a standard Gilbert cell becomes difficult or even impossible. For this reason, the Gilbert mixer is often implemented without the tail current source, as shown in Fig. 28. In this case, the IIP3 of the mixer can be approximated by assuming that the mixer linearity is dominated by the linearity of the resistively degenerated common-emitter RF input stage, for which the IIP3 can be approximated as [79]

$$v_{IIP3} = 4\sqrt{2}V_t \frac{(1 + g_m R_E)^2}{\sqrt{|1 - 2g_m R_E|}} \tag{38}$$

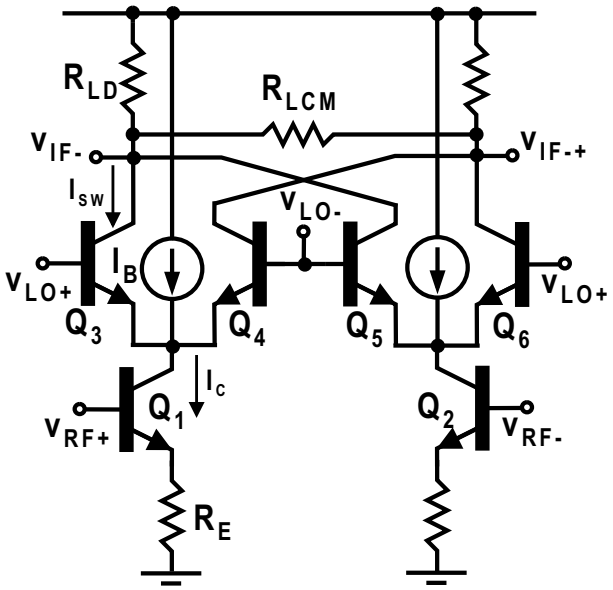

Figure 28: Resistively degenerated Gilbert mixer without the tail current source.

The IIP3 of the degenerated common-emitter RF transconductor is higher by a factor of $\sqrt{2(1+g_mR_E)/|1-2g_mR_E|}$ than the corresponding IIP3 of the degenerated differential pair given by Eq. (37). The drawback of the common-emitter RF input stage is its inability to reject common-mode interference and its IM2 characteristics, as will be shown in Chapter 4.3.1.

In the following, the properties of the downconversion mixer shown in Fig. 28 are analyzed in more detail and the design flow and optimization of the mixer are considered. In the mixer shown in Fig. 28, resistors R_{CM} and R_{LD} determine the mixer output common-mode level and conversion gain, respectively. In addition, current boosting by a current source (I_B) is employed to relax low-voltage operation [70]. By current boosting, higher conversion voltage gain can be achieved, since larger resistors can be utilized at the output, and a lower mixer noise factor is achievable without sacrificing the mixer third-order nonlinearity.

As the current conversion loss through the switching quad Q_3-Q_6 is theoretically $2/\pi$, it is easy to show that the voltage conversion gain of the mixer shown in Fig. 28 can be approximated as

$$A_v = \frac{2}{\pi}\frac{g_m}{1+g_mR_E}R_L. \tag{39}$$

where R_L is the equivalent load resistor of the mixer. Moreover, as the conversion gain depends on $g_m = I_C/V_T$ of Q_1, the mixer has to be biased by using the PTAT current [37]

$$I_C = \frac{kT}{qR_{ref}}\ln A \tag{40}$$

in order to compensate the temperature variations of the gain. In addition, if R_L and R_E are realized by using the same material as the reference resistance R_{ref}, the mixer gain is in a first-order approximation independent of the process or temperature variations of the resistance material. This type of biasing arrangement stabilizes the gain against supply, temperature, and process variations and therefore guarantees very robust performance.

The DSB noise factor of the downconversion mixer shown in Fig. 28 can be estimated by considering the noise due to the mixer RF input transconductance stage, load, and switches. The noise factor is calculated by finding separately all the noise voltage contributions at the mixer output. Only white noise is considered, since, in practice, in a downconversion mixer with BJT switches, the flicker noise is not usually an issue, even in a direct conversion receiver for narrow-band applications, such as GSM.

First, the expressions for the different contributions to the output noise current of the RF input stage are derived. By applying a straightforward circuit analysis, it is easy to show that the total noise current at the RF differential transconductor output is given by

$$\begin{aligned}\overline{i^2_{on,g_m}} &= 2 \times (\overline{i^2_{n,R_s}} + \overline{i^2_{n,r_b}} + \overline{i^2_{n,i_b}} + \overline{v^2_{n,i_c}} + \overline{i^2_{n,R_E}}) \\ &= \frac{2 \times \left(g_m^2 \overline{v_s^2} + g_m^2 \overline{v_b^2} + g_m^2 (R_s + R_E)^2 \overline{i_b^2} + \overline{i_c^2} + g_m^2 R_E^2 \overline{i_E^2} \right)}{(1 + g_m R_E)^2}\end{aligned} \tag{41}$$

where the factor of two accounts for the differential operation and $\overline{i^2_{n,R_s}}$, $\overline{i^2_{n,r_b}}$, $\overline{i^2_{n,i_b}}$, $\overline{i^2_{n,i_c}}$, and $\overline{i^2_{n,R_E}}$ represent the noise contributions of the source resistance R_s, base resistance r_b, base shot noise i_b, collector shot noise i_c, and R_E, respectively. In addition, here $\overline{v_s^2} = 4kTR_s\Delta f$, $\overline{v_b^2} = 4kTr_b\Delta f$, $\overline{i_b^2} = 2qI_C\Delta f/\beta_0$, $\overline{i_c^2} = 2qI_C\Delta f$, and $\overline{i_E^2} = 4kT\Delta f/R_E$.

If the mixer commutation is assumed square-wave like, the LO frequency and its odd harmonics will downconvert the components of the RF input stage white noise $\overline{i^2_{on,g_m}}$ to the IF frequency. Therefore, the corresponding noise voltage components at the IF are given by [41]

$$\overline{v^2_{on,g_m}} = n \times \left(\frac{2}{\pi} R_L \right)^2 \overline{i^2_{on,g_m}} \tag{42}$$

where the factor n represents accumulated noise after aliasing. For the harmonic amplitudes of the square wave $n = \pi^2/4$.

The mixer output noise voltage due to the white noise in the four switches Q_3-Q_6 in a double-balanced mixer can be approximated as [41]

$$\overline{v^2_{on,sw}} = 4 \times 2kT \frac{R_L^2 I_{SW}}{\pi A_{LO}} \Delta f \tag{43}$$

where A_{LO} is the LO amplitude and I_{SW} is the bias current of the switching pair (in a mixer with current boosting, I_{SW} is different from the I_C of the g_m-stage). Eq. (43) is derived by considering only switch collector shot noise.

The output noise voltage due to the equivalent load resistors (R_L) is given by

$$\overline{v_{on,R_L}^2} = 2 \times 4kTR_L\Delta f \tag{44}$$

where the factor of two is due to the two load resistors in the mixer.

The DSB noise factor for a downconversion mixer can be written as

$$F_{DSB} = \frac{\overline{v_{on}^2}}{\overline{v_{on,R_s}^2}} = \frac{\overline{v_{on,g_m}^2} + \overline{v_{on,sw}^2} + \overline{v_{on,R_L}^2}}{\overline{v_{on,R_s}^2}} \tag{45}$$

where $\overline{v_{on}^2}$ is the total mixer output noise and $\overline{v_{on,R_s}^2}$ is the output noise due to the noise of the source resistance R_s at the main and image band [81]. The downconverted output noise voltage due to the noise of R_s at the main and image band is given by

$$\overline{v_{on,R_s}^2} = 2 \times \left(\frac{2}{\pi}R_L\right)^2 2\overline{i_{n,R_s}^2} = 4\left(\frac{2}{\pi}R_L\right)^2 \frac{g_m^2\overline{v_s^2}}{(1+g_mR_E)^2} \tag{46}$$

where the first factor of two is due to the assumption that the mixer conversion gain is equal for both main and image bands. The second factor of two takes into account the noise in the differential source resistor $(2R_s)$.

By combining the equations derived above, the DSB noise factor can be written as

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{r_b}{R_s} + \frac{g_m(R_s+R_E)^2}{2R_s\beta_0} + \frac{1}{2g_mR_s} + \frac{R_E}{R_s} + \frac{I_{SW}(1+g_mR_E)^2}{g_m^2R_s\pi A_{LO}} + \frac{(1+g_mR_E)^2}{g_m^2R_LR_s}\right) \tag{47}$$

From Eq. (47), it is seen that, in order to reduce the noise contributions of the RF input transistors Q_1-Q_2, sufficiently large base-emitter area devices with small r_b should be used. Moreover, since all terms involving g_m, excluding the term due to the base shot noise, decrease with I_C, the noise factor of the mixer decreases with practical values of I_C. The value of R_E should be minimized to maximize the gain of the RF transconductor stage and to minimize the noise contributions of the switching transistors and load. However, since the decrease of R_E reduces the loop gain of the negative feedback, the IIP3 of the mixer decreases accordingly (see Eq. (38)). Finally, the white noise due to the switching quad Q_3-Q_6 can be reduced by biasing the switching transistors at lower collector current I_{SW} and by utilizing LO swing with a sufficiently large amplitude A. However, I_{SW} can not be arbitrary low, because, otherwise, the linearity of the switches is deteriorated. In addition, a very large LO amplitude results in excessive current being pumped into to the common-emitter node of the switching quad through the base-emitter junction capacitance (C_{je}). Thus, additional third-order intermodulation is generated [76].

Figures 29 and 30 plot the simulated IIP3 and DSB-NF $(10\log(F_{DSB}))$ of the direct conversion downconversion mixer shown in Fig. 28, realized in a 0.35-μm BiCMOS technology with a supply voltage of 2.7 V, at 2 GHz, as a function of the RF input BJT collector

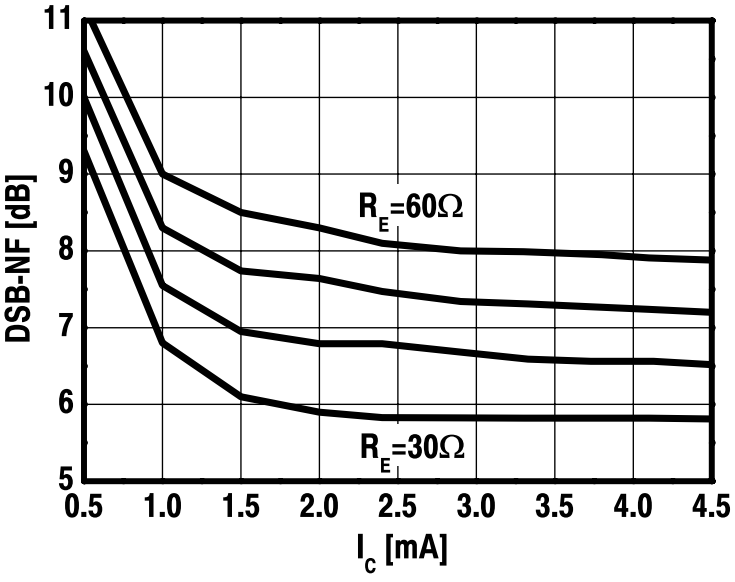

Figure 29: Simulated DSB-NF of downconversion mixer shown in Fig. 28 as a function of RF input stage collector current.

current I_C with different values of emitter resistance ($R_E = 30, 40, 50, 60\ \Omega$). The IIP3 is presented as an input power in dBm and the differential RF input voltage is referred to a 100-Ω source resistor $(2R_s)$. In addition, the spot DSB-NF at the IF frequency of 100 kHz is expressed with respect to the noise in 100 Ω. The RF input BJT is realized with four unit transistors in parallel to minimize the noise contribution of r_b. Again, the unit NPN transistor has two base contacts and an emitter size of 0.4 x 10 μm^2. In this simulation, the LO voltage swing driving the mixers is about 0.6 V_{p-p} single-ended. Moreover, at each point, the values for the load resistors R_{LCM}-R_{LD} and bias current I_B are selected to provide a 10-dB conversion voltage gain and 2-V common-mode level at the mixer output.

From Figures 29 and 30, it is seen that the downconversion mixer with an RF input collector current of 2.9 mA (the total current consumption of the mixer is thus 5.4 mA) and $R_E = 50\ \Omega$ achieves an IIP3 of 10 dBm and DSB-NF of 7.3 dB. The resistors $R_{LD} = 340\ \Omega$ and bias current of $I_B = 900\ \mu$A realize 10-dB gain and a 2-V mixer output common-mode level. Although a DSB-NF of 7.3 dB represents a spot NF, the simulations show that this also corresponds very accurately to the actual integrated DSB-NF, for instance, for a direct conversion receiver for GSM or WCDMA applications (assuming NF in GSM and WCDMA applications is integrated over a bandwidth of 100 Hz-135 kHz and 10 kHz-1.92 MHz, respectively). It is concluded that the bipolar switching transistors contribute negligible flicker noise at the mixer output.

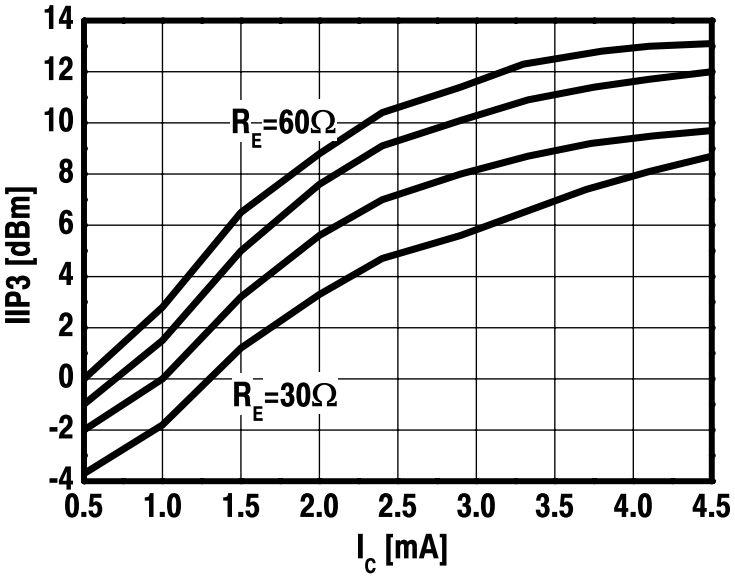

Figure 30: Simulated IIP3 of downconversion mixer shown in Fig. 28 as a function of RF input stage collector current.

Figure 31 illustrates the simulated mixer gain and IIP3 as a function of the LO amplitude. Here I_C =2.9 mA (the whole mixer consumes 5.4 mA), $R_E = 50\ \Omega$, $R_{LD} = 340\ \Omega$ and $I_B = 900\ \mu$A. It is seen that the IIP3 improves by increasing the LO amplitude, but, as discussed above, a too large LO swing produces additional distortion.

In BiCMOS technology, the RF input transconductor of the downconversion mixer can also be implemented with a grounded-source pair, as shown in Fig. 32 [3]. Since the common-source transconductor biased at a given overdrive voltage $V_{eff} = V_{GS} - V_t$ exhibits smaller third-order nonlinearity than the FET differential pair at equal bias [48], the common-source RF input stage is often preferred to the differential pair. However, as will be discussed in detail in Section 4.3.1, the drawbacks of the conventional common-source circuit are its IM2 characteristics and its inability to reject common-mode interference.

Unlike the common-emitter RF transconductor (see Fig. 28), the common-source RF input stage can be effectively linearized without degeneration. If the MOS transistor is modeled with

$$i_{DS} = \frac{K}{2}\frac{W}{L}\frac{(v_{GS} - V_T)^2}{1 + \theta(v_{GS} - V_T)} \tag{48}$$

the IIP3 of the downconversion mixer utilizing the common-source RF input transconductor can be estimated by considering the IIP3 of the common-source circuit, which can

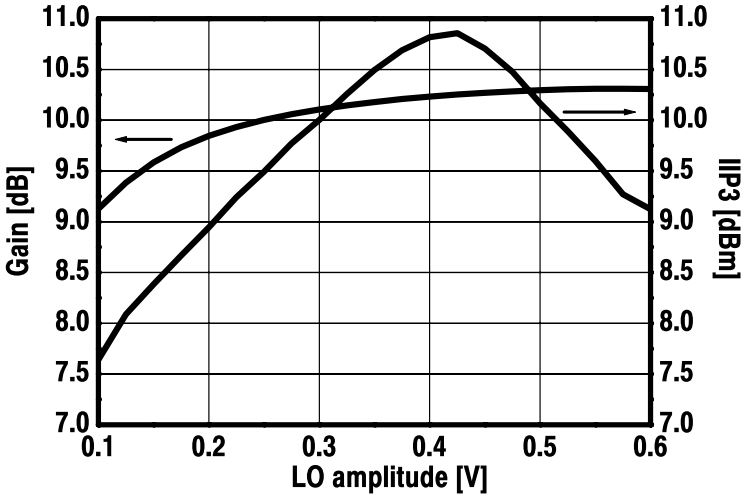

Figure 31: Simulated voltage gain and IIP3 of downconversion mixer shown in Fig. 28 as a function of LO amplitude.

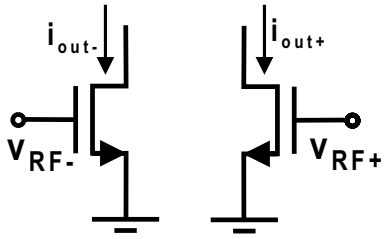

Figure 32: Common-source RF input transconductor for double-balanced downconversion mixer.

be approximated as [Paper V]

$$v_{IIP3} = \frac{4}{\sqrt{3}}\sqrt{\frac{V_{eff}(2+\theta V_{eff})}{\theta}}(1+\theta V_{eff}) \approx 4\sqrt{\frac{2}{3}\frac{V_{eff}}{\theta}} \tag{49}$$

where $V_{eff} = V_{GS0} - V_T$, V_{GS0} is the bias voltage at the gates of M_1-M_2, and the approximation holds if $\theta V_{eff} \ll 1$ [79]. Thus, it is seen that the IIP3 of the mixer utilizing common-source RF transconductor can be scaled up by increasing the RF input V_{eff}. In addition, since θ is inversely proportional to the channel length L, long-channel FETs at the mixer input improve the linearity.

The DSB noise factor of the BiCMOS downconversion mixer employing a common-source RF g_m-stage can be analyzed by considering the noise due to the mixer g_m-stage, load, and BJT switches. For simplicity, only the channel thermal noise of the RF transconductor is considered. By utilizing the results derived for the BJT mixer above, it is easy to

show that the DSB noise factor of the BiCMOS downconversion mixer with a common-source RF g_m-circuit is given by

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{\gamma}{g_m R_s} + \frac{I_{SW}}{g_m^2 R_s \pi A_{LO}} + \frac{1}{g_m^2 R_L R_s}\right) \tag{50}$$

where the first term is due to the channel thermal noise ($\overline{i_d^2} = 4kT\gamma g_m \Delta f$) of the input FETs M_1-M_2. It is seen that the noise factor decreases by scaling up the g_m of the RF input FETs.

Equations (49) and (50) provide insight and guidelines for the BiCMOS mixer design process. First, the required IIP3 determines the RF input transconductor V_{eff}. Next, as seen from Eq. (50), the desired noise factor target largely defines the RF input stage g_m given by

$$g_m = \frac{K}{2}\frac{W}{L}\frac{(2 + \theta V_{eff})V_{eff}}{(1 + \theta V_{eff})^2} \tag{51}$$

and thus the W/L ratio of the input transistors. Accordingly, the target values for the mixer IIP3 and noise factor together determine the mixer current consumption (see Eq. (48)). Finally, as the mixer RF input stage is designed for the target performance, the mixer voltage gain can be set to the desired value by designing the mixer load accordingly.

As bipolar transistors have, in general, much lower flicker noise than MOS devices, it is beneficial to employ BJTs as switching devices in active BiCMOS downconversion mixers targeted for zero- or low-IF receivers [3]. In addition, since BJT switches provide better matching than their FET counterparts, higher mixer IIP2 and lower offset voltage are generally attainable with bipolar switches. Finally, the BJT switching quad requires a much lower LO voltage swing to experience complete switching than does an FET counterpart [40], thus making it easier to save power in the LO buffers and to reduce the LO leakage.

4.2 Low-voltage CMOS downconversion mixers

As CMOS technology scales down, the lower supply voltage poses problems for the analog and RF circuit design. Currently, typical supply voltages in state-of-art sub-micron CMOS processes (i.e. 65-130 nm) are in the order of only 1 V. In general, low supply voltage degrades the circuit's ability to handle large unwanted signals [8]. Thus, as the downconversion mixer typically limits the RF front-end's linearity and the capability to tolerate large blocking or interference signals, the mixer design at low supply voltage becomes very challenging. In modern CMOS processes, critical analog and RF circuits can naturally be implemented with dual-gate or thick-oxide FETs, which tolerate higher supply voltages, but this solution increases the cost, since additional processing masks are required. For this reason, the development of low-voltage CMOS analog and RF circuits is economically advantageous. In the following, the tradeoffs and problems in the design of low-voltage (i.e. 1-1.5 V) CMOS mixers for cellular (such as GSM and WCDMA) direct conversion and low-IF receivers are studied.

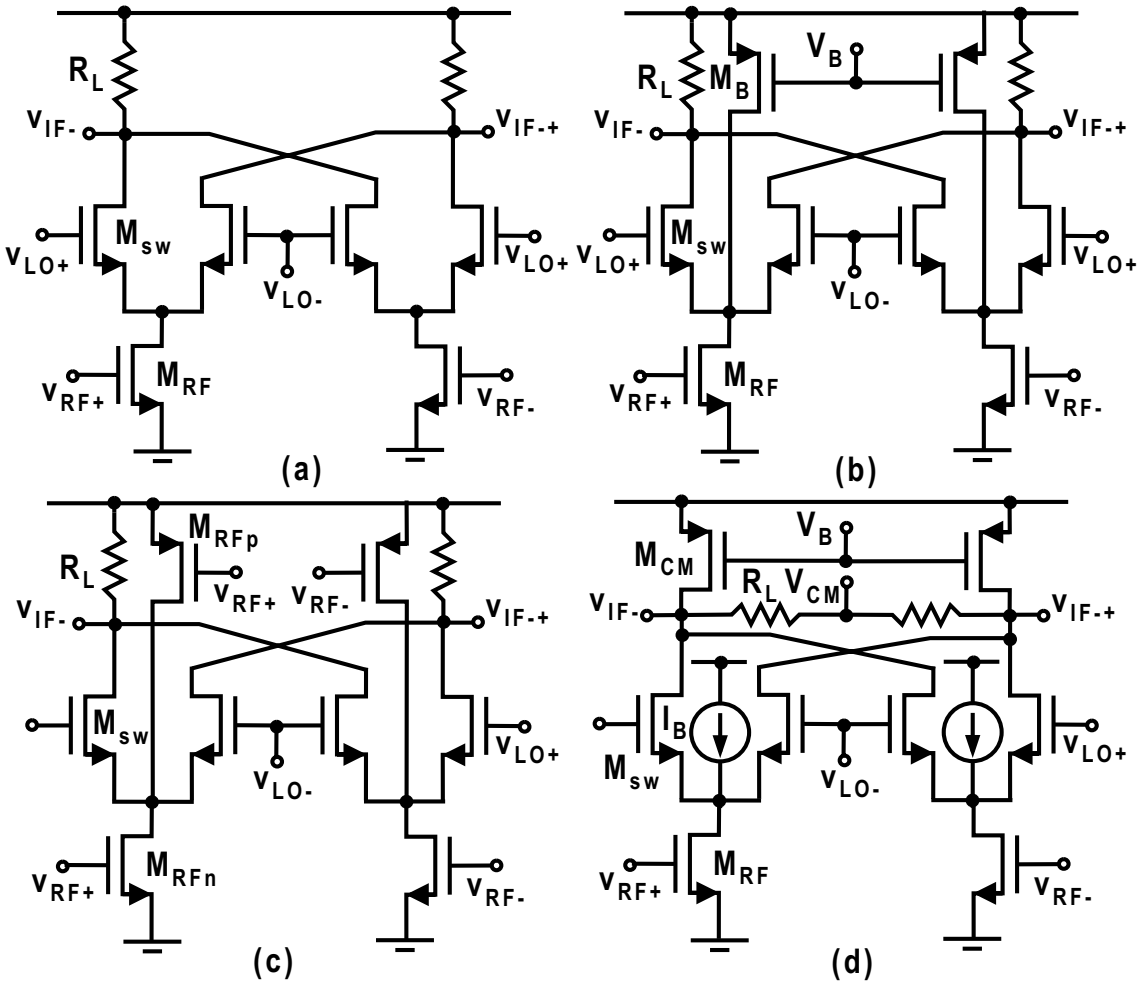

Figure 33: Active CMOS downconversion mixer topologies.

Figure 33(a) illustrates a typical active CMOS downconversion mixer circuit. As described earlier, the V_{eff} of the RF input FET (M_{RF}) is chosen to obtain certain IIP3. Then, the dimensions (W/L) of M_{RF} determine the desired input stage transconductance

$$g_m = \frac{K}{2}\frac{W}{L}\frac{(2+\theta V_{eff})V_{eff}}{(1+\theta V_{eff})^2} \approx \frac{2I_{DS}}{V_{eff}} \tag{52}$$

and bias current (I_{DS}). The RF input stage g_m must be sufficiently large to provide tolerable input-referred noise and DSB noise factor, which, for the mixer shown in Fig. 33(a), can be approximated as [41] (considering only white noise)

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{\gamma}{g_m R_s} + \frac{2\gamma I_{DS}}{g_m^2 R_s \pi A_{LO}} + \frac{1}{g_m^2 R_L R_s}\right) \tag{53}$$

Moreover, the mixer conversion gain

$$A_v = \frac{2}{\pi} g_m R_L \approx \frac{2}{\pi}\frac{2I_{DS}}{V_{eff}} R_L \tag{54}$$

must be high enough to overcome the noise due to the mixer load (R_L) and the following baseband circuits. Unfortunately, as the output common-mode level of the mixer (see Fig. 33(a)) is given by $V_{OCM} = V_{DD} - R_L I_{DS}$, the dc voltage drop $(R_L I_{DS})$ across the resistor loads links the maximum obtainable gain to the supply voltage (V_{DD}). Accordingly, at low supply voltage, it is difficult to scale up the gain by increasing R_L or I_{DS} without V_{OCM} becoming too low for the switch and RF input FETs to remain in saturation. For this reason, the realization of a reasonable amount of gain (i.e. 5-15 dB) with sufficient linearity and tolerable noise performance with the basic mixer shown in Fig. 33(a) at low voltage is difficult, at least for cellular applications.

In active current commutating CMOS mixers, flicker noise in the FET switches appears at the output at baseband without frequency translation [41]. This can significantly raise the noise factor in a zero- or low-IF receiver particularly in narrow-band applications such as GSM. In a zero- or low-IF receiver, the RF input FETs contribute only white noise at the mixer output [83]. Moreover, the mixer load resistors are free of $1/f$ noise.

In an active mixer, switches contribute flicker noise to the mixer output in two different ways. In direct mechanism, flicker noise modulates the time instants of mixer switching whereas in indirect mechanism, it induces current in the tail capacitance, which is commutated to the output. At the output of the double-balanced mixer shown in Fig. 33(a), the flicker noise current due to the direct mechanism is given by [41]

$$i_{o,n} = 4I_{SW} \times \frac{v_n}{S \times T} \tag{55}$$

where I_{SW} is the bias current of each switch pair, v_n represents the equivalent flicker noise of the switching quad, S is the slope of the LO signal at the switching instant, and T is the LO period. Thus, the flicker noise due to the direct mechanism can be lowered by reducing I_{SW}, increasing the slope of the LO signal, or by reducing the flicker noise component of the switching FETs (i.e. v_n) by increasing the size $W \times L$ of the switches. On the other hand, the flicker noise due to the indirect mechanism at the mixer output can be reduced by reducing the tail capacitance at the common-source of the switches.

In Fig. 33(b), current boosting by a current source (M_B) [70] is employed to relax low voltage operation, to decouple the conversion gain from the supply voltage, and to reduce the bias current of the switches I_{SW} to lower the flicker noise at the output. Since M_B supplies part of the RF input stage bias current I_{DS}, the larger input stage g_m or R_L can be utilized with M_{RF} and M_{SW} operating safely in saturation. However, the white noise of the current source adds to that of the transconductance stage, increasing the mixer white noise factor. In particular, by utilizing the results derived in Section 4.1 and [41], [81], it can be shown that the white-noise DSB noise factor of the mixer employing current boosting can be approximated as

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{\gamma_n}{g_m R_s} + \frac{\gamma_p g_{mB}}{g_m^2 R_s} + \frac{2\gamma_n I_{SW}}{g_m^2 R_s \pi A_{LO}} + \frac{1}{g_m^2 R_L R_s}\right) \tag{56}$$

where the third term is due to the channel thermal noise of M_B $(\overline{i_d^2} = 4kT\gamma_p g_{mB}\Delta f)$, and γ_n and γ_p are the channel current noise factors of NMOS and PMOS transistors, respec-

tively. For a given bias current, PMOS sources M_B should be biased at large $V_{eff,B}$ or their $(W/L)_B$ should be small to lower their thermal noise at the mixer output.

The current boosting technique can also be modified to include RF signal amplification in the bias transistor M_B, as shown in Fig. 33(c) [82]. As the total RF input stage transconductance of the mixer with a complementary RF input stage is $(g_{mn} + g_{mp})$ where g_{mn} and g_{mp} are the transconductances of M_{RFn} and M_{RFp}, respectively, lower R_L can be utilized at the mixer output to realize a given voltage gain. This enhances the operation at low voltage. In addition, since for given current consumption and voltage gain the mixer with the complementary input stage has higher total transconductance than the mixer with conventional current boosting, the mixer with complementary RF input stage has lower input-referred noise. As a matter of fact, it can be shown that the white-noise DSB noise factor of the mixer shown in Fig. 33(c) can be estimated as

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{\gamma_n g_{mn} + \gamma_p g_{mp}}{(g_{mn}+g_{mp})^2 R_s} + \frac{2\gamma_n I_{SW}}{(g_{mn}+g_{mp})^2 R_s \pi A_{LO}} + \frac{1}{(g_{mn}+g_{mp})^2 R_s R_L}\right) \quad (57)$$

At low supply voltage, the nonlinearity contribution of the mixer switching quad M_{SW} is not usually negligible. The FETs in the commutating differential pair create nonlinearity due to the signal-dependent current division [51]. Sharp transitions in the LO waveform lower the distortion and flicker noise due to the mixer switches [31] and thus it is often beneficial to raise the amplitude of the LO signal to sharpen the transition. Unfortunately, at low supply voltage, only a small headroom margin for the mixer switches to remain in saturation can be guaranteed and high LO amplitude reduces this margin further. Thus, a too-large LO amplitude will force the switch FETs into the triode region and degrade the mixer linearity due to the nonlinear mixer output resistance. Mixers employing the current boosting technique and complementary RF input stage reduce the bias current I_{SW} of the mixer switches in order to enable low-voltage operation and to lower the flicker noise at the output. Unfortunately, reducing the bias current of the switches raises the impedances seen at their sources, increases the RF voltage swing at the common-source node of the switches, and therefore degrades the mixer linearity and bandwidth [83]. Thus, for given switch FET dimensions, mixer switches must be biased at sufficient current to guarantee that the mixer switching quad do not limit the mixer third-order linearity. Unfortunately, for given voltage gain, increasing the bias current of the switches lowers the output common-mode level of the mixers shown in Figures 33(a)-(c) and reduces the saturation margin of the transistors. For these reasons, at low supply voltage the mixers shown in Figures 33(a)-(c) are usually too nonlinear for cellular applications, at least when a practical amount of conversion voltage gain (i.e. 5-15 dB) is to be implemented. For instance, simulated in the 0.13-μm CMOS technology, the mixer with a complementary RF input stage shown in Fig. 33(c) achieves a voltage conversion gain of 10 dB, IIP3 of +1 dBm, and a white-noise DSB-NF $(10\log(F_{DSB}))$ of 4 dB with respect to the noise in a 100-Ω differential resistor. Its $1/f$ corner frequency lies at 470 kHz. Unfortunately, an IIP3 in the order of +1 dBm is not usually sufficient for cellular systems. Moreover, although the mixer has a very low white-noise NF, the flicker noise increases the integrated NF significantly. For instance, assuming the DSB-NF in GSM and WCDMA direct conversion receiver is integrated over a bandwidth of 100 Hz-135 kHz and 10 kHz-1.92 MHz,

the integrated DSB-NF for GSM and WCDMA applications is about 18 dB and 7.5 dB, respectively. The mixer draws 4 mA from a 1.2-V supply.

By utilizing a common-mode feedback (CMFB) circuit at the mixer output (Fig. 33(d)), the bias current of the mixer switches can be increased to improve the mixer linearity without lowering the common-mode level at the output [30]. In addition, the conversion gain can be increased by scaling up the differential load resistors without altering the output dc level. Unfortunately, noise from the two CMFB current source FETs (M_{CM}) appears as differential noise at the mixer output. In this case, the white-noise DSB noise factor of the mixer can be approximated as

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{\gamma_n}{g_m R_s} + \frac{\gamma_p g_{mB}}{g_m^2 R_s} + \frac{2\gamma_n I_{SW}}{g_m^2 R_s \pi A_{LO}} + \frac{1}{g_m^2 R_L R_s} + \frac{\gamma_p g_{mCM}}{g_m^2 R_s}\right) \qquad (58)$$

where the last term is due to the channel thermal noise of M_{CM} $(\overline{i_d^2} = 4kT\gamma_p g_{mCM}\Delta f)$. To fit into a low supply voltage, CMFB FETs should be biased at small $V_{eff,CM}$, which unfortunately increases their $g_{mCM} = (2I_{DS,CM})/V_{eff,CM}$ and enhances their noise. In addition, the flicker noise of the CMFB FETs further increases the mixer noise factor, particularly in narrow-band applications. To reduce the flicker noise due to the CMFB FETs, large-area devices have to be applied. Moreover, although increasing the bias current of the mixer switches improves the mixer linearity, it increases the flicker noise due to the switches at the output (see Eq. (55)). For instance, simulated in the 0.13-μm CMOS technology, the mixer shown in Fig. 33(d) achieves a gain of 10 dB, IIP3 of +6 dBm, and a white-noise DSB-NF of 9 dB. Its $1/f$ corner frequency is as high as 1.1 MHz. As a result, its integrated DSB-NF for GSM and WCDMA zero-IF receiver is as high as 27 dB and 16 dB, respectively. The mixer draws 4 mA from a 1.2-V supply. As a conclusion, although the mixer with active loads shown in Fig. 33(d) has higher linearity, it is usually too noisy at least for narrow-band zero- or low-IF receivers.

An input-referred flicker noise in FET can be approximated as [37]

$$\overline{v_n^2} = \frac{K_f}{WLC_{ox}f}\Delta f \qquad (59)$$

where K_f is the flicker noise coefficient and C_{ox} is the oxide capacitance. Due to the buried channel conduction induced by the threshold adjust implant [41], the flicker noise coefficient of PMOS devices is lower than the corresponding coefficient of NMOS transistors. For this reason, it can be advantageous to employ PMOS instead of NMOS switches in an active CMOS downconversion mixer, in order to lower the flicker noise at the mixer output [84], [85]. In Fig. 34(a), a current-folding downconversion mixer utilizing PMOS switches is illustrated [4]. Besides utilizing the PMOS switching quad, the flicker noise at the mixer output can be lowered by scaling up the PMOS switch gate area $W \times L$ and by sharpening the transitions in the LO signal waveform by raising the LO amplitude. This can be accomplish, for instance, by utilizing CMOS inverters as LO buffers, which can provide almost rail-to-rail LO swing. In addition, as the RF input and switching FETs in the current-folding mixer can be biased at different currents, the bias current of the

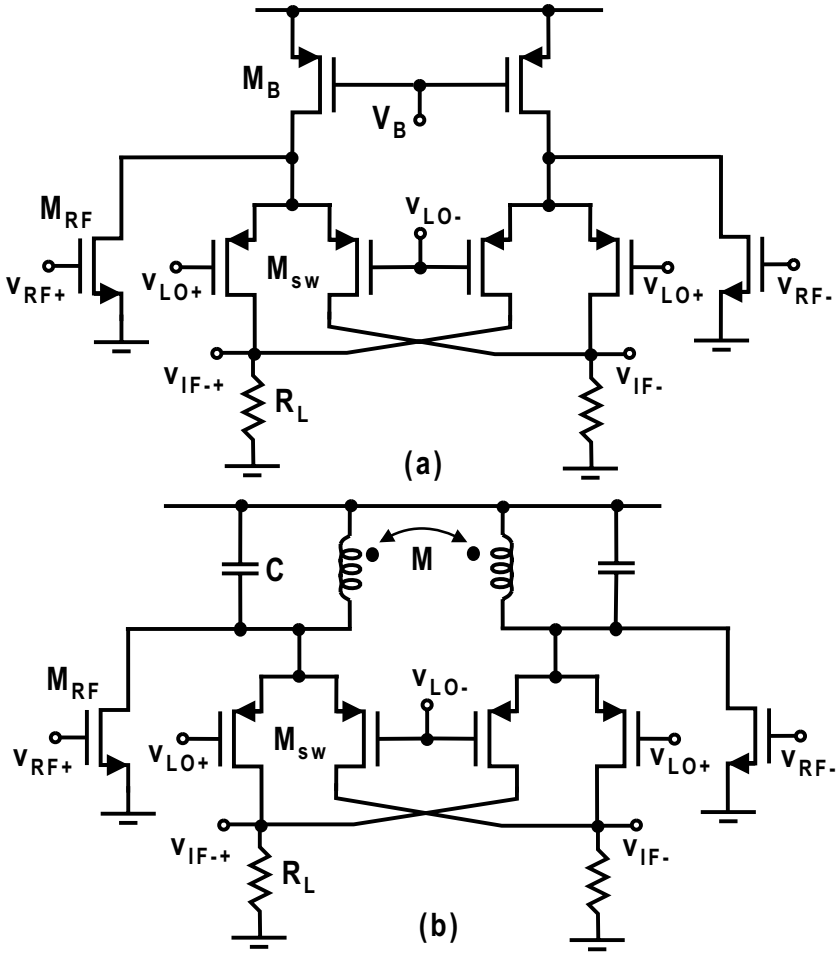

Figure 34: Folded CMOS downconversion mixer circuits.

switches can be reduced to lower the flicker noise at the output without altering the RF input bias. For the same reason, the mixer gain can be independently increased either by increasing the RF input stage g_m or R_L. However, as in a mixer with current boosting (see Fig. 33(b)), the white noise of the current source M_B adds to that of the RF input stage, increasing the mixer white noise factor significantly [4]. In particular, the white-noise DSB noise factor of the current-folded mixer shown in Fig. 34(a) can be approximated as

$$F_{DSB} = \frac{\pi^2}{8}\left(1 + \frac{\gamma_n}{g_m R_s} + \frac{\gamma_p g_{mB}}{g_m^2 R_s} + \frac{2\gamma_p I_{SW}}{g_m^2 R_s \pi A_{LO}} + \frac{1}{g_m^2 R_L R_s}\right) \tag{60}$$

where the third term is due to the channel thermal noise of M_B ($\overline{i_d^2} = 4kT\gamma_p g_{mB}\Delta f$) .

In order to operate properly at low supply voltage, PMOS current sources M_B shown in Fig. 34(a) must be biased at small or moderate $V_{eff,B}$, which unfortunately increases their thermal noise contribution at the mixer output ($\overline{i_d^2} = 4kT\gamma_p\Delta f(2I_B/V_{eff,B})$). In practice, the limited $V_{eff,B}$ of M_B results in a several-dB increase in the mixer white noise figure. In addition, the current sources introduce additional parasitic capacitance

at the common source of the switches, resulting in $1/f$ noise due to the switching quad translating indirectly to the output. Simulated in the 0.13-μm CMOS technology, the mixer shown in Fig. 34(a) achieves a gain of 10 dB, IIP3 of +5 dBm, and white-noise DSB-NF of 9 dB. The $1/f$ corner frequency lies at 246 kHz and the integrated DSB-NF of the mixer for GSM and WCDMA zero-IF receiver is 21 dB and 12 dB, respectively. The mixer consumes 4 mA from a 1.2-V supply.

Both the white noise due to the current sources and $1/f$ noise due to the indirect mechanism in the current-folding mixer (Fig. 34(a)) can be removed by replacing the current sources with an LC-tuned resonator, which provides a high-impedance at the RF operation frequency (Fig. 34(b)). The resulting LC-folded cascode mixer topology [86], [12], [Paper VI] is ideally suited for low-voltage operation, since, at the mixer input and output, only one and two devices consume voltage headroom, respectively. This allows the implementation of a 5-15 dB conversion voltage gain and improves the mixer linearity, since the headroom margin for the saturation condition for the transistors is increased. In addition, again the bias currents of the RF input and switching FETs can be optimized and chosen separately. In Fig. 34(b), an LC-tuned impedance, implemented by a differential inductor parallel resonating with the capacitor C and parasitics, provides a high-impedance at the desired RF frequency ω_{RF} and a low-impedance at the second-harmonic frequency $2\omega_{RF}$ and $2\omega_{LO}$ as well as at the low-frequency $\Delta\omega = \omega_{RF1} - \omega_{RF2}$ [12]. For this reason, the LC resonator simultaneously improves the mixer RF input stage IIP3 and filters out the IM2 distortion components $\Delta\omega$ generated at the mixer RF input stage. Finally, since the tail capacitance at the common-source node of the switching FETs at ω_{RF} is tuned out by the differential inductor (L_{md}), $1/f$ noise due to the indirect mechanism at the mixer output is significantly suppressed [51].

Simulated in the 0.13-μm CMOS technology, the LC-folded cascode mixer achieves a gain of 10 dB, IIP3 of +11 dBm, and white-noise DSB-NF of 6.2 dB. Its $1/f$ corner frequency is as low as 24 kHz. Accordingly, the integrated DSB-NF of the mixer for GSM and WCDMA zero-IF receiver is 10 dB and 6.4 dB, respectively. The mixer consumes 4 mA from a 1.2-V supply. It is concluded that, compared to the other mixers discussed, the LC-folded cascode mixer provides superior noise and linearity performance at low supply voltage.

4.3 Second-order intermodulation distortion in active downconversion mixers

As described earlier, one of the most difficult problem in zero- and low-IF receiver architectures is the envelope distortion due to the even-order nonlinearity [28], [42]. Many cellular systems require very high IIP2 performance if a direct conversion or low-IF receiver is to be used. In a well-designed receiver, the most dominant source of second-order intermodulation (IM2) distortion is the downconversion mixer. Usually the downconversion mixers are based on the double-balanced topologies, which generate a small amount of even-order distortion. Moreover, in an ideal mixer, the low-frequency beat present or generated at the mixer RF input is upconverted. Unfortunately, in reality, mixers present

a finite feedthrough from the RF input to the IF output, which results in a finite IIP2 [40].

As discussed in Section 4.1, most of the active double-balanced mixers utilized in wireless receivers are realized as Gilbert-type mixers [78]. In general, both the RF input transconductor and switching devices contribute to the mixer nonlinearity, and the mixer IIP2 is determined by the mixer second-order nonlinearity, mismatches, and offsets. As a conclusion, in order to maximize the mixer IIP2, it is essential to develop techniques for minimizing the IM2 products generated in the mixer, since the device matching and offsets cannot be improved beyond certain limits. On the other hand, in order to minimize the IM2 distortion due to the self-mixing, the RF-to-LO coupling has to be minimized and a sufficiently large LO amplitude has to applied [28].

4.3.1 IM2 distortion suppression techniques in mixer RF input transconductors

In a perfectly balanced mixer, stimulated and sensed differentially, the IM2 components at the mixer output are presented as common-mode signals with equal amplitude and are therefore cancelled. Unfortunately, in the presence of offsets and mismatches, the cancellation is not perfect, which results in finite mixer IIP2. If the second-order nonlinearity of the mixer switching devices is neglected, the IIP2 of a double-balanced mixer can be approximated as [42]

$$v_{IIP2} = \frac{\sqrt{2} \cdot v_{IIP2,g_m}}{\pi \eta_{nom}} \cdot \frac{4}{(2\Delta\eta(\Delta g_m + \Delta A_{RF}) + \Delta R(1 + \Delta g_m)(1 + \Delta A_{RF}))} \quad (61)$$

where η_{nom} is the nominal value of the duty cycle in a single-switch, $\Delta\eta$ is the mismatch in the duty cycles, Δg_m is the mismatch between the mixer RF input transconductances, ΔA_{RF} is the amplitude imbalance of the RF signal, ΔR is the imbalance of the mixer load resistances, and v_{IIP2,g_m} is the single-ended (or common-mode) IIP2 of the mixer RF input transconductor, measured from the single-ended output of the transconductor.

From Eq. (61), it is seen that due to the mismatch, for instance, in mixer load resistors and switching transistors, the IM2 currents generated by the RF input transconductor are directly transmitted or leaked to the mixer output. The corresponding direct leakage mechanism can be lowered by employing large-area switching transistors for better matching and by utilizing a large LO amplitude [28], [52]. On the other hand, the IM2 products generated by the RF input transconductor can also be transferred to the mixer output via an indirect mechanism that is induced by the parasitic capacitance at the common-emitter (or source) node of the switching stage [28] (see Fig. 35). Fortunately, both of these mechanisms can be, at least ideally, eliminated by minimizing the level of the common-mode IM2 components in the output current of the RF transconductor. Simultaneously, the matching requirement for the mixer output resistances can be lowered and the need for mixer IIP2 calibration [6] or trimming [42] can be reduced or even avoided.

The common-mode IM2 products generated in the mixer RF input transconductor can be eliminated, or at least, in practice, minimized in the presence of offsets [88], [89], by a fully differential RF input stage such as a differential pair [28]. Unfortunately, as the IIP3

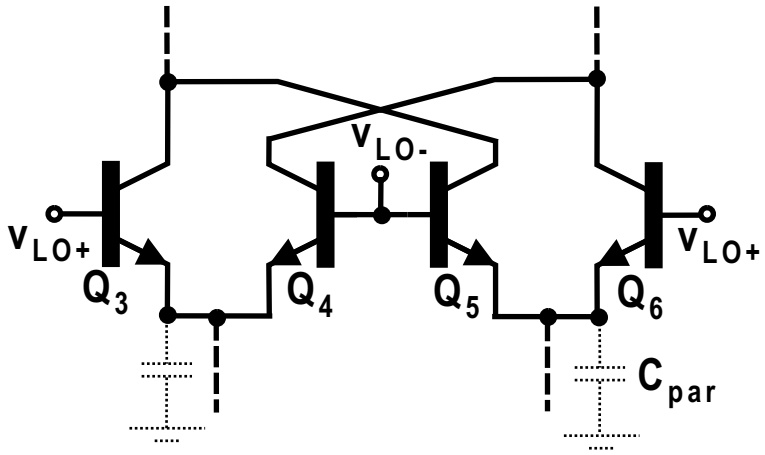

Figure 35: Parasitic capacitance C_{par} loading common-emitter node of switching pair.

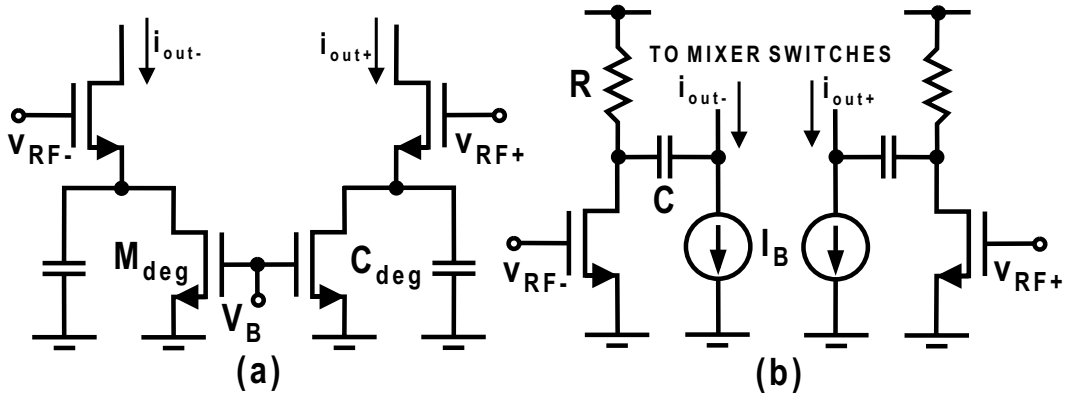

Figure 36: Circuit techniques to minimize the level of common-mode IM2 products generated at mixer RF input stage.

of the differential pair is worse than the IIP3 of the common-source (emitter) transconductor at a given bias [90] (see, for instance, Equations (37) and (38)), the common-source (emitter) RF input transconductor is usually preferred to the differential pair. Moreover, as supply voltage scales down with transistor technology, the realization of a Gilbert-type mixer with a differential pair RF input stage becomes difficult.

An RF input transconductor featuring a large degeneration resistance at low frequencies and a low degeneration impedance at RF operation frequency can simultaneously obtain a high IIP3 and a low level of IM2 components at its output current [92]. However, at low supply voltage, a large resistor cannot usually be used due to the voltage headroom limitations. Instead, as shown in Fig. 36(a), an FET biased in the triode region (M_{deg}) in parallel with a degeneration capacitance (C_{deg}) can realize the desired function. Nevertheless, M_{deg} still consumes some voltage headroom and its nonlinear output resistance may cause additional distortion.

The common-mode IM2 products generated in the mixer RF input transconductor can also be eliminated by ac-coupling the RF input stage from the switches [21], as illustrated in Fig. 36(b). Unfortunately, additional current sources (I_B) and load resistors (R) needed in the RF input stage increase the mixer noise factor and introduce additional parasitic capacitance at the common-node of the switching devices. This parasitic capacitance increases the second-order nonlinearity of the switching devices [28] and translates $1/f$ noise due to the switching quad indirectly to the mixer output [41].

For the reason that the common-source transconductor biased at a certain V_{eff} exhibits higher IIP3 than the differential pair at equal bias [90], most of the reported low-voltage CMOS downconversion mixers usually utilize the common-source transconductor as their RF input stage (see Fig. 37(a)) [2], [3], [4], [5], [90]. Unfortunately, the drawback of the common-source circuit is its second-order intermodulation characteristics. Namely, it is easy to show that if the common-source circuit is excited with two closely spaced RF signals with an equal amplitude $v_{RF}(t) = v_{in}\cos(\omega_1 t) + v_{in}\cos(\omega_2 t)$, the common-source circuit displays a common-mode IM2 component at the frequency of $f_1 - f_2$ at its output [Paper V]. In a perfectly balanced mixer, this common-mode component is cancelled in the mixer's differential output. However, in the presence of mismatches, the cancellation is not perfect. In particular, it can be shown that the IIP2 of the common-source RF input transconductor, measured at the single-ended transconductor output (i.e. i_{out+} or i_{out-} in Fig. 37(a)), can be approximated as [79], [Paper V]

$$v_{IIP2} = 2V_{eff}(1 + \theta V_{eff})(2 + \theta V_{eff}) \approx 4V_{eff} \tag{62}$$

which represents the differential RF input voltage. Both input FETs (M_1 and M_2) experience half of this voltage. Accordingly, in the sense of the entire mixer IIP2, the presence of the common-mode IM2 component at the output current is a clear drawback of the common-source RF transconductor.

Figure 37(b) illustrates a simple biasing circuit technique, which can be employed to cancel the IM2 distortion in the common-source transconductor [91], [Paper V]. In this circuit, the original bias transistor shown in Fig. 37(a) is divided into two equal-sized FETs half the size $W/(2L)$ of the original transistor. Moreover, the differential RF input signal is also applied to the gates of the bias FETs $(M_{B1}$-$M_{B2})$. Assuming that both the transconductors shown in Figures 37(a) and (b) employ equal sized FETs and bias currents, both transconductors provide an equal input stage g_m.

The operation principle of the IM2 cancellation technique shown in Fig. 37(b) can be understood by considering the IM2 product at the output current of the nonlinear transconductance, such as a single FET or BJT, which in general is given as [94]

$$i_{out+,\Delta\omega} = i_{NL2} + g_m v_{c,\Delta\omega} = K_{2_{g_m}} v_{c,\omega_1}^2 + g_m v_{c,\Delta\omega} = \frac{1}{2}\frac{\partial g_m}{\partial v_c} v_{c,\omega_1}^2 + g_m v_{c,\Delta\omega} \tag{63}$$

where g_m is the transconductance, v_c is the voltage (i.e. v_{GS} of FET) that controls the nonlinear transconductance, and $K_{2_{g_m}}$ is the second-order nonlinearity coefficient of the

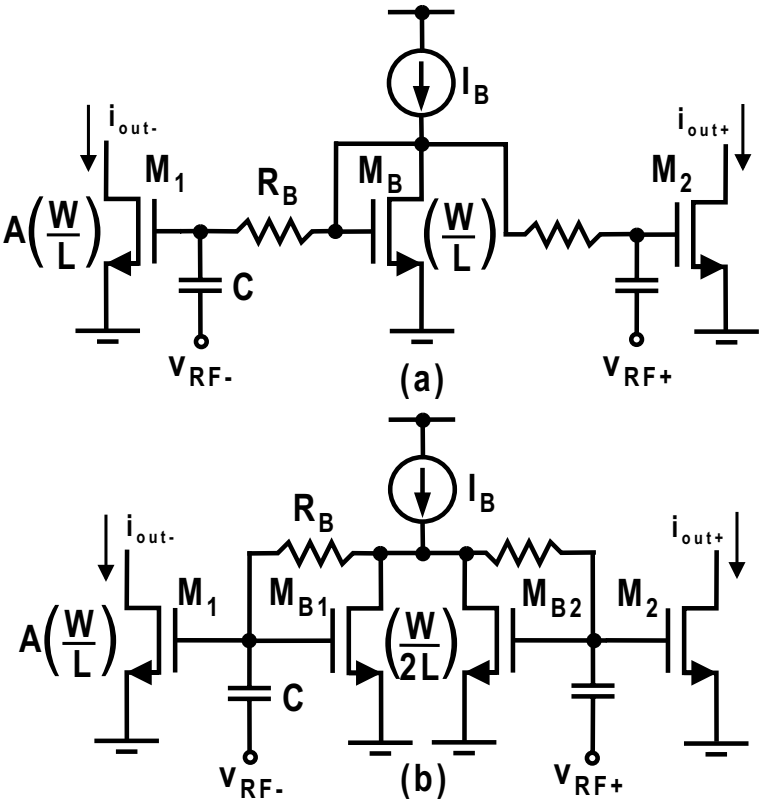

Figure 37: (a) Traditional common-source RF transconductor. (b) Biasing technique for cancellation of common-mode IM2 distortion in common-source circuit.

nonlinear transconductance. It is seen that $i_{out+,\Delta\omega}$ consists of two different components. The first component is due to $K_{2_{g_m}}$ of the transconductor. This term also depends on the value of the control voltage v_{c,ω_1} at the fundamental frequency ω_1. On the other hand, the value of the control voltage $v_{c,\Delta\omega}$ at $\Delta\omega$ also has effect on $i_{out+,\Delta\omega}$ via g_m, as seen from Eq. (63). Now, if by some means the value of $v_{c,\Delta\omega} = -i_{NL2}/g_m$ at $\Delta\omega$ can be generated, the IM2 component at the transconductor output can be cancelled. As a matter of fact, by applying a direct calculation of nonlinear responses [94], [Paper V], it can be shown that the bias circuit shown in Fig. 37(b) at $\Delta\omega$ generates the required control voltage $v_{c,\Delta\omega} = -i_{NL2}/g_m$, which cancels the common-mode IM2 component at the output of the common-source transconductor. The fact that the RF input transconductor shown in Fig. 37(b) does not display any common-mode IM2 components at its output is a clear improvement to the conventional common-source RF transconductor with respect to the IIP2 of the entire mixer.

The proposed IIP2 enhancement circuit has properties similar to the conventional differential pair in the sense that it ideally displays no IM2 distortion, provided that the transconductor is excited differentially and all the transistors in the circuit match with each other. However, as in the conventional differential pair, in the presence of offsets

and mismatches, a small residual IM2 distortion is generated [Paper V]. Nevertheless, on the contrary to the differential pair, the proposed transconductor circuit is very suitable for operation at low supply voltage, because it has only one device stacked between the transconductor input and output. In the conventional differential pair, two devices consume the voltage headroom. It is also easy to show that, for given bias and device dimensions (and thus for given RF input g_m), the proposed RF input transconductor has a noise performance equivalent to the traditional common-source transconductor [Paper V]. Finally, for given V_{eff}, the IIP3 of the proposed transconductor is slightly higher than the IIP3 of the differential pair transconductor. In particular, the IIP3 of the RF input stage shown in Fig. 37(b) can be approximated as [Paper V]

$$v_{IIP3} = \frac{4V_{eff}(1+\theta V_{eff})(2+\theta V_{eff})}{\sqrt{4+3\theta V_{eff}(2+\theta V_{eff})}} \approx 4V_{eff} \tag{64}$$

where the approximation holds for long-channel FETs (i.e. when $\theta V_{eff} \ll 1$).

From Eq. (64) it is seen that similarly as the IIP3 of the conventional common-source RF input transconductor (Fig. 37(a)), the IIP3 of the proposed transconductor (Fig. 37(b)) can be scaled up by biasing the input FET at larger V_{eff}.

Fig. 38 plots the simulated IIP3 of the proposed common-source transconductor (0.35-μm NMOSFET in 0.35-μm BiCMOS) versus the effective gate voltage, together with theoretical values ($\theta = 1.5\ V^{-1}$). The theoretical values are calculated from Eq. (64), as the corresponding power in dBm dissipated in a 100-Ω differential resistor. In addition, here the comparison between theory and simulation is made only for $V_{eff} \geq 300$ mV, because Eq. (48), used to derive Eq. (64), is a reasonable estimate for the drain current only in the strong inversion. For weak and moderate inversion, appropriate model for the drain current has to be applied [95]. Nevertheless, from Fig. 38 it is concluded that for $V_{eff} \geq 300$ mV in strong inversion, simulated values compare well with theoretical values.

The IIP3 of the proposed transconductor is larger than the IIP3 of the differential pair by a factor of $\sqrt{3(2+\theta V_{eff}(2+\theta V_{eff}))/(4+3\theta V_{eff}(2+\theta V_{eff}))}$ when biased at equal V_{eff} [Paper V]. At small V_{eff} ($\theta V_{eff} \ll 1$), the difference is about $\sqrt{3/2}$ i.e. 1.8 dB. However, at large V_{eff} ($\theta V_{eff} \gg 1$), the transconductors have approximately equal IIP3s. On the other hand, compared to the conventional common-source transconductor, the proposed RF transconductor has, by a factor of $\sqrt{(4+3\theta V_{eff}(2+\theta V_{eff}))/(3\theta V_{eff}(2+\theta V_{eff}))} \approx \sqrt{2/(3\theta V_{eff})}$ smaller IIP3 at a given bias, assuming $\theta V_{eff} \ll 1$. Notice that as V_{eff} is increased, the difference between the IIP3s of the conventional and proposed transconductors is decreased.

Figure 39(a) illustrates a conventional resistively degenerated common-emitter mixer RF input transconductance circuit. Suppose that the current mirror ratio is A as shown. The bias BJT (Q_{Bb}) provides base currents for the main bias BJT (Q_b) and RF BJTs (Q_1-Q_2). As in the conventional common-source circuit, the output current of the degenerated common-emitter RF transconductor displays a common-mode IM2 component, which is a

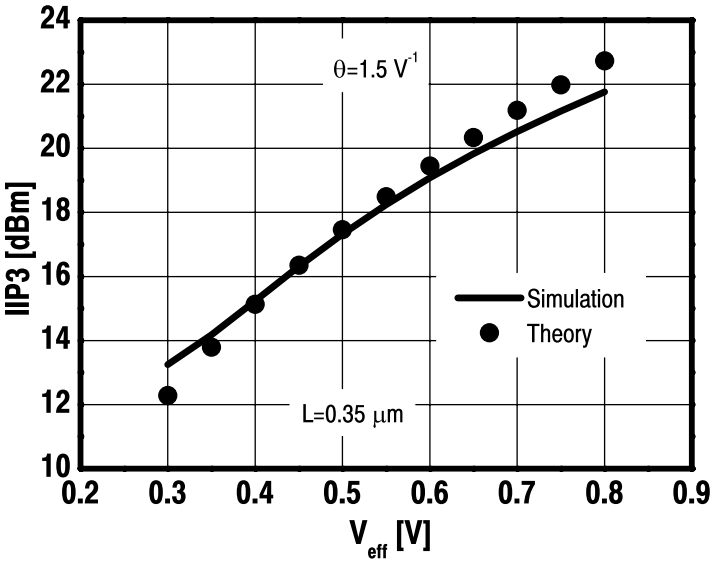

Figure 38: Theoretical (dots) and simulated (solid line) IIP3 versus effective gate voltage, $V_{eff} = V_{GS} - V_T$, for the proposed FET input transconductor.

drawback of the common-emitter RF input transconductor regarding the mixer IIP2. The IIP2 of the common-emitter transconductor, measured at the single-ended transconductor output, is given by [79]

$$v_{IIP2} = 4V_t(1 + g_m R_E)^2 \tag{65}$$

which represents the differential RF input amplitude. Feedback improves the degenerated common-emitter RF input transconductor second-order linearity compared to the transconductor without degeneration, but at the expense of the reduced input stage transconductance. Moreover, the feedback does not totally remove the IM2 distortion.

The biasing circuit technique that was employed to cancel the IM2 distortion in the FET transconductor can also be employed to cancel the IM2 distortion in the resistively degenerated common-emitter circuit (see Figure 39(b)). Again, the original bias BJT shown in Fig. 39(a) is divided into two equal-sized bias BJTs half the size of the original BJT. The values of the emitter resistances are doubled. Although the proposed BJT transconductor is presented with degeneration, the biasing technique also applies to the common-emitter circuit without degeneration.

The proposed BJT transconductor circuit shown in Fig. 39(b) operates exactly the same as its FET counterpart. Thus, provided that the transconductor is excited differentially and all the devices in the circuit match with each other, the output current of the proposed BJT RF input transconductor does not display any common-mode IM2 components. Again, this is a significant improvement on the conventional common-emitter RF transconductor.

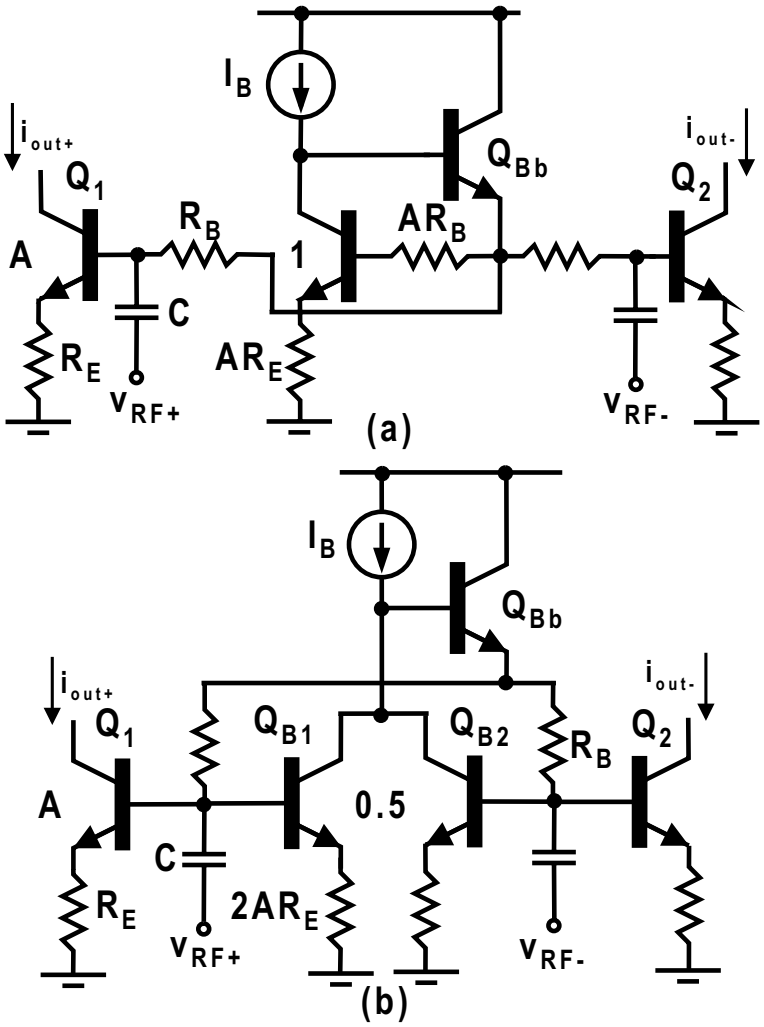

Figure 39: (a) Traditional resistively degenerated common-emitter RF transconductor. (b) Biasing technique for cancellation of common-mode IM2 distortion in common-emitter circuit.

The IIP3 of the proposed BJT transconductor shown in Fig. 39(b) can be estimated as [Paper V]

$$v_{IIP3} = 4\sqrt{2}V_t \frac{(1+g_m R_E)^2}{\sqrt{1+2g_m R_E}} \tag{66}$$

As the IIP3 of the conventional degenerated common-emitter RF input transconductor shown in Fig. 39(a), the IIP3 of the proposed transconductor (Fig. 39(b)) can be improved by increasing the loop gain of the negative feedback, i.e. scaling up I_C or R_E.

Fig. 40 plots the simulated IIP3 of the proposed BJT input transconductor, realized in 0.35-μm BiCMOS, versus the collector biasing current, together with theoretical values ($R_E = 40\ \Omega$). The latter are calculated from Eq. (66), as the corresponding power in

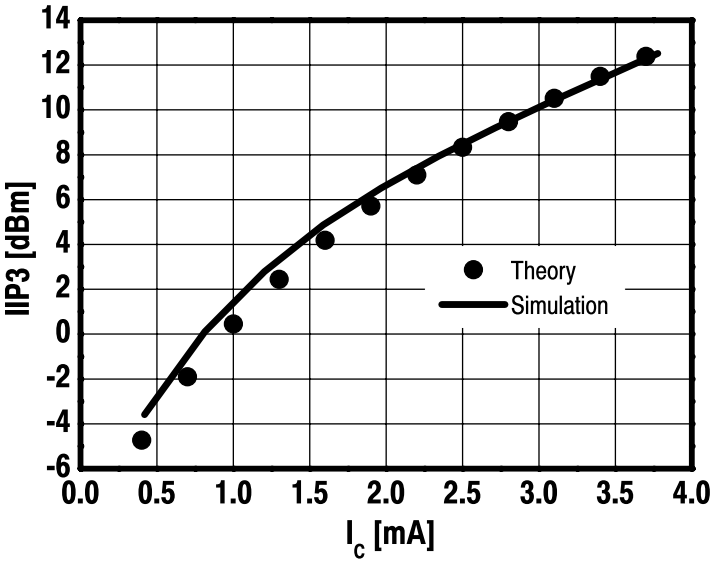

Figure 40: Theoretical (dots) and simulated (solid line) IIP3 versus collector current, for the proposed BJT input transconductor.

dBm dissipated in a 100-Ω differential resistor. A good agreement between simulation and theory is evident.

The IIP3 of the proposed degenerated common-emitter RF transconductor is higher by a factor of $\sqrt{2(1+g_mR_E)/(1+2g_mR_E)}$ than the corresponding IIP3 of the degenerated differential pair given by Eq. (37). The difference between the IIP3 of the proposed approach and differential pair transconductor is at the largest $\sqrt{2}$ i.e. 3 dB corresponding to no feedback or $R_E = 0$. With a very large feedback loop gain ($g_mR_E \gg 1$), the transconductors have approximately equal IIP3s.

The IIP3 of the degenerated common-emitter RF transconductor shown in Fig. 39(a) is higher by a factor of $\sqrt{(1+2g_mR_E)/|1-2g_mR_E|}$ than the corresponding IIP3 of the presented approach. On the other hand, if $g_mR_E \ll \frac{1}{2}$ or $g_mR_E \gg \frac{1}{2}$, the transconductors have approximately equal IIP3. Finally, as with CMOS, the proposed BJT transconductor is more suitable for operation at low supply voltage than the traditional BJT differential pair.

4.3.2 Nonlinearity in switching stage

As described in the previous section, the IM2 products generated at the mixer RF input transconductor can be, at least ideally, eliminated by utilizing several well-known techniques. However, besides the RF input stage, the IM2 products are generated by the nonlinearity in the switching stage [28]. At low frequencies, the dominant nonlinearity

effect of the transistors in the switching differential pair is the signal-dependent current division between the commutating transistors [51]. Nevertheless, at low frequencies the switching stage usually gives rise to negligible IM2 products at the mixer output. However, at high frequencies, the second-order nonlinearity of the switching pair is degraded significantly due to the parasitic capacitance at the common-emitter (or source) node of the switching stage (see Fig. 35) [28]. Accordingly, the second-order nonlinearity due to the switching transistors can be lowered by biasing the given-sized switching quad at a sufficiently large biasing current [28] and possibly tuning out the parasitic capacitance (C_{par}) at the frequency of interest by an inductor with the same impedance at f_{LO} [92].

4.3.3 Calibration techniques

Besides the techniques described above to improve the IIP2 of the downconversion mixer, the IM2 characteristics can be enhanced by means of calibration techniques. For instance, the IIP2 can be trimmed by controlling the load resistor of the RC-loaded Gilbert-type mixer by applying a controllable resistor matrix at the mixer output [96]. Unfortunately, the drawback of this technique is the deterioration of the IIP2 at the baseband frequency. However, by tuning the load capacitors as well as the load resistors, a high IIP2 can be maintained over the entire baseband channel [97]. Finally, the IIP2 can also be trimmed, for instance, by introducing an intentional asymmetry (i.e. digitally programmable) into the mixer in order to null blocker-induced dc offsets, thereby canceling the IIP2 [6], or by applying a deliberate dc offset at the LO stage to compensate the inherent mismatches presented in the mixer [16].

5 Interface Issues in RF Front-End

In RFIC design, interface issues are very important. Accordingly, since in the RF front-end different blocks have a strong effect on each other, these circuits have to be designed and simulated together. In addition, the interfaces to the circuits preceding and following the RF front-end have to be modeled and simulated properly. Only in this way, can an optimum performance be achieved in practice.

5.1 Preselect filter-LNA

As described earlier, the input impedance of the LNA has to be designed to match the characteristic impedance, e.g., 50 Ω, of the external preselect or duplex filter (see Fig. 1). Moreover, as the parallel capacitance C_p due to the package and ESD parasitics drastically lowers the input impedance level of the inductively degenerated common-emitter (source) LNA, an impedance transformation network, in general, is needed to transform the LNA input impedance upwards. Moreover, if the real part of the impedance looking into the base or gate of the LNA input transistor (see for instance R_{ing} in Fig. 13) is very low compared to the source impedance R_s, an impedance transformation network with a large scaling factor is required accordingly. Unfortunately, when scaling the impedance by a large factor, the required Q factor of the matching circuit grows quadratically and the LNA input matching becomes sensitive to parasitics, process and component variations [36]. This will also result in narrow-band input matching (i.e. in a bandwidth for which $S_{11} < -10$ dB). Thus, for this reason, it is important to provide sufficiently large real part of the impedance looking into the base or gate of the LNA input transistor by an appropriate circuit design.

Figure 41 illustrates two possible ways to implement the input impedance matching network of the inductively degenerated common-source LNA. It is assumed that, due to the package and ESD parasitics, the LNA input impedance needs to be transformed upwards. Moreover, usually the requirement for the LNA noise factor dictates that the matching components need to be realized as external high-Q elements. In Fig. 41(a), the matching network is implemented with series inductors and a parallel capacitor, whereas, in Fig. 41(b), a parallel inductor and series capacitors realize the input matching, respectively. Since off-chip lumped capacitors are usually cheaper than the corresponding inductors, the matching network shown in Fig. 41(b) results in lower cost. Moreover, the matching network shown in Fig. 41(b) automatically ac-couples the LNA input from the preceding balun or filter. If the ac-coupling is required, the matching network illustrated in Fig. 41(a) needs additional series capacitors for this purpose.

5.2 LNA-downconversion mixer

In zero- and low-IF receivers, LNA typically drives I and Q mixers directly on-chip. However, if for some reason an external bandpass filter must be utilized between the LNA and mixer [16], both the LNA output and mixer input need to be matched to the characteristic impedance of the filter. Nevertheless, in the case of direct on-chip connection between

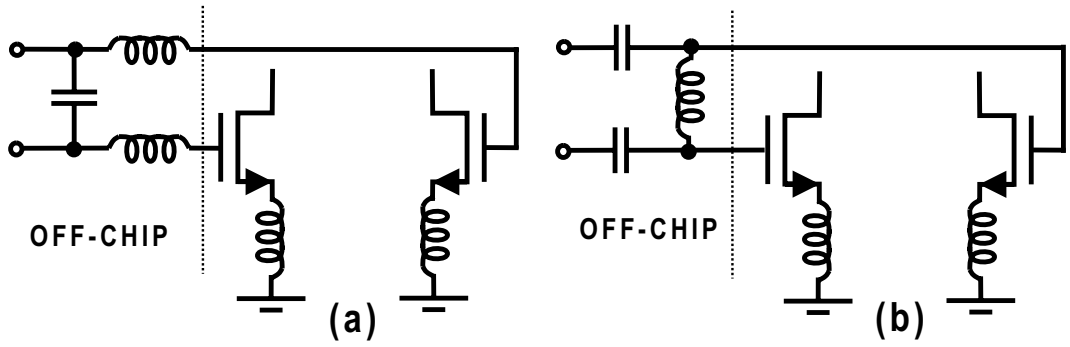

Figure 41: LNA input matching networks.

the LNA and mixer, the LNA-mixer interface usually operates in the voltage domain, i.e. both the LNA output and the mixer input employ voltage-mode signal processing. Moreover, in most cases, it is beneficial to utilize ac-coupling at the interface. This way the low-frequency IM2 distortion generated in the LNA can be filtered out and the dc-levels at the LNA output and at the mixer input can be set independently.

The input stage of the inductively degenerated common-source LNA provides its output signal in current domain. Moreover, since the switching quad of a Gilbert-type mixer also commutes current, translating it in frequency, these circuits can be cascaded in current [51]. Eliminating the voltage-to-current conversion at the mixer RF input stage also removes the associated source of nonlinearity. Accordingly, the resulted current-mode cascade LNA and mixer, or simply a low-noise mixer, can possibly achieve higher linearity than a conventional LNA and mixer cascaded in the voltage domain.

In a zero- or low-IF receiver, the LNA must drive two mixers to produce quadrature outputs. With the LNA and mixer cascaded in the current domain, this can be realized by coupling the differential LNA into the tails of two commutating differential pairs in parallel, which together comprise two double-balanced mixers [51] (see Fig. 42). The voltage conversion gain of the low-noise mixer shown in Fig. 42 can be approximated as

$$A_v = \frac{1}{2} \cdot \frac{2}{\pi} \cdot G_{m,LNA} R_L = \frac{G_{m,LNA} R_L}{\pi} \tag{67}$$

where $G_{m,LNA}$ is the input stage transconductance of the LNA and the factor of $(1/2)$ results from the fact that the LNA drives two mixers in parallel. The voltage gain of the conventional RF front-end utilizing the voltage-mode interface between the LNA and mixers is given by

$$A_v = G_{m,LNA} R_{L,LNA} \cdot \frac{2}{\pi} \cdot G_{m,mixer} R_{L,mixer} \tag{68}$$

where $R_{L,LNA}$ is the LNA load impedance at the RF frequency, $G_{m,mixer}$ is the mixer RF input stage transconductance, and $R_{L,mixer}$ is the mixer load resistance. Eq. (68) assumes that I and Q mixers have their own RF input stage. By comparing Equations (67) and (68),

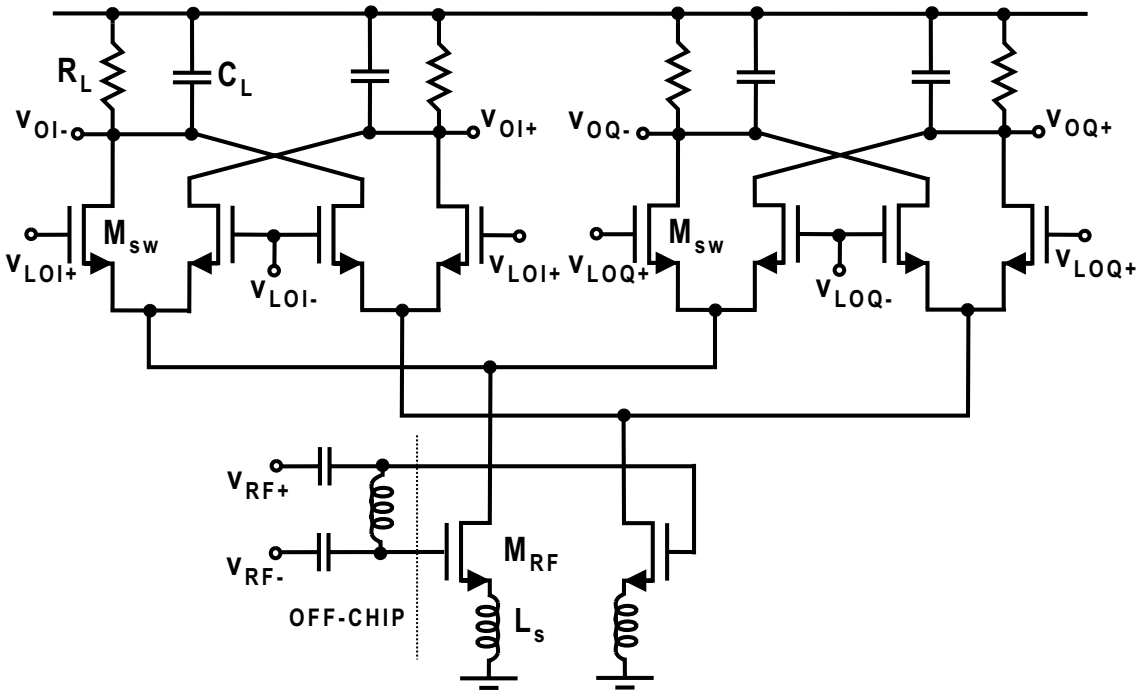

Figure 42: Differential LNA merged with quadrature mixers.

it is seen that, for a given $G_{m,LNA}$ and $R_{L,mixer}$, the front-end with voltage-mode interface provides by an amount of $2 \cdot G_{m,mixer} R_{L,LNA}$ larger voltage gain compared to the low-noise mixer. Moreover, the gain of the low-noise mixer can only be increased either by increasing $G_{m,LNA}$ or $R_{L,mixer}$. For these reasons, the low-noise mixer can usually provide only a limited amount of voltage gain, in practice, below 25 dB [51]. Unfortunately, in cellular receivers, this amount of RF front-end voltage gain is not usually sufficient to suppress the noise contribution of the analog baseband [53].

5.3 Quadrature generation

Direct conversion transmitters and receivers (as well as low-IF receivers) need a local oscillator with quadrature outputs for vector modulation and demodulation, respectively [19]. Usually, quadrature LO signals needed to drive I and Q mixers are generated either by a quadrature VCO [98], passive polyphase filter [29], or by a divide-by-two circuit consisting of two cross-clocked D flip-flops [40].

In a direct conversion transceiver, the required LO coincides in frequency with the large modulated signal at the transmitter (or power amplifier (PA)) output. Accordingly, the PA may disturb the VCO frequency, resulting in an effect known as LO pulling by the PA [40]. Moreover, since the LO quadrature generation methods relying on the quadrature VCO and polyphase filter are most straightforwardly realized with the VCO running at the final LO frequency, these techniques are usually susceptible to LO pulling. On the other hand, if the quadrature VCO is realized, for instance, at two-thirds of the LO fre-

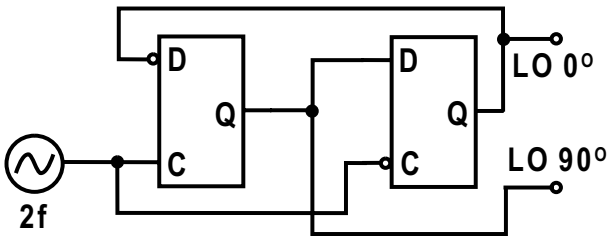

Figure 43: Block diagram of divide-by-two circuit.

quency to prevent the PA from pulling the VCO, an additional divide-by-two circuit and mixers required to produce quadrature signals at the final LO frequency increase the complexity, silicon area, current consumption, and cost [99]. Moreover, a quadrature VCO requires twice as many inductors than a differential single-phase VCO.

Balanced quadrature LO signals can also be generated by utilizing a differential oscillator running at the final LO frequency in combination with a differential-to-quadrature converting polyphase filter [4]. Often, at least a second-order polyphase filter has to be applied to provide sufficient I/Q accuracy over a bandwidth of interest and to guarantee safety margin against process and temperature variations. Unfortunately, higher-order filters have large attenuation and they consume a larger amount of power in buffers at the VCO-polyphase interface [100]. Moreover, since the amplitudes of the I and Q LO signals are equal only at the pole frequency, limiting LO buffers are also needed at the polyphase-mixer interface. Finally, since polyphase structure is frequency-selective and every separate band therefore needs its own filter, the use of polyphase filters in multi-mode or multi-band receivers is difficult or impractical [50] and die-area consuming.

Figure 43 illustrates a simple approach for generating quadrature LO signals for I and Q mixers [40]. Here, a pair of source-coupled D flip-flops in a ring clocked by the double-frequency VCO realizes divide-by-two and produces the desired LO frequency with quadrature phases. Provided that the differential input signal has a 50% duty cycle, the differential output signals are 90^0 out of phase. Moreover, since this architecture utilizes VCO running at two times the LO frequency, the pulling effect is avoided. In addition, since one divide-by-two circuit can be employed for generating quadrature LO signals for several frequency bands, a frequency divider-based quadrature generator is ideally suited for multi-mode or multi-band receivers [50]. As shown in Fig. 44, latches in the divide-by-two circuit can be realized, for instance, by utilizing source-coupled FET logic (SCL) (or, equivalently, emitter-coupled BJT logic (ECL)). An SCL-based divide-by-two circuit can be realized even at low voltage (i.e. in 0.13-μm CMOS technology with 1.2-V supply voltage), because, in an SCL latch, it is acceptable to force a CMOS switch into the triode region [36].

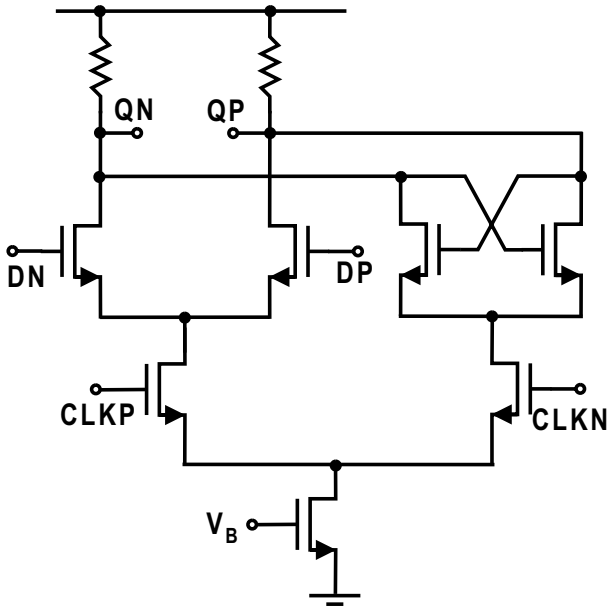

Figure 44: Circuit of single latch.

5.4 LO circuitry-downconversion mixer

A switching quad in a double-balanced downconversion mixer should be driven by a sufficiently large LO amplitude signal to minimize its white noise contribution (see for instance Eq. (47)). Moreover, since sharp transitions in the LO waveform lower the distortion and flicker noise due to the mixer switches [31], it is also, in this sense, beneficial to raise the amplitude of the LO signal to sharpen the transition. Finally, a large LO amplitude also lowers the direct leakage mechanism of the IM2 products, generated at the mixer RF input stage, to the mixer output [28], [52]. Nevertheless, the LO amplitude should not be arbitrary large. First, in a mixer with BJT switches, a very large LO amplitude may result in excessive current being pumped into to the common-emitter node of the switching quad, producing additional third-order intermodulation [76]. On the other hand, in a low-voltage CMOS mixer, a too large LO amplitude will force the switch FETs into the triode region and degrade the mixer linearity due to the nonlinear mixer output resistance. Finally, although the BJT switching quad in general requires a much lower LO voltage swing to experience complete switching than does an FET counterpart [40], mixers in both technologies practically always require an LO buffer to guarantee an appropriate LO signal to drive the capacitive load of the switching devices. Moreover, although LC-tuned LO buffers can be employed to tune out the capacitive load seen at the mixer LO input, and therefore to save power in the LO buffers, integrated inductors consume silicon area and should therefore be avoided, if possible.

Figure 45 illustrates a so-called totem-pole circuit [101], which can be employed as an LO buffer to drive the capacitive load of a BJT switching quad. The totem-pole circuit combines the advantages of emitter-follower and common-emitter circuits. It is a well-known

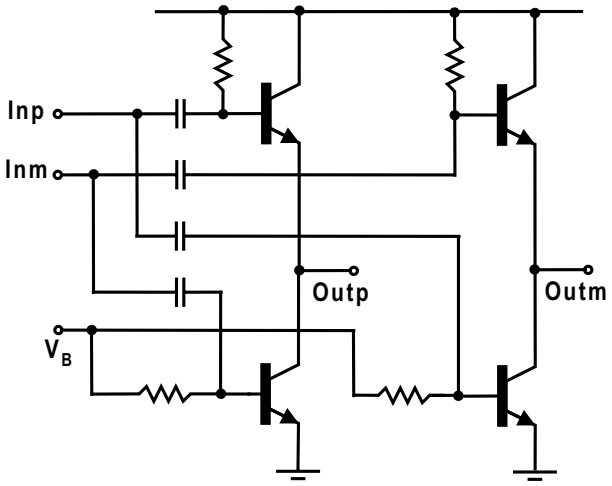

Figure 45: BJT LO buffer based on totem-pole circuit.

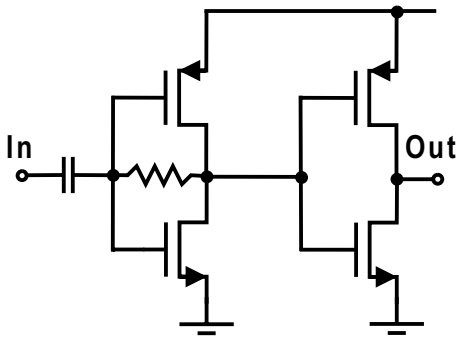

Figure 46: CMOS LO buffer based on cascade of CMOS inverters.

fact that the common-emitter amplifier provides fast discharging of load capacitance but rather slow charging. On the other hand, the opposite is obtained in the emitter-follower amplifier. Thus, an optimum stage to drive the load capacitance is the combination of the common-emitter and the emitter-follower configurations.

In CMOS technology, a chain of CMOS inverters can be utilized to achieve an almost rail-to-rail LO swing to drive the capacitive load of the FET switches (see Fig. 46). In Fig. 46, the input of the first inverter is biased at an optimum dc voltage to guarantee a rail-to-rail output voltage swing, even in the absence of a rail-to-rail input swing.

5.5 Downconversion mixer-analog baseband

Traditionally, a downconversion mixer-analog baseband interface has been realized in the voltage domain, i.e. the downconverted IF current has been converted to the IF voltage at the mixer load [78]. Moreover, often it is beneficial to improve the mixer out-of-band blocking characteristics and the linearity of the preceding analog baseband circuit by uti-

lizing a passive RC-impedance at the mixer output. Unfortunately, as the supply voltage scales down with transistor technology, the effect of the nonlinear mixer output resistance to the mixer linearity becomes increasingly important and this effect is emphasized at the voltage-mode interface. Moreover, since the mixer output node usually experiences the largest voltage swing in the RF front-end (assuming the mixer has a conversion gain), at low voltage, the signal clipping at the mixer output usually determines the RF front-end compression point.

To improve the mixer linearity and its blocking characteristics at low supply voltage, a current-mode instead of voltage-mode signal processing can be utilized at the mixer output [4], [Paper VI]. Figure 47 illustrates this concept. The PMOS switching quad downconverts the RF current to the baseband, and the differential-mode mixer output current is driven to the feedback loop of the RC integrator (transimpedance amplifier). The common-mode current of the mixer is sinked by the CMFB current source FETs (M_{cmfb}). The transimpedance amplifier low-pass filters the mixer differential-mode output current and converts it back to voltage. High-gain operational amplifiers (op-amps) shown in Fig. 47 can swing rail-to-rail at minimum distortion. Moreover, the transimpedance amplifier has a high common-mode rejection. This is essential in a direct conversion receiver because, after downconversion, the common-mode IM2 distortion generated in the mixer must be blocked before it becomes differential as a result of a device mismatch at the baseband [102].

The op-amp in the negative feedback loop [4] provides a virtual ground at the mixer output (see nodes 'OP' and 'ON' in Fig. 47). Thus, ideally there is no voltage swing present at the mixer output. Moreover, since there is no voltage swing at the drain of the switching devices (M_{sw}), the nonlinearity due to the switches is minimized and the blocking characteristics of the mixer are significantly improved.

The current-mode interface needs a CMFB circuit to operate properly. Unfortunately, without the dynamic matching technique, the CMFB FETs M_{cmfb} add uncorrelated flicker noise at the mixer output, which, in practice, can dominate the mixer low-frequency noise. For the same reason, the use of the entire current-mode interface is often disqualified. Scaling up the FET gate area $W \times L$ lowers the flicker noise, but this increases the gate-source capacitance of M_{cmfb} and worsens the stability of the CMFB circuit.

As shown in Fig. 47, the flicker noise of M_{cmfb} can be suppressed by applying a dynamic matching or chopper stabilization technique [64], [103], [Paper VI]. Earlier, the dynamic matching, in the context of downconversion mixers, has been used to reduce the flicker noise generated in the actual mixer core [77]. In effect, one mixer preceding, and a second one following, the main mixer core have been used to boost the IIP2 and to lower the flicker noise of the main mixer core. On the contrary, here dynamic matching technique is used to reduce the flicker noise of the mixer common-mode load, rather than the mixer core itself directly.

In Fig. 47, dynamic matching is utilized as follows. Transistors M_{ch}, operating as switches,

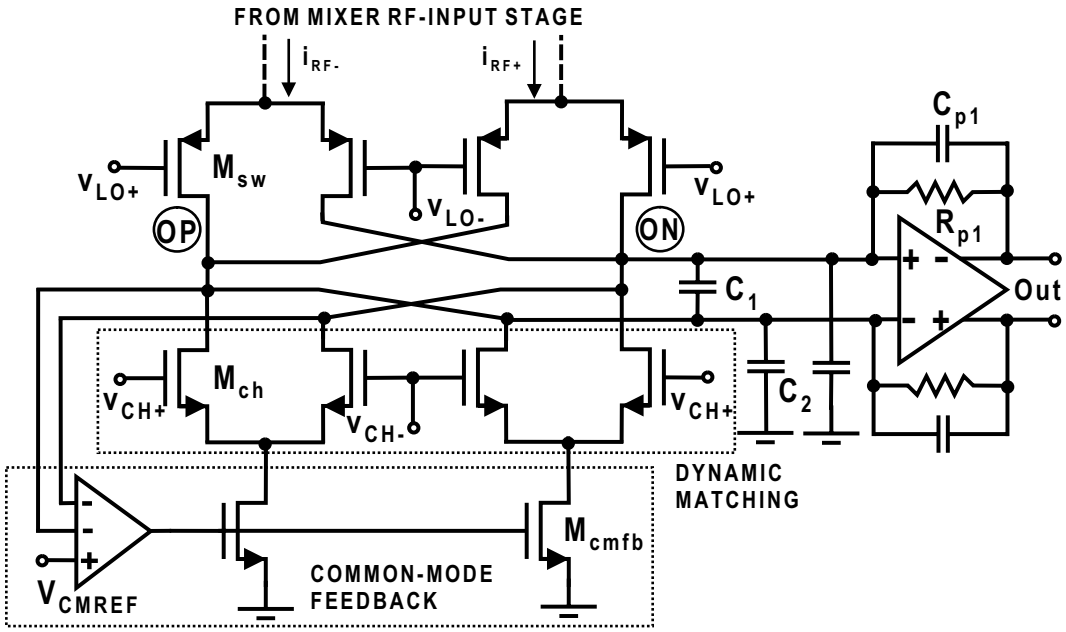

Figure 47: Current-mode downconversion mixer-analog baseband interface.

are driven by rail-to-rail signals v_{CH+} and v_{CH-} in antiphase at the chopper frequency. Signals v_{CH+} and v_{CH-} can be generated from the LO signal by a frequency division, and a reasonable choice might be, for instance, $f_{CH} = f_{LO}/16$ [Paper VI]. Thus, FETs M_{ch} essentially form an upconversion mixer, which upconverts the flicker noise of CMFB FETs M_{cmfb} to the chopper frequency, and therefore outside the signal band of interest. Moreover, since the differential-mode interference signals at the mixer output do not flow through the CMFB circuit, the switching quad (M_{ch}) does not downconvert the interference signals to the signal band of interest. In addition, by driving the switches M_{ch} by a large amplitude square wave at the relatively low-frequency to a deep triode region, their voltage headroom consumption and noise contribution can be made insignificant. Finally, without the dynamic matching, the mismatch in FETs M_{cmfb} would directly effect the RF front-end IIP2 and dc offset. However, by applying the chopper stabilization, both of these effects due to the mismatch in M_{cmfb} are suppressed. It can also be shown that the dynamic matching has no effect on the white noise contribution of M_{cmfb} to the mixer output noise [Paper VI].

An active filter very often contributes the largest noise of all the building blocks in an integrated direct conversion receiver [2]. However, the noise contribution of the filter can be minimized by utilizing a current-mode interface between the downconversion mixer and filter, or by employing a filter with a current-mode input stage (i.e. a transimpedance amplifier). For instance, if the input-referred noise voltage of the op-amp in the transimpedance amplifier shown in Fig. 47 is $v_{n,in}$, its output noise voltage at the filter passband is given as $v_{n,out} = (1 + R_{p1}/R_{out,m}) \times v_{n,in}$ where $R_{out,m}$ is the parallel output impedance of the mixer and CMFB circuit. If $R_{p1} << R_{out,m}$ then $v_{n,out} \approx v_{n,in}$. Thus,

the input-referred noise voltage of the op-amp experiences no voltage gain from the op-amp input to the op-amp output. On the contrary, in a filter with a voltage-mode input stage, the corresponding noise voltage gain can be significant.

The current-mode interface between the mixer output and analog baseband input is also very beneficial regarding to the offset voltage of the op-amp in the transimpedance amplifier. Similarly, as the input-referred noise voltage, the input-referred offset voltage of the op-amp in the transimpedance amplifier experiences no voltage gain to the op-amp output. Again, in a filter with a voltage-mode input stage, the corresponding gain can be significant.

As described above, the differential-mode mixer output current is injected to the feedback loop of the first RC integrator. Ideally, the differential-mode input impedance $(Z_{in,ta})$ of the transimpedance amplifier should be as small as possible to ensure a maximum transfer of current from the mixer output to the transimpedance amplifier output. However, $Z_{in,ta}$ is small only in the frequency range where the open loop gain of the op-amp shown in Fig. 47 is high [104]. The op-amp must therefore be designed for high-frequency operation. The blocker signals at the frequencies beyond the op-amp gain-bandwidth product (GBW) can be attenuated by the capacitors C_1 and C_2 at the mixer output. In addition, they prevent the op-amp from slewing due to the high-frequency mixer output signals. Finally, capacitors C_2 determine the dominant pole of the CMFB circuit.

As a conclusion, compared to the traditional voltage-mode interface between the down-conversion mixer output and analog baseband input, the current-mode interface improves the receiver performance in several ways. Firstly, since there is no voltage swing at the mixer output, the nonlinearity due to the mixer switching devices is minimized and the mixer blocking performance is improved. The current-mode interface also minimizes the noise contribution of the analog baseband in such a way that it requires only a moderate voltage gain (or transconductance) in the LNA and mixer. Both of these issues are very essential when operating at low supply voltage. Nevertheless, to operate properly, the current-mode interface requires a CMFB circuit. A drawback of a conventional CMFB circuit is its large flicker noise, which, in practice, can dominate the entire mixer low-frequency noise and prevent the use of the current-mode interface. However, by utilizing the dynamic matching technique at the interface, the flicker noise of the CMFB circuit can be suppressed and the use of the entire current-mode interface can be enabled.

6 Summary and Conclusions

In this thesis, the design, analysis, and optimization of RF front-ends for wireless receivers with CMOS and BiCMOS technologies are studied. The research concentrates on direct conversion and low-IF radio receiver architectures, because typically these receiver topologies allow the highest level of integration. Usually, the RF front-end, especially the LNA and mixer, limits the performance of the entire zero- and low-IF receiver. In this work, the emphasis is on the challenges posed by mass production to the design of integrated RF circuits.

In order to protect the circuits from mechanical stress and to ease the automatic soldering of chips to PCB, commercial RFICs must be mounted in a package and for reliability reasons, off-chip interfaces must be protected by ESD protection structures. In the circuit design for RF frequencies, the package and ESD parasitics have a significant effect on the circuit performance and in general, these parasitics do not scale down with technology. In this work, it is shown that the equivalent parallel parasitic capacitance C_p due to the ESD and package parasitics drastically lowers the achievable input impedance Z_{in} level of the inductively degenerated common-emitter (source) LNA, which is the most popular LNA architecture. In order to transform Z_{in} upwards to the source impedance R_s, a passive impedance matching network can be utilized at the amplifier input. However, an impedance matching network with a high impedance scaling factor can make the LNA input matching sensitive to process and component variations. The matching network also amplifies the incident voltage and lowers the noise contribution due to the active device at the LNA input. In fact, in an LNA with a sufficiently high device f_T and voltage gain in the matching network, the LNA noise factor can be dominated by the losses of the input matching network instead of active device noise. However, very high insertion gain in the matching circuit lowers the IIP3 of the amplifier and may not actually even lead to the minimum achievable noise factor. Instead, the minimum noise factor of the inductively degenerated common-source sub-micron LNA can be found when both the matching circuit and the active device at the LNA input contribute an equal amount of noise to the amplifier output.

In order to maximize the yield of receiver RFIC, the circuit performance must be stabilized against process, temperature, and supply voltage variations. For this purpose, appropriate circuit techniques and biasing methods must be utilized. Moreover, in order to reduce the variations of the receiver dynamic range due to the temperature and process variations, it is shown that it is very important to stabilize the gain of the LNA. In particular, to regulate the voltage gain of the inductively degenerated LNA against variations, the magnitude of the LNA load impedance ($|Z_L(\omega_0)|$) must be stabilized against variations. To achieve this, a gain stabilization technique for tuned integrated LNAs is proposed in this thesis. The proposed method is shown to regulate the LC-tuned load impedance of the amplifier at the operation frequency against variations of passive devices in the IC process. The impedance stabilization technique is based on the excellent relative accuracy of integrated resistors. By applying the proposed method, the voltage gain variation of the inductively degenerated LNA is shown to be reduced several decibels. As a conse-

quence, the entire radio receiver can more easily meet its specifications in the presence of IC process variations and the product yield is improved.

One of the most limiting problem in zero- and low-IF receivers is the envelope distortion due to the even-order nonlinearity. Usually, in a zero- or low-IF receiver, the most dominant source of IM2 distortion is the downconversion mixer. Moreover, in general both the RF input transconductor and switching devices contribute to the mixer nonlinearity, and the mixer IIP2 is determined by the mixer second-order nonlinearity, mismatches, and offsets. As a conclusion, in order to maximize the mixer IIP2, it is essential to develop techniques for minimizing the IM2 products generated in the mixer, since the device matching and offsets cannot be improved beyond certain limits. To enhance the IIP2 of the mixer, a new biasing technique for cancelling the IM2 distortion generated in the common-source or common-emitter mixer RF input stages is proposed in this thesis. The proposed circuit can be utilized as an RF input transconductor in double-balanced downconversion mixers. It is shown that the proposed approach increases the yield of the entire radio receiver by enhancing the mixer IIP2. The presented circuit displays ideally no IM2 distortion, provided that the transconductor is excited differentially and all the transistors in the circuit match with each other. Moreover, in this circuit, no extra noise sources in practical cases of interest are added in the mixer and no integrated inductors are required, which results in a small die area. Finally, the presented circuit is also more suitable for operation at low supply voltage than for instance a conventional differential pair, because it has only one device stacked between the transconductor input and output. The IIP3 of the proposed circuit is slightly higher than the IIP3 of the differential pair at given bias.

Down-scaling of supply voltage with transistor technology poses challenges for the analog and RF circuit design. The challenge is how to achieve a large dynamic range and comply with circuit specifications, which do not relax as the process scales down. In practice, low supply voltage limits the upper end of the dynamic range determined by the circuit's linearity and prevents stacking of several devices. In addition to low supply voltage, $1/f$ noise present in sub-micron CMOS processes is very problematic in the design of direct conversion RF front-ends, especially for narrow-band systems such as GSM. The approach adopted in this study alleviates these problems by utilizing an appropriate downconversion mixer architecture, i.e. the LC-folded cascode mixer, which provides superior $1/f$ noise and linearity performance compared to the other active low-voltage mixers. In addition, compared to the traditional voltage-mode interface, a current-mode interface between the downconversion mixer output and analog baseband input improves the receiver performance in several ways. Firstly, since there is no voltage swing at the mixer output, the nonlinearity due to the mixer switching devices is minimized and the mixer blocking performance is improved. The current-mode interface also minimizes the noise contribution of the analog baseband in such a way that it requires only a moderate voltage gain (or transconductance) in the LNA and mixer. Both of these issues are very essential when operating at low supply voltage. Nevertheless, to operate properly, the current-mode interface requires a CMFB circuit. The dynamic matching technique is used to suppress the flicker noise of the CMFB circuit, which otherwise would dominate the mixer low-frequency noise, and thereby enable the entire current-mode concept.

References

[1] B. Razavi, "A 900 MHz CMOS direct conversion receiver," in *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 113-114, 1997.

[2] A. Rofougaran, G. Chang, J. J. Rael, J. Y. C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, J. Min, E. W. Roth, A. A. Abidi, and H. Samueli, "A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS-part II: receiver design," *IEEE J. Solid-State Circuits*, vol. 33, pp. 535-547, Apr. 1998.

[3] A. Pärssinen, J. Jussila, J. Ryynänen, L. Sumanen, and K. A. I. Halonen, "A 2 GHz wide-band direct conversion receiver for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1893-1903, Dec. 1999.

[4] M. S. J. Steyaert, J. Janssens, B. De Muer, M. Borremans, and N. Itoh, "A 2-V CMOS cellular transceiver front-end," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1895-1907, Dec. 2000.

[5] T. P. Liu and E. Westerwick, "5-GHz CMOS radio transceiver front-end chipset," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1927-1933, Dec. 2000.

[6] R. Magoon, A. Molnar, J. Zachan, G. Hatcher, and W. Rhee, "A single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-N synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1710-1720, Dec. 2002.

[7] P. van Zeijl, J.-W. T. Eikenbroek, P.-P. Vervoort, S. Setty, J. Tangenberg, G. Shipton, E. Kooistra, I. C. Keestra, D. Belot, K. Visser, E. Bosma, and S. C. Blaakmeer, "A bluetooth radio in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1679-1687, Dec. 2002.

[8] A. A. Abidi, "RF CMOS comes of age," *IEEE J. Solid-State Circuits*, vol. 39, pp. 549-561, April 2004.

[9] F. Behbahani, H. Firouzkouhi, R. Chokkalingam, S. Delshadpour, A. Kheirkhahi, M. Nariman, M. Conta, and S. Bhatia, "A fully integrated low-IF CMOS GPS radio with on-chip analog image rejection," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1721-1727, Dec. 2002.

[10] L. Perraud, M. Recouly, C. Pinatel, N. Sornin, J.-L. Bonnot, F. Benoist, M. Massei, and O. Gibrat, "A direct-conversion CMOS transceiver for the 802.11a/b/g WLAN standard utilizing a Cartesian feedback transmitter," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2226-2238, Dec. 2004.

[11] E. Duvivier, G. Puccio, S. Cipriani, L. Carpineto, P. Cusinato, B. Bisanti, F. Galant, F. Chalet, F. Coppola, S. Cercelaru, N. Vallespin, J.-C. Jiguet, and G. Sirna, "A fully integrated zero-IF transceiver for GSM-GPRS quad-band application," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2249-2257, Dec. 2003.

[12] Y.-J. Kim, Y.-S. Son, V. N. Parkhomenko, I.-C. Hwang, J.-K. Cho, K.-S. Nah, and B.-H. Park, " A GSM/EGSM/DCS/PCS direct conversion receiver with integrated synthesizer," *IEEE Trans. Microwave Theory Tech.*, vol. 53, pp. 606-613, Feb. 2005.

[13] E. Duvivier, G. Puccio, S. Cipriani, L. Carpineto, P. Cusinato, B. Bisanti, F. Galant, F. Chalet, F. Coppola, S. Cercelaru, N. Vallespin, J.-C. Jiguet, and G. Sirna, "Highly integrated direct conversion receiver for GSM/GPRS/EDGE with on-chip 84-dB dynamic range continuous-time $\Sigma\Delta$ ADC," *IEEE J. Solid-State Circuits*, vol. 40, pp. 403-411, Feb. 2005.

[14] R. Gharpurey, N. Yanduru, F. Dantoni, P. Litmanen, G. Sirna, T. Mayhugh, C. Lin, I. Deng, P. Fontaine, and F. Lin, "A direct-conversion receiver for the 3G WCDMA standard," *IEEE J. Solid-State Circuits*, vol. 38, pp. 556-560, Mar. 2003.

[15] S. K. Reynolds, B. A. Floyd, T. Beukema, T. Zwick, U. Pfeiffer, and H. Ainspan, "A direct-conversion receiver IC for WCDMA mobile systems," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1555-1560, Sept. 2003.

[16] M. Hafizi, S. Feng, T. Fu, K. Schulze, R. Ruth, R. Schwab, P. Karlsen, D. Simmonds, and G. Qizheng, "RF front-end of direct conversion receiver RFIC for CDMA-2000," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1622-1632, Oct. 2004.

[17] J. Cho, P. Good, M. Kamat, E. McCarthy, K. Rampmeier, W. Cops, A. El Moznine, H. Truong, Y. He, D. Yates, G. Taskov, C.-H. Lee, D. Koh, and S. Lloyd, "A dual-band tri-mode CDMA IF receiver with programmable channel-match filter," in *Proc. of IEEE RFIC Symposium*, Philadelphia, PA, 2003, pp. 391-394.

[18] H. Waite, P. Ta, J. Chen, H. Li, M. Gao, C. S. Chang, Y. S. Chang, W. Redman-White, O. Charlon, Y. Fan, R. Perkins, D. Brunel, E. Soudee, N. Lecacheur, and S. Clamagirand, "A CDMA2000 zero-IF receiver with low-leakage integrated front-end," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1175-1179, Oct. 2004.

[19] A. A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1399-1410, Dec. 1995.

[20] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, pp. 873-887, June 2001.

[21] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 428-435, June 1997.

[22] P. M. Stroet, R. Mohindra, S. Hahn, A. Schuur, and E. Riou, "A zero-IF single-chip transceiver for up to 22 Mb/s QPSK 802.11b wireless LAN," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2001, pp. 204-205.

[23] W. Kluge, L. Dathe, R. Jaehne, S. Ehrenreich, and D. Eggert, "A 2.4GHz CMOS transceiver for 802.11b wireless LANs," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2003, pp. 360-361.

[24] V. Aparin, N. Kim, G. Brown, Y. Wu, A. Cicalini, S. Kwok, and C. Persico, "A fully-integrated highly linear zero-IF CMOS cellular CDMA receiver," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2005, pp. 324-326.

[25] J. Rogin, I. Kouchev, G. Brenna, D. Tschopp, and Q. Huang, "A 1.5-V 45-mW direct-conversion WCDMA receiver IC 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2239-2248, Dec. 2003.

[26] S. Dow, B. Ballweber, L.-M. Chou, D. Eickbusch, J. Irwin, G. Kurtzman, P. Manapragada, D. Moeller, J. Paramesh, G. Black, R. Wollscheid, and K. Johnson, "A dual-band direct-conversion/VLIF transceiver for 50GSM/GSM/DCS/PCS," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2002, pp. 230-231.

[27] E. Götz, H. Kröbel, G. Märzinger, B. Memmler, C. Münker, B. Neurauter, D. Römer, J. Rubach, W. Schelmbauer, M. Scholz, M. Simon, U. Steinacker, and C. Stöger, "A quad-band low power single chip direct conversion CMOS transceiver with $\Sigma\Delta$-modulation loop for GSM," in *Proc. of the European Solid-State Circuits Conference*, Estoril, Portugal, 2003, pp. 217-220.

[28] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order distortion mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, pp. 394-406, Mar. 2003.

[29] J. Crols and M. S. J. Steyaert, "A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1483-1492, Dec. 1995.

[30] S. Mahdavi and A. A. Abidi, "Fully integrated 2.2-mW CMOS front end for a 900-MHz wireless receiver," *IEEE J. Solid-State Circuits*, vol. 37, pp. 662-669, May 2002.

[31] F. Behbahani, J. C. Leete, Y. Kishigami, A. Roithmeier, K. Hoshino, and A. A. Abidi, "A 2.4-GHz low-IF receiver for wideband WLAN in 0.6-μm CMOS-architecture and front-end," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1908-1916, Dec. 2000.

[32] D. K. Shaeffer, A. R. Shahani, S. S. Mohan, H. Samavati, H. R. Rategh, M. del Mar Hershenson, M. Xu, C. P. Yue, D. J. Eddleman, and T. H. Lee, "A 115-mW, 0.5-μm CMOS GPS receiver with wide dynamic-range active filters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2219-2231, Dec. 1998.

[33] A. J. Scholten, L. F. Tiemeijer, R. van Langevelde, R. J. Havens, A. T. A. Zegers-van Duijnhoven, and V. C Venezia, "Noise modeling for RF CMOS circuit simulation," *IEEE Trans. Electron Devices*, vol. 50, pp. 618-632, Mar. 2003.

[34] G. Gramegna, M. Paparo, P. G. Erratico, and P. De Vita, "A sub-1-dB $\pm$2.3-kV ESD-protected 900-MHz CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1010-1017, July 2001.

[35] H. Darabi and A. A. Abidi, "A 4.5-mW 900-MHz CMOS receiver for wireless paging," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1085-1096, Aug. 2000.

[36] A. A. Abidi, G. J. Pottie, and W. J. Kaiser, "Power-conscious design of wireless circuits and systems," in *Proc. of IEEE*, vol. 88, pp. 1528-1545, Oct. 2000.

[37] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley and Sons, 1993.

[38] R. G. Meyer and W. D. Mack, "A 1-GHz BiCMOS RF-front-end integrated circuit," *IEEE J. Solid-State Circuits*, vol. 29, pp. 350-355, Mar. 1994.

[39] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998.

[40] B. Razavi, *RF Microelectronics*, Prentice Hall PTR, 1998.

[41] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, pp. 15-25, Jan. 2000.

[42] K. Kivekäs, A. Pärssinen, and K. A. I. Halonen, "Characterization of IIP2 and DC-offsets in transconductance mixers," *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 1028-1038, Nov. 2001.

[43] A. Matsuzawa, "RF-SoC-Expectations and required conditions," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 245-253, Jan. 2002.

[44] T. Manku, G. Beck, and E. J. Shin, "A low-voltage design technique for RF integrated circuits," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 1408-1413, Oct. 1998.

[45] O. E. Erdogan, R. Gupta, D. G. Yee, J. C. Rudell, J. S. Ko, R. Brockenbrough, S. O. Lee, E. Lei, J. L. Tham, H. Wu, C. Conroy, and B. Kim, "A single-chip quad-band GSM/GPRS transceiver in 0.18μm standard CMOS," in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2005, pp. 318-319.

[46] A. Rofougaran, J. Y. C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF front-end IC for a direct-conversion wireless receiver," *IEEE J. Solid-State Circuits*, vol. 31, pp. 880-889, July 1996.

[47] H. T. Fris, "Noise figures of radio receivers," in *Proc. of IRE*, vol. 32, pp. 419-422, July 1944.

[48] B. Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LAN's," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1382-1385, Oct. 1999.

[49] K. L. Fong, C. D. Hull, and R. G. Meyer, "A class AB monolithic mixer for 900-MHz applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1166-1172, Aug. 1997.

[50] K. Kivekäs, "Design and characterization of downconversion mixers and the on-chip calibration techniques for monolithic direct conversion radio receivers," Ph.D. Dissertation, Helsinki University of Technology, Espoo, Finland, 2002.

[51] H. Sjöland, A. Kamiri-Sanjaani, and A. A. Abidi, "A merged CMOS LNA and mixer for a WCDMA receiver," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1045-1050, June 2003.

[52] F. Gatta, D. Manstretta, P. Rossi, and F. Svelto, "A fully integrated 0.18-μm CMOS direct conversion receiver front-end with on-chip LO for UMTS," *IEEE J. Solid-State Circuits*, vol. 38, pp. 15-23, Jan. 2004.

[53] M. Brandolini, P. Rossi, D. Manstretta, and F. Svelto, "Toward multistandard mobile terminals-fully integrated receivers requirements and architectures," *IEEE Trans. Microwave Theory Tech.*, vol. 53, pp. 1026-1038, Mar. 2005.

[54] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745-759, May 1997.

[55] G. Girlando and G. Palmisano, "Noise figure and impedance matching in RF cascode amplifiers," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 1388-1396, Nov. 1999.

[56] P. Rossi, A. Liscidini, M. Brandolini, and F. Svelto, "A variable gain RF front-end, based on a voltage-voltage feedback LNA, for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 40, pp. 690-697, Mar. 2005.

[57] B. A. Floyd, J. Mehta, C. Camero, and K. K. O, "A 900-MHz, 0.8μm CMOS low noise amplifier with 1.2-dB noise figure," in *Proc. Custom Integrated Circuits Conf.*, 1999, pp. 661-664.

[58] P. Andreani and H. Sjöland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 835-841, Sept. 2001.

[59] T. K. Nguyen, C. H. Kim, G. J. Ihm, M. S. Yang, and S. G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 1433-1442, May 2004.

[60] P. Leroux and M. Steyaert, "High-performance 5.2GHz LNA with on-chip inductor to provide ESD protection," *Electron. Lett.*, vol. 37, pp. 467-469, Mar. 2001.

[61] P. Leroux, J. Janssens, and M. Steyaert, "A 0.8-dB NF ESD-protected 9-mW CMOS LNA operating at 1.23 GHz," *IEEE J. Solid-State Circuits*, vol. 37, pp. 760-765, June 2002.

[62] J. Chang, "An integrated 900 MHz spread-spectrum wireless receiver in 1-μm CMOS and a suspended inductor technique", Ph.D. Thesis, UCLA, Mar. 1998.

[63] V. Chandrasekhar and K. Mayaram, "Analysis of CMOS RF LNAs with ESD protection," in *IEEE Int. Circuits and Systems Symp.*, 2002, pp. 779-802.

[64] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Saunders College Publishing, 1987.

[65] R. T. Chang, M. T. Yang, P. P. C. Ho, Y. J. Wang, Y. T. Chia, B. K. Liew, C. P. Yue, and S. S. Wong, ”Modeling and optimization of substrate resistance for RF-CMOS,” *IEEE Trans. Electron Devices*, vol. 51, pp. 421-426, Mar. 2004.

[66] W. Guo and D. Huang, ”Noise and linearity analysis for a 1.9GHz CMOS LNA,” in *Proc. Asia-Pacific Circuits and Systems Conf.*, 2002, pp. 409-414.

[67] A. Vilander and P. Sivonen, ”Gain stabilization technique for narrow band integrated low noise amplifiers,” U.S. Patent no. 6963247, Nov. 2005.

[68] J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, and K. Halonen, ”RF gain control in direct conversion receivers,” in *IEEE Int. Circuits and Systems Symp.*, Scottsdale, Arizona, 2002, pp. 117-120.

[69] J. Ryynänen, ”Low-noise amplifiers for integrated multi-mode direct-conversion receivers,” Ph.D. Dissertation, Helsinki University of Technology, Espoo, Finland, 2004.

[70] J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, and K. A. I. Halonen, ”A dual-band RF front-end for a WCDMA and GSM applications,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1198-1204, Aug. 2001.

[71] S. Tadjpour, E. Cijvat, E. Hegazi, and A. A. Abidi, ”A 900-MHz dual-conversion low-IF GSM receiver in 0.35-μm CMOS,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1992-2002, Dec. 2001.

[72] K. L. Fong, ”Dual-band high-linearity variable-gain low-noise amplifiers for wireless applications,” in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 1999, pp. 224-225.

[73] H. Darabi, S. Khorram, Z. Zhou, T. Li, B. Marholev, J. Chiu, J. Castaneda, E. Chien, S. Anand, S. Wu, M. Pan, R. Rofougaran, H. Kim, P. Lettieri, B. Ibrahim, J. Rael, L. Tran, E. Geronaga, H. Yeh, T. Frost, J. Trachewsky, and A. Rofougaran, ”A fully integrated SoC for 802.11b in 0.18μm CMOS,” in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2005, pp. 96-97.

[74] A. Zolfaghari and B. Razavi, ”A low-power 2.4-GHz transmitter/receiver CMOS IC,” *IEEE J. Solid-State Circuits*, vol. 38, pp. 176-183, Feb. 2003.

[75] F. Behbahani, Y. Kishigami, J. Leete, and A. A. Abidi, ”CMOS mixers and polyphase filters for large image rejection,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 873-886, June 2001.

[76] K. L. Fong and R. G. Meyer, ”Monolithic RF active mixer design,” *IEEE J. Solid-State Circuits*, vol. 46, pp. 231-239, Mar. 1999.

[77] E. E. Bautista, B. Bastani, and J. Heck, ”A high IIP2 downconversion mixer using dynamic matching,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 1934-1941, Dec. 2000.

[78] B. Gilbert, ”The MICROMIXER: A highly linear variant of the Gilbert mixer using a bisymmetric class-AB input stage,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 1412-1423, Sep. 1997.

[79] W. Sansen, ”Distortion in elementary transistor circuits,” *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 315-325, Mar. 1999.

[80] K. L. Fong and R. G. Meyer, ”High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages,” *IEEE J. Solid-State Circuits*, vol. 33, pp. 548-555, Apr. 1998.

[81] M. T. Terrovitis and R. G. Meyer, ”Noise in current-commutitating CMOS mixers,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 772-783, June 1999.

[82] V. Vidojkovic, J. van der Tang, A. Leeuwenburg, and A. H. M. van Roermund, ”A low-voltage folded-switching mixer in 0.18-μm CMOS,” *IEEE J. Solid-State Circuits*, vol. 40, pp. 1259-1264, June 2005.

[83] H. Darabi and J. Chiu, ”A noise cancellation technique in active RF-CMOS mixers,” in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2005, pp. 544-545.

[84] D. Manstretta, R. Castello, and F. Svelto, ”Low 1/f noise CMOS active mixers for direct conversion,” *IEEE Trans. Circuits Syst. II*, vol. 48, pp. 846-850, Sep. 2001.

[85] Z. Xu, S. Jiang, Y. Wu, H. Jian, G. Chu, K. Ku, P. Wang, N. Tran, Q. Gu, M. Lai, C. Chien, M. Chang, and P. Chow, ”A compact dual-band direct-conversion CMOS transceiver for 802.11a/b/g WLAN,” in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2005, pp. 98-99.

[86] E. Abou-Allam, J. J. Nisbet, and M. C. Maliepaard, ”Low-voltage 1.9-GHz front-end receiver in 0.5-μm CMOS technology,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1434-1442, Oct. 2001.

[87] T. W. Kim, B. Kim, and K. Lee, ”Highly linear receiver front-end adopting MOSFET transconductance linearization by multiple gated transistors,” *IEEE J. Solid-State Circuits*, vol. 39, pp. 223-229, Jan. 2004.

[88] D. Coffing and E. Main, ”Effects of offsets on bipolar integrated circuit even-order distortion terms,” *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 23-30, Jan. 2001.

[89] A. A. Abidi, ”General relations between IP2, IP3, and offsets in differential circuits and the effects of feedback,” *IEEE Trans. Microwave Theory Tech.*, vol. 51, pp. 1610-1612, May 2003.

[90] S. Wu and B. Razavi, ”A 900-MHz/1.8-GHz CMOS receiver for dual-band applications,” *IEEE J. Solid-State Circuits*, vol. 33, pp. 2178-2185, Dec. 1998.

[91] A. Vilander and P. Sivonen, ”Method and apparatus providing cancellation of second order intermodulation distortion and enhancement of second order intercept point (IIP2) in common source and common emitter transconductance circuits,” U.S. Patent no. 6992519, Jan. 2006.

[92] M. Brandolini, P. Rossi, D. Sanzogni, and F. Svelto, ”A CMOS direct down-converter with +78dBm minimum IIP2 for 3G cell-phones,” in *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, 2005, pp. 320-321.

[93] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, 1998.

[94] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits*, Kluwer Academic Publishers, 1998.

[95] C. C. Enz and E. A. Vittoz, ”CMOS low-power analog circuit design,” Designing Low Power Digital Systems, Emerging Technologies (1996), 1996, pp. 79-133.

[96] K. Kivekäs, A. Pärssinen, J. Ryynänen, J. Jussila, and K. Halonen, ”Calibration techniques of active BiCMOS mixers,” *IEEE J. Solid-State Circuits*, vol. 37, pp. 766-769, June 2002.

[97] M. Hotti, J. Ryynänen, K. Kivekäs, and K. Halonen, ”An IIP2 calibration technique for direct conversion receivers,” in *Proc. of ISCAS Symposium*, Vancouver, Canada, 2004, pp. 257-260.

[98] A. Rofougaran, G. Chang, J. J. Rael, J. Y. C. Chang, M. Rofougaran, P. J. Chang, M. Djafari, M. K. Ku, E. W. Roth, A. A. Abidi, and H. Samueli, ”A single-chip 900-MHz spread-spectrum wireless transceiver in 1-μm CMOS-part I: Architecture and transmitter design,” *IEEE J. Solid-State Circuits*, vol. 33, pp. 515-534, Apr. 1998.

[99] H. Darabi, S. Khorram, H.-M. Chien, M. Pan, S. Wu, S. Moloudi, J. C. Leete, J. J. Rael, M. Syed, R. Lee, B. Ibrahim, M. Rofougaran, and A. Rofougaran, ”A 2.4-GHz CMOS transceiver for bluetooth,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 2016-2024, Dec. 2001.

[100] E. Song, Y. Koo, Y.-J. Jung, D.-H. Lee, S. Chu, and S.-I. Chae, ”A 0.25-μm CMOS quad-band GSM RF transceiver using an efficient LO frequency plan,” *IEEE J. Solid-State Circuits*, vol. 40, pp. 1094-1106, May 2005.

[101] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Saunders College Publishing, 1991.

[102] J. Ryynänen, K. Kivekäs, J. Jussila, L. Sumanen, A. Pärssinen, and K. A. I. Halonen, ”A single-chip multimode receiver for GSM900, DCS1800, PCS1900, and WCDMA,” *IEEE J. Solid-State Circuits*, vol. 38, pp. 594-602, Apr. 2003.

[103] J-P. Tervaluoto, A. Ruha, and T. Ruotsalainen, ”Mixer circuit,” U.S. patent application, January 2004.

[104] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, ”A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver,” in *Proc. Custom Integrated Circuits Conf.*, San Jose, CA, 2003, pp. 459-462.

Abstracts of Publications I-VI

I. This paper presents an RF front-end with on-chip VCO fabricated in 0.35-μm SiGe BiCMOS technology for a direct conversion GPS receiver. The circuit design of packaged inductively degenerated common-emitter LNA with ESD protection is described, and theoretically calculated LNA performance is compared with simulations. The DSB-NF and IIP3 of the resistively degenerated Gilbert-type down-conversion mixer are analyzed, and theoretically estimated mixer performance is compared with simulations. The approximative equations describing the entire RF front-end DSB-NF and IIP3 are also given. By applying the derived formulas, the front-end performance can be readily estimated and optimized. The implemented RF front-end achieves low noise (DSB-NF of 2.7 dB @ 1.575 GHz) at low power consumption (15.3 mA from a 2.7 V supply).

II. In this paper, the effects of packaging and ESD protection on the performance of inductively degenerated common-emitter LNA are examined and the equations describing the input impedance, transconductance, voltage gain, and NF of the packaged amplifier are derived. From the equations several guidelines for the LNA design are obtained and a systematic approach for the LNA design can be derived. Furthermore, by applying the formulas, the performance of the amplifier can be readily estimated and optimized in the very early stage of the circuit design, immediately as the process data is available. It is concluded that the equivalent parallel parasitic capacitance (C_p) due to the package and ESD parasitics limits the achievable impedance level at the LNA input and it lowers the noise contributions of the LNA input circuit (i.e. base resistance and base shot noise) to the LNA NF. The measurement results of the implemented 0.35-μm SiGe RF front-end with inductively degenerated common-emitter LNA are found to agree well with theoretical calculations and simulations.

III. A gain stabilization technique for tuned integrated LNAs is presented in this paper. The proposed method is shown to regulate the magnitude of the LC-tuned load impedance of the amplifier at the operation frequency against variations of passive devices in the IC process. The impedance stabilization technique is based on the excellent relative accuracy of integrated resistors. Although the absolute deviation of the integrated resistors can be as large as $\pm 20\%$, the relative deviation can be made smaller than $\pm 1\%$ provided that resistors are placed close to each other. In the paper, the design equations for the gain stabilization technique are derived and the necessary conditions for the method to operate properly are presented. By applying the proposed method, the voltage gain variation of the inductively degenerated LNA is shown to be reduced several decibels. As a consequence, the entire radio receiver can more easily meet its specifications in the presence of IC process variations and the product yield is improved. Finally, besides of the LNAs, the presented stabilization technique can also be utilized in other tuned amplifiers, filters or oscillators employing damped LC-tuned loads.

IV. In this paper, the effects of packaging in inductively degenerated common-source LNAs with ESD protection are studied and the performance of the packaged LNA is optimized. Equations describing the input impedance, transconductance, voltage gain, and NF of the packaged amplifier are derived and the effects of the LNA input matching network, package, and ESD parasitics on these amplifier quantities are highlighted. From the equations, several design guidelines for the packaged LNA are obtained and a systematic approach for the ESD-protected LNA optimization is deduced. It is also shown that in the presence of an equivalent parallel package parasitic capacitance (C_p), the NF in a well-optimized LNA is easily dominated by the losses of the input matching network, instead of active device noise. Based on the theoretical results, a packaged inductively degenerated common-source LNA with ESD protection is designed in the $0.13\ \mu m$ CMOS process. The amplifier achieves a low NF of 1.6 dB at 2 GHz while consuming 8.4 mW from a 1.2 V supply.

V. In this paper, a biasing technique for cancelling second-order intermodulation (IM2) distortion and enhancing IIP2 in common-source and common-emitter RF transconductors is presented. The proposed circuit can be utilized as an RF input transconductor in double-balanced downconversion mixers. It is shown that the proposed approach increases the yield of the entire radio receiver by enhancing the mixer IIP2. The presented circuit displays ideally no IM2 distortion provided that the transconductor is excited differentially and all the transistors in the circuit match with each other. Moreover, in this circuit, no extra noise sources in practical cases of interest are added in the mixer and no integrated inductors are required, which results in a small die area. Finally, the presented transconductor is also suitable for operation at low supply voltages, because it has only one device stacked between the transconductor input and output. The IIP3 of the proposed transconductor is slightly higher than the IIP3 of the differential pair transconductor at given bias. In the paper, the operation principle of the proposed transconductor is explained and analyzed by direct calculation of the nonlinear responses and the nonidealities of the transconductor are discussed. The theoretical analysis is also verified with experimental circuit simulations and the proposed transconductor is simulated as a part of the complete downconversion mixer.

VI. In this paper, a 1.2-V RF front-end realized for a PCS direct conversion receiver is presented. The RF front-end comprises an LNA, quadrature mixers, and active RC low-pass filters with gain control. Quadrature LO signals are generated on chip by a double-frequency VCO and frequency divider. A current-mode interface between the downconversion mixer output and analog baseband input, together with a dynamic matching technique, is shown to simultaneously improve the mixer linearity, lower the flicker noise due to the mixer switches, and minimize the noise contribution of the analog baseband. The dynamic matching technique is employed to suppress the flicker noise of the CMFB circuit utilized at the mixer output, which otherwise would dominate the low-frequency noise of the mixer. Various low-voltage circuit techniques are employed to enhance both the mixer second- and third-order linearity, and to lower the flicker noise. The RF front-end is fabricated in a 0.13-μm CMOS process utilizing only standard process options.

ISBN 951-22-8366-2
ISBN 951-22-8367-0 (PDF)
ISSN 1795-2239
ISSN 1795-4584 (PDF)