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Thermal Simulation of the Solidification of Lead-Free Solder Interconnections

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Abstract—Two thermal models of different level, a component model and an interconnection model, were established to simulate the solidification of lead-free solder interconnections of a chip-scale packaged component during reflow soldering. The thermal properties of the interconnections were derived with the help of thermodynamic calculations relevant to the phase transformations occurring during melting and solidification. Experimental measurements were carried out and the data were used to determine some parameters so that the model is more realistic. Although the results of the component model agreed with the experimental measurements in the faster cooling of the component than the board, the interconnection model suggested that the temperature gradients over the interconnections were unlikely to be of significance until the invariant eutectic reaction commenced. The findings imply that solder/metallization interfaces on printed wiring board and component sides are equally likely sites for initiating the solidification of interconnections. On the basis of the simulated temperature distribution, the growth conditions of the primary Sn are evaluated and an explanation for the sequence of solidification steps has also been given.

Index Terms—Interconnection, lead-free solder, microstructure, reliability, Sn–Ag–Cu, solidification, thermal modeling, thermodynamics.

I. INTRODUCTION

RELIABILITY of portable electronics products is one of the most important issues in the fields of electronics production today, in response to the requirements of higher performance, miniaturization, larger scales of integration, and environmental friendliness. Although the reliability of novel electronic products has been studied extensively, and new lead-free materials and component technologies have been involved, the solder interconnections are increasingly susceptible for failure. The reliability of lead-free solder interconnections is dependent on many factors but ultimately is controlled by the microstructures of the interconnections [1]. Since microstructures are first generated during the solidification of liquid interconnections, any investigation should commence at this point. The most important microstructural units in solidified interconnections are cell, dendrite, colony of Sn, in addition, includes also second-phase particles like Cu_6Sn_5 and Ag_3Sn . The amount, shape, and distribution of second-phase particles are particularly important from the point view of plastic deformation, recovery,

and recrystallization. In order to understand the evolution of microstructures, especially during service, it is important to understand how the structures are originally formed and to be aware of the initial microstructure as it appears immediately after the solidification of the interconnections.

During reflow soldering, interconnections are heated to about 25 °C above the liquidus temperature of the solder alloy, and after that are subjected to a cooling of 1°C/s–2°C/s. Measurement of the temperature profile of the assembly is relatively straightforward, but it is very difficult to determine experimentally, the temperature fields and distributions inside components. Numerical modeling thus becomes a powerful tool for the purpose. Conway *et al.* [2]–[5] established a board-level thermal model of the reflow process in order to perform on-line predictions of temperature profiles in a reflow oven. Eftychiou *et al.* [6], [7] set up a two-dimensional model with both oven- and board-level simulations. Several other research groups have developed the model further [8], [9]. A computational fluid dynamic (CFD) model to simulate the flow field inside a typical reflow oven has also been established [10]. A detailed three-dimensional thermal simulation at component or interconnection level has not yet been presented, probably because of the complexity of interconnection level modeling. On the one hand, time-dependent temperature distribution inside interconnections is an important characteristic and the solidification of solder strongly depends on it. On the other hand, solidification itself introduces a thermal effect and influences the temperature distribution. Analysis of the solidification of interconnections demands, therefore, that thermal simulation be combined with thermodynamic and kinetic considerations. This is a challenge for theoretical simulations.

In this paper, the solidification of interconnections for a chip-scale packaged (CSP) component inside a reflow oven will be simulated and verified experimentally. The temperature distribution at the component level is determined first, after which the detailed temperature distributions inside individual interconnections are calculated. Thermodynamic considerations will be applied to evaluate the thermal properties of a lead-free solder material as function of temperature and the thermodynamic databank system [11] was used for the purpose. The aim is using a combination of thermal and thermodynamic tools to predict the microstructures formed during solidification and to compare those one with observed microscopy images. Even though the contribution of supercooling is not included yet, the thermodynamic calculations based on the local equilibrium concept are anticipated be reasonable, and therefore very useful information on the solidification process can be achieved.

Manuscript received July 5, 2004; revised January 17, 2005. This work was recommended by Associate Editor C. Amon upon evaluation of the reviewer's comments.

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Digital Object Identifier 10.1109/TCAPT.2005.848590

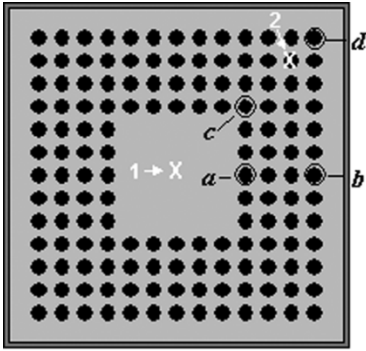


Fig. 1. Solder bump array of the CSP component. Numbers 1 and 2 are locations of thermocouples; letters a–d are the interconnections simulated in the interconnection model.

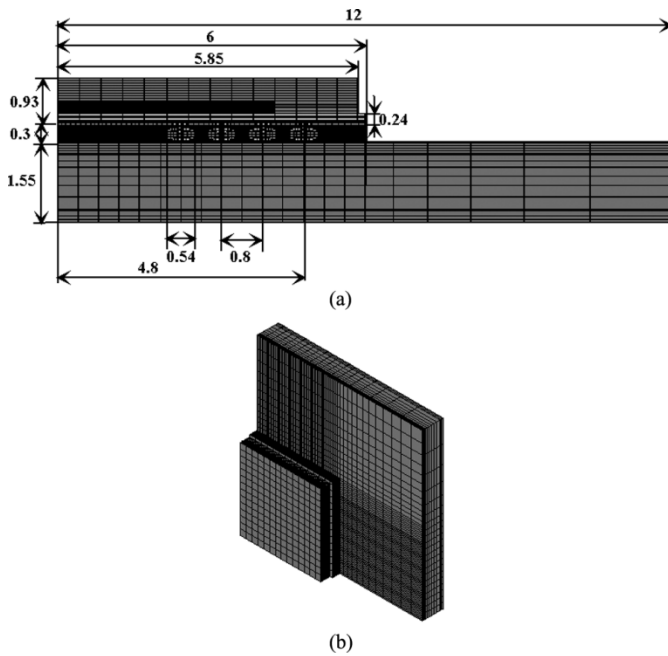


Fig. 2. Component model established in ANSYS. (a) Side view (dimensions in millimeters). (b) 3-D view.

II. COMPONENT AND INTERCONNECTION MODELS

A solid conduction model was employed to simulate the thermal behavior of a CSP component during the reflow process. The CSP component had 144 (13×13 minus 5×5) solder bumps, arranged as shown in Fig. 1, and was mounted onto a double-sided four-layer printed wiring board (PWB) with a commercial lead-free solder paste ($\text{Sn}_{3.8}\text{Ag}_{0.7}\text{Cu}$). Since the size of the interconnection is very small compared with the component, computational limits do not permit a detailed temperature field to be achieved inside the interconnection with a single simulation. The model is therefore established hierarchically in two steps, first the component and then the interconnection model.

In the component model, both the geometry and convective boundaries of the CSP and vicinal board area are assumed to be symmetric in X and Y directions, so that only one fourth of the structure needs to be modeled as shown in Fig. 2. The assumption of symmetry only approximately satisfies the real

situation, but it reduces the required computational resources dramatically.

For three-dimensional unsteady conduction problems, the controlling partial differential equation can be expressed as follows:

$$\frac{\partial}{\partial x} \left(k_x \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \left(k_y \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \left(k_z \frac{\partial T}{\partial z} \right) + \dot{q} = \rho c_p \frac{\partial T}{\partial t}. \quad (1)$$

Here, $\partial T/\partial x$, $\partial T/\partial y$, and $\partial T/\partial z$ are temperature gradients, k_x , k_y , and k_z are thermal conductivities in x , y , and z direction, respectively, \dot{q} is the heat-generating rate, ρ and c_p are the density and specific heat of the material, $\partial T/\partial t$ is the time dependency of temperature. By using finite element method (FEM), (1) is solved numerically for the solid model with the help of ANSYS.

Forced convection is applied to the surfaces of both component and board and the corresponding boundary conditions need to be defined for the model. The convective heat can be expressed as

$$q = \alpha(T_{\text{oven}} - T_{\text{surface}}) \quad (2)$$

where q is the local heat flux, α is the local heat transfer coefficient, T_{surface} and T_{oven} were surface and oven temperatures. The oven temperature T_{oven} was measured experimentally, as will be described in the experimental section.

The heat transfer coefficient α was a function of time and location, depending on the surrounding airflow. The averaged heat transfer coefficient $\bar{\alpha}$ could be used to exclude the variance with location, but the difference between the upper and lower surfaces required to use separate values $\bar{\alpha}_{\text{upp}}$ and $\bar{\alpha}_{\text{bot}}$. Since the heating or cooling air was impinged from the top and shielded by the board, it generated little airflow below the board. The coefficient $\bar{\alpha}_{\text{bot}}$ on the bottom surface could therefore be regarded as small and constant over time. On the upper surfaces, $\bar{\alpha}_{\text{upp}}$ is sensitive to instantaneous airflow and must be presented as a function of time.

Empirically the heat transfer coefficient of forced convection between airflow and a solid surface is proportional to the square root of the Reynolds number on the surface ($\text{Re} = \rho v L / \mu$, where ρ and μ are density and viscosity of air, L is the characteristic length). The heat transfer coefficient is roughly proportional to the square root of ambient air velocity v

$$\bar{\alpha}_{\text{upp}} = A\sqrt{v} \quad (3)$$

where A denotes the ratio. An earlier simulation of the flow field inside the reflow oven [10] offered the square root of air velocity, as shown in Fig. 3, and this was used to estimate the instantaneous heat transfer coefficient $\bar{\alpha}_{\text{upp}}$.

It can be seen that two unknown parameters, $\bar{\alpha}_{\text{bot}}$ and the proportionality ratio A in (3), must be introduced. In this work, they were determined by trial and test method: several simulations were performed with different reasonable values, and the optimal set was selected through comparison of the calculated and measured temperature profiles (see Section IV). The test value for variable A is selected to be in such a range that the $\bar{\alpha}_{\text{upp}}$ falls into the typical range of forced convection with gas, $25\text{--}250 \text{ W/m}^2 \cdot \text{K}$; while the test value of $\bar{\alpha}_{\text{bot}}$ is between 2 and

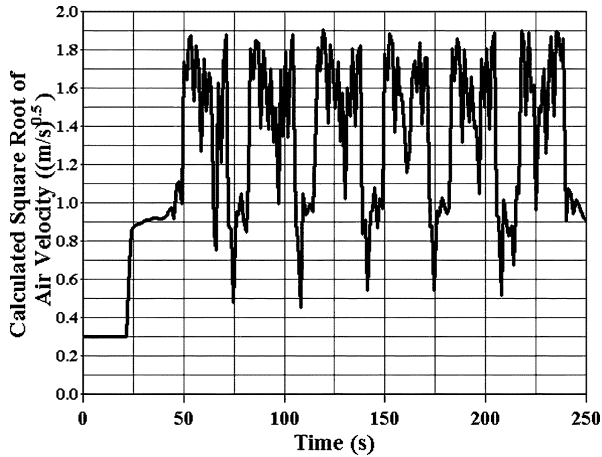


Fig. 3. Calculated square root of instantaneous air velocity based on the simulation in [10]. Conveyor speed 0.92 m/min.

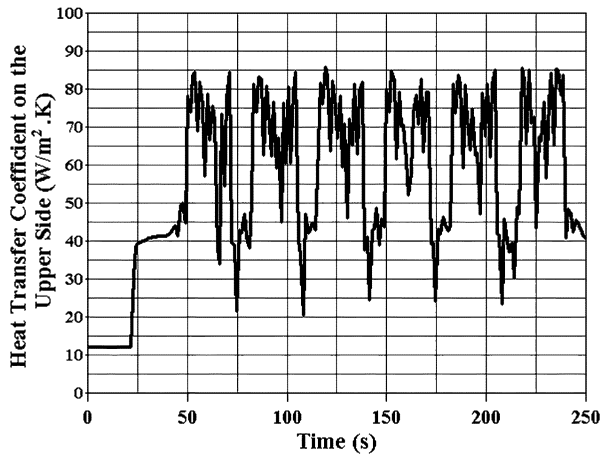


Fig. 4. Heat transfer coefficient $\bar{\alpha}_{\text{upp}}$ on upper surfaces adopted in the component model.

20 $\text{W}/\text{m}^2 \cdot \text{K}$, which is slightly smaller than $\bar{\alpha}_{\text{upp}}$. Finally the adopted value of $\bar{\alpha}_{\text{upp}}$ was plotted in Fig. 4 and $\bar{\alpha}_{\text{bot}}$ was set to 5 $\text{W}/\text{m}^2 \cdot \text{K}$.

The interconnection model was established on the basis of the component model with the purpose of revealing the detailed temperature variations inside the interconnection. The model is zoomed to the vicinity of a single solder interconnection through submodeling performed on the component model in ANSYS, as shown in Fig. 5. The component model offers the boundary conditions along the surface of its calculation domain. Since the geometries of all the interconnections are the same, different interconnections can be investigated simply by changing the location of interconnection model relative to the component model.

Four typical interconnections of the CSP component were analyzed, with locations as marked in Fig. 1. Interconnections *a* and *b* are inner and outer interconnections along the centerline of the component, while *c* and *d* are interconnections in the diagonal direction. Since solidification was our main interest, the simulation only covers the cooling period.

A concern may arise from the contact thermal resistance at interfaces between interconnections and soldering pads, if they are not perfectly contacted. In the component model, the contact resistance is not considered because of low accuracy required at

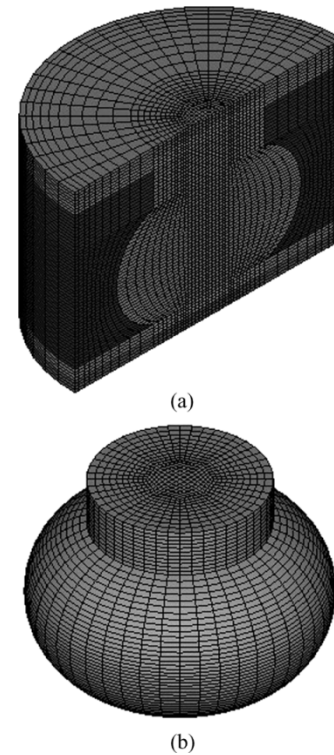


Fig. 5. Interconnection model. (a) One half of the model, which shows how the interconnection is embedded inside the model. (b) Interconnection after removal of surrounding materials.

this level. In the interconnection model, only the situation after the melting of solders needs to be investigated. As long as good wettability is ensured, liquid solder should spread over the surface of soldering pad. If the interconnections are assumed to be free of voids or other defects, the contact resistance mainly comes from the intermetallic layers formed along the interfaces. This is simulated in the interconnection model by introducing an 8- μm -thick intermetallic layer at both ends of the interconnection.

III. THERMAL PROPERTIES OF THE INTERCONNECTION SYSTEM

Before the controlling partial differential (1) can be solved, the thermal conductivity k , specific heat c_p , and density ρ have to be known for all materials. The thermal properties, except those for the solder material, are listed in Table I. The properties of the conductor layers were averaged from those of Cu and dielectric material taking into account the coverage ratio. Air in the gap between board and component is taken to be a “solid” material with the same thermal properties as air since it is effectively still. This simplification avoids the difficulty of defining a realistic convective boundary condition on bump surfaces.

Fields and Low [12] have discussed the physical properties of three common intermetallic compounds: Cu_6Sn_5 , Cu_3Sn and Ni_3Sn_4 . Of these, Cu_6Sn_5 tends to form in lead-free solder alloys and its thermal properties are adopted for the present model.

A more detailed evaluation of the thermal properties of the solder interconnection is required, since our objective is to simulate the solidification. Reflow soldering is a complex procedure; besides the melting and solidification of the solder alloy, the evaporation of solvent from the solder paste during preheating

TABLE I
MATERIAL PROPERTIES USED FOR THERMAL MODELLING

Material		Thermal Conductivity (W/m.K)	Specific heat (J/kg.K)	Density (kg/m ³)
Solder Mask		0.2	1400	1120
Still Air	27°C	0.0263	1007	1.1614
	77°C	0.0300	1009	0.9950
	127°C	0.0338	1014	0.8711
	177°C	0.0373	1021	0.7740
	227°C	0.0407	1030	0.6964
	277°C	0.0439	1040	0.6329
Prepreg		0.3	1400	1800
Plastic Encapsulation		0.7	1000	1900
Copper		400	385	8930
Patterned Copper	50% coverage	200	700	5400
	20% coverage	80	880	3300
FR-4	Horizontal (k_x, k_y)	0.5	880	1200
	Vertical (k_z)	0.3		
Silicon	0°C	203.7	700	2330
	127°C	98.9		
	327°C	52.1		
Polyimide		0.19	1100	1400
Intermetallic Layer		34.2	165	8370

and soaking periods also has a certain amount of thermal effect. The evaporation occurs very early, however, before the melting of solder, so that only the behavior of the solder alloy has to be considered.

Solder interconnections are assumed to be of fixed shape, with constant volume, weight and composition. Considering the dissolution of metallizations and the amount of intermetallic layer formed, we take the final composition of the interconnections to be Sn_{0.5}Ag_{0.3}Cu. This composition is approximately the same as the composition during solidification and is adopted in the following thermodynamic analysis.

Since the solder is a multiphase alloy, its material properties should be derived from all existing phases in the system, whose equilibrium ratios vary with temperature. The phase changes of the alloy Sn_{0.5}Ag_{0.3}Cu need to be analyzed beforehand, therefore. A liquidus projection of the Sn-rich corner of the SnAgCu phase diagram was calculated, as shown in Fig. 6, by using a commercial databank system [11]. The thermodynamic database of the SnCuAg system was given in [13]. The equilibrium solidification path of the Sn_{0.5}Ag_{0.3}Cu alloy, that is, the path of the liquid composition during solidification, is plotted by the dotted line in the figure. The amount and the sequence of formation of the phases during solidification are described in Fig. 7. Primary Sn starts to nucleate at 229 °C, binary eutectic Sn + Cu₆Sn₅ is formed at 223 °C, and finally the solidification terminates with the isothermal ternary eutectic reaction ($L \rightarrow Sn + Cu_6Sn_5 + Ag_3Sn$) at 217 °C. Three temperature ranges are involved: a two-phase range (223–229 °C), a three-phase range (217 °C–223 °C) and an isothermal four-phase range (217 °C).

The noticeable variation in the ratios of phases during solidification makes it difficult to evaluate the specific heat of the alloy. However, the thermodynamic variable enthalpy, denoted as H ,

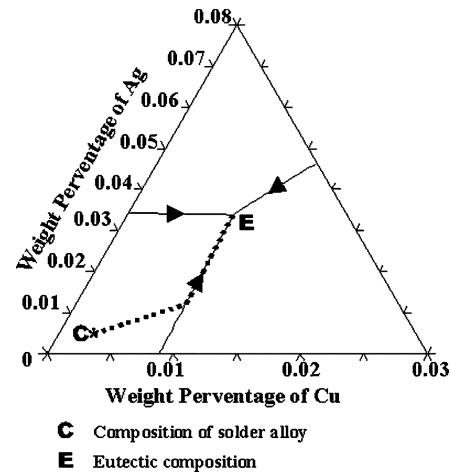


Fig. 6. Calculated liquidus projection in Sn-corner of Sn-Cu-Ag phase diagram.

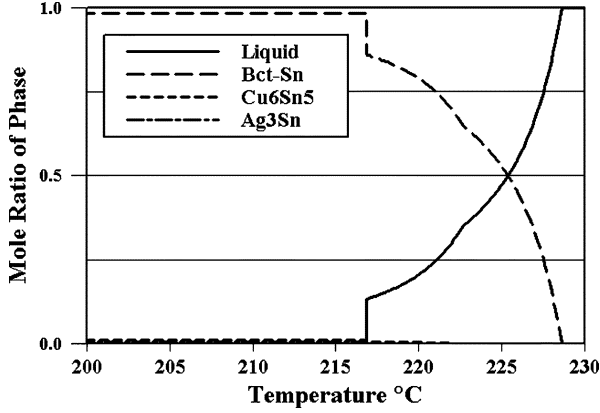
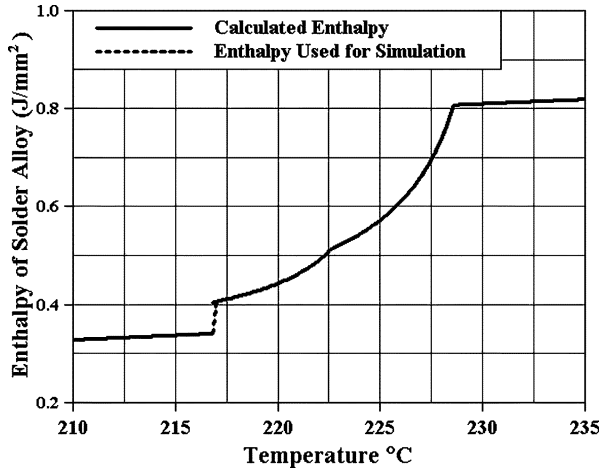
can be used in the thermal modeling instead [14]. The relation between enthalpy and specific heat is

$$c_p = \frac{dH}{dT}. \quad (4)$$

The enthalpy is a function of temperature and the specific heat is its derivative. For purpose of the ANSYS program, the enthalpy should be expressed in unit volume (J/m³ or J/mm³).

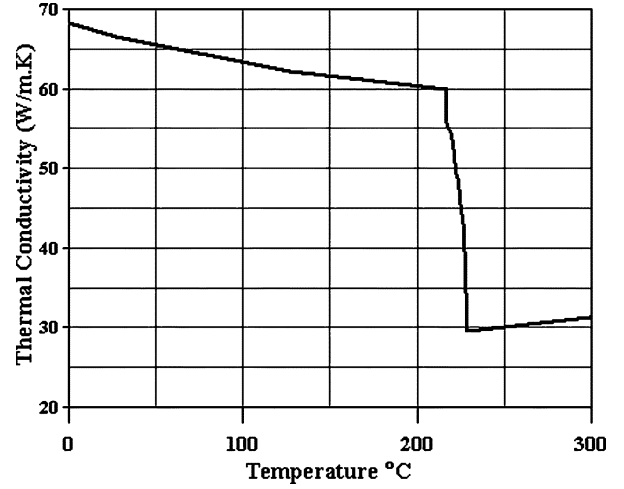
The total enthalpy of the alloy can be obtained by summing up the enthalpies of all the phases as follows:

$$H_{tot} = y_{liq}H_{liq} + y_{Sn}H_{Sn} + y_{Cu_6Sn_5}H_{Cu_6Sn_5} + y_{Ag_3Sn}H_{Ag_3Sn}. \quad (5)$$

Fig. 7. Calculated equilibrium phase percentages for the alloy $\text{Sn}_{0.5}\text{Ag}_{0.3}\text{Cu}$.Fig. 8. Calculated system enthalpy of $\text{Sn}_{0.5}\text{Ag}_{0.3}\text{Cu}$ solder material and that adopted in thermal simulation.

The enthalpies above are the enthalpies for 1 mole matter, either for the alloy or for discrete phases, depending on their subscripts. The variable y denotes the mole ratios of the phases as plotted in Fig. 7. Both H and y can easily be calculated thermodynamically in the databank system, so that the total enthalpy of 1 mole solder alloy is obtained. The total enthalpy can then be converted to the enthalpy in unit volume J/m^3 or J/mm^3 , assuming that the solder alloy has the same density as Sn, or 7310 kg/m^3 . The calculated results are shown in Fig. 8.

The following assumptions are made to validate the enthalpy function in thermal simulations: First, equilibrium solidification is assumed and the supercooling is regarded as small. Second, the distribution of the solidification product, primary Sn, and binary and ternary eutectic structures is assumed to be even (that is, the microstructure is homogenous at the scale of the calculation mesh). Third, since the isothermal eutectic reaction introduces a discontinuity in Fig. 8, which cannot be handled by ANSYS, a very steep slope line is assumed to replace it. The temperature range of the slope ($216.8 \text{ }^\circ\text{C}$ – $217.0 \text{ }^\circ\text{C}$) was carefully selected because too narrow a range causes divergence of the thermal simulation, while too wide a range causes too wide deviation from the original enthalpy function. Rather than constant temperature, the temperature range $216.8 \text{ }^\circ\text{C}$ – $217.0 \text{ }^\circ\text{C}$

Fig. 9. Thermal conductivity of $\text{Sn}_{0.5}\text{Ag}_{0.3}\text{Cu}$ alloy adopted in thermal simulation.

is thus correlated with the ternary eutectic reaction in the following.

Since (4) must be satisfied for both the alloy and all its phases, the specific heat of the alloy is expressed as

$$c_{p,\text{tot}} = (y_{\text{liq}}c_{p,\text{liq}} + y_{\text{Sn}}c_{p,\text{Sn}} + y_{\text{Cu}_6\text{Sn}_5}c_{p,\text{Cu}_6\text{Sn}_5} + y_{\text{Ag}_3\text{Sn}}c_{p,\text{Ag}_3\text{Sn}}) + \left(\frac{dy_{\text{liq}}}{dT}H_{\text{liq}} + \frac{dy_{\text{Sn}}}{dT}H_{\text{Sn}} + \frac{dy_{\text{Cu}_6\text{Sn}_5}}{dT}H_{\text{Cu}_6\text{Sn}_5} + \frac{dy_{\text{Ag}_3\text{Sn}}}{dT}H_{\text{Ag}_3\text{Sn}} \right). \quad (6)$$

Besides the average of the specific heats of the coexisting phases, (6) also expresses the thermal effect due to phase transformations. The second part of (6) is only significant at temperatures between the liquidus and eutectic temperature, which means that the influence of latent heat during melting or solidification is automatically included when the enthalpy curve in Fig. 8 is used for simulation, and it is not needed to define the heat-generating rate \dot{q} in (1). This is an advantageous feature.

Regarding multiphase material as a composite mixture of coexisting phases, its thermal conductivity could be simplified to be the weighted average upon the volume fractions of all the phases. As shown in Fig. 7, the mole ratios of the two intermetallics, Cu_6Sn_5 (< 0.01) and Ag_3Sn (< 0.007), are very small and the conductivity of the solder alloy can be averaged from liquid and solid Sn alone. Using their densities, 6900 kg/m^3 for liquid and 7310 kg/m^3 for solid Sn, we calculated the volume ratios from mole ratios. The resulting thermal conductivity of the solder alloy is presented in Fig. 9. Since the amounts of dissolved Cu and Ag are small, the properties of pure Sn are adopted in the calculation [15].

IV. EXPERIMENT

Experimental measurement of reflow profiles of the CSP component were performed to obtain the oven temperature, optimize the unknown parameters and check the validity of

the simulation. The reflow process was carried out in a typical forced-convection reflow oven with five heating zones and one cooling zone (EPM/EWOS 5.1 N2) [16]. The flow field of the oven has been simulated earlier [10]. Temperature profiles were recorded with a multichannel concurrent logger (SuperM.O.L.E. Gold from ECD). Six thermocouples were attached to the CSP component on a PWB with Ni(Au) finish. The measurements lasted for 250 s.

K-type thermocouples were introduced to the component and positioned as close to the solder interconnection as possible, from both upper and bottom sides, at the positions 1 and 2 as shown in Fig. 1. A pair of thermocouples was embedded at each site with the tips carefully positioned to touch the interconnection metallizations on the component side and on the soldering pad on the board metallization. The positions of the thermocouples were checked by focused X-ray (Fein Focus) to ensure that the thermocouples were as close as possible to the metallization pads. An additional pair of thermocouples was used to record the temperature of the reflow atmosphere, above and below the test board.

The accuracy of the temperature measuring facility is $\pm 1^\circ\text{C}$. However, since the thermocouple tips (0.4 mm) and the holes drilled to place them (0.7 mm) are slightly larger than interconnections, they may disturb the local temperature field and the error of the measurement could be easily up to several degrees. This is why the application of experimental measurement is limited here and theoretical simulation becomes necessary to reveal the detailed temperature field inside interconnections.

The measured temperature profiles and oven temperatures are plotted in Fig. 10(a). An enlarged view of the results around the peak temperature is presented in Fig. 10(b). Different temperature profiles are observed on the component and board sides of interconnections and the temperature of component side appears to be more sensitive to the oven temperature.

The microstructures of the solder interconnections after the reflow process were analyzed by using scanning electron microscopy (SEM).

V. RESULTS

The results of the component and interconnection models are now presented.

A. Component Level Model

The simulated temperature fields of the component board as it passes the final heating zone and the cooling zone of the oven are shown in Fig. 11. The temperature scale has been configured so that details in the solidification temperature range are revealed. The calculated temperature profile and the measured results fit fairly well as shown in Fig. 12. Because of the size of the thermocouple and the positioning error, the calculated profiles were taken at positions 0.5 mm away from the board or component surfaces. The simulated temperature difference between the CSP and board side temperatures was slightly less than the measured value. This is a reasonable result since the thermocouples were connected to the data logger through wires that were heated and cooled by the surrounding air. In fact, the measurement tended to exaggerate the temperature difference.

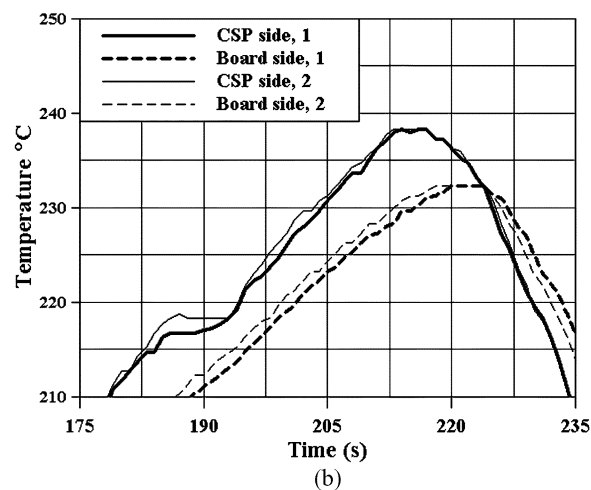
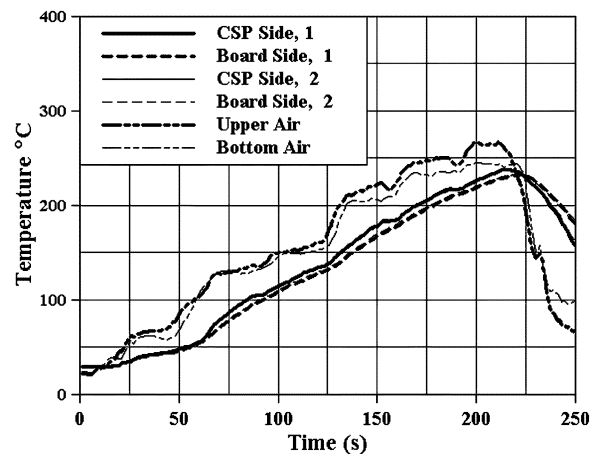


Fig. 10. Measured temperature profiles. (a) Complete temperature profiles. (b) Temperature profiles near the peak temperature.

Because of the larger surface area, stronger convection and relatively smaller thermal capacitance, the component was more easily heated and cooled than the board. This was observed in the measurement and verified in the model. Although the peak value is higher, the CSP-side temperature dropped earlier and faster than the board side temperature. In principle, this difference produces a negative vertical temperature gradient over the solder interconnection. If it is significant enough, solidification should start from the upper end of the interconnections and proceed downwards. However, the component-level model did not offer sufficient detail to confirm this supposition and it was explored instead with an interconnection-level model.

The edges of the component, especially the corners, are heated and cooled faster than the other parts. How this affects the solidification of different interconnections will be discussed in the content of the following interconnection model.

B. Interconnection Model

The interconnection model describes a similar history of temperature difference ($T_{\max} - T_{\min}$) for all the interconnections, as illustrated in Fig. 13. Three different periods can be identified in the figure.

The first period covers the time when the interconnection temperature is higher than the isothermal eutectic temperature. In

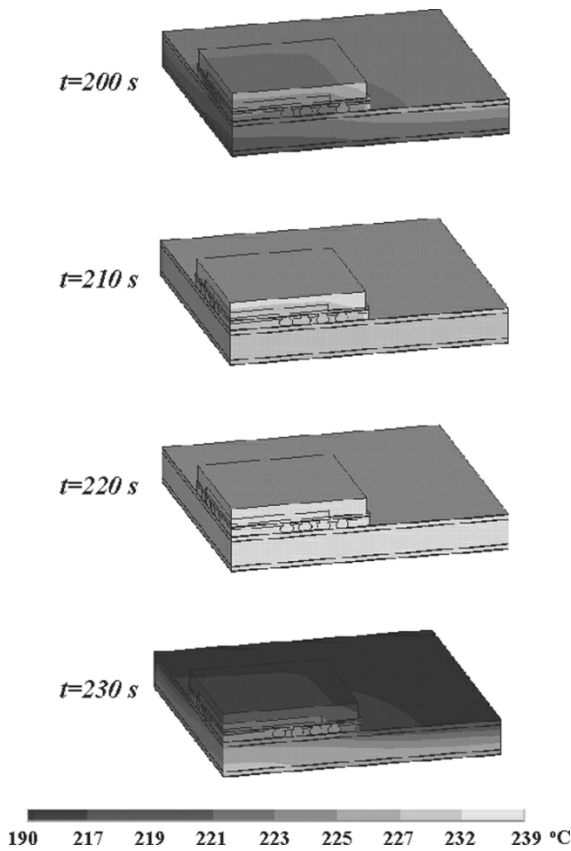


Fig. 11. Simulated temperature field in the component model as the board passes the peak and cooling zones of the reflow oven.

view of the considerable temperature difference between the component and board, the temperature gradients over the interconnections are not as great as expected. Especially for the inner interconnection *c*, the temperature difference drops to a level below 0.05 °C during this period. The other interconnections experienced a slightly larger but still not substantial temperature difference.

The result was explained when the thermal conductivities of the materials were examined. The solder interconnection behaves as a highly conductive material embedded inside good insulators. Evidently the thermal impedance of the interconnection is only a minor part of the total impedance between component and board. The corresponding temperature drop was insignificant therefore.

Even though the total temperature difference between component and board gradually becomes larger upon cooling during the first period, the temperature difference decreases gently and steadily with time. Two things may have contributed to such decrease: 1) the solidification releases a certain amount of heat and further smoothes the temperature difference inside the interconnections; and 2) the volume of the solid phase increases as solidification proceeds, and the thermal conductivity is increased accordingly, as shown in Fig. 9.

The situation changed when the temperature reached the ternary eutectic temperature. The temperature gradient inside interconnection ramped up quickly during the second period (Fig. 13) and a sharp peak with width of 0.3–0.45 s appeared.

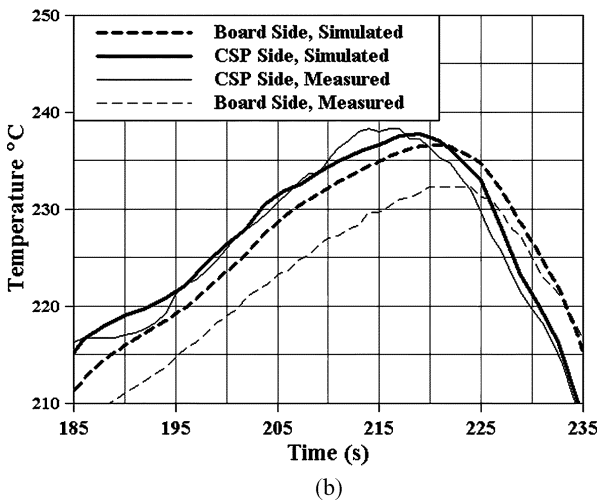
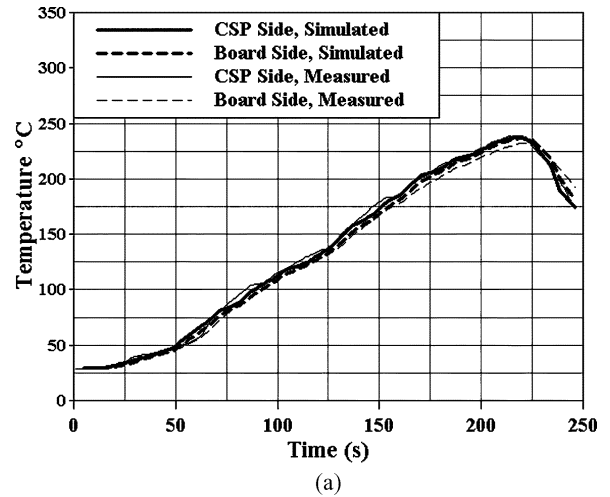


Fig. 12. Comparison of simulated and measured reflow profiles at location 1 in Fig. 2. Similar results were obtained for location 2 not shown. (a) Complete profile. (b) Enlarged figure near the peak temperature.

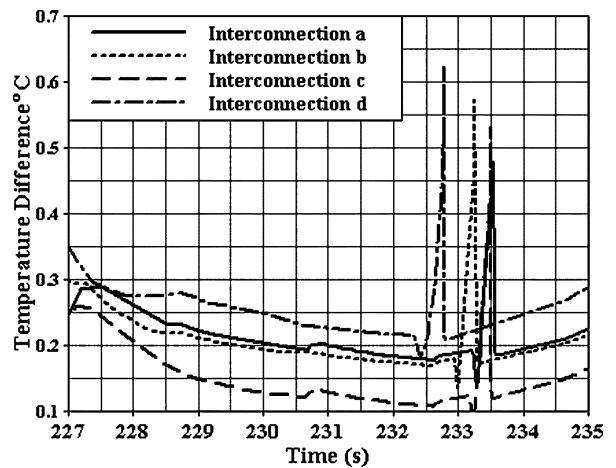


Fig. 13. Simulated temperature difference ($T_{max} - T_{min}$) of the interconnections.

By way of example, Fig. 14 shows how the temperature field changed for the interconnection *b* during this period of time.

After the solidification in period three, the temperature difference over the interconnection dropped back to a slightly higher

TABLE II
SUMMARY OF CALCULATED DATA FOR THE HISTORY OF INTERCONNECTION TEMPERATURES

Interconnection		a	b	c	d
Time to reach 229°C		226.9s	226.6s	226.7	226.6
Time to reach 223°C		230.6s	230.3s	230.7	229.5
Time for minimum temperature to reach 217.0°C		233.2s	233.0s	233.2	232.4
Time for maximum temperature to reach 216.8°C		233.6s	233.3s	233.5	232.8
Total time for solidification		6.7s	6.6s	6.8s	6.2s
Primary Sn range	Time	3.8s	3.7s	3.9s	2.9s
	Average temperature difference	0.05 °C	0.05 °C	0.03°C	0.07 °C
	$G/R^{1/2}$ (°C/cm ^{1.5} s ^{0.5})	16	17	10	21
Binary eutectic range	Time	2.6s	2.7s	2.6s	2.9s
	Average temperature difference	0.09°C	0.09 °C	0.05°C	0.13 °C
Ternary eutectic range	Time	0.32s	0.31s	0.30s	0.4s
	Maximum temperature difference	0.53°C	0.62 °C	0.42°C	0.63°C

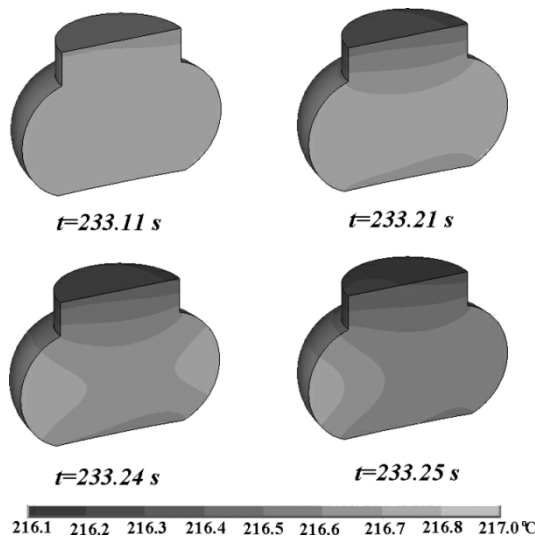


Fig. 14. Calculated temperature field of interconnection b during the second step, that is, during the isothermal eutectic. Only half of the joint is shown in order to present the temperature field inside.

level, which may be ascribed to the enhanced total temperature difference.

Differences between the inner and outer interconnections are apparent in the summary of the calculation in Table II as well as the temperature fields during the last moments of solidification (see Figs. 13 and 15) reveal some clear difference. First, the inner interconnections *a* and *c* solidify relatively slowly; the interconnection *d* reaches the liquidus temperature (228.6 °C) 0.5 s earlier than the interconnection *a* and the difference increased to 0.8 s in the final stage of solidification. Second, the inner interconnections *a* and *c* exhibit a much more uniform temperature field than the outer interconnections *b* and *d*. The maximum temperature difference is smaller for the inner interconnections *a* and *c* than for outer interconnections *b* and *d*. Finally, there is little difference between the two inner interconnections *a* and *c*, while the outer interconnection at corner (*d*) shows greater temperature gradient and faster cooling than the interconnection at edge (*b*).

Although the temperature gradient through interconnections was generally vertical the isotherms inside were not exactly horizontal. A temperature gradient from right to left side can be seen for interconnection *b* (Fig. 15), whereas for interconnection *d* the gradient is turned to the diagonal direction. The same

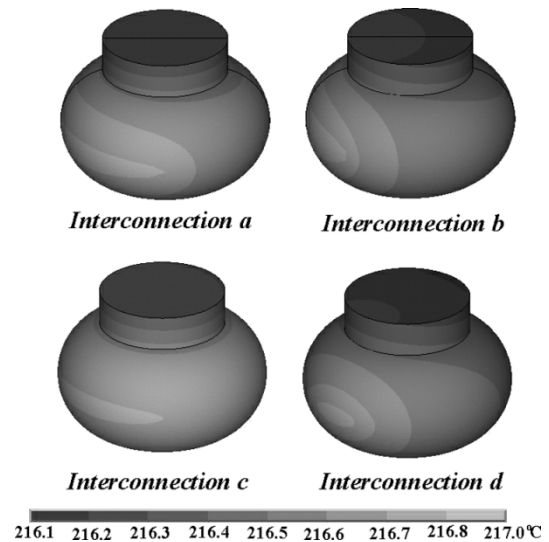


Fig. 15. Calculated temperature fields of the four interconnections during the last moments of solidification.

tendency is evident but less pronounced for the inner interconnections *a* and *c*. During solidification the side of the interconnection nearest the center of the component is always hotter than the corresponding outermost side, consistent with the temperature field at the component level.

VI. DISCUSSION

The solidification process and the solidified microstructure of the solder interconnections will now be discussed on the basis of thermodynamic analysis and thermal simulation.

A. Growth Conditions for Primary Sn

Because a certain amount of supercooling is needed for nucleation of primary Sn and the temperature field is more or less uniform, solidification might be expected to start at any place. In practise, however, solidification starts at locations where nucleation of primary Sn is promoted by an interface, most notably the solder–metallization interfaces at the two ends of the interconnection. No preference for either side of the interconnection was observed in the present research; the two sides are equally effective places for primary Sn nucleation. The thermal simulation readily explains this phenomenon.

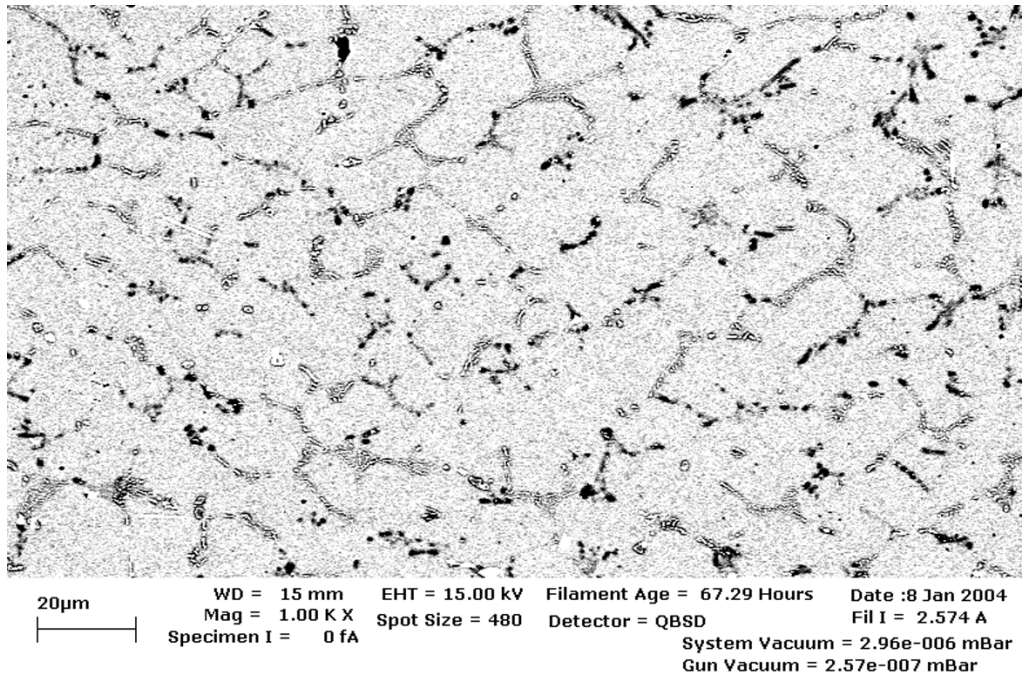


Fig. 16. Typical microstructure of a solder joint of the CSP component under investigation. The picture comes from a vertical plane of an interconnection after reflowing.

At the beginning of solidification, primary Sn forms and its morphology significantly affects the final microstructure. Usually, when an alloy solidifies, either cellular or dendritic structure is formed, depending on the growth conditions. The growth variables included the growth rate R , the temperature gradient ahead of the solid–liquid interface G and the solute concentration C_0 . For the solder interconnections of the CSP component investigated in this paper, the cellular structure of primary Sn was always observed. A typical micrograph of the cellular structure of the interconnections is shown in Fig. 16.

The cell size of the structure affects the mechanical properties of solder interconnections and is of great interest from the reliability point of view. Plaskett and Winegard [17] investigated the solidification of three tin-rich binary alloys Sn–Pb, Sn–Bi, and Sn–Sb and found that the cell size was independent of the type of solute and solute concentration, but dependent upon temperature gradient G and growth rate R . While the measured cell size was plotted versus the $G/R^{0.5}$ value, the result was almost the same for the three systems, as shown in Fig. 17.

We made a rough estimate of the growth conditions for primary Sn with the help of our model. The growth rate R was evaluated by assuming that the growth time is the total time at which the interconnection temperature is within the temperature range of primary Sn formation and that primary Sn grows through the interconnection. Combining R with the temperature gradient G from the model, we calculated $G/R^{0.5}$ for each interconnection as presented in Table II. The results ranged from $10^\circ\text{C}/\text{cm}^{1.5}\text{s}^{0.5}$ for the inner interconnections c to the maximum value of $21^\circ\text{C}/\text{cm}^{1.5}\text{s}^{0.5}$ for the interconnection d at the corner.

According to the micrograph in Fig. 16, the cell size in interconnections of a CSP component varies between 20 and $30\ \mu\text{m}$. From Fig. 17, we see that this corresponds to the $G/R^{0.5}$ value between 10 and $40^\circ\text{C}/\text{cm}^{1.5}\text{s}^{0.5}$. According

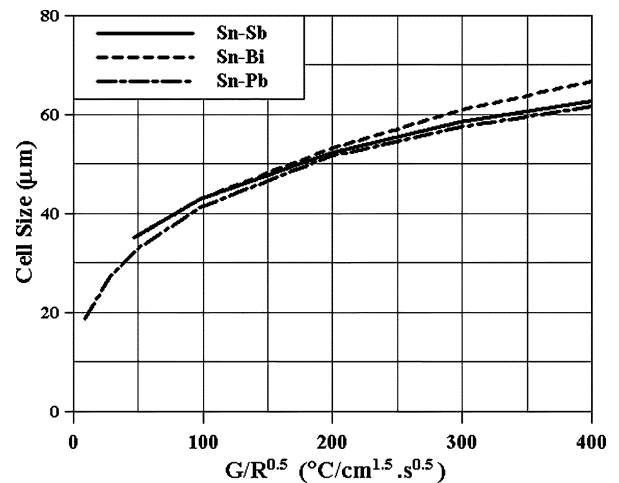


Fig. 17. Measured cell size of primary Sn as function of the growth condition $G/R^{0.5}$ of Sn–Sb, Sn–Bi, and Sn–Pb binary alloy, according to Plaskett and Winegard [17].

to Plaskett and Winegard [17], neither solute type nor concentration affects the cell size in binary Sn alloy. If, then, the plot also holds for solder, the calculated growth conditions and the observed microstructure are in good agreement.

Recently, a series of important theoretical investigations was focused on the unsteady-state unidirectional solidification of binary alloy [18], [19]. Hunt and Lu [18] proposed equations for the growth conditions to predict the cellular and dendrite transition as well as the cellular spacing. In an examination of solidification of Sn–Pb alloy, Roch *et al.* [20], [21] found poor agreement between predicted cellular size and experimental results. Generalizing from their experiments, they used the parameter $\eta = (G/R)(1/C)$ to determine the transition in cellular and dendritic structures for Sn–Pb alloy. Although these studies

offer interesting ideas for understanding of the microstructure of lead-free solder interconnections, we were unable simply to apply the equation to our work because the redistribution of solute atoms in ternary solder alloy is much more complex than that in binary alloy. Hunt and Lu's equations cannot be applied directly and a careful analysis of the growth mechanism would have performed first. Hence, our estimation of the growth conditions was checked, qualitatively, only against the experimental information in Fig. 17. Our work nevertheless confirms that thermal models can be used to estimate the growth conditions of primary Sn in solder interconnection, providing essential information for such analysis in the future.

B. Final Stage of Solidification

The temperature gradient ramps up in the final stage of solidification, when the invariant ternary eutectic reaction begins. Before this, the interconnection was composed of 13.2% liquid and 86.8% solid phases, including primary Sn and binary eutectic structure. We assumed that this amount of liquid residues would distribute homogeneously in the primary Sn phases, support for this assumption was provided by the final microstructure in Fig. 16, which shows the presence of intermetallic compounds along the boundaries between the fine cells of primary Sn.

Because of the fairly uniform temperature field, the isothermal eutectic reaction commenced in the whole interconnection almost simultaneously and released large amount of latent heat at constant temperature. As mentioned above, any point of temperature between 216.8 °C and 217.0 °C in the results should be regarded as a point at eutectic temperature where the invariant eutectic reaction is ongoing. These regions correspond to the brightest areas in the temperature fields shown in Figs. 14 and 15.

The progress of the invariant reaction clearly depends on how fast the latent heat can be dissipated. The temperature of the completely solidified parts of the interconnection drops upon cooling, while the solidifying parts remain at constant temperature. A temperature gradient inside the interconnection was accordingly constructed.

The latent heat could be conducted away either through the component and board or through the air gap between the component and the board, but the former route would seem to be the major one. Since the component cooled faster than the board, solidification was first completed at the component end and the corresponding solidified region enlarged steadily downwards. A short time later, another solidified region formed at the board end and grew upward. The two solidified parts merged in the middle of the interconnection. The reacting region then receded from the point of merger to the interconnection surface. The process lasted for 0.3–0.45 s, depending on the position of the interconnection. It was longer for the interconnection d at the corner but was completed about 0.8 s earlier there than in the inner interconnections.

Potentially reliability might be correlated with such steps in final solidification, despite that there has been no clear understanding of them until now. For example, with 13.2% liquid present before the eutectic reaction, the solder should still have

ability to release stress upon applied force. This capability is lost and the residual stress begins to accumulate only after complete solidification. The final distribution of residual stress, at both component and interconnection level, is strongly affected by solidification. Correlation of stress distribution with the steps in the final solidification would be an interesting topic for future research.

VII. SUMMARY

Two models of different level, a component model and an interconnection model, were established hierarchically to simulate the reflow process for a CSP component in a forced-convection reflow oven. The component level model simulated the temperature field inside the component and the vicinal board area and, most importantly, it provided boundary conditions for the interconnection level model. The interconnection level model revealed a detailed temperature field inside interconnections and offered information on the solidification of interconnection.

Thermal properties of SnAgCu solder were presented with the help of a thermodynamic analysis of the equilibrium solidification process. The enthalpy of the solder alloy, obtained from a thermodynamic databank system, was used instead of the conventional specific heat so that the influence of latent heat during melting and solidification could be taken into account in the thermal simulation.

Before the simulation, temperature profiles and oven temperature were measured with a multichannel concurrent logger. The measured results were used to optimize and check the validity of the models.

Both the experimental data and the component model indicated that the component cools faster than the board. However, the interconnection model revealed that the temperature gradient over the interconnection was not likely to be large because of the high conductivity of solder. Noticeable temperature gradient inside interconnections occurred only at the final stage of the solidification when the invariant eutectic reaction occurred. It was also suggested that inner interconnections in CSP-type components are subjected to a more uniform temperature field and slower solidification than are outer interconnections.

The microstructure of solder interconnections was discussed in the context of thermodynamic analysis and thermal simulation. Uniform temperature fields explained why the two sides of interconnections are equally attractive for primary Sn nucleation. The growth condition $G/R^{0.5}$ of primary Sn was estimated and an explanation for the sequence for the solidification steps was also given.

The solidification study was carried out based on the local equilibrium assumption. Even though the supercooling of liquid phase was not taken into account, very useful information has been achieved. Most importantly, the thermodynamic description given in this work provides the basis for further kinetic analysis, which is needed for detailed simulation of the solidification of lead-free solder interconnections.

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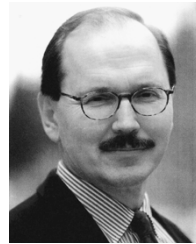
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Dr. Kivilahti has been appointed to Advanced Research Fellow of Academy of Finland. He is a Member of the National Centre of Excellence in Tissue Engineering and Biomaterials. He has received the Order of the White Rose of Finland for his contributions to electronics industry.